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2-Mbps Power-Line Communication Transmitter Based on Switched Capacitors for Automotive Networks

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Abstract: Nowadays, automotive wire harnesses have become very complex systems as the number of electronic components and Electronic Control Units (ECUs) inside a vehicle have increased dramatically. To manage this complexity, and to support the automotive systems of tomorrow, new communication techniques need to be investigated. In this work, a direct modulated Power-Line Communication (PLC) method is proposed to drastically reduce the number of interconnections and give advantages in cost, complexity, and weight. Two transmitter topologies based on a Switching Capacitor approach are presented and implemented in a Test Chip fabricated in a 180 nm HV-CMOS SOI technology. The proposal is validated by communication tests connecting the designed chip and a discrete component-based demonstrator receiver through an unshielded twisted pair cable. Compared to commercially available solutions, the proposed approach can reach a data rate of 2 Mbps, making it able to implement high-speed event-driven networks, such as the Controller Area Network (CAN).

Keywords: Power-Line Communication (PLC); transmitter (TX); Switching Capacitor; automotive harness; CAN bus; High-Voltage (HV) switch

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1. Introduction

The automotive industry is living a big transformation as even more tasks are entrusted to electric and electronic systems. This allows carmakers to improve safety, comfort, and entertainment and to introduce new functions such as Advanced Driver-Assistance Systems (ADAS). According to forecasts, electronics account for about 80% of automotive innovation, and vehicle electronic content growth will reach 50% by 2030 [1,2]. Electronic systems and subsystems are distributed over the entire vehicle and are controlled by dedicated modules named Electronic Control Units (ECUs). Besides the power supply, ECUs need one or more communication cables and usually an addressing line. The number of ECUs in a single vehicle is constantly increasing, and there can be up to 150 of them in a modern car. As a result, the number of interconnections is raised, and the wiring harness complexity, weight, and cost increase, making it one of the most critical blocks to design [3]. A physical merge of the supply and communication lines can drastically reduce the amount of needed cables and provide enormous benefits. The feasibility of Power-Line Communication (PLC) systems in an automotive environment has already been proven by commercially available proposals based on a carrier modulation [4–6]. However, the resulting data rate $\leq$500 kbps and latency would disable the use in high-speed event-driven applications ($\geq$1 Mbps), such as the Controller Area Network (CAN) [7]. Therefore, a base-band PLC system is examined to realize a CAN protocol with a modified physical layer. In this work, two transmitter circuits are presented, and are validated by a prototype implemented in a 180 nm HV-CMOS SOI technology.

Concept and proposed transmitter topologies are described in Section 2. Detailed circuit implementation is presented in Section 3. In Section 4, the fabricated Test Chip is

shown. Simulation setup and measurements results follow in Section 5, validating the proposals, and Section 6 concludes the paper.

2. Switched-Capacitor Transmitter Topologies

In the proposed PLC system, the power supply for the connected nodes is embedded in the data connection lines. Thus, a coupling feed from the power source is needed to separate it from the communication channel [8]. All devices connected to the bus are supplied via an inductive feed that reduces high current variations. The basic concept is to inject defined charges on the transmission line to obtain signal pulses for the communication [9]. Two different transmitter topologies based on switching capacitors are proposed in Sections 2.1 and 2.2 to fulfill this task.

To understand the principle of the charge injection, and to evaluate some design specifications, the discharge phase of a functional Switching Capacitor C_f is studied. In Figure 1, the equivalent s-domain model of a charge injection event is shown. C_f is connected by a switch with finite on-resistance R_{SW} to the transmission line. The line has characteristic impedance $|Z_0|$, and it is terminated by resistor R_{t1}. The capacitance C_p associated with the physical implementation aspects is also included. Finally, the coupling feed is composed of L_c and R_{t2}. In the following analysis, the inductance L_c is assumed to be sufficiently high so that $X_{Lc} >> |Z_0|$ at 10 MHz. Assuming that the capacitor is initially charged to the DC supply level $V_s(0)$, the pulse waveform of a discharge event can be evaluated by solving the inverse Laplace transform of the presented scheme [10]:

$$V_p(t) = V_{peak}\left(e^{-\frac{t}{\tau_2}} - e^{-\frac{t}{\tau_1}}\right), \tag{1}$$

The peak voltage, the rising (τ_1), and falling (τ_2) time constants are:

$$V_{peak} = \frac{Q_{C_f} R_t}{\kappa} \approx \frac{Q_{C_f} R_t}{C_p R_t + C_f(2R_{sw} + R_t)} \tag{2}$$

$$\tau_{1,2} = \frac{2C_f C_p R_{sw} R_t}{C_p R_t + C_f(2R_{sw} + R_t) \pm \kappa}. \tag{3}$$

with

$$\kappa = \sqrt{\left(C_p R_t + C_f(2R_{sw} + R_t)\right)^2 - 8\, C_f C_p R_{sw} R_t} \tag{4}$$

and $R_t = R_{t1} = R_{t2}$. Simulation results with different sizes of C_f are shown in Figure 2, where it has been assumed to design a switch with $R_{sw} = 10\ \Omega$ and, $R_t = |Z_0| = 100\ \Omega$, $C_p = 10$ pF, $L_c = 100\ \mu$H, $V_S(0) = 12$ V.

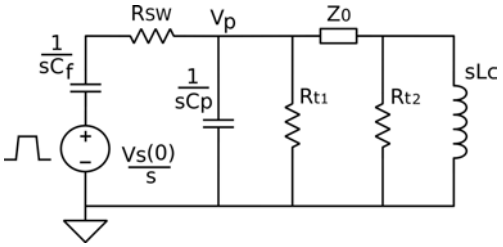
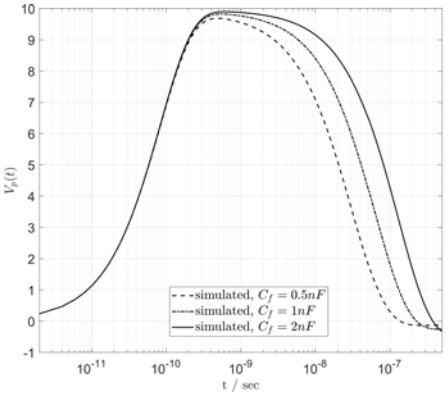


Figure 1. Equivalent s-domain model of the charge injection.



C_f	T2
0.5 nF	29.9 ns
1.0 nF	59.4 ns
2.0 nF	118.4 ns

Figure 2. Simulation results of a discharge event.

It can be deduced that switching capacitor ≤2 nF is required to reach a data rate of 2 Mbps (falling time $\tau_{2max} \approx 100$ ns). To ensure communication robustness, C_f also needs to be at least one order higher than C_p, i.e., ≥100 pF. Therefore, a trade-off between switching capacitor size and data rate is shown. This analysis leads to considering external capacitor C_f in the developed proposal, both for the area occupation and for the higher flexibility.

2.1. H-Bridge Topology

The first transmitter topology is the H-Bridge implementation of Figure 3. The supply is applied on the transmission line through the coupling feed composed of $R_t/2$ and L_c. Moreover, the line is terminated by an AC-coupling capacitor (C_c) and two series $R_t/2$ resistors.

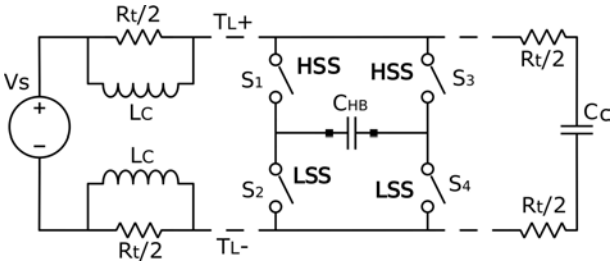


Figure 3. H-Bridge TX topology.

The circuit consists of a switching capacitor (C_{HB}), which can be connected to the transmission line through two equal High-Side Switches (HSS), S_1 and S_3, and two equal Low-Side Switches (LSS), S_2 and S_4, which operate in an H-Bridge topology. The circuit commutes among three possible states, as described in Table 1, which are alternating at each received data edge. Assuming that C_{HB} is initially discharged, at the first Charge-State (e.g., Charge 1–4), it is charged to $Q_{CHB} = C_{HB} \times V_S$. As a guard against overlap and unwanted cross currents between the transmission rails, an Open-State is always placed after a charge event, during which the charge in C_{HB} is preserved. As the next step, the second Charge-State (e.g., Charge 2–3) is reconnecting the capacitor to the transmission line, and is charging it to $-Q_{CHB}$. As illustrated in Figure 4, a drop in the differential transmission line V_{TLdiff} occurs for each edge of received data as a result of the charge transferred from the line itself to C_{HB}.

Table 1. States of H-Bridge transmitter topology.

State	S_1, S_4	S_2, S_3	Description
Open	Open	Open	C_{HB} not connected. Charge is preserved
Charge 1–4	Close	Open	charge accumulated during Charge 2–3 phase is recharged to V_S level
Charge 2–3	Open	Close	charge accumulated during Charge 1–4 phase is recharged to the $-V_S$ level

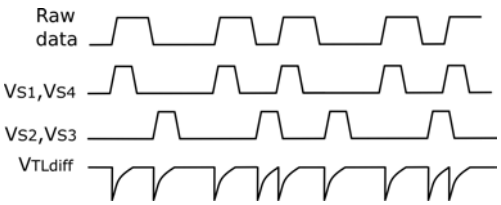


Figure 4. Example of transmission in H-Bridge TX topology.

The obtained timing constant (τ_{charge}), and the average current consumption (I_{HB}) can be evaluated as follows:

$$\tau_{charge1-4,2-3} = (R_t/2 + R_{HSS} + R_{LSS}) \times C_{HB} \quad (5)$$

$$I_{HB} = 2C_{HB} \times V_S \times DR \quad (6)$$

where DR is the data rate. The transmitted signal is unipolar and thus a pre-coding is needed since falling or rising edges of the data signal cannot be distinguished. Hence, for an uncoded data stream applied to the TX, the protocol frame structure needs to be taken into account so that a message header such as in [11] can be used to assign the correct data polarity. However, the simplest encoding to resolve the ambiguity is to encode the data as a unipolar Return-to-Zero (RZ) stream [12].

2.2. 3-Switches Topology

The second proposed transmitter topology is the 3-Switches SC scheme of Figure 5 where two capacitors (C_{S1}, C_{S2}) are charged and discharged according to the three possible states described in Table 2. During the Charge-State, C_{S1} and C_{S2} are charged in parallel through S_1 (HSS) and S_2 (LSS) to $Q_{CH} = 2C_S \times V_S$, where $C_S = C_{S1} = C_{S2}$. In the next step, the capacitors are discharged in series through S_3 (Floating Switch, FS) to $Q_{DH} = \frac{1}{2}C_S \times V_S$. Similar to the H-Bridge, an Open-State is placed in between to avoid cross currents, during which the charges are preserved. As a result, as shown in Figure 6, positive and negative pulses appear on the differential transmission line, so the data polarity can be recovered directly. Unlike the H-Bridge, the states are not symmetrical, and the charging (τ_{charge}) and discharging ($\tau_{discharge}$) timing constants are not equal:

$$\tau_{charge} = (R_t/2 + (R_{HSS}//R_{LSS})) \times 2C_S \quad (7)$$

$$\tau_{discharge} = (R_t/2 + R_{FS}) \times C_S/2 \quad (8)$$

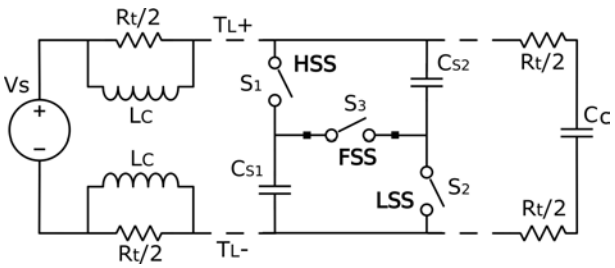


Figure 5. 3-switches TX topology.

Table 2. States of 3-switches transmitter topology.

State	S_1, S_2	S_3	Description
Open	Open	Open	C_{S1}, C_{S2} not connected. Charges are preserved
Charge	Close	Open	C_{S1}, C_{S2} are connected in parallel to the bus and charged to V_S
Discharge	Open	Close	C_{S1}, C_{S2} are connected in series and discharged to $V_S/2$

The average current consumption (I_{3S}) can be evaluated as

$$I_{3S} = C_S/4 \times V_S \times DR \tag{9}$$

and, assuming that the same data rate and capacitors size are used, is 8-times less than in the previous approach.

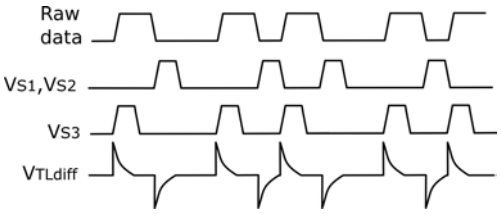


Figure 6. Example of transmission in the 3-switches TX topology.

3. Switch Implementations

Transmitter operation requires proper switch functions. The proposed schemes of Figures 3 and 5 require efficient low-side switch (LSS) (connected to ground), high-side switch (HSS) (connected to V_S), and floating switch (FS) (i.e., not connected to ground or V_S). According to Equations (5), (7) and (8), switches with on-resistance of $\leq$10 Ω are required to reach a data rate of 2 Mbps if switching capacitors of 1 nF are used. The design is made in a technology which includes HV (High-Voltage) devices up to 40 V and LV (Low-Voltage) devices up to 5 V. Both the HV and the LV devices have a gate-source voltage range between −5.5 V and 5.5 V, which must be guaranteed for safe operations. The circuits share a common current master mirror fed by a 10 µA current provided by the Supply System of the designed chip.

3.1. Floating Switch

The FS is connected between two floating points, and so it is the most demanding switch to design. The schematic is proposed in Figure 7, where the HV-NMOS M_{F0} is the FS device. According to Figure 5, its source is connected to the node between C_{S2} and the LSS S_2, which varies between 0 and $V_S/2$, and its drain is connected to the node between C_{S1} and the HSS S_1, which varies between V_S and $V_S/2$. M_{F0} dimensions are L = 0.4 µm and W = 1 mm realizing a nominal 9 Ω on-resistance switch.

When $V_{ON} = 5$ V, M_{F1} operates as a current source providing a current five times bigger than the 10 µA biased by the master CM. The generated current passes through the PMOS unity factor current mirror consisting of M_{F2} and M_{F3}, and pulls up the gate of M_{F0} turning the FS on. M_{F8} operates as a source follower and keeps V_{GSMF0} below the technology upper limit. A stack of diode-connected PMOS (D_{F2}) is placed to also ensure a high overdrive ($V_{GSMF0} = V_{SGMF8} + V_{DF2} = 5$ V). The turn-on timing constant is dominated by the C_{GSMF0}, which is estimated to be around 720 pF in saturation. The PMOS mirror is always on thanks to the constant voltage VPC that feeds the gates of the cascode HV-PMOSs M_{FC2} and M_{FC3}. This voltage is generated by the additional 10 µA current tail from by M_{F6}, which is applied on the diode-connected PMOS M_{F7}. Similarly to

D_{F2}, D_{F1} is also a stack of diode-connected PMOS (about two times bigger than D_{F2}) and protects the gate–source interface of M_{F7}.

The off branch is enabled when $V_{OFF} = 5$ V, so that M_{F4} generates a 200 µA pull-down current to turn off the FS. The NMOS M_{F9} operates as a source follower and ensures that the V_{GSMF0} is not violating the lower limit of the functional range. In case both V_{ON} and V_{OFF} are down, and the 3-Switches TX is not enabled, a permanent 2.5 µA pull-down off current is applied by M_{F5} to ensure a no floating gate.

By using switching capacitors of 1 nF, the turn-on and turn-off times from post layout simulations are, respectively, 17.5 ns and 36.3 ns in typical conditions, and 21.7 ns and 43.4 ns in the worst corner over a temperature range from −40 °C to 125 °C.

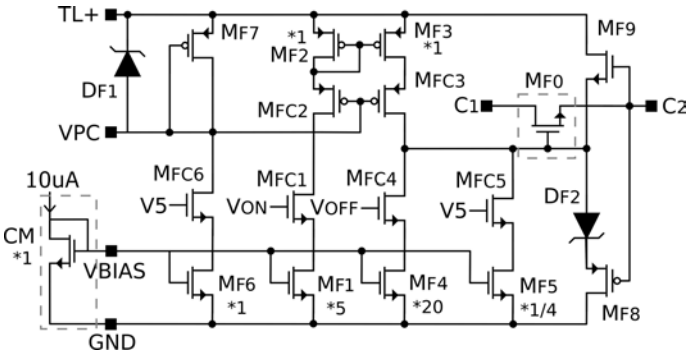


Figure 7. FS schematic.

3.2. Low Side Switch

The LSS is implemented by the circuit of Figure 8. The switching HV-NMOS M_{L0} is sized with L = 0.4 µm and W = 1 mm to realize a nominal 9 Ω on-resistance switch. The source is directly connected to $TL-$ while the drain is connected to the external pad through the ESD protection diode D_{L0}.

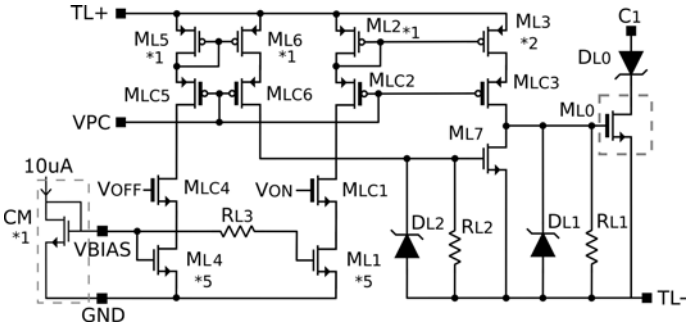


Figure 8. LSS schematic.

The switch is turned on by applying $V_{ON} = 5$ V on the gate of the cascode HV-NMOS M_{LC1}. A 50 µA current is injected into the PMOS mirror consisting of M_{L2} and M_{L3}, which has a mirroring factor equal to 2. The resulting 100 µA current pulls up the gate of M_{L0} turning it on with a timing constant given by $R_{L1} \times C_{GSML0}$. C_{GSML0} is estimated to be ≈720 pF in saturation, while $R_{L1} = 50$ kΩ, which also leads to $V_{GSML0} = R_{L1} \times I_{ML3} = 5$ V in steady state.

The turn-off starts when V_{OFF} rises, enabling M_{L4} to provide a 50 µA current tail that, through the unity factor PMOS mirror M_{L5}, M_{L6}, turns M_{L7} on and thus M_{L0} off. Resistor R_{L2} = 25 kΩ is sized to obtain $V_{GSML7} = R_{L2} \times I_{L6} = 5$ V, while the diode-connected PMOS stack D_{L1} and D_{L2} are used as gate-source protection. M_{L7} is a small low voltage NMOS with a small C_{GS}, so its turn-on timing constant $R_{L2} \times C_{GSML7}$ can be neglected. The LSS turn-off timing constant can then be evaluated as $C_{GSML0} \times (R_{L1} // ron_{ML7}) \approx C_{GSML0} \times ron_{ML7}$.

The resulting turn-on and turn-off times from post layout simulations are respectively 18.2 ns and 16.2 ns in typical conditions, and 28.7 ns and 22.5 ns in the worst corner over a temperature range from −40 °C to 125 °C.

3.3. High Side Switch

Initially, the idea of using an HV-NMOS with a bootstrap circuit as HSS was considered to save area and ensure symmetry with the LSS [9]. However, due to the spikes on the communication bus, it is difficult to guarantee correct operation without violating the technological limits (such as the maximum voltage at the gate–source interface) using this kind of circuit; thus, a HV-PMOS is preferred. The same nominal on-resistance of 9 Ω is desired to obtain a symmetrical structure, and so M_{H0} is sized with L = 0.5 µm and W = 3 mm. Due to the lower mobility, this device is around three times bigger than the LSS and the FS, and so is its C_{GS}. The source is connected to $TL+$ while the drain is connected to the external pad through an ESD protection diode as shown in Figure 9. The signal V_{ON} enables a 300 µA current that pulls down the gate of M_{H0}, turning it on. Resistor R_{H1} = 16.5 kΩ is sized to furnish $V_{SGMH0} = 5$ V in steady state. The timing constant is given by $C_{GSMH0} \times R_{H1}$ and, compared to the LSS, a higher current is applied to obtain similar behavior.

The switch is turned off by raising V_{OFF} to apply a 100 µA pull-down current on the gate of the low voltage PMOS M_{H3} ($R_{H2} = 50$ Ω). Similar to the LSS, the turn-off constant can be evaluated as $C_{GSMH0} \times (R_{H1} // ron_{MH3}) \approx C_{GSMH0} \times ron_{MH3}$ where the turn-on time of M_{H3} is neglected. Protection diodes D_{H1}, D_{H2} are also placed to ensure safe operations.

Turn-on and turn-off from post layout simulations result in being respectively 19.9 ns and 3.8 ns in typical conditions, and 30 ns and 4.5 ns in the worst corner over a temperature range from −40 °C to 125 °C. As expected, the turn-on times of the LSS and the HSS are not very different so that the effect on the transmission lines is also similar, ensuring symmetry.

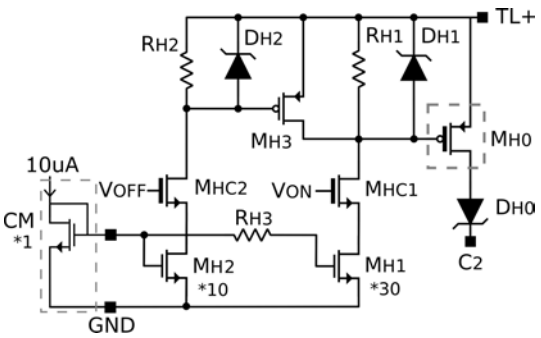


Figure 9. HSS schematic.

4. Fabricated Prototype

A test chip has been fabricated in 180 nm HV-CMOS SOI technology and packaged in a QFN 24 pins to validate the proposal. A 2000× Micrographs picture is shown in Figure 10. The TX includes both the two proposed implementations since each offers different interesting advantages. The H-Bridge proposal requires less external components (1 capacitor) than the 3-Switches topology (2 capacitors), but the current consumption is higher. Moreover, a coding is required to reconstruct the transmitted signal. The full TX occupies an area of 820 × 220 µm^2, and since it requires one switch more, the H-Bridge implementation is 1.4 times bigger than the 3-Switches.

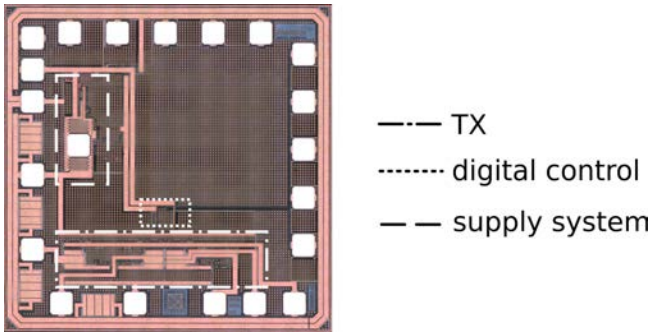


Figure 10. Test Chip 2000× micrographs picture.

The Supply System is composed of several already existing IP blocks such as a 5 V regulator and a bandgap reference. Besides generating the needed 5 V from the V_S supply, it also furnishes the 10 µA biasing current to the master mirror for the switches. The Digital Control manages the supply system settings and drives the transmission. First, one of the TX topologies is enabled; then, the switch control signals are generated according to Tables 1 and 2 to implement the possible states.

In the designed chip, an empty space in the top right region is intentionally left to insert the receiver in a second version to implement the full transceiver. For the same reason, only 20 of the 24 pins have been used [13].

5. Measurements Results

The fabricated chip is placed on PCB for testing, which includes the switching capacitors (C_{HB}, C_{S1}, C_{S2}) and the supply coupling feed as highlighted in Figure 11. The DC power supply is differentially coupled to the terminals of the transmissions line $T_L\pm$, by two inductors $L_C = 100$ µH, which are bypassed by $R_t/2 = 50\ \Omega$ to realize a match to the line impedance.

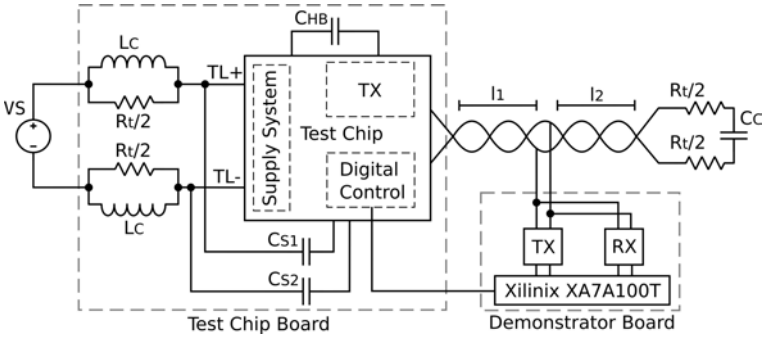


Figure 11. Measurement setup.

A demonstrator board composed of off-the-shelf components is connected to the Test Chip Board by a twisted pair cable of l_1 length and operates as a receiver. A 4 GHz LNA LTC6268-10 is coupled to the transmission line and acts as a high-speed differential amplifier whose single-ended output is compared to generated low and high thresholds by two LVDS comparators. An FPGA Xilinx XA7A100T is placed on top of the demonstrator board and is managing all signal processing and interfacing. The FPGA contains a clock, as well as a modulator/demodulator for the unipolar RZ coded signal used in the H-Bridge approach and for the direct coded signal used in the 3-Switches approach. The transmission line is symmetrically terminated after another segment of twisted pair cables of l_2 length using an AC-coupling capacitor $C_C = 100$ nF in series to two $R_t/2 = 50\ \Omega$ connected to the ends of the transmission line.

By using 820 pF switching capacitors in Equations (5), (7) and (8), the obtained timing constants are:

$$\tau_{charge1-4,2-3} = (R_t/2 + R_{HSS} + R_{LSS}) \times C_{HB} = (50\ \Omega + 18\ \Omega) \times 820\ \text{pF} = 55.7\ \text{ns} \quad (10)$$

$$\tau_{charge} = (R_t/2 + (R_{HSS}//R_{LSS})) \times 2C_S = (50\ \Omega + 4.5\ \Omega) \times 1640\ \text{pF} = 89.3\ \text{ns} \quad (11)$$

$$\tau_{discharge} = (R_t/2 + R_{FS}) \times C_S/2 = (50\ \Omega + 9\ \Omega) \times 410\ \text{pF} = 24.1\ \text{ns} \quad (12)$$

making it possible to complete a state (4τ that can be assumed as reference time to complete a charge or discharge phase) in 500 ns and therefore to reach a data rate of 2 Mbps with both of the proposed solutions. The Transmission Bus at Demonstrator node received data and clock are shown in Figure 12 for the H-Bridge and the 3-Switches topologies in case l_1 = 6 m and l_2 = 0.25 m are applied. As a data source, a 2 Mbps pseudo-random bit stream (PRBS) generator is implemented in the FPGA according to Tables 1 and 2. Pulse amplitude and timing constants for three different tested combinations of l_1 and l_2 are reported in Tables 3 and 4. Furthermore, tests with smaller capacitances have been carried out to reach data rates of up to 10 Mbps. Measurement results at 5 Mbps and 10 Mbps are shown in Figure 13 for the H-Bridge TX, and data are reported in Tables 3 and 4 as well. The peaks amplitude in the 3-Switches implementation are lower than in the H-Bridge as expected by comparing Equation (2) in the different circuits and phases.

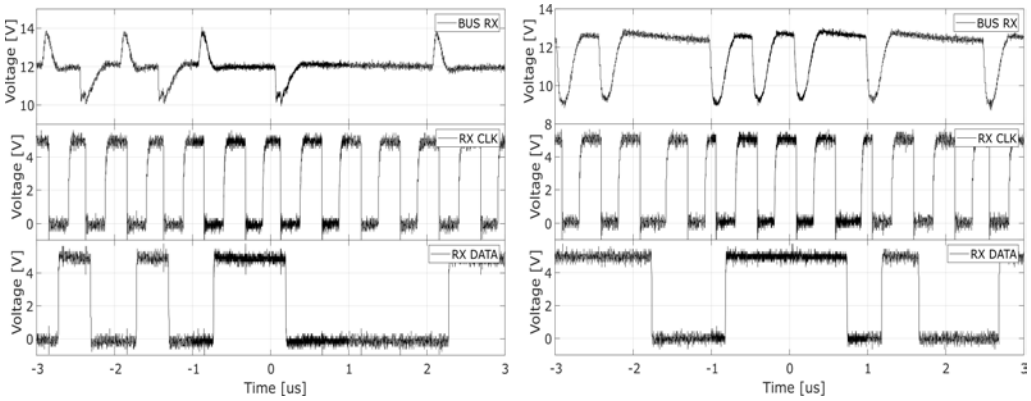


Figure 12. Transmission Bus, received data and received clock at 2 Mbps (switching capacitors = 820 pF) for the 3-Switches (**left**) and the H-Bridge (**right**) transmitters.

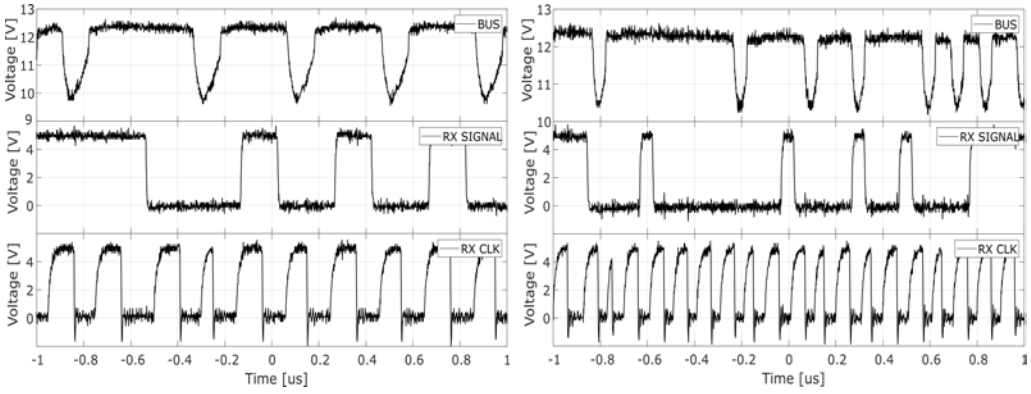


Figure 13. Transmission Bus, received data and received clock at 5 Mbps (switching capacitors = 330 pF) and 10 Mbps (switching capacitors = 180 pF) for the H-Bridge transmitter.

Table 3. Measurement results for the H-Bridge TX.

	l1 = 0.25 m l2 = 0.25 m		**l1 = 6 m l2 = 0.25 m**		**l1 = 0.25 m l2 = 6 m**	
	Charge 1–4/2–3		**Charge 1–4/2–3**		**Charge 1–4/2–3**	
	ΔV	4τ	ΔV	4τ	ΔV	4τ
820 pF	3.29	240	2.85	251	4.35	246
330 pF	3.16	120	2.6	124	4.04	125
180 pF	2.75	81	2.19	91	3.14	83

Table 4. Measurement result for the 3-Switches TX.

	l1 = 0.25 m l2 = 0.25 m				**l1 = 6 m l2 = 0.25 m**				**l1 = 0.25 m l2 = 6 m**			
	Charge		**Discharge**		**Charge**		**Discharge**		**Charge**		**Discharge**	
	ΔV	4τ	ΔV	4τ	ΔV	4τ	ΔV	4τ	ΔV	4τ	ΔV	4τ
820 pF	2.88	211	2.5	96	2.13	254	1.81	95	3.38	203	2.81	94
330 pF	2.63	97	1.31	72	1.59	140	1.03	72	2.88	114	1.56	70
180 pF	2.16	55	0.78	65	1.44	96	0.59	59	2.44	78	0.97	60

6. Conclusions

A PowerLine-Communication method based on direct modulation for the automotive environment is presented in this paper. Two Switching Capacitors' transmission circuits are analyzed, and a Test Chip has been implemented in HV-CMOS SOI 180 nm technology to validate the proposal. Communication tests with a discrete component receiver board show that a data rate of 2 Mbps is reachable even using 6 m of wiring in the between. Moreover, results show that this method can potentially reach a data rate of up to 10 Mbps still offering pulses amplitude of 500 mV. The implementation allows low latencies in the applied communication, making it able to implement high-speed, time-triggered, and event-driven automotive networks.

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