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Thermoelectric Nanostructured Silicon Obtained by Metal-assisted Chemical Etching

A dissertation for the degree of Doctor of Philosophy in Materials Science and Nanotechnology

Stefano Magagna
Università di Milano-Bicocca/Aix-Marseille Université
Supervised by Prof. Dario Narducci and Dr. Claude Alfonso

SCUOLA DI DOTTORATO
UNIVERSITÀ DEGLI STUDI DI MILANO-BICOCCA

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Magagna Stefano

MAT: 835005

Tutor: Prof. Dario Narducci

Co-Tutor: Dr. Claude Alfonso

Coordinator: Prof. Marco Bernasconi

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"Let your boat of life be light, packed with only what you need - a homely home and simple pleasures, one or two friends, worth the name, someone to love and someone to love you, a cat, a dog, and a pipe or two, enough to eat and enough to wear, and a little more than enough to drink; for thirst is a dangerous thing."

Three Men In A Boat - Jerome K. Jerome

Abstract

The necessity of sustainability in energy production and the continuous increasing of global warming, which leads to tremendous consequences, are among the most complicated challenges faced by humanity along its history. Reduction of the energy wastes and a strong energetic efficiency improvement are the most relevant solutions proposed, since nearly the 60 % of the energy generated around the world is wasted as heat. The possibility to recover even a small amount of this wasted energy could lead to a significant decrease of CO_2 emission.
Thermoelectric devices can actively contribute to this cause since they allow to generate electrical power even with small temperature gradients and without moving parts. Their efficiency is described by the figure of merit $zT = \frac{\alpha^2 \times \sigma}{\kappa} \times T$, where the numerator is named Power Factor (PF) and is the the product between the square of the Seebeck coefficient (α) and the electrical conductivity (σ), and the denominator is the thermal conductivity (κ). Therefore, an ideal thermoelectric material should have, at the same time, good electrical properties combined to a low thermal conductivity, a difficult challenge considering that, normally, a good electrical conductor is also a good thermal conductor. However, property modification at nanoscale opened a new pathway in thermoelectric materials research.
The work of this PhD thesis is focused on the nanostructuration of a non-toxic, earth-abundant material such as Silicon. Due to the

high thermal conductivity, bulk silicon is not suitable for thermoelectric application. Anyway, nanostructuration offers efficient and innovative ways to lower silicon thermal conductivity and to open novel opportunities to its usage as thermoelectric material.
In the first part of this dissertation, the mechanism of Silver-assisted Chemical etching (SaCE), a one-step method chosen for the production of silicon nanowires (NWs) will be presented. Particularly, the results of an extended analysis of the interplay among doping level and type of silicon, nanowire morphology and the parameters controlling the chemistry of SaCE will be shown. SaCE occurs at the outer substrate surface as a result of Si extrusion by sinking self-propelled Ag particles which causes Si flakes to be exposed at the outer solution-substrate. Here, the etching actually occurs through either 2- or 4-electron electrochemical oxidation of Si. NW surface is found to be either porous (potholed) or crystalline depending on the predominant electrochemical process. The prevalence of either 2- or 4-electron processes is controlled by the material resistivity and therefore by the voltage sensed by silicon. Two-electron processes occur at low voltages for conductive, heavily doped Si,and causes the formation of superficially potholed NWs. Four-electron processes occur for weakly doped Si and lead to fully crystalline NWs.
Secondly, the production, by means of SaCE, and the characterization of a recently introduced category of material, the so-called Nanophononic Metamaterial (NPM), will be presented. This material is composed by an array of silicon nanopillars on top of a silicon thin film. The hybridization of the locally-resonant phonon modes introduced by the NWs with membrane phonon modes leads to a thermal conductivity reduction. NPM demonstrates to retain electrical and thermal conductivity of the wafer from which it is etched. Preliminary thermal measurements showed a thermal conductivity reduction of $\frac{2}{3}$ with respect of bulk silicon.
In the third part, the characterization of heavily doped Si NWs arrays, produced by SaCE, will be presented. This kind of arrays shows very low thermal conductivity (around 2 W/ (m K)) and a

Seebeck coefficient comparable with that of heavily doped bulk silicon. Anyway, due to the presence of the substrate (very thick if compared with NWs length), it is complicated to have a precise measurement of NW resistivity. To overcome this issue, a new structure exclusively made of NWs and free from any substrate contribution will be presented.

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CHAPTER 1

Introduction

1.1 The Challenge of Climate Change and Energy Sustainability

Our planet has always known variation and oscillation in his climate. Very known is, for instance, the Little Ice Age (LIA) that interested the Earth between the half of XIV century and the half of XIX century, with a consistent lowering of temperatures all around the globe, due mainly to solar and volcanic activity. In the last few decades, the unbridled postbellum development of industry and technology in Europe and USA firstly and, more recently, in Asia and South America and the consequent increased of world population caused a positive change in global temperatures. Since the '60s, human activities have impacted climate in a way that has never occurred before [1].

Emission in the atmosphere of Greenhouse gases (GHGs) can be easily indicated as the principal responsible of global warming. The tonnes of GHGs emitted every year since industrialization increased year after year due to the growing demand of energy (and the consequent increasing of thermal combustion processes to produce this energy) of a continuously growing world population which

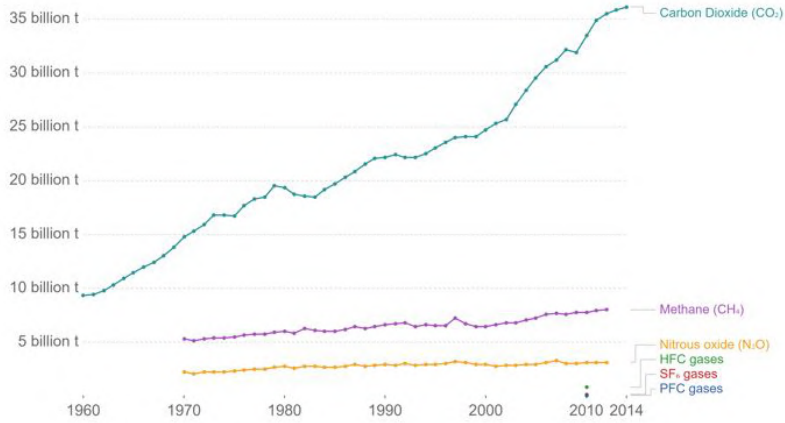

FIGURE 1.1: Greenhouse gas emission by gas from 1960 to 2014[2]

will be more than 10 billion in 2100 [3]. The development that China has known in the last two decades, that is ongoing in second world countries, such as India and south-west Asia, and that Africa will know in the next decades, will not contribute to the decrease of GHGs emission. Furthermore, the important increasing of developing countries population will cause the rise of their energy demand, as shown in figure 1.2, moving the epicentre of GHGs emissions from western countries to Asia and leaving the OECD (Organization for Economic Co-operation and Development) energy consumption substantially constant [4].

Another important index to consider is the pro-capita energy consumption. Around the world this value, expressed in Gigajoules per head (GJ/head), floats between 240 for US, 149 for EU, and 15 for Africa. Plus, average global energy consumption per capita increased by 1.8% in 2018 to 76 GJ/head in 2018. Growth in 2018 was significantly higher than the historical average (0.3% for the

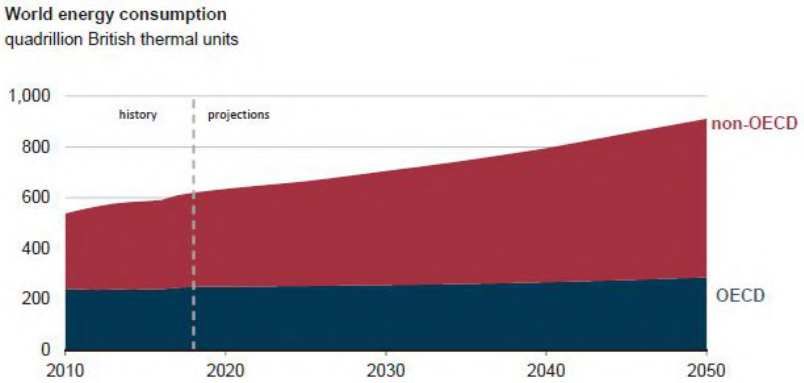

FIGURE 1.2: World Energy consumption projection until 2050, expressed in quadrilion British thermal units[5]

period 2007-17)[6] and this tendency will continue in that direction, as shown in figure 1.2. From the data presented above and many others that will not be discussed in this work, it is clear how, without an immediate trend reversal, the world is heading to a crisis that has never faced before, both from an energetic and climatic point of view, aspects that are strongly connected. With the continuous utilization of carbon fossil sources for energy production and the increasing energy demand, the emission of GHGs into Earth atmosphere will not diminish and the world will quickly reach +2°C above its pre-industrial average temperature. The consequences will be dramatic: glacier melting, sea level rising, drought, extinction of several animal and vegetal species and extreme and unpredictable climate events [8].

Scientific community, altogether with political and economic institutions support, needs to make as its priority the safeguard of our planet. Numerous efforts must be done in order to preserve the

delicate equilibrium that stands between Earth and its inhabitants, and to diminish as much as possible carbon fingerprints of our actions, making energy and environmental sustainability not only an utopia.

1.1.1 Renewable Sources of Energy and Energy Recovery

Even if carbon emission situation, as explained in the previous section, is very serious and needs to be considered as a priority, efforts, in the last couple of decades, have been actuated to mitigate this problem and to try to create an alternative to fossil fuels. This has been done mainly with the implementation and use of renewable sources of energy. The term "renewable sources of energy", generally indicates a class of resources which are naturally replenished and the utilization of which does not prevent the possibility of their future exploitation. Renewables are a great, versatile and virtually inexhaustible source of energy at our disposition; some of the most known and exploited include wind, hydro, solar, biomass, biofuels, and geothermal energies. Their potential is enormous, much higher than actual energy demand and, slowly, the interest of industry and society in general towards them is becoming more and more important, year after year. This is well proven by data reported in figure 1.3 which shows how, with the passing of time, the number of countries that adopt regulatory policies in terms of power generation, transports, carbon pricing and heating and cooling systems has decisively increased, as well as the Gigawatts produced by renewable sources added yearly to the global energy production [7].
Even though the tendency shown in figure 1.3 seems encouraging, it is clearly not enough and many efforts must be done to improve the worldwide situation. In fact, a look at the energy produced by different sources, immediately proves how only 10% of global energy production of 2017 comes from renewable sources [7]. Furthermore, predictions of energy consumption up to 2050 clearly

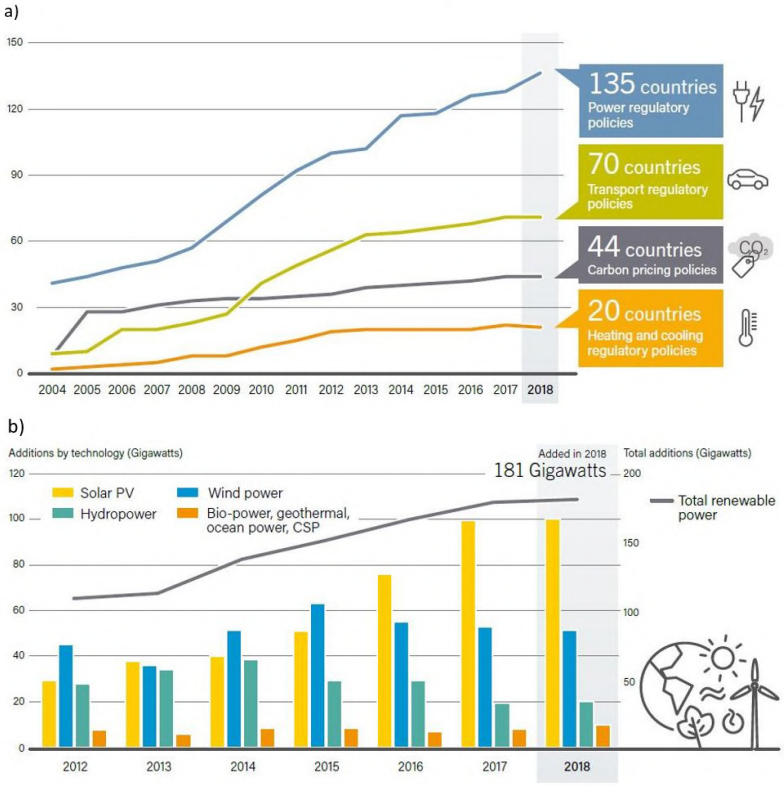

FIGURE 1.3: Number of Countries with Renewable Energy Regulatory Policies and Carbon Pricing Policies, 2004-2018 (a) and Annual Additions of Renewable Power Capacity, by Technology and Total, 2012-2018 (b)[7]

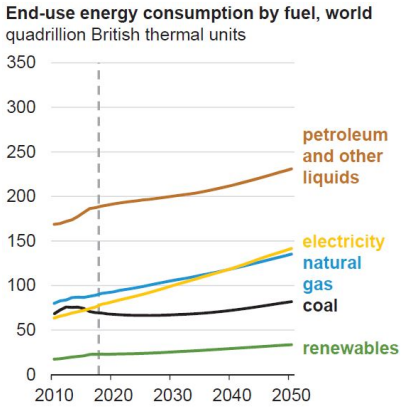

FIGURE 1.4: End-use energy consumption by fuel expressed in quadrillion British thermal unit, 2010-2050 [4].

shows how, despite the constant increase of utilization of renewables source of energy, also fossil fuels consumption will continue to grow (figure 1.4) [4].
Fossil fuels combustion will continue to be, as shown in figure 1.4b, the main source of energy, in the foreseeable future. It this clear, so, how it is necessary to undertake a parallel path besides an always more relevant investment and utilization of renewable energies: the development and optimization of technologies that are able to recover, convert and exploit the waste or excess products of energy transformations. In actual working conditions, the vast majority of energy is lost in heat. For instance, in Europe, almost 60% of the energy produced by power plants is lost in the wasted heat during production [9] and about 8% -15% is dissipated in heat inside power lines for transport and processing [10]. Therefore, only 35% of the energy produced in the plants reaches the places where it is actually consumed. Another example concerns the sector of road transport in which 40% of the energy in one car is lost in heat and

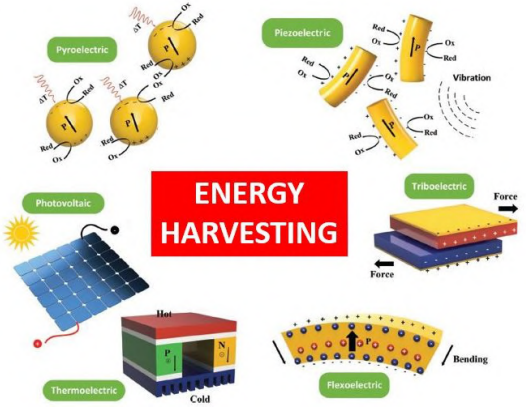

FIGURE 1.5: principal physical effects exploited in EH processes.

another 40% is used for engine cooling, leading to a 70% energy losses [11]. It is, therefore, crucial to find ways to recover wasted energy, in order to increase processes efficiency. From this concept, in last decades, it has been developed the concept of Energy Harvesting (EH) which can be defined as a process wherein sources of wasted energy such as mechanical load, vibrations, temperature gradients and light, etc., are scavenged and converted to obtain electrical power. The physical phenomena utilized for the conversion are numerous and diverse and the include: photovoltaic, pyroelectric effect, thermoelectric effect, piezoelectric effect as well as flexoelectric and triboelectric effects [12].
Since the main way to produce electricity consists in the combustion of fuel, it is clear how, among all the form of energies wasted, heat is the one that offers more potential for recovery. As explained

above, the amount of wasted heat is relevant in a number of processes, both in industry and transport for instance. The transformation from chemical (combustion of fuel), to thermal, to mechanical (rotation of a turbine), to electrical energy (through an alternator) represents the production system of around the 60% of energy worldwide [6, 7]. Efforts have been done to improve efficiency of these processes. In fact, the introduction of the so called cogenerative systems (or combined heat and power, CHP) allowed to reutilize the heat produced for practical purposes, as for example building heating, instead to use it for conversion in electricity. This allowed to bring efficiencies from 40% to around 80%. Nevertheless, dissipated heat remains consistent in many other systems and it is a great opportunity for energy recovery, the greatest in this field.

In a context like the one just described, research and study of thermoelectric devices, which are extremely useful in recovering heat and converting it into usable electricity, can offer a contribution to the achievement of a more sustainable world.

1.2 The Potential of Thermoelectricity

A thermoelectric generator (TEG) can be defined as a solid-state device capable of converting heat into electricity thanks to a difference of temperature in between a hot and a cold side. They are free of moving parts, they are silent, reliable and scalable, making them ideal for small, distributed power generation [10, 14]. Thermoelectricity has been successfully implemented since its discovery for temperature sensing in thermocouples, which remains nowadays their wider and the most present application in everyday life. Its use broadens to more hidden technologies which comprehend portable fridge cooling and power source for deep space missions. For instance, aerospace probes like Voyager 1, Voyager

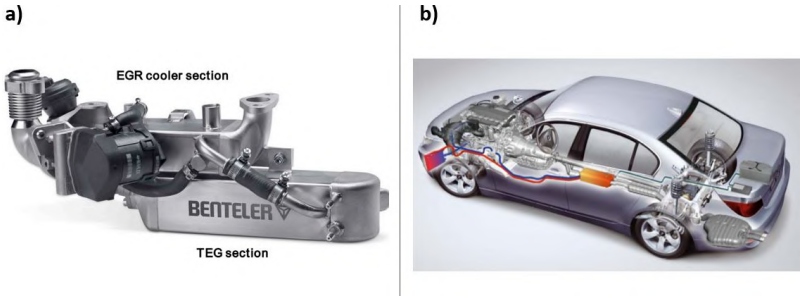

FIGURE 1.6: a) BMW waste recovery unit, consisting of a TEG section and a conventional cooler section; b) integration inside the vehicle.

2, Cassini or, recently, New Horizons are powered by thermoelectric generators with radioisotopes or RTGs (Radioisotope Thermoelectric Generators) that use the heat generated by the decay of the radioisotope ^{238}Pu to generate electricity with Si-Ge or PbTe thermoelectric modules[15].

Thermoelectricity, besides the aspects briefly presented above, has become more and more a niche field of research, because of the impossibility to overcome 5% efficiency of TEG. Therefore technology moved towards more efficient engines for energy production [4]. Only over the fist years of the 90s, with the advent of nanotechnology and nanostructuration, thermoelectricity has gained again high attention in scientific community, thanks to the renowned models presented by L. D. Hicks and Mildred Dresselhaus of the Massachusetts Institute of Technology [12, 13]. Today, attention towards thermoelectricity has increased again because of the necessity, as stated above, of pursuing a sustainable society to assure prosperity and health to the next generations, from an energetic and climatic point of view. Although thermoelectric generators, based on state-of-the-art materials, remain far from being competitive, in terms of efficiency, with more conventional engines, as

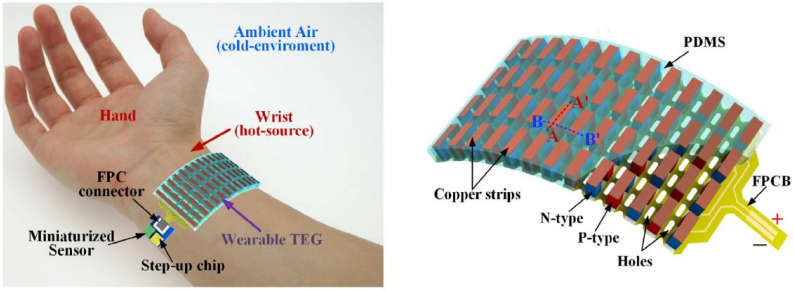

FIGURE 1.7: example of wearable thermoelectric device. It consists in 52 pairs of rectangular-shaped P-type and N-type thermoelectric legs embedded in Poly-Imide to guarantee flexibility and non-toxicity [21]

provocatively presented in [19], a big window of potentiality is opened when they are used in combination with other primary engines, providing a way to partially recover the waste heat and thus increase the overall efficiency of the engine.
A clear example of this application is in the automotive industry, where TEG has been successfully integrated to recover part of the 60% of energy lost in car fuel combustion. With the setup shown in figure 1.6, a TEG output of up to 200W has been achieved at a constant vehicle speed of 130 km/h. At this operating point and the corresponding exhaust gas temperatures, a temperature of 250°C is achieved at the thermoelectric material, indicating PbTe as the ideal foundation material for the modules [20].
Another thermoelectric application that has attracted attentions among researchers is wearable thermoelectric devices for micro-harvesting. It is in fact clear how self-rechargeable devices and consequently electronics able to harvest enough energy in order to recharge themselves, or at least to increase their operative time, would open new markets. Noting that human body constantly generates heat, micro-harvesting for powering wearable sensors

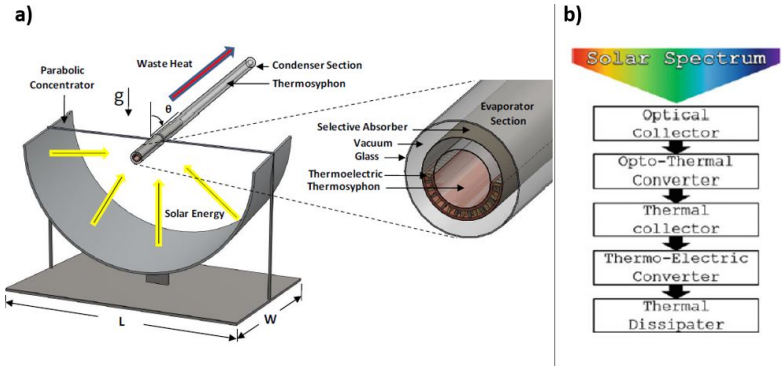

FIGURE 1.8: a) Schematic of a hybrid solar thermoelectric system (HSTEG) [24]; b) Scheme of the main components of a STEG system [25]

and electronics is extremely interesting as it would enable harnessing uninterrupted energy from body heat. Of course, there are some limitations for this application such as the high thermal resistance of human body, or the necessity to have a perfect contact between the skin and the device and, obviously, the non-toxicity of the materials that compose the wearable device. Meeting these requirements it is easier said than done. Despite that, many effort has been spent on this field, which remains one of the most promising thermoelectric application (figure 1.7) [21, 22, 23].
One of the most attractive application, where thermoelectricity can manifest its potential, is the exploitation of the heat produced by solar light. In this field, it is possible to distinguish two separates categories: Hybrid Solar-ThermoElectric Generators (HSTEGs), and pure ThermoElectric Generators (STEGs). Concerning the first ones, the general operating principle consists in the focusing of the solar energy, by a parabolic concentrator, on the evaporator section of the evacuated tube absorber (thermosyphon), which heats the thermoelectric hot side, causing temperature difference which produces electrical power [24]. A schematic picture of a HSTEG is

presented in figure 1.8a. Regarding the latter, as schematically illustrated in figure 1.8b, the system is generally made by an optical collector, which collects photons coming from the Sun; an opto-thermal converter, which converts photons into heat; a thermal collector, which drives the heat towards the thermoelectric converter; a thermoelectric converter, which converts heat into electricity and a thermal dissipation system, which dissipate heat at the TEG cold side. These technologies have attracted great attention in literature [24, 26, 27, 28, 29] and a detailed analysis of both, from a practical and theoretical point of view, can be found in [25].

To summarize, many efforts are ongoing towards more efficient and more easily implementable thermoelectrics. It appears plausible that beyond the niche fields of research, e.g. space missions, thermoelectrics has the potential to embrace a wider range of heat recovery applications, considering the percentage of energy wasted in almost every process. To make this possible, it is critically important to find new materials that could guarantee an acceptable integrability in the already existing technologies and, also, made of inexpensive, earth- abundant elements, in order to address the requirements imposed by sustainability criteria.

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CHAPTER 2

Thesis Background

2.1 Thermoelectric Effects and Efficiency

In 1794, Alessandro Volta, studying electricity-related effects on frog bodies in University of Pavia, observed contractions of legs caused by a difference of temperature of the solutions in which the legs were immersed, when a metallic arc was put in contact with the solutions (figure 2.1). He was the first to observe a thermoelectric phenomenon [1].
In 1821, the Estonian physicist Thomas Johann Seebeck discovered how a circuit composed by two dissimilar metals with junctions at different temperatures could deflect a compass magnet. He related such behaviour to a magnetic field generated by temperature difference and called the observed phenomenon "thermomagnetism" (figure 2.1) [2].
In 1834, the French watchmaker Jean Charles Peltier observed that if a current is passing through the junction of dissimilar metals, the junction is heated or cooled depending on the direction of the current. The scientist tried to correlate his discovery to Joule's heat dissipation, but he failed. The observed effect remained unexplained for many years [3].

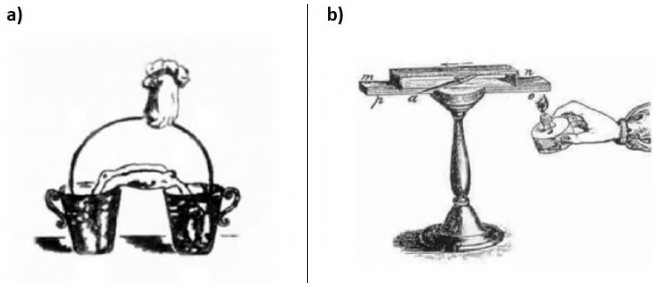

FIGURE 2.1: sketch of Volta (a) and Seebeck (b) experiments.

Only in 1854, William Thomson, known as Lord Kelvin, eventually proposed a comprehensive explanation for both Seebeck and Peltier effects [4].

Thermoelectric phenomena can be defined as non-equilibrium processes which connect differences in temperature to differences in voltage. As such, they allow for partial conversion of heat into electricity or the transfer of heat from a hot thermostat to a colder one. They are three and they are named after three scientists mentioned before: the Seebeck effect, related to the conversion of heat into electricity, and the Peltier effect, process opposite to the Seebeck effect, and which therefore concerns the possibility of transferring heat from a cold to a hot sink by applying an electric current. A third thermoelectric effect, the Thomson effect, was discovered later and allowed to demonstrate the connection between Seebeck and Peltier effect.

Next sections of this dissertation will be dedicated to a quick overview of the fundamental physical phenomena which rule thermoelectricity.

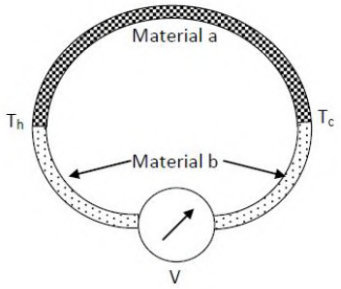

FIGURE 2.2: Seebeck effect in an open circuit consisting of two different materials. The temperature difference between the two materials generates a potential difference measured by a voltmeter at the ends of the circuit.

2.1.1 Seebeck Effect

As briefly mentioned above, Seebeck effect was named after the Estonian scientist, even if he misinterpreted his results and link them to magnetism. It was in 1823 when the Danish physician Ørsted corrected Seebeck interpretations and showed that the temperature gradient in the two materials generated a difference in electrical potential (in the two junctions at different temperatures), giving rise to a flow of current which, in agreement with Ampere's law, generated a magnetic field that deflected the needle of the compass.
Therefore, the Seebeck effect explains why a potential difference is generated when the junction between two different conductive materials is heated. Now, considering the open circuit in figure 2.2, it is possible to measure a potential difference ΔV, at the ends of the circuit, when a temperature difference ΔT is applied to the joints between the material A and material B.
The proportionality coefficient between the measured potential and

the difference of temperature is called *Seebeck coefficient* (α) , conventionally measured in $\mu V/K$ or mV/K and defined as:

$$\alpha = -\frac{\Delta V}{\Delta T} \tag{2.1}$$

Seebeck coefficient is positive for p-type materials and negative for n-types; its sign gives, therefore, the main carriers of the material. When one of the two junctions is heated, the majority of charge carriers, holes or electrons, have an energy and speed higher than those present in the cold junction. This generates a diffusion of the carriers from the hot side towards the cold side, thus creating a thermoelectric potential. For this reason, Seebeck coefficient can also be interpreted as the amount of entropy carried by charge carriers of the material [5].

2.1.2 Peltier Effect

Another phenomenon, closely related to Seebeck effect, is Peltier effect. In fact, it can be defined as the amount of reversible heat absorbed or released at the interface between two different materials crossed by a current. With reference to the circuit presented in figure 2.3, Peltier coefficient is defined as the ratio between the quantity of heat per unit of time absorbed or released at the junction of two different materials and the electric current passing through the circuit:

$$\Pi_{a,b} = \frac{dQ/dt}{I} \tag{2.2}$$

Where $\Pi_{a,b}$ is the *Peltier coefficient* of the junction, dQ/dt is the heat absorbed or released by the material and I is the current through the junction. The direction of the current determines the release or the absorption of heat at the junction. Similarly to the Seebeck coefficient, Peltier coefficient can be positive or negative, for p-type materials and for n-type materials respectively.
From a thermodynamic point of view, Peltier effect could be defined as the reversible change in heat at the interface between two

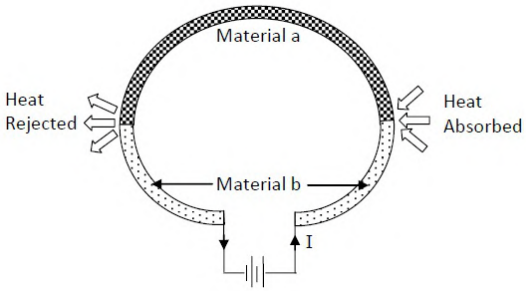

FIGURE 2.3: Peltier effect in a circuit consisting of two different conductive materials a and b traversed by a current I.

different materials, caused by the change in the entropy of an electrical charge [6].

2.1.3 Thomson Effect and Kelvin Relations

Considering a conductor, such the one shown in figure 2.4, with a thermal gradient dT/dx along the x direction and with a current density $\mathbf{J_x}$ flowing along the x direction only, it is possible to identify two thermal effects inside the material: the first is Joule effect which always corresponds to dissipated energy and is due to the increase the temperature as a result of the resistance opposed by the material to the passage of the current; the second effect, dependent on the temperature gradient along the material, represents instead the Thomson heat released or absorbed by the conductor. In such material, the quantity of heat produced per unit of time and per unit of volume is given by the following equation:

$$\dot{Q} = \frac{\mathbf{J}_x^2}{\sigma} - \mu \mathbf{J}_x \frac{dT}{dx} \tag{2.3}$$

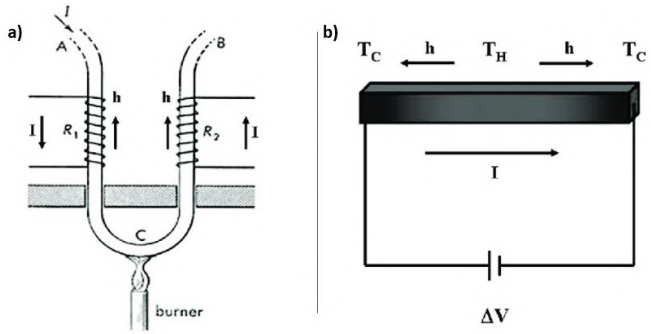

FIGURE 2.4: original sketch of Thomson experiment (a); Single conductive material to explain the thermoelectric effect postulated by Thomson, with a temperature gradient and a current flowing along x direction.

where the first term, dependent on electrical conductivity σ and the square of density current, can be traced back to the heat developed by Joule effect. The second term, linearly dependent on current density and gradient of temperature, represents the Thomson effect. The coefficient in the second term takes the name of *Thomson coefficient* which is defined as the rate of heating per unit length that results from the passage of unit current along a conductor in which there is unit temperature gradient. Always Lord Kelvin in 1854, after his own discovery of the Thomson effect managed to unite the three thermoelectric phenomena in the so-called Kelvin relations:

$$\mu = \frac{Td\alpha}{dT} \tag{2.4}$$

$$\Pi = T\alpha \tag{2.5}$$

Kelvin relations allow to deduce all the thermoelectric properties of the material through the knowledge of the Seebeck coefficient,

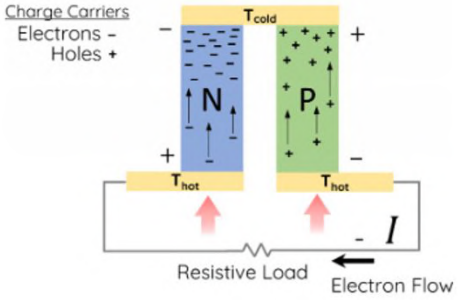

FIGURE 2.5: typical scheme of a thermoelectric generator for converting heat into power electrical, consisting of the junction of an n-type and p-type material and connected to an electrical resistance.

which is the most easily measurable thermoelectric quantity experimentally [7].

2.1.4 Thermoelectric Efficiency

As mentioned in Chapter 1, a thermoelectric generator (TEG) can be defined as a solid-state device capable of converting heat into electricity (or vice versa) thanks to a difference of temperature in between a hot and a cold side, with an efficiency η. It is generally composed by several junctions between two thermoelectric materials, one with $\alpha(T)$ positive (p-type) and the other with $\alpha(T)$ negative (n-type), conventionally called *"legs"*, connected, electrically in series and thermally in parallel, by a third conducting material. Considering the circuit illustrated in Figure 2.5, which is maintained by the heat source at a temperature difference $\Delta T = T_H - T_C$, where T_H is the hot side temperature and T_C is the cold side temperature, and connected to a load resistance R_L, it is possible to

define the electrical output power produced by the TEG as:

$$W = \left[\frac{(\alpha_p - \alpha_n)\Delta T}{R_L + R}\right]^2 \tag{2.6}$$

where α_p and α_n are the Seebeck coefficient of the p-type and n-type legs respectively and $R = R_p + R_n$ which are the materials resistance. The amount of heat per unit of time entering from the side hot is definable as:

$$\frac{dQ}{dt} = (\kappa_p + \kappa_n)\Delta T + (\alpha_p - \alpha_n) I T_c - \frac{1}{2} I^2 R \tag{2.7}$$

where κ_p and κ_n are the thermal conductivities of the materials and I is the current flowing through the TEG.

By combining eq.2.6 and eq.2.7, it's easily defined the efficiency η of the TEG:

$$\eta = \eta_C \frac{m/(m+1)}{1 + \frac{m+1}{Z_{12} T_H} - \frac{1}{2}\frac{\Delta T}{T_H m+1}} \tag{2.8}$$

where $m = R_L/R$ and $\eta_C = \frac{(T_H - T_C)}{T_H}$ and Z_{12} is the figure of merit of the TEG, defined as:

$$Z_{12} = \frac{(\alpha_p - \alpha_n)^2}{(\sqrt{\kappa_p \rho_p} + \sqrt{\kappa_n \rho_n})^2} \tag{2.9}$$

where ρ_n and ρ_p are the resistivities of the n and p legs.

Considering a single material, it is possible to express the thermoelectric efficiency through the figure of merit:

$$Z = \frac{\alpha^2 \sigma}{\kappa} \tag{2.10}$$

where σ is the electrical conductivity of the material and κ, which is the thermal conductivity of the material, is given by the contribution of κ_l, owed to the lattice thermal transport, i. e. phonon contribution, and κ_e, owed to the charge carrier ability to transport

heat. Conventionally, the figure of merit is expressed in its dimensionless form, zT, which is obtained by multiplying eq.2.10 by the absolute temperature T. The numerator of eq.2.10 describes the electronic performance of the material:

$$PF = \alpha^2\sigma \tag{2.11}$$

It is named *Power Factor* (PF) and it is widely utilized for describing the electronic compartment of a thermoelectric material [8].

2.1.5 Optimization Of Figure Of Merit

Figure 2.6 shows the trends of the different properties of a thermoelectric material and of the figures of merit that describes the thermoelectric efficiency [9]. Considering figure 2.6 and equation 2.10 it is clear how the properties that make a material a good thermoelectric material are strongly connected to each other. Figure of merit zT shows, in fact, that a good thermoelectric material has to have, at the same time, good electronic properties and bad thermal properties. Decoupling of electrical conductivity from thermal conductivity is, in fact, one of the greatest challenge that thermoelectricians have to face, since, normally, the two dimensions go in the same direction. Moreover, PF trend shows that there is maximum, reached in the area of heavily doped semiconductors, given that an increasing of electrical conductivity leads to a decreasing of Seebeck coefficient. Therefore, lots of effort must be concentrated in finding always new ways to decrease, as much as possible, lattice contribution to thermal conductivity, κ_l, without affecting too much electronic properties of the material.
Thus, the perfect thermoelectric material should follow the *phonon glass-electron crystal* concept: it should conduct charge carriers like long-range ordered crystalline materials (having large σ values) and should conduct thermal current like amorphous ones (having small κ values). In other words, a material in which the phonon mean free paths are as short as possible and in which the electron

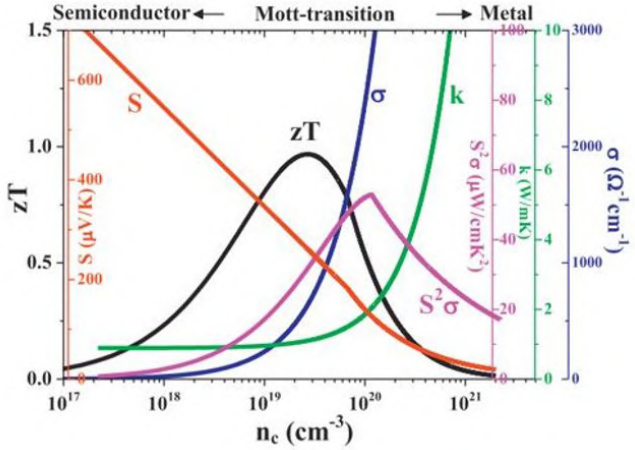

FIGURE 2.6: *PF* and *zT* trend versus carrier concentration. It is noted the interdependence of the different properties [9].

mean free paths are as long as possible [10]. Starting from this idea several approaches are possible to create or obtain an efficient thermoelectric material:

- identify elemental solids which exhibit good electronic properties, but high thermal conductivities. By combining them, one can possibly obtain a reduction in κ of one order of magnitude, still preserving the starting electronic features. Following the same path, the possible presence of additional disorder sources, such as vacancies or isotopic substitutional disorder, may contribute to further reducing the thermal conductivity value. This method can be simply defined as *alloying* and it results more effective when it involves heavy atoms;

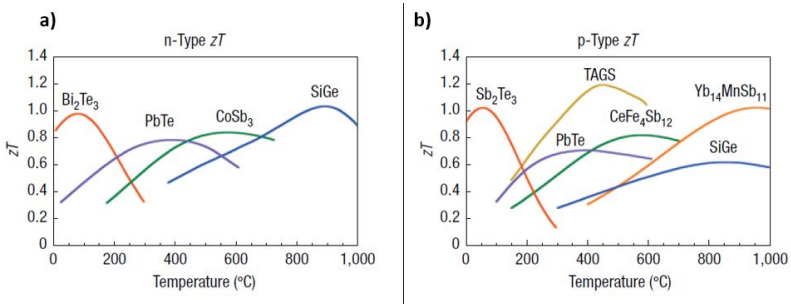

FIGURE 2.7: zT of state-of-art Thermoelectric Commercial Materials n-type (a) and p-type (b)[14]

- another approach consists in choosing materials characterized by atomic framework that shows voids, channels, layers can be conveniently filled with heavy, small ions able to loosely rattle about inside the framework, thereby degrading phononic propagation inside the material. This path establish the utilization of the so called *complex lattice structures* [11];
- since 1993, year of the works of Dresselhaus and Hicks [12, 13], reduction of the phonon mean free path due to enhanced layer scattering effects and quantic confinement in nanostructured semiconductor superlattices and low-dimensional systems has been intensively explored.

Following mainly the three paths presented above, a number of materials has been presented in literature in the past decades. Regarding the first category is worth to mention, for instance, BiSb [15, 16], ZnSb [17] and SiGe [18, 19] alloys which are of extensive use in current TE devices as well as alloys with binary tellurides like Bi_2Te_3 [20, 21], Sb_2Te_3 [22], PbTe [23] and GeTe [24]. Among the *complex lattice structures* one can count compounds as Half-Heusler alloys [25, 26, 27, 28], skutterudites [29, 30, 31] or clathrates [32, 33].

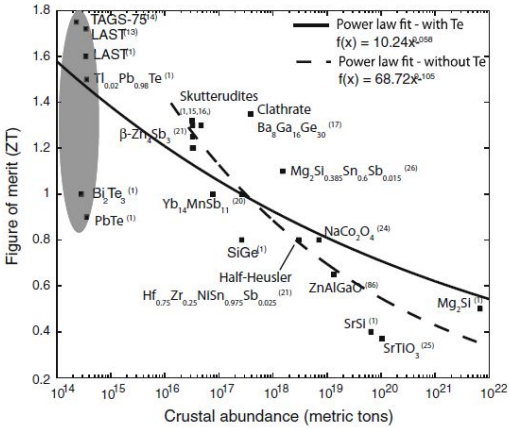

FIGURE 2.8: zT versus crustal abundance for bulk thermoelectric materials [34].

Considering the brief list of materials presented above and figure 2.7 too, it is noted how classic bulk thermoelectric materials are composed by mostly heavy elements. Figure 2.8 shows the figure of merit zT vs the earth crust abundance expressed in metric tons, for bulk thermoelectric materials [34]. From the graph, a trend is easily pinpointed: the highest zT values are obtained with the least crust abundant materials. This fact is greatly detrimental for thermoelectric research, development and wide diffusion, for a number of reasons: the utilization of rare elements leads to a consistent increasing of the price for TEG production, quickly leading to an economical unsustainability and, equally, to an environmental unsustainability, since their use would exhaust them. Moreover, the majority of these elements are very toxic, making their utilization even less attractive. A trend reversal is necessary to make thermoelectricity suitable to the mandatory requirement of sustainability. A push in this direction can be given by *material nanostructuration* which can make adapt materials that would not be usable in their bulk form and can decouple thermal and electrical properties.

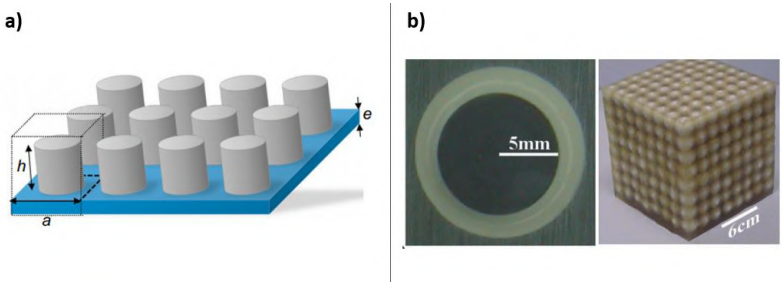

FIGURE 2.9: Schematic view of a phononic crystal made of a square lattice of finite cylinders deposited on a homogeneous plate [48] (a) and the first acoustic metamaterial presented in literature composed by centimeter- sized lead balls coated with a 2.5-mm layer of silicone rubber, in a cubic structure of 8 x 8 x 8 [51] (b).

This is, for instance, the case for a number of oxides, both p-type ($Ca_3Co_4O_9$, in form of sintered powder [35]) and n-type (as $SrTiO_3$, both in form of sintered powder [36], or thin films [37], ZnO thin films doped with Al, Ga or In [38, 39]), nanowires (NW) [40, 41], superlattices [42, 43, 44] as well as polycrystalline nanomaterials [45].

Recently, it has been explored the possibility to exploiting the difference between the phonon and the carrier mean free paths (MFP) for thermal conductivity reduction [46, 47]. This can be done by phonon scattering through solid imperfections, like point defects, aggregates and nanovoids. In this context, is worth to mention the concept of *phononic crystal* and *acoustic metamaterials*. Phononic crystals are defined as heterogeneous elastic media composed of a periodic array of inclusions embedded in a matrix [48]. Their main characteristic is the opening of a gap based on the destructive interference of the scattered waves by the inclusions and therefore creating a phonon band gap [50]. An acoustic metamaterial, instead, can be defined as a material designed to control, direct, and

manipulate sound waves [49]. An example of this two categories of material is shown in figure 2.9.

Despite the promising reduction of the thermal conductivity at which these methods can lead, the presence of inclusions, voids as well as grain boundaries inside the electronic pathway inevitably brings a detrimental effect to the electronic properties. Moreover, production of nanomaterials that presents a periodic substructure can be very difficult and expensive, not to mention their scalability.

2.2 Silicon as Thermoelectric Material

Silicon is the best known and most exploited semiconductor material. It is used, together with its compounds, in many technological sectors, especially in electronics, micro/nanoelectronics, of which it is a fundamental component, in the steel industry, in telecommunications and also as a material for photovoltaic applications, just to mention a few examples. The great success that silicon has in our age must not be attributed solely to its greatness availability (it is in fact the second most abundant element on the earth's crust, being around 27.7% in weight) and its relatively low cost, but, above all, for its chemical-physical and thermodynamic properties and the great know-how accumulated in the last decades. It is indeed possible to have a great control on its purity in the manufacturing phase and, with the development of nanotechnologies, it is possible to create silicon-based nanometric structures that can be easily integrated into different applications. Moreover, one of the greatest advantage of silicon is the possibility to tune very precisely its electronic properties through doping. In fact, silicon can be doped with elements of the III group (specifically Al, Ga, B, In) to obtain p-type silicon. Doping with elements of the V (specifically P, Ar, Sb) group allows to obtain n-type silicon, as shown in figure 2.10.
It is therefore not surprising, from what has just been said, that silicon thermoelectric properties have already been investigated. The

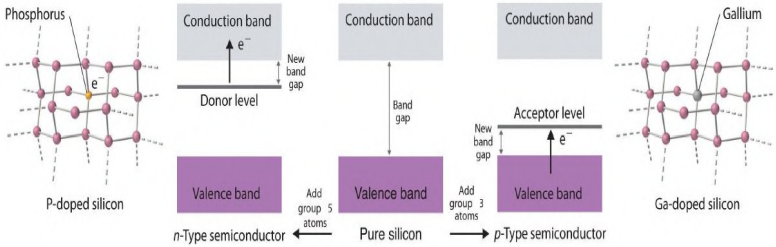

FIGURE 2.10: Band structure of intrinsic, p-doped and n-doped silicon. It is noted the inclusion of P (donor) and Ga (acceptor) inside silicon crystal structure.

first thermoelectric measurements on monocrystalline silicon were made by Geballe and Hull [52] in the 1950s. Monocrystalline silicon, in the case of the optimum carrier concentration of $1.10^{19} cm^{-3}$ at room temperature (see figure 2.6) has a relatively high PF, comparable to Bi_2Te_3 (3.5 mW/m^2K for heavily doped Si, 4 mW/m^2K for Bi_2Te_3). Contrarily, the large value of thermal conductivity (around 148 W/mK at room temperature) contributes to maintain low the figure of merit zT of silicon around 0.01, too low to be useful for thermoelectric applications. It is undeniable that, as stated in the previous section, research in thermoelectric silicon needs to move towards new methods and techniques to lower the thermal conductivity of silicon without decreasing, at the same time, electrical conductivity. Nanostructuration could be the answer and, among the various possibilities, this manuscript will focus on silicon nanophononic metamaterial and on silicon nanowires.

2.2.1 Silicon Nanophononic Metamaterial

The concept of a *nanophononic metamaterial* (NPM) has been introduced by *Mahmoud I. Hussein* of University of Colorado first in

2014 [53] and deepened by a series of successive investigations regarding the underlying physics, performance characteristics and geometries [54, 55, 56, 57]. The basic idea, in this new class of material, is to find a new path for the reduction of the thermal conductivity and consists in a crystalline medium, serving as a host, and an array of intrinsic nanostructures which serve as nanoresonators. This structure consists in an array of nanopillars on top of a thin membrane Both the base material and the nanoresonators can be composed by any material, but they are, typically, made out of a semiconductor. Among the numerous semiconductor materials, silicon is the one suggested as the NPM foundation by the authors, both for economical reasons and for the great know-how on it which allows various strategies for silicon nanostructuration. Given that, NPM can possibly consist of an array, or a forest, of silicon nanopillars distributed on one (or two) face(s) of a free-standing monocrystalline silicon membrane free of interior scatterers. This kind of configuration causes the coupling between the local resonances of the substructures (silicon nanopillars/forest) and the heat carrying phonons traveling in the host material (silicon membrane). This coupling creates a mechanism of resonance hybridization between vibration modes of the local substructure (vibrons[1]) and wavenumber-dependent wave modes of the host medium (phonons). It is possible to consider that in a nanopillared membrane, phonons motion is confined to the in-plane directions within the base membrane, while vibrons move primarily in the domain of each nanopillar; the former may be viewed as traveling waves propagating in an infinite medium, and the latter may be viewed as standing waves taking shape in finite structures branching out orthogonally from this infinite medium.
The authors, starting from the Boltzmann transport equation and following the single-mode-relaxation time approximation, defined the lattice thermal conductivity (κ) of a membrane-like crystalline

[1] the term vibron is utilized in numerous and often not congruent way in literature. In this thesis, vibron is referred to the vibrational modes of the pillars, where Bloch-type wavefunctions are ill-defined

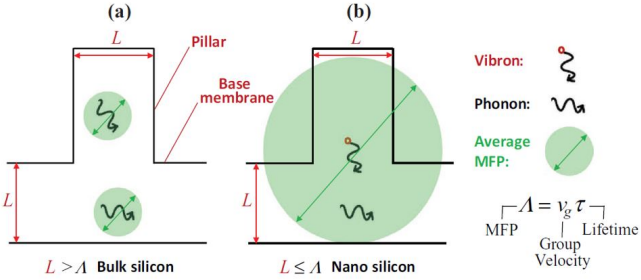

FIGURE 2.11: Schematic of a unit cell of a nanopillared silicon membrane. If the average MFP is smaller than the characteristic dimensions of the nanostructure, the medium behaves like a bulk material (a). If the average MFP is at least on the order of the feature sizes, then the system behaves as a nanostructured material (b) [57]

material with free-surfaces as [53, 57]:

$$\kappa = \frac{1}{V}\frac{A_c}{4\pi}\sum_m \int_0^{\kappa_{max}} C(k,m)v_g^2(k,m)\tau(k,m)\kappa d\kappa \tag{2.12}$$

where A_c is the unit-cell cross sectional area that is an area of dimensions $aA_x \times aA_y$, with a is the lattice constant; V is the unit-cell volume; C, v_g, τ are respectively specific heat, group velocity and scattering time constant (lifetime). The integration is over all phonon wavenumbers from $k = 0$ to $k_{max} = \pi/aA_x$ for branch m and the summation is over all the phonon branches. $k = 2\pi/\lambda$, with λ as the wavelength. The authors calculated the phonon specific heat C for each mode following the Bose-Einstein distribution and can be defined as:

$$C(\kappa, m) = k_B \frac{\chi^2 e^\chi}{(e^\chi - 1)^2} \tag{2.13}$$

where k_B is the Boltzmann constant and $\chi = \chi(\kappa, m) = \hbar\omega/k_B T$, where T is the temperature, ω is the frequency, and $\hbar$ is the reduced Planck constant. Equation 2.12 is applied to the unit cell shown in the upper part of figure 2.13. Thermal conductivities of the different NPMs are constructed through the summation of all the phonon modes in the spectrum and through the integration over the Brillouin zone along the direction of interest.
In such configuration, the overall lattice thermal conductivity gets reduced by primarily three different mechanisms:

- the phonon group velocities decrease at the coupling locations in the phonon band structure, as is shown in figure 2.12(a). Stronger couplings generate sharper curve flattenings and larger reductions in the group velocities;

- localization of the atomic motion occurs exclusively in the nanopillar region. The author claims that the nanoresonator is acting like a "phonon siphon" sucking the energy from the base membrane and retaining it in the nanopillar portion, leaving an almost "thermal silence" in the base membrane portion. This phenomenon is significant because these localized modes appear in the band structure as flat (or almost flat) dispersion relations and thus exhibit zero (or-near-zero) group velocities (figure 2.12(b));

- the phonon lifetimes decrease due to changes in the scattering precesses, including both phonon–phonon scattering and boundary scattering. Shorter life times implies shorter mean free paths. This must not interfere with the wave mechanisms of hybridization described above in order to contribute to the thermal conductivity reduction.

Equation 2.12 shows that thermal conductivity directly depends on the square of phonon group velocity and as well as on the phonon scattering time constant. The drop of these two quantities (particularly of the group velocity) leads inevitably to a strong reduction

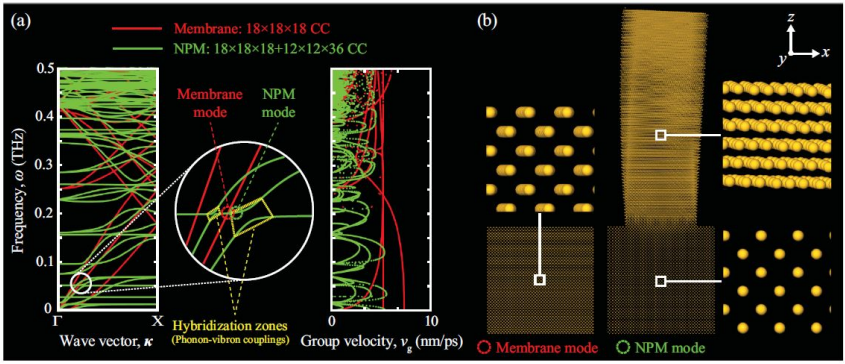

FIGURE 2.12: Phonon band structure and group velocity distribution of a silicon membrane with (green) or without (red) silicon nanopillars standing on one surface (a). Atomic displacements for a heat carrying phonon mode in the acoustic regime of a uniform membrane compared to NPM atomic displacements of the same mode (b) [56]

of the thermal conductivity. The architecture consisting of a free-standing silicon film with an array of silicon nanopillars distributed on the surface allows to leave the main body of the base membrane free of any voids, inclusions, as well as grain boundaries or defect of any kind, in the case of monocrystalline silicon. The membrane base serves as the electron pathway, this layout is very favorable for electron transport, since electron scattering occurs only near the membrane surfaces and not in the bulk. Compared to the other phonon engineering techniques that allows a creation of a phonon band gaps, where the scatterers are in the main body of the medium (e.g. phononic crystals or acoustic metamaterials), this setup provides the unique advantage of practically decoupling the lattice thermal conductivity from the Seebeck coefficient and the electrical conductivity, essential to create a significant increase in zT.

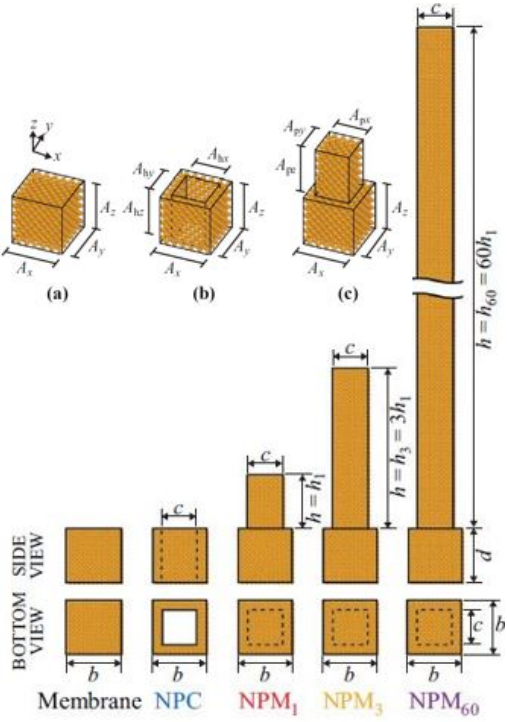

FIGURE 2.13: Schematics representing the five membrane-based material systems considered: NPM_1, NPM_3 and NPM_{60} are identical except for the nanopillar heights. The width of the nanoholes in NPC is identical to the width of the nanopillars. All membranes have identical base dimensions and thickness. Atomic-scale models of uniform membrane (a), membrane based nanophononic crystal (b) and membrane-based nanophononic metamaterial (c), are shown above [57].

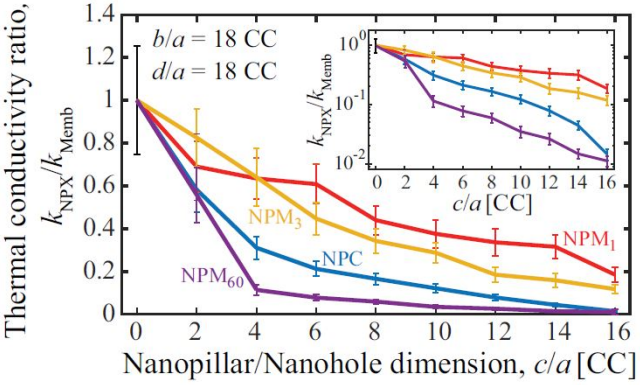

FIGURE 2.14: effect of the nanopillar width for three membrane-based NPMs with different nanopillar heights on the thermal conductivity reduction [57].

Another advantage that NPM shows compared to phononic crystals or acoustic metamaterials is that while the latter affect mostly the hertz-to-megahertz operational range and typically revolve around a single frequency or a narrow range of frequencies, the former thanks to the nanoscale thermal transport which is highly nonlinear, extends well into the terahertz frequency regime. Moreover, this strategy could make suitable for thermoelectric application a material as monocrystalline silicon, much more attractive than classical thermoelectric materials, for all the reasons illustrated in the previous section.

In their simulations, Hussein and his research group explored some different configurations both of the membrane and the nanopillars on top of it. They also considered a nanophononic crystal (NPC), as comparison, and geometrical parameter of the different nanopillars considered are shown in figure 2.13, as well as the unit-cell model of the suspended membrane with dimensions A_x x A_y x A_z. For the

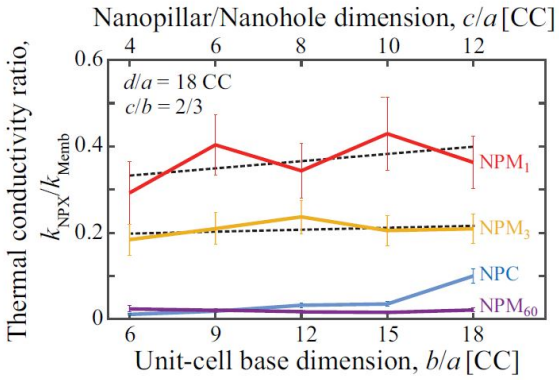

FIGURE 2.15: Effect of varying unit-cell base size on thermal conductivity reduction versus separation distance between nanopillars for three NPMs with different nanopillar heights but a fixed membrane thickness [57].

NPM unit cell, a nanopillar is erected on top of the base membrane and its dimensions are A_{px} x A_{py} x A_{pz}.
Figure 2.14 displays the effect of the nanopillar width for three membrane-based NPMs with different nanopillar heights on the thermal conductivity reduction, considering a fixed membrane thickness and a fixed separation distance between the nanopillars. All results are normalized with respect to the thermal conductivity of a uniform membrane with the same thickness and the inset shows the same results in logarithmic scale. The first observation is that the in plane thermal conductivity is massively reduced in all the cases presented in the graph. Particularly, it appears that both the increasing of width (c) and height (h) of the nanopillars lead to a decrease of $\kappa_{NPM}/\kappa_{Memb}$. The authors explain that this reduction is mainly due to the enrichment of the phonon band structure with a higher vibrons-to-phonons ratio. This phenomenon gets more

significant with the increasing of nanopillars dimensions and contributes to the physical effects, described above, that are the foundation of thermal conductivity reduction in NPM.
Figure 2.15 considers again NPM_1, NPM_3 and NPM_{60} and NPC in plane thermal conductivity versus separation distance between nanopillars with a fixed membrane thickness. It is observed that as the size of NPM_1 is proportionally increased in the lateral directions, the ratio $\kappa_{NPM}/\kappa_{Memb}$ tends to increase. However, this increase appears to be less significant for NPM_3, while NPM_{60} experiences no noticeable change as the lateral size of the unit cell is increased. As reported by Honarvar and Hussein [56], the slope of thermal conductivity trend with size may be inverted when the volume of the nanopillar is kept higher than the volume of the base-membrane portion. This phenomenon has been described as the *"compensatory effect"*.

In summary, nanophononic metamaterials enable local resonance to mix in with conventional phonon transport mechanisms leading to thermal conductivity reduction through group velocity reductions, mode localizations and phonon-vibron coupling across the entire spectrum, differently from conventional technique. A NPM with tall nanopillars, with 79% nanopillar coverage, is predicted to exhibit $\kappa_{NPM}/\kappa_{Memb} = 0.9\%$, leaving the base membrane free from any defect and, therefore leaving untouched the electrical conductivity, ideal for increasing the thermoelectric figure of merit zT. Moreover, the local resonances are phase independent which makes NPM free from necessities of periodicity or specific geometries, a huge advantage from an experimental point of view. Moreover, the utilization of silicon as foundation material of NPM may open a new window on thermoelectric field. Clearly, NPM upscaling is critical since, as the unit-cell feature sizes start to be comparable to the MFP distribution, classical phonon–phonon scattering mechanisms will be prevalent and the effect of resonance will gradually diminish. How far one may go in upscaling before this limit becomes practically detrimental remains an open question.

2.2.2 Silicon NWs for Thermoelectricity

Theoretical studies predict a large enhancement of zT inside NWs due to their stronger quantum confinement and phonon scattering, in comparison to their three-dimensional counterparts [12]. As claimed in the previous section, many materials have been explored in form of NWs for thermoelectric applications, but, still for the same reasons, silicon is one of the most attractive. In 2008, Hochbaum and Boukai reported [58, 59] zT values around 0.6 and 1 at 300 K and 200 K, respectively, in silicon NWs. Such high values are possible thanks to the phonon scattering effects due to the wall roughness that characterized these NWs morphology. Numerous works, both experimental and theoretical [60, 61, 62, 63], have demonstrated that NWs surface roughness influences the conduction of phonons even more than NWs diameters, allowing to reach thermal conductivity values below the so-called Casimir limit, which is the minimum thermal conductivity theoretically obtainable when a completely diffusive phonon scattering on the nanowire surface is assumed [63].

From the data presented above, Si NWs seem to be a promising thermoelectric material when their dimensions/roughness are adapted to allow phonon scattering phenomena, but not so small to cause electron scattering, leaving untouched the electrical conductivity. The main problem about thermoelectric Si NWs is their integrability in efficient TEGs: there is, in fact, the necessity to create large areas of NWs array, in order to have a satisfying power output. Numerous work are present in literature regarding the integration of Si NWs arrays in thermoelectric devices [65, 66, 67, 68, 69]. Their thermoelectric properties have been measured and it has been proved how the porosity of the NWs is beneficial for the Seebeck effect and, as well, for thermal conductivity reduction. Thanks to these factors, Si NWs arrays reached zT values of around 0.5 at room temperature [70], proving their potentiality in thermoelectric applications.

Given the great knowledge on silicon properties and nanostructuration, silicon NWs synthesis techniques range from *bottom-up* to *top-down* approaches. One of the most common method, firstly reported in 1964 by Wagner and Ellis [71], is the synthesis of silicon NWs via Vapour–Liquid–Solid (VLS) growth by using gaseous SiH_4 as precursor and Au nanoparticles as catalysts. At high temperatures, an eutectic alloy is formed by the metal and Si which is supplied by a precisely calibrated SiH_4 (or others silicon-based gases) flux. At this point, supersaturation of the melt occurs and the liquid alloy phase is transformed to solid Si, crystallized under the metal nanoparticle. In this way, crystalline silicon nanowhiskers grow perpendicularly to the substrate [72, 73]. However, VLS and related methods, such as Molecular Beam Epitaxy (MBE) [74], have the great disadvantage of requiring high temperatures, long times, being the growth rate, for VLS silicon NWs at 400 °C [75], 0.048 $\mu m/min$, as well as high vacuum. They are, in fact, very expensive techniques from an energetic point of view. Moreover, it is difficult to obtain very dense NWs arrays on large areas, necessary for having a good thermoelectric output, and crystal quality control of the obtained NWs is very complicated and delicate, requiring a strict control on growth parameters.
The *top-down* approaches have the advantage of starting from macroscopic structures, such as crystalline silicon wafers that allow a great crystalline quality as starting point. Most of them, as standard processes for integrated circuit fabrication, rely on a necessary step of lithography in the substrate, that can often be complicated and a big obstacle for the exploitation of these technique. Though, when periodicity is not required, *Metal-assisted Chemical Etching* (MaCE) is the technique that has attracted the majority of attentions in literature for several reasons. MaCE, in fact, is a simple and low-cost method that allows the fabrication of various Si nanostructures, on large areas, using wet chemistry, with the possibility to control different parameters, without requiring high vacuum or high temperatures. Furthermore, it enables control of the

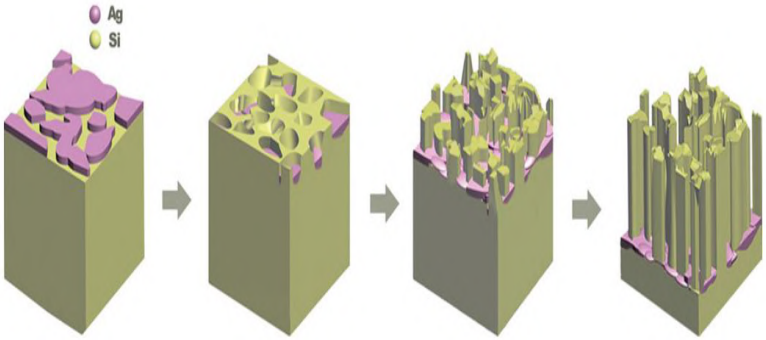

FIGURE 2.16: Schematic of Metal-assisted Chemical Etching process. The illustration shows a *two-step*, silver assisted MaCE [82].

orientation of Si NWs relative to the substrate, very high aspect ratio and a generally good crystal quality [76, 77, 78, 79]. In a typical MaCE procedure, a Si substrate, partially covered by a noble metal, is subjected to an etchant composed of HF and an oxidative agent. The process is based on the local oxidation of silicon, catalyzed by the noble metal particles, and on the removal of the generated silicon dioxide by hydrofluoric acid. MaCE processes can be *one-step*, when the catalyst acts also as oxidant in the solution, or *two-step*, in which there is firstly a deposition of noble metals nanoparticles (typically Au or Ag nanoparticles via thermal evaporation [80] or sputtering [81]) followed by the immersion in a solution containing an oxidant (e.g. H_2O_2) along with HF. A detailed analysis on *one-step* MaCE mechanism will be provided in the next Chapter.

Si NWs, in summary, offer a great opportunity for the development of silicon-based thermoelectric devices, both for the enhancement

of the figure of merit that is possible to reach through 1D Si nanostructuration and for the numerous ways that silicon technology offers in the realization of these nanostructures.

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CHAPTER 3

Metal-assisted Chemical Etching on Silicon

As mentioned in the previous chapter, Silicon MaCE is one of the most appealing and widespread method for Si NWs formation. In fact, MaCE meets essential requirements such as low production costs and the possibility of controlling wire length, orientation, doping type, doping level and enabling very high aspect ratios. Moreover, crystalline quality of Si NWs obtained by MaCE is generally high, with low densities of crystallographic defects. This chapter [1] focuses on NWs formation in one-pot Silver-assisted Chemical Etching (SaCE) [1]. Generally, SaCE is a localized electrochemical process where Ag^{+} ions reduce to metallic Ag while Si is oxidized to Si^{4+} and is then removed from the surface as SiF_6^{2-}. Ag particles are also catalytic centres, acting as favourite Ag^{+} reduction sites and then localizing Si oxidation, which is followed by HF chemical etching. Despite its seeming simplicity, the dependence of the SaCE process on Si doping (level and type) and temperature is rather complex. Therefore, in the next sections the results of an extended analysis of the interplay among doping level and type of

[1] This Chapter mostly reports results appeared in S. Magagna, D. Narducci, C. Alfonso, E. Dimaggio, G. Pennelli, A. Charaï, 'On the mechanism ruling the morphology of silicon nanowires obtained by one-pot metal-assisted chemical etching', Nanotechnology, 31 (2020) 404002.

Sample	Dopant	Doping (cm^{-3})	Fermi Energy (eV)
p(B)	Boron	2 x 10^{15}	-5.19
p(B)+	Boron	1 x 10^{17}	-5.29
p(B)++	Boron	4 x 10^{18}	-5.39
n(P)	Phosphorus	1 x 10^{15}	-4.60
n(P)+	Phosphorus	1 x 10^{17}	-4.48
n(P)++	Phosphorus	8 x 10^{18}	-4.36
n(As)+	Arsenic	8 x 10^{17}	-4.42
n(As)++	Arsenic	2 x 10^{19}	-4.34

TABLE 3.1: Schematic of the different substrates utilized for samples preparation. Fermi levels are calculated with respect to the vacuum level.

silicon, nanowire nanomorphology and the parameters controlling the chemistry of the etching process will be reported.

3.1 Samples Preparation and Characterization

The starting point of SaCE is a monocrystalline Si wafer. In order to have a broad view on the NWs obtained in different conditions, substrates vary in characteristics and they are summarized in Table 3.1. The crystal orientation of the substrates is [100]. Wafer thicknesses are various and they will be specified when necessary. Different samples geometries have been explored, but the standard dimensions of the chips utilized for NWs production are 1x1 cm^2. Prior to use, native oxide was removed from substrate surface using HF solution (5% in weight), rinsed with deionized water and then dried with N_2. Etching solutions were prepared by dissolving $AgNO_3$ powders (Roth 99.9999 % ROTIMETIC) into HF (Carlo Erba, 39.5% in weight, for analysis, ACS-ISO). Final concentrations are 5 M for HF and 16 mM for $AgNO_3$, even if different molarities have been explored for the latter (when used at concentration different from 16 mM, this will be specified in the text). NWs were

obtained by soaking the cleaned chips into the etching solution for different times in a thermostatic bath (Polystat 36, Fisher Scientific) at temperatures of 5, 10, 20, 30 °C. At the end of the NWs fabrication, Ag^0 aggregates were removed by oxidizing them with HNO_3 (Merck, 50 % vol., 2 minutes). The whole process was carried out in ambient air and light.

In order to elucidate SaCE mechanism and peculiarities, samples have been extensively characterized from a morphological point of view, through electron microscopy.
Scanning Electron Microscopy (SEM) images were obtained using a Zeiss Gemini 500 Field Emission Scanning Electron Microscope equipped with an *in lens* and a High effciency Everhart-Thornley (HE-SE2) secondary electron detector. Samples for Transmission Electron Microscopy (TEM) and High-Resolution Transmission Electron Microscopy (HR-TEM) analyses were prepared through ultrasonic treatment of NWs chips in isopropanol for five minutes. Few droplets of the solution containing the dispersed NWs were put on carbon holey grids and left overnight in air to let the solvent evaporate. TEM images and electron diffraction (ED) analyses were acquired using a LaB_6 FEI Tecnai TEM at 200 kV. HR-TEM images were obtained instead using a field-emission-gun FEI Titan C_s-corrected microscope operating at 200 kV.

3.2 Phenomenology

Silicon exposition to etching solution causes an immediate nucleation of Ag nanoparticles onto Si surface. Ag aggregates quickly grow forming dendritic structures that cover completely Si surfaces. Considering reaction stoichiometry, silver reduction leads to the formation of 3.42 cm^3 of Ag for each cm^3 of etched Si, easily explaining the large quantity of Ag that is present on the Si surfaces after etching process. The formation of Ag particles after nucleation leads to elongated dendritic structures. While their bottom

tips sink immediately into Si, their top ends rapidly extend normal to the substrate surface, reaching heights in the order of centimeters at the end of etching longer than one hour. An example of these structures, after 5 minutes of etching, is showed in Figure 3.1.

Anisotropic growth witnesses the rapid depletion of Ag^+ ions in the proximity of the surface, even in well-stirred solutions. The dendritic shape of the larger Ag aggregates provide a confirmation on the diffusion limited Ag growth. It should be noted, however, that much smaller Ag particles, clearly visible in Figure 3.1, are observed on the substrate surface, at the bottom of Si NWs. Secondary Ag nucleation is consistent with possible reoxidation of Ag^0 to Ag^+ by either water or dissolved oxygen [2], therefore causing a local surge of Ag^+ concentration in very close proximity of silver dendrimers.

As soon as Si is exposed to the solution, localized etching occurs and roughly aligned NWs form protruding from the substrate, with diameters ranging from 100 to 200 nm. Electron microscopy characterization shows that NWs may be either single crystalline or partially porous, with their nanostructure depending on the etching temperature and on the Si doping level and type. Typical morphology of nanowires obtained by SaCE is shown is Figure 3.2.

3.3 Electrochemistry of SaCE

Silver-assisted chemical etching is an electrochemical process involving the reduction of Ag^+ to Ag^0 and the oxidation of Si to Si^{+4} and a chemical process, namely the etching of oxidized silicon.
The electrochemistry of MaCE, particularly the two step process on surfaces previously patterned either with Au or Ag with the use of H_2O_2 and HF, has received the widest attention in literature [2, 3, 4, 5, 6], as it enables the fabrication of ordered nanostructures. When periodicity is not required, one pot process, for instance SaCE, is preferred due to its semplicity [7, 8, 9]. Clearly, some aspects of this complex reaction are involved also in process

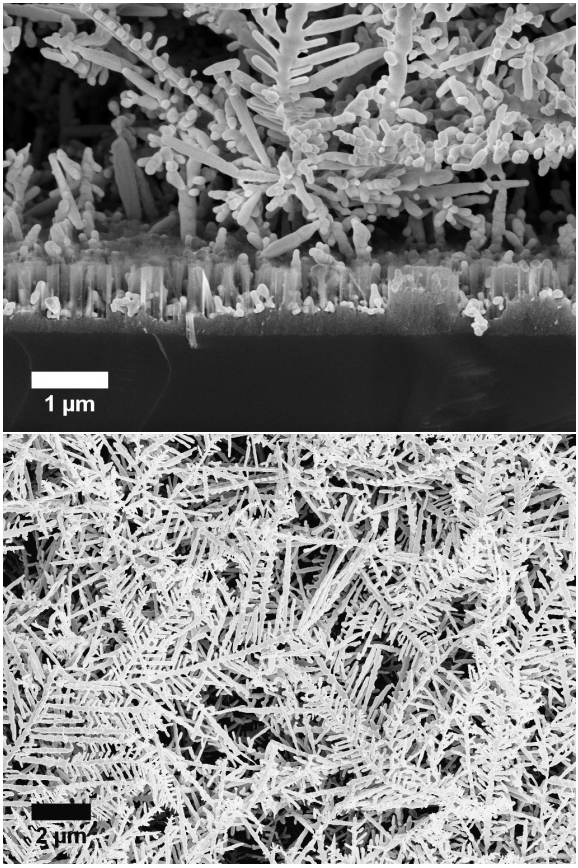

FIGURE 3.1: Ag dendritic structures and beginning of NWs formation observed after 5 minutes of etching at 20°C on an n++(P) substrate (up). It is possible to notice the great vertical developement of the dendritic structures and the presence of small Ag nanoparticles on the bottom of NWs. Top-view of the Ag dentrites observed after 5 minutes of etching (down). It is possible to notice that the substrate surface is completely covered by Ag dendrites.

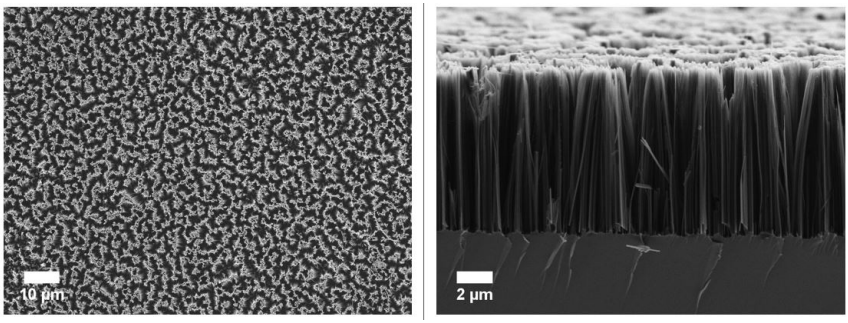

FIGURE 3.2: Typical morphology of nanowires obtained by SaCE in top-view (left) and cross-section (right).

where silver or gold is catalysts and either Ag^+ or H_2O_2 as oxidizing agents. Nonetheless, in what follows we will focus exclusively on chemical etching where silver acts at one time as the oxidizing agent and the catalyst.
It is well assessed that the electroless redox process implies the reduction of Ag^+ ions to metallic Ag at the cathode, either at Si or Ag surface:

$$Ag^+_{(aq)} \longrightarrow Ag_{(s)} + h^+$$

$$E^\circ = +0.79 \text{ V vs. NHE} \tag{3.1}$$

At the anode, holes are then injected into Si that oxidizes to Si^{4+} or to Si^{2+}, according to two different mechanisms. The first is the direct Si oxidation to SiO_2 at the solid surface as:

$$Si_{(s)} + 4h^+ + 6H_2O_{(aq)} \longrightarrow SiO_{2\,(s)} + 4H_3O^+_{(aq)}$$

$$E^\circ = -0.84 \text{ V vs. NHE} \tag{3.2}$$

and then SiO_2 is etched away by HF:

$$SiO_{2(s)} + 6HF_{(aq)} \longrightarrow SiF^{2-}_{6\,(aq)} + 2H_3O^{+}_{(aq)} \tag{3.3}$$

This 4-electron process is often referred to as electropolishing, leading either to a smooth, regularly etched silicon surface or, when localized, to the formation of single-crystalline NWs [11].
The alternate oxidation path for Si is a 2-electron process, where Si is initially oxidized to Si^{2+} at Si surface:

$$Si_{(s)} + 2h^{+} + 4HF_{(aq)} + 4H_2O_{(aq)} \longrightarrow SiF^{2-}_{4\,(aq)} + 4H_3O^{+}_{(aq)}$$

$$E^{\circ} = -1.2 \text{ V vs. NHE} \tag{3.4}$$

The oxidation to Si^{4+} is then completed in solution thanks to the concurrent chemical reduction of two hydronium ions:

$$SiF^{2-}_{4\,(aq)} + 2HF_{(aq)} \longrightarrow SiF^{2-}_{6\,(aq)} + H_{2\,(g)} \tag{3.5}$$

This mechanism leads to the formation of a porous silicon layer or, when localized, to (partially) porous silicon NWs [10].
It is well assessed in literature, that the 2-electron and the 4-electron processes are in competition and occur simultaneously. When the reaction is carried out in an electrochemical cell, electropolishing is the prevalent process at high current densities, with an estimated threshold current $j_{PS} \approx 0.5$ A/cm^2 [11]. The interplay between electrochemical etching of silicon and chemical dissolution of oxide may give an explanation of the threshold current that separates the two regimes [12]. The 2-electron and the 4-electron reactions have different oxidation rates and they occur at the same time, at any given potential. However, considering SiO_2 dissolution by HF, potential changes the kinetics of the reaction. At low potentials, in fact, oxide dissolution is the fast reaction step and it is etched as soon as it forms. Given the different oxidation rates of the 2- and the 4-electron processes, silicon surface will not be homogeneously

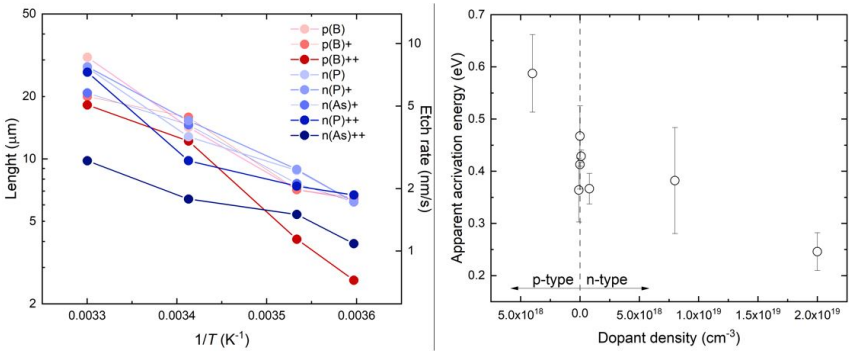

FIGURE 3.3: Nanowire lengths and Si etch rates after 60 minutes of exposure to the SACE solution (left) and apparent activation energies as a function of the doping level of the Si samples (right).

oxidized and the areas where the slower electrochemical reaction proceeds will be dissolved more slowly. As a result, porous silicon is obtained. On the other hand, at higher potentials the whole silicon surface is covered by an homogeneous layer of SiO_2, since oxide formation is now the fast step, independently of the electrochemical reaction. So, oxide dissolution has become the slow step and it occurs homogeneously on all silicon surfaces, leading to electropolishing.

NWs lengths (ℓ_{NW}) after one hour etching at different temperatures (5, 10, 20, 30 °C) on all the substrates are displayed in Figure 3.3. Apparent activation energies (ε), always shown in Figure 3.3, have been fitted as:

$$\ell_{NW} = \ell^{\circ}_{NW} \exp\left(-\frac{\varepsilon}{k_B T_{etch}}\right) \tag{3.6}$$

where ℓ°_{NW} is a constant, k_B is the Boltzmann constant, and T_{etch} is the etching temperature.

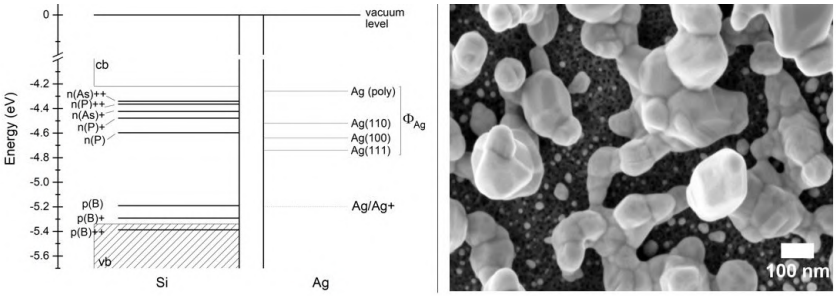

FIGURE 3.4: Compared electronic band structures of Ag and Si, displaying the position of the Fermi level in Si (thick lines) depending on sample doping (left), and polycristallinity of Ag aggregates (right). Note that, Φ_{Ag} of polycristalline Si is much lower than one normally considered in literature.

It can be noted, in Figure 3.3, that, while etch rates tend to decrease with dopant concentration independently of their type, activation energies decrease passing from p++ to n++ substrates. Etch rates trend shows that 2-electrons process prevails either at p- or n-type heavily doped silicon that lead to porous NWs. Porosity is also obtained for NWs formed from lightly doped substrates at higher reaction temperatures where injected current densities j are higher. This behaviour is the opposite of what expected and, therefore, a direct connection between etch rates and porosity is not fully supported by experimental data. In fact, the prevalence of one oxidation process to the other seems to be ruled by voltage instead of current density. Holes must be injected into Si at silicon–solution surface for the redox process to occur. Hole injection has been a matter of discussion in literature. Most of SaCE studies claims that a Schottky barrier forms at the Ag-Si interface [6, 11, 13, 14, 15]. In this case, the associated electric field would be favorable for the holes to flow inside p-type silicon, while it would hinder holes flow in n-type silicon. Literature assumes that Ag work function Φ is

4.72 eV, a value that is consistent with numerous determinations on fully cured, ultraclean (111) surfaces [16, 17]. However, (100) surfaces exhibit lower values [18, 19] and polycristalline Ag deposited on silicon at low temperatures shows a Φ of 4.26eV [19, 20]. Figure 3.4 (right) clearly shows the polycristallinity of Ag aggregates and allows to consider Φ_{Ag} = 4.26 eV as a correct value in the case at issue. Figure 3.4, on the left, displays how the choice of Φ_{Ag} change the nature of Ag-Si interface where a barrier that opposes to hole injection may not be present.

In Figure 3.5 Si surfaces after 10 s of exposure at 20 °C to the etching solution are reported. It is possible to notice that, during initial stages SaCE process, Ag nanoparticles morphology changes evidently with the changing of doping type and level. In fact, nucleation density regularly decreases moving from p++ to n++ substrates, while the nuclei size follows the opposite trend. Even though literature reports [2] that Ag nucleation density cannot be directly related to the surface density of dopants, it is found to be depend on the doping type and level of the substrate. It is reasonable to think that, since Ag nucleation entails the reduction of Ag^+ to metallic Ag, the process is favourable to p-type substrates, where electric potential at the Ag-Si interface facilitates hole injection. Figure 3.5 clearly shows how nucleation density is larger on p-type silicon and it grows with the growing of dopant concentration. On the other hand, average Ag grain diameter is smaller on p-type substrates, compared to n-type Si where diameters and distances among nuclei increase with dopant concentration.

As claimed above, both 2- and 4-electron processes [half-cell reactions, respectively (3.4)–(3.5) and (3.2)–(3.3)] occures at any Si doping level and type, when coupled with Ag reduction. Furthermore, the formation of either porous or crystalline nanopillars depends on which oxidation process is prevalent, with the 2-electron oxidation responsible for the formation of porous silicon. Therefore, the voltage sensed by Si during the redox process is expected to be controlled simply by the material resistivity ρ and not by a potential barrier at Ag-Si contacts (Figure 3.4, left). Considering that

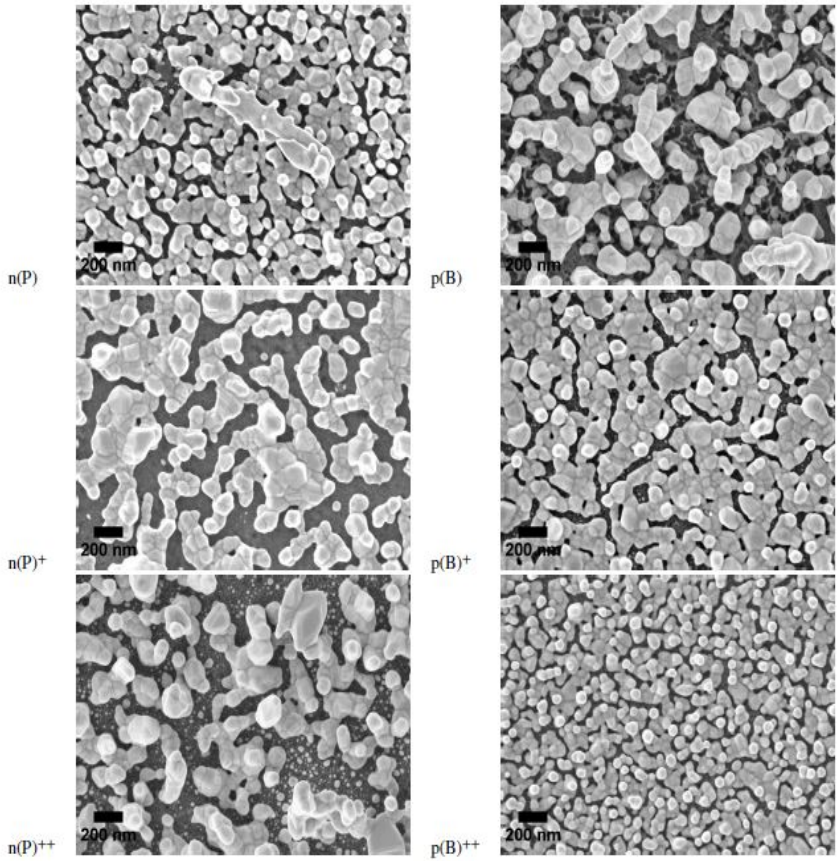

FIGURE 3.5: SEM images of Si surfaces after 10 s of exposure at 20 °C to the Ag^+/HF solution. It is possible to notice the regular decrease of Ag nucleation density moving from p++ to n++ substrates and the opposite trend of Ag nuclei size.

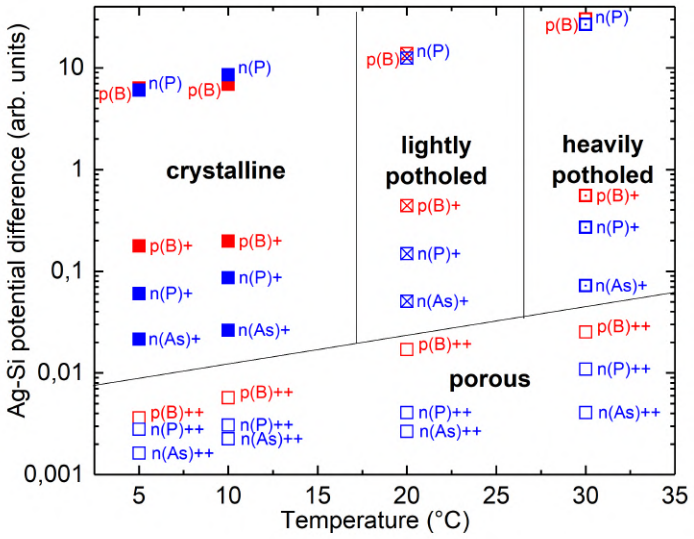

FIGURE 3.6: Estimate of the voltage applied to Si during the redox process vs. temperature. Symbols refer to NW structure: crystalline (■), lightly or heavily pocked (⊠ and ⊡, respectively) and porous (□).

the current density j is proportional to the etch rate, then $V = j\rho\ell$ (where ℓ is a measure of the distance between cathodic and anodic regions).

Figure 3.6 shows the plot of V/ℓ at the various etching temperatures and doping level. From the graph, it is clear that porous Si NWs are obtained only at low V/ℓ and so at low j. This is in agreement with the model advanced by Zhang *et al.* [12] concerning the electrochemical formation of porous silicon. Also, the potential range where porous silicon NWs are formed seems to extend when

the temperature increased. Anyway, it is impossible to draw any quantitative conclusion because of the narrow range of temperature explored. Qualitatively, it is sensible to claim that, at higher temperatures, the range of potential differences where HF removal is not the limiting reaction steps broadens and therefore formation of porous NWs is observed, as predicted by Zhang [12].

3.4 SaCE Etching Localization

When performed in the right conditions, any MaCE process allows to obtain Silicon NWs. Therefore, a key characteristic of this kind of etching is the localization. On (100) silicon substrates, etching rates are identical at all {100} surfaces. In light of this, it is sensible to expect a lateral bore etching caused by the holes injected into Si and diffused to neighbouring regions. Since this is not the case, some mechanism of protection, either chemical or electrochemical, must be present. It is suggested in literature [12] that, in the case of two-step MaCE, etching occurs preferentially at the bottom of the bores as pore wall would be denuded of Ag particles. Figure 3.7 shows how the bores are overfilled by Ag dendritic structures and the mechanism indicated for two-pot SaCE it is not suitable for one-pot process.
Other hypothesis have been advanced in literature. For instance, it is reported [21] that defects created by the ongoing oxidation process cause lower stability (higher reactivity) of Si surfaces at the bottom of the bore and, therefore, the etching would be favorable near those areas. This can be, actually explanatory for the preferential etching at Ag-Si interface, but not for the slow etching of bore walls. In a different view, since hydrogen is released by the 2-electron processes, it has been considered that wall protection can be helped by this process. Of course, this would not explain the preferential etching direction of SaCE that leads to fully crystalline NWs in the case of the 4-electrons reaction [22].

Also, the role of capillarity (surface tension) and/or of adhesion

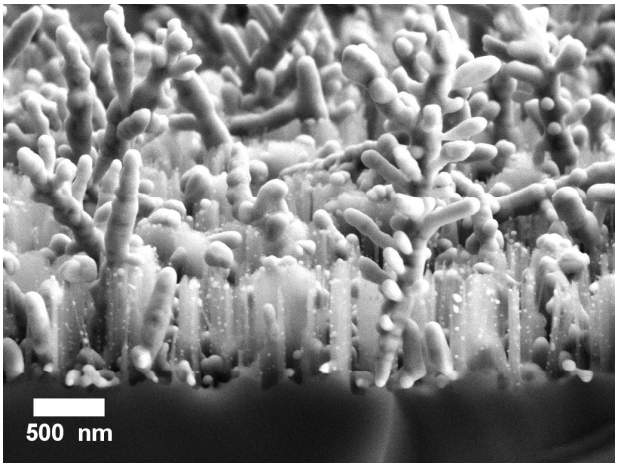

FIGURE 3.7: Cross section of Si NWs and Ag dendrites after 5 minutes at 20 °C. It is possible to notice how Ag dendrites overfill the bores.

has been largely explored. In fact, it has been considered in literature that Si NWs obtained with this kind of etching are flexible and, therefore, capillary forces at the Si-water interface can bend them [23, 24]. A careful analysis of both top-view and cross-section SEM images displays that NWs invariably form aggregates (tufts), with NWs sharing their outer ends. NWs form therefore average angles of approximately 10°with respect to the substrate surface, as seen in literature (Figure 3.8). It has been proposed by Chang *et al.* [25] that capillary forces during drying arises from surface tension at the solid-liquid interface. In light of this, that authors subject samples to a process where liquid-vapor phase transition takes place continually, called critical point drying. In this way, phase transition occurs with zero surface tension and ultrathin wires (with diameters of ≈ 20 nm) are obtained not forming tufts until a length of ≈ 4 μm. Other analyses have been proposed in literature. For in-

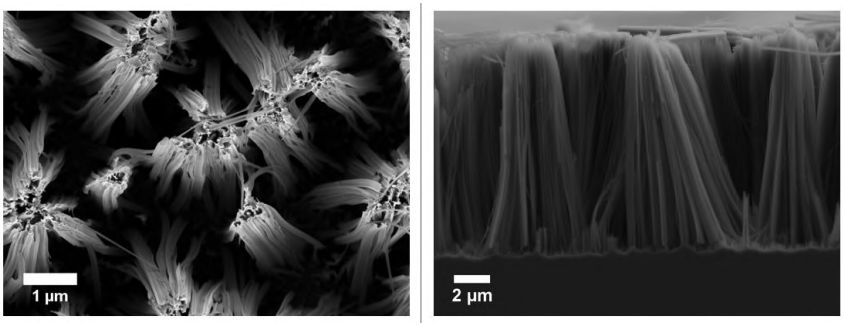

FIGURE 3.8: Typical morphology of nanowires obtained by SaCE in top-view (left) and cross-section (right). Note that NWs seem to gather together at their outer ends with an average inclination of 10°with respect to the substrate normal.

stance, it has been observed that surface adhesion could be not negligible because it could prevail over capillarity phenomena. Zeniou *et al.* [26], in fact, showed that, for 1 μm pitch, neighbouring NWs bend and collapse for wire lengths exceeding 10 μm, providing an alternate explanation for the formation of NW tufts.
It is clear that capillarity is involved in NWs formation in SaCE, but an alternate mechanism can be proposed, based on the dynamic of Ag particles in HF/H_2O_2 etching solutions. In fact, a detailed study on motility of silver particles onto a silicon substrate have been presented by Peng *et al.* [27]. The study regards two-step MaCE process where in the first step Ag nanoparticles are deposited/grown on a silicon substrate. After this, the second step consists on an oxidizing etching in HF/H_2O_2 where H_2O_2 acts as the oxidant. In this case, Ag acts solely as catalyst and no further growth of Ag nanoparticles is possible during the etching step. The experiment shows that, when silver starts sinking into the substrate, silicon flakes surrounding the bores are formed as a result of the Si displacement caused by Ag penetration. With the continuation of the

process, Ag penetration inside Si is supposed to be propelled by a self-electrophoresis mechanism. In two-step MaCE, in fact, H_2O_2 reduction generates H_3O^+ ions at the anodic region of the metal particle (Ag-Si contact). Due to a difference of potential between the cathodic and the anodic areas, hydronium ions migrate toward the solution (through the double layer surrounding the particle or across grain boundaries) and Ag particle moves in the opposite direction, sinking into Si. Regarding SaCE case, it is sensible to think that a similar mechanism is present, although propulsion is given by Ag^+ reduction.

It is possible to consider the anodic area of silver particles at the interface between the silver aggregate and the extruded Si (the Si flakes) while the whole interface between Ag and the solution is the cathodic area. Ag particles act as a short-circuited galvanic cell, with electron flux that moves from the anodic to the cathodic sites, inside the particle. Ag^+ ions approach the cathodic area and give their momentum $\vec{p}$ to Ag dendrites. By symmetry, only the $\vec{p}$ component orthogonal to the substrate ($p_\perp$) has an average value different from zero. It is possible to have an estimate of the value of $p_\perp$ considering that the velocity u of the approaching Ag^+ ions can be calculated by the kinetic energy acquired by them over a distance λ that is equal to their mean free path in solution. In water, the distance is $\lambda \simeq (M_{H_2O}/\rho_{H_2O})^{1/3}$, where M_{H_2O} is the water molecular mass and ρ_{H_2O} is the water density. Therefore, it is possible to estimate $\lambda \approx 0.3$ nm, a value that is of the order of the thickness of the Stern layer (SL), as expected. The kinetic energy acquired by Ag^+ ions is calculated from $e\mathcal{E}\lambda$, where $-e$ is the electron charge and $\mathcal{E}$ is the local electric field. It is possible, now, to calculate the dynamic pressure applied by Ag to Si surface, which is $P = \frac{1}{2}\rho_{Ag^+}u^2$. Considering a potential difference of 0.5 V applied over a Stern Layer of 0.1 nm [28], $\mathcal{E} \approx 4$ V/nm. Since $[Ag^+] = 16$ mM, it is easy to calculate that $P \approx 4 \times 10^6$ Pa, an acting pressure sufficient to promote the self-propulsion of silver into the substrate. A summary of the overall mechanism of SaCE is illustrated in Figure 3.9.

Even if two-pot and one-pot processes have a different mecha-

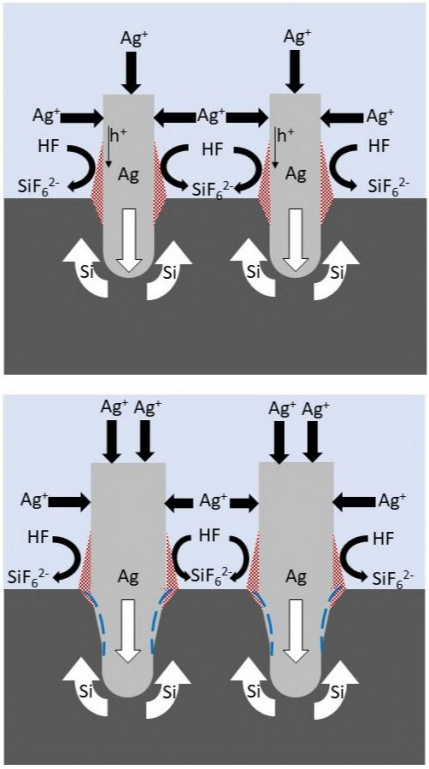

FIGURE 3.9: Ag^+ ion reduction injects holes into Ag aggregates protruding into the solution. The unbalanced transfer of momentum normal to the substrate surface propels Ag aggregate into Si, causing Si extrusion at the substrate surface. Si flakes (dashed red regions) are exposed at the outer solution-substrate interface and are the sites where the oxidation of Si may be completed by efficient HF etching. This is consistent with the observed inclination of NWs, that results from the combined effect of enlarging Ag aggregates and of HF-diffusion-limited region subjected to etching (dashed blue lines).

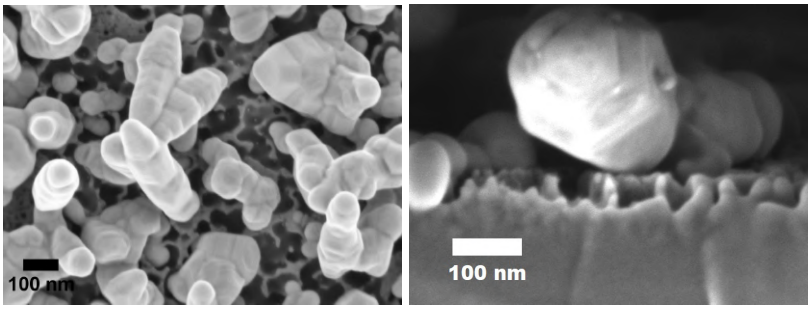

FIGURE 3.10: Evidence of Si flakes protruding from the substrate, in top-view and cross-section.

nism, in both cases it is possible to see the sinking of the metal particle as a result of the displacement of solid Si toward the solution. The validity of the mechanism advanced for SaCE is proven by Figure 3.10, where SEM micrographs show the Si flakes surrounding the sinking Ag particles, both in top-view and in cross-section. Considering that HF needs to reach SiO_2 to etch it away, it makes sense that both oxidation and etching occurs only at the protruded flakes.

The mechanism proposed easily accounts for lateral bore protection and can give a concurrent explanation on NWs tuft formation. In fact, both lateral etching of silicon at the Si-solution interface and the enlargement of Ag dendrites concur to bend and fold NWs, explaining their increasing inclination with respect to the substrate normal. It is needed to be said that also capillary forces may concur to NWs bending and that the presented model is compatible with the residual bending reported in Chang's critical point drying experiment [25]. Furthermore, it has been observed that, with the increasing of Ag^+ concentration, the etching process tends to lose its selectivity, leading to (almost) completely polished surfaces (Figure 3.11). This is consistent with the fact that an increase of NW inclination at higher solution oxidizing power causes adjacent

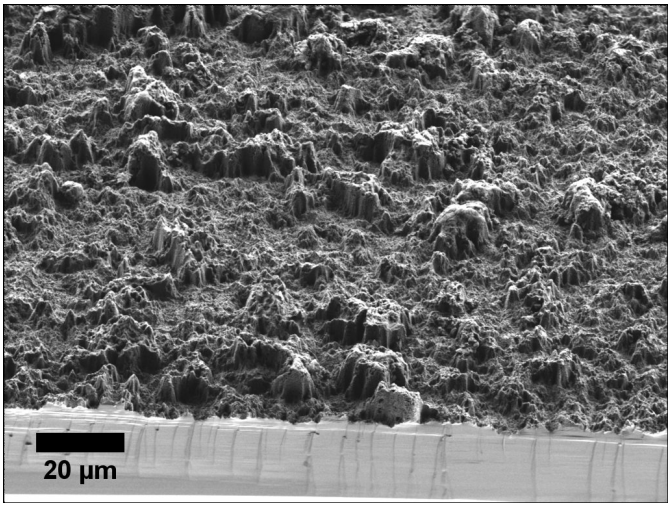

FIGURE 3.11: Top-view of silicon surface obtained at $[Ag^+] = 50$ mM. It is noted how the etching tends to become homogeneous and less localized since NWs lateral bores are meeting at high Ag^+ concentrations.

bores to meet.

3.5 Morphology of Si NWs

Previous studies [2, 14, 23] reported the formation of fully crystalline Si NWs at low substrates doping level, both in p-type or n-type. This is in agreement with SEM and TEM analysis of n and p silicon NWs obtained by etching conditions described in the experimental section. Micrographs reported in Figure 3.12 clearly display how the surface of low doped NWs is completely smooth and no lateral etching on the NWs occurred. ED analyses, moreover, proves the crystallinity of the specimens since diffraction spots are easily pinpointed.

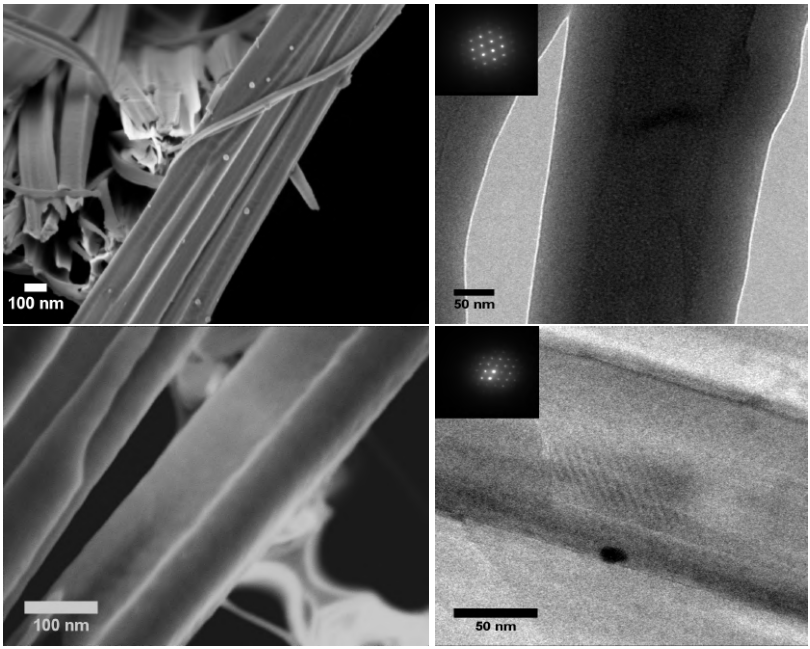

FIGURE 3.12: SEM and TEM images and ED of Si NWs obtained from n (P) (top) and p (B) (bottom) substrates at 20 °C.

Morphology of Si NWs obtained from p+ (B) and n+ (P) substrates is shown in Figure 3.13. Differently from the previous case, it is noted that NW surface is not completely smooth, but some kind of roughness/porosity is present. It is clear, anyway, how lateral potholes are superficial either from SEM/TEM images or ED analyses which shows the crystallinity of the NWs, at least in the inner part of them.
At high dopants concentration, superficial roughness of the NWs increases significantly. This is clearly displayed in Figure 3.14 where porosity of NWs is clear and much more substantial than in the previous cases. Anyway, electron diffraction analysis shows that,

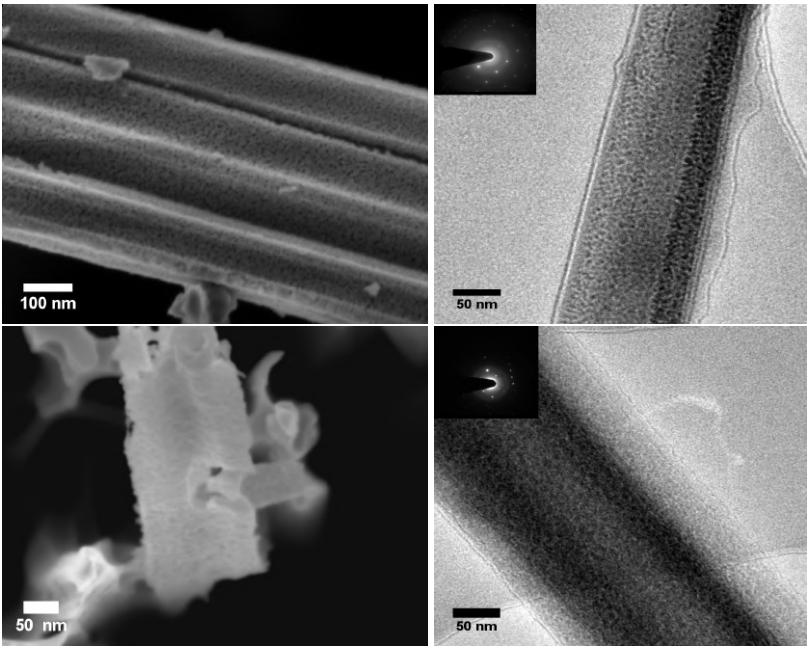

FIGURE 3.13: SEM and TEM images and ED analysis of Si NWs obtained from n+ (P) (top) and p+ (B) (bottom) substrates at 20 °C.

despite the high porosity, inner crystalline structure of the NWs obtained by n++ (P) and p++ (B) substrates is preserved since reflection spots are present and evident. Additionally, it is possible to notice how pores morphology appears to be different in heavily doped substrates. In fact, even if in p++ substrates porosity is important and evident, pores seems to be more regularly located on lateral surfaces of the NWs and from TEM image they seem to impact only the outer surfaces. On the other hand, in n++ NWs pores are deeper and they appear to affect more the NW structure. A deeper understanding of Si NWs nanostructures is provided by HR-TEM images, reported in Figure 3.15. It can be noted that, at

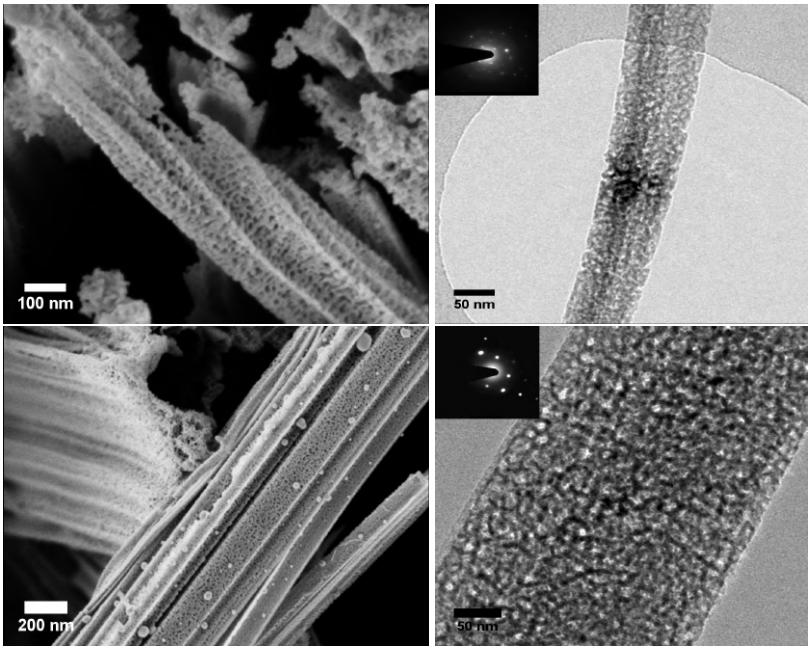

FIGURE 3.14: SEM and TEM images and ED analysis of Si NWs obtained from n++ (P) (top) and p++ (B) (bottom) substrates at 20 °C.

low doping levels, atomic lines are clearly visible proving the full crystallinity and the smoothness of NW surfaces. Only the outer layer of the NW appears to be amorphous and this is easily explained by the formation of the native oxide which is favorite in a high surface/volume structure as a NW. With the increasing of dopants concentration, both in p and n-type, superficial roughness seems to increase and it is notable from the images. Anyway, the main crystal structure is preserved since atomic columns are visible, even if not as clearly as in low doped substrates meaning that roughness is limited to the first nanometers below the surface. Figure 3.16 reports HR-TEM images of Si NWs obtained from n++

and p++ substrates. It is possible to identify areas where atom columns are clearly visible, and areas where an amorphous part seems to be present. Of course the amorphous portion of the NWs is due to its oxidation but it is also an effect of the roughness of the NWs. In fact, bumps and holes that are present on highly doped NWs surfaces do not allow the microscope to focus the whole surface, giving the impression of a great amorphization of the surface. Thus, it is possible to conclude that, also at high dopants concentration, the majority of NW crystalline structure is preserved. These results are in good agreement analyses reported in literature [15] and further support the mechanism we advanced. In fact, it has been proved that etching causes eventual modifications of the pristine crystalline structure only within some tens of nanometers from the Si-solution interface at the extruded Si flakes. This seems to confirm that the limiting SaCE step is the removal of the oxidized silicon by HF. In the case of a process limited by holes diffusion, deeper structural modifications (within distance of the order of some micrometers) should have been observed.

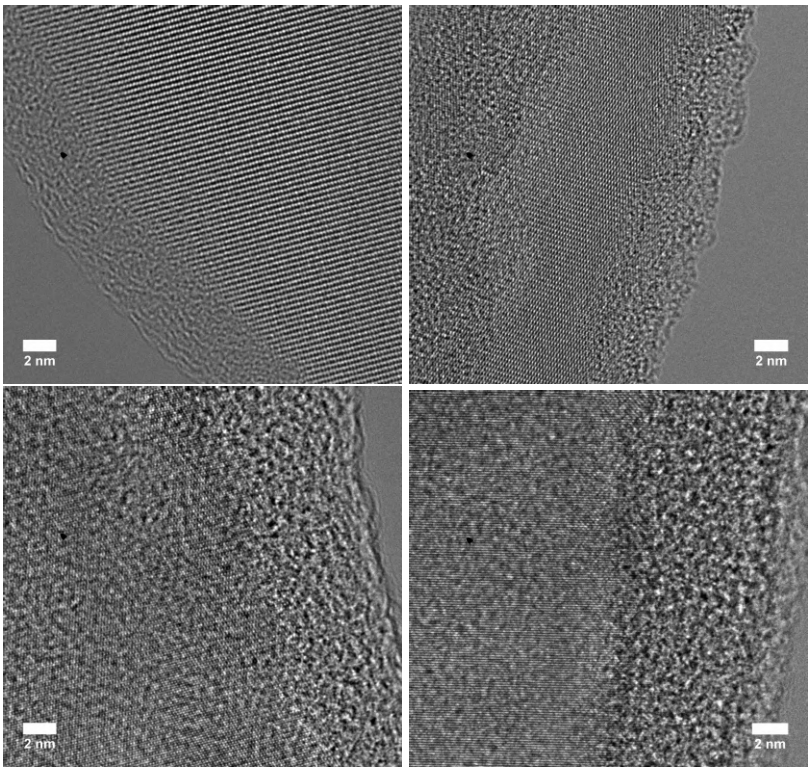

FIGURE 3.15: HR-TEM images of Si NWs obtained from n and n+ (right), p and p+ (left) sustrates.

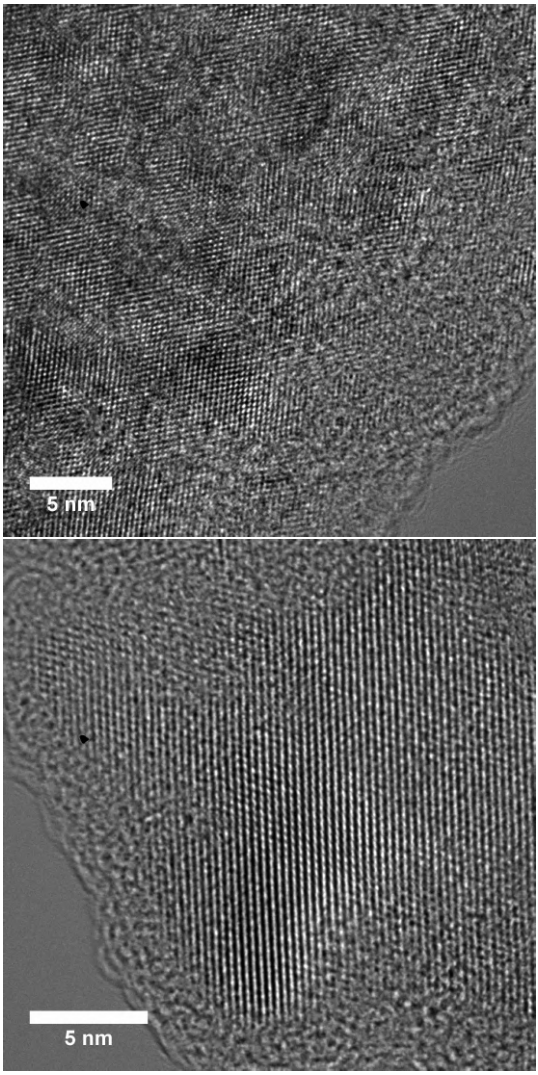

FIGURE 3.16: HR-TEM images of Si NWs obtained from n++ (top) and p++ substrates (bottom).

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CHAPTER 4

Nanophononic Metamaterial

As described in Chapter 2, Nanophononic Metamaterials are one of the most promising new classes of material when it comes to thermal conductivity reduction [2, 3, 4, 5, 6]. The possibility that it offers in decoupling thermal and electrical conductivity is pretty unique, innovative and it is perfect for thermoelectric applications. NPM configuration as presented by Hussein does not require any periodicity for the local resonances to be present. This is a great advantage from a practical point of view since it allows to avoid critical steps such as lithography. Moreover, it allows the utilization of an earth abundant element and well-known material as silicon. Since NPM configuration consists in an array of NWs on top of a Si membrane, Metal-assisted Chemical Etching can provide a sustainable method for the production of large areas of such nanomaterial.

4.1 Samples Preparation and Characterization

The production of NPM starts from a monocrystalline Si wafer, [100] oriented and Double-Side-Polished (DSP). Substrate thickness is 200 μm and it is a p-type (B) wafer with a reported electrical resistivity between 5 and 10 $\Omega \times$cm. The substrate has been subjected to

SaCE, in order to create NW arrays on both faces. Prior to etching, substrates have been cut with diamond tip in different dimensions according to which characterization the sample was subjected to. Etching experimental steps are as described in the previous chapter: native oxide was removed from substrate surface using HF solution (5% in weight), rinsed with deionized water and then dried with N_2. Etching solutions were prepared by dissolving $AgNO_3$ powders (Roth 99.9999% ROTIMETIC) into HF (Carlo Erba, 39.5% in weight, for analysis, ACS-ISO). Final concentrations are 5 M for HF and between 16 and 18 mM for $AgNO_3$. NWs were obtained by soaking the cleaned chips into the etching solution in a thermostatic bath (Polystat 36, Fisher Scientific) at a temperature of 20 °C. Etching times were different and they were chosen in order to regulate Si membrane thickness, by tuning NWs lenght on both sides. At the end of the NWs fabrication, Ag^0 aggregates were removed by oxidizing them with HNO_3 (Merck, 50% vol., 2 minutes). The whole process was carried out in ambient air and light.

Morphological characterization of NPM has been performed through Scanning Electron Microscopy (SEM) images using a Zeiss Gemini 500 Field Emission Scanning Electron Microscope equipped with an in lens and a High efficiency Everhart-Thornley (HE-SE2) secondary electron detector.

NPM electrical and thermoelectrical properties have been evaluated by measuring the electrical conductivity and Seebeck coefficient. The first has been determined by current-voltage characteristics at room temperature. Seebeck coefficient, on the other hand, was measured with a lab-made apparatus, using the so-called integral method. In this method one side of the sample ends is kept at a fixed temperature while the other side is brought to a higher temperature varied through the range of interest. In this way, Seebeck coefficient at a selected temperature can then be obtained from the slope of the Seebeck voltage (V_{th}) versus temperature, $\alpha = \frac{dV_{th}(T)}{dT}$,

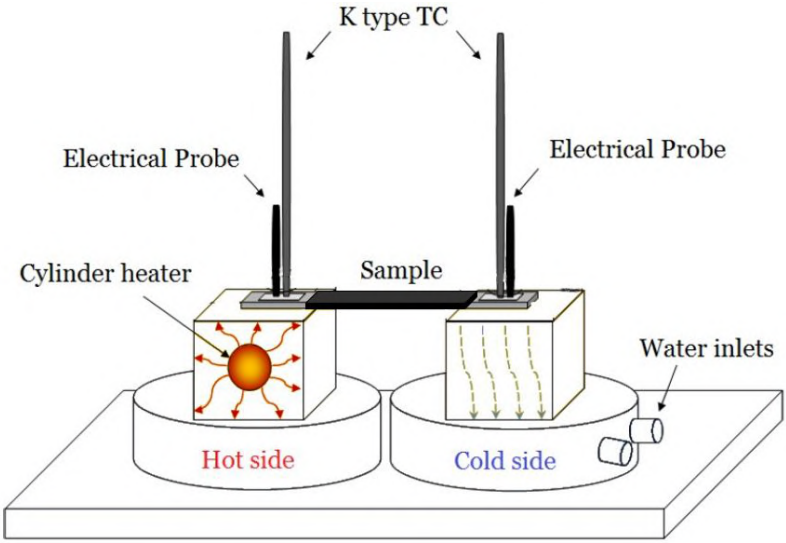

FIGURE 4.1: Scheme of the experimental setup for Seebeck and electrical conductivity measurements.

at that temperature. When Seebeck coefficient does not change, along the range of temperature explored, the slope $\frac{dV_{th}(T)}{dT}$ is constant and therefore V_{th} exhibits a linear relation along T [7]. This has been always verified in the measured samples.
The set-up utilized for these measurements is displayed schematically in Figure 4.1. It consists in two copper sample holders that act as hot and cold side. Voltage and temperature are measured by a thermocouple and an electrical probe for each side. The cold side temperature is kept constant by a water recirculation and it is around 7 °C. On the other hand, the hot side is heated by an electric heater from room temperature to a maximum of around 60 °C. The hot temperature was manually adjusted by changing the power supplied to the heater. Data points were collected only when steady state conditions for both temperatures and voltage output

were reached. Three measurements at different hot temperatures for each sample were acquired and then a linear fit was performed in order to obtain the value of Seebeck coefficient.

NPM thermal conductivity (k_t) has been determined by a measure of the thermal transient of the sample. Particularly, a side of the sample has been heated until steady state conditions where reached. Then, the heating was removed and the system has been evaluated as the equivalent of an RC circuit. This kind of circuit are composed by a resistor and a charged capacitor connected to one another in a single loop, without an external voltage source. Once the circuit is closed, the capacitor begins to discharge its stored energy through the resistor. Following Kirchhoff's current law, the voltage across the capacitor can be found:

$$C \times \frac{dV}{dt} + \frac{V}{R} = 0 \tag{4.1}$$

where C is the capacitance of the capacitor. Solving for V:

$$V_{(t)} = V_{(0)} e^{-\frac{t}{RC}} \tag{4.2}$$

where $V_{(0)}$ is the capacitor voltage at t = 0
Equation 4.2 is the formula for exponential decay. The time required for the voltage to fall to $\frac{V_{(0)}}{e}$ is called RC time constant. It is specific for every circuit and it is given by [1]:

$$\tau = R \times C \tag{4.3}$$

The apparatus utilized for the evaluation of the time constant τ is schematically displayed in Figure 4.2. The sample is squeezed between two blocks (plates) of aluminum $40 \times 20 \times 10 mm^3$. The top aluminum block is maintained to a temperature T_H by an electrical (Joule) heater, which is supplied with an electrical power $P_H = V \times I$ where V and I are, respectively, the supplied voltage

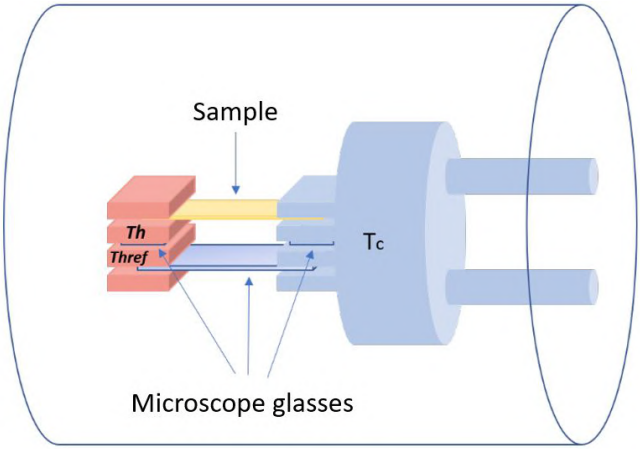

FIGURE 4.2: Scheme of the experimental setup for NPM thermal measurements.

and current. The cold block has the same dimensions of the others aluminium blocks and, even if it is equipped with water inlets, it is not cooled. T_H is measure by RTD (class A Pt 100) temperature sensors, applied at its side. A third aluminium block, named H_{ref}, is placed under the block H and electrically isolated from it with a piece of microscope glass. Another joule heater applies to H_{ref} block the power $P_{Href} = V \times I$, electronically controlled in order to have less then 0,5 °C of difference between T_H and T_{Href}. In this way, the thermal power exchange between H and H_{ref} can be considered negligible. All measurements are carried out in high vacuum ($\approx 10^{-6} atm$) so that losses due to the air thermal conductivity and convection are minimal. Given the difference of volume between the aluminium blocks and the sample, the thermal capacity C_T has been attributed exclusively to the blocks and it is supposed to be the same for every measurement. Therefore, the exponential fit of the thermal transient of the sample, gives us its characteristic time constant τ, from which it is possible to calculate the thermal

resistance R_T of the sample.

4.2 Morphology of NPM

Even if it is possible, as explained in the previous section, to take advantage of thermal conductivity reduction phenomenon in one-pillared NPM (meaning with Si nanopillars array present only on one face of Si membrane), in this work only two-pillared NPMs have been considered, for experimental reasons. In fact, the starting point of NPM is a double side polished, 200 μm thick, silicon wafer. Thanks to the versatility of SaCE, the immersion of the DSP substrate into the etching solution allows the formation of identical NWs array on both silicon faces. In this way, by increasing nanopillars length on both faces, it is possible to progressively decrease the membrane thickness that lays between these two arrays. By tuning nanopillars length, meaning by choosing the right etching condition in terms of etching time and silver nitrate concentration, it is possible to create double-pillared NPM in a one-step process. Moreover, this synthesis process does not require any kind of surface protection and SaCE allows to control precisely nanopillars length and, consequently, membrane thickness.

Etching solution is the same as described in Chapter 3, but etching time has been increased between 4 hours and 6.5 hours, depending on the required membrane thickness. $AgNO_3$ concentration has been varied also in the range between 16 and 18 mM, since it has been observed that an increase of Ag^+ concentration allows to increase etch rate. Therefore, with a higher Ag^+ concentration is possible to obtain very long NWs (and consequently very thin membrane) with shorter etching time. This fact is a proof that SaCE is limited by Ag^+ diffusion and that Ag^+ concentration is a crucial parameter of this process. Even if SaCE offers the possibility to obtain NWs on different substrates, p or n type, low or heavily doped, this etching has proven to be much more controllable in low

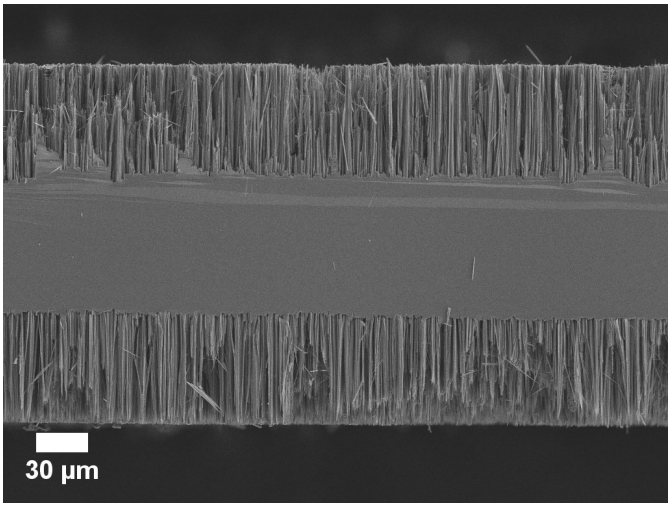

FIGURE 4.3: Morphology of a NPM obtained after 5 hours and 30 minutes with [$AgNO_3$] = 16 mM.

doped substrates. For this reason, NPM has been created only on a p-type substrate with resistivity between 5-10 $\Omega\times$cm. At this doping concentration, as seen already in Chapter 3, etch rate is higher and the resultant NWs are less porous. This allows to obtain a sample with higher mechanical resistance which is fundamental for the handling during samples characterization.

Morphology of a NPM obtained after 5.5 hours at 20 °C with [$AgNO_3$] = 16 mM is shown in Figure 4.3. The resultant membrane is 78 μm thick and it is formed by the simultaneous silicon etching of both silicon faces. In fact, it is possible to notice how NWs have the same length (61 μm) on both sides and they show the same straight membrane/NWs interface, meaning that the etching process occurs at the same time and indistinctly on both directions. NWs microstructure, despite the longer etching time, maintains the same features described in Chapter 3 for a p-doped substrate with [B]

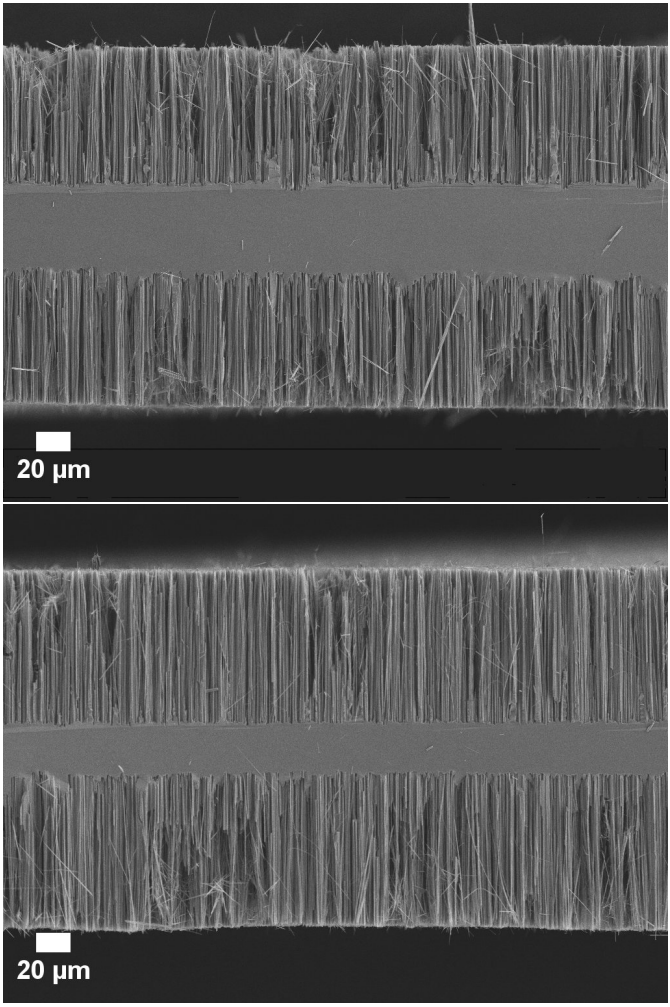

FIGURE 4.4: Morphology of a NPM obtained after 5 hours and 45 minutes with Ag^+ concentration of 17 mM (up) and after 4 hours with Ag^+ concentration of 18 mM (down).

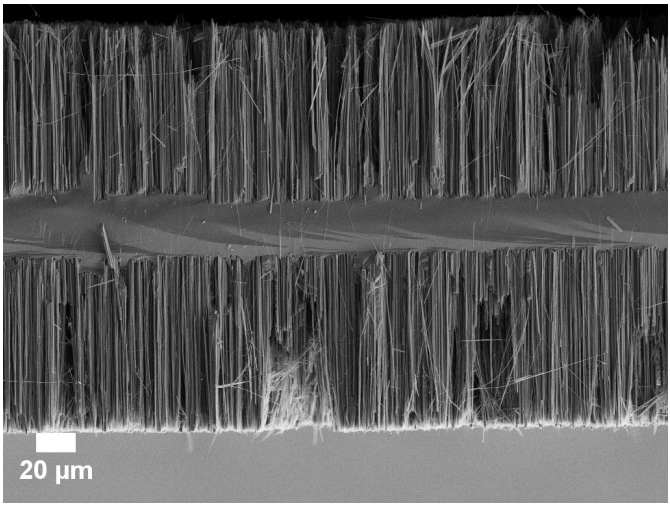

FIGURE 4.5: Morphology of a NPM obtained after 6 hours and 30 minutes with Ag^+ concentration of 16 mM.

= 10^{15} × cm^{-3}. In fact, NWs present smooth surfaces, their individual structures tend to agglomerate on the tips forming tufts and they show a very good crystallinity, fundamental to allow local resonances. Moreover, the NWs keep a diameter between 80 and 120 nm, reaching impressive aspect ratios.

Morphology of NPM obtained after 5.75 hours of etching with Ag^+ concentration of 17 mM is displayed in the upper part of Figure 4.4. In this condition, a residual membrane of 53 μm thick is obtained with 73 μm long NWs on both faces. It is notable how the increase of [$AgNO_3$] of 1 mM allowed to obtain much longer NWs with almost the same etching time. The lower part of Figure 4.4 shows a NPM obtained after 4 hours of etching with Ag^+ concentration of 18 mM. With the increase of [$AgNO_3$] a residual

membrane thickness of 30 μm is obtained, meaning that 85 μm of NWs are formed on both sides. This sample proofs how Ag^+ concentration is a key parameter for long etching. In fact, SaCE is a diffusion limited process and the increase of Ag^+ availability in solution leads to the obtainment of longer NWs.
Figure 4.5 shows a NPM obtained after 6.5 hours with Ag^+ concentration of 16 mM. A membrane of around 20 μm is formed in between 90 μm of NWs etched on both faces. Having such thin membrane makes the sample mechanically delicate. In fact, even if theoretically it is possible to increase NWs length and to decrease membrane thickness, it would be practically impossible to handle the sample for characterization without breaking it. As a consequence, characterized samples in this work have a membrane not thinner than 30 μm.

4.3 Electrical and Thermoelectrical Properties

A variety of NPM samples with different membrane thicknesses has been evaluated in terms of electrical conductivity and Seebeck coefficient by the apparatus shown in the previous sections. It is necessary to point out that the copper sample holders of the measurement system are equipped with two slots 5 mm wide. The hot holder and the cold holder need to be few centimeters far from each other because at first they must be electrically isolated from each other and, therefore, not in contact, and secondly the distance between them allows to obtain a higher ΔT at sample sides. Hence, samples geometry needs to adapt to the system and substrates before etching have been cut in rectangular shapes with a width shorter than 5 mm and a length of around 50 mm.
In order to have a useful surface where contacts for measures can be put, few mm of the sample sides have been protected from the etching solution thorough the application of adhesive tape before the etching. When the etching is completed, the tape is removed by an immersion in isopropilic alcohol. Thanks to sides protection, it

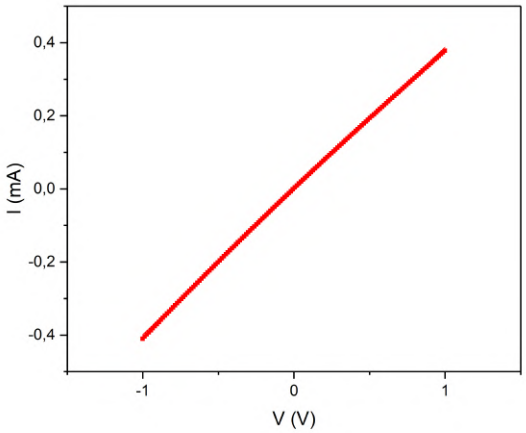

FIGURE 4.6: Characteristic IV curve of the monocrystalline silicon used as substrate for NPM production.

is possible to obtain a flat and clean surface where contacts can be placed and thanks to the very reduced area of the protected parts, where electrical resistivity can be considered as negligible when compared to the one of the nanopillared part.. Electrical contacts have been made by scratching with a diamond tip a small part of the unetched sides in order to create defects and then by putting a drop of Gallium-Indium eutectic (99.99 %, Alfa Aesar) onto the scratches. In this way, an ohmic contact is created.

Electrical and thermoelectrical properties of the substrate, from which NPM samples have been etched, have been evaluated. In fact, this kind of comparison is necessary in order to establish if NPM configuration allows to retain electrical and thermoelectrical properties of the starting monocrystalline silicon.

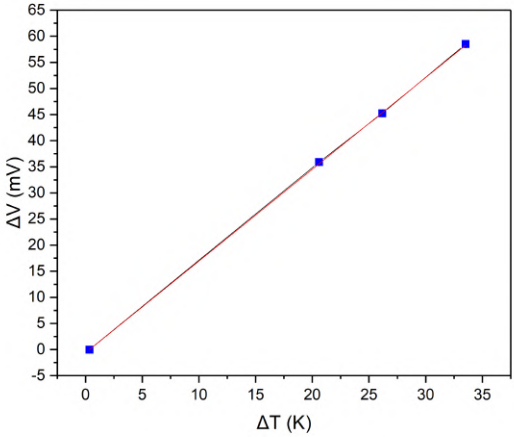

FIGURE 4.7: Seebeck coefficient evaluation of the monocrystalline silicon, p-type (B) used as substrate for NPM production.

Figure 4.6 shows the characteristic IV curve of the monocrystalline silicon, p-type (B), 200 μm thick and with a reported electrical resistivity between 5 and 10 $\Omega\times$cm, used as substrate for NPM production. It is possible to appreciate the linearity of the trend I vs V, considering the range of the applied voltage. This confirms that ohmic contacts were obtained at the interface between the scratched silicon parts and the Gallium Indium. A set of five different pieces of the same wafer,the same also utilized for NPM production, have been measured in a voltage range that goes from +1V to -1V. The average resistivity measured is 7.12 $\pm$ 1.37 $\Omega\times$cm, perfectly included in the range indicated by the supplier. This value of resistivity will be considered as the value to be compared with NPM resistivity.

Figure 4.7 reports the trend of ΔT vs ΔV of the monocrystalline

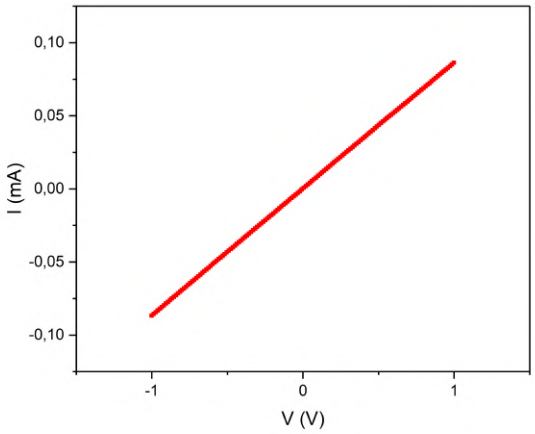

FIGURE 4.8: Characteristic IV curve of a Nanophononic Metamaterial with a residual membrane 33 μm thick.

silicon, p-type (B), 200 μm thick and with a measured electrical resistivity of 7.12 $\Omega\times$cm, used as substrate for NPM production. The curve, whose slope is the Seebeck coefficient, is linear for all the difference of temperatures explored. A set of five characterizations on different pieces of the same wafer led to an average measured Seebeck coefficient of 1.71 $\pm$ 0.05 mV/K. This value has been compared with monocrystalline silicon Seebeck coefficient determination presented in literature and it is resulted consistent with the measurement performed by Geballe *et al.* [10], considered as the reference for silicon Seebeck coefficient. The value of 1.71 mV/K will be the term of comparison for Seebeck coefficient of NPM.

Nanophononic Metamaterials have been electrically and thermoelectrically characterized as described above. Membrane thicknesses of the measured NPM are in a range that goes from 74 to 30 μm and

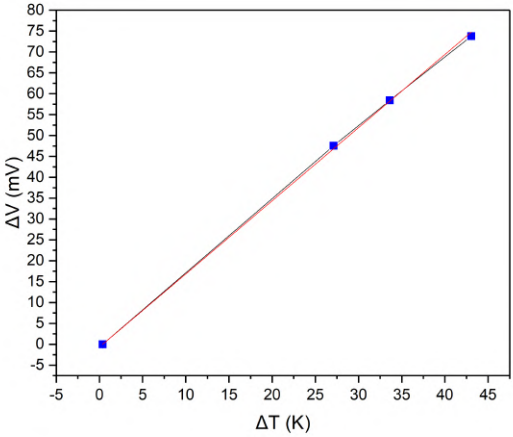

FIGURE 4.9: Seebeck coefficient evaluation of a Nanophononic Metamaterial with a residual membrane 33 μm thick.

consequently a NW length that goes from 63 μm (on each face) to 85 μm (on each face). Figure 4.8 displays the characteristic IV curve of a NPM with a residual membrane 33 μm thick. From the graph, it is possible to appreciate the linearity of the curve I vs V, meaning that an ohmic contact is created between silicon and Gallium Indium. This condition is respected for all the characterized sample. The average NPM electrical resistivity is 7.87 $\pm$ 2.35 $\Omega\times$cm. This value is very close to the one measured for the unetched substrate (7.12 $\pm$ 1.37 $\Omega\times$cm), meaning that electrical properties are retained. Figure 4.9 shows the Seebeck coefficient evaluation of a NPM with a residual membrane 33 μm thick. Again, the trend ΔT vs ΔV is linear along the difference of temperature considered and its slope is the Seebeck coefficient. This condition is respected for all the measured samples. Considering the set of NPM characterized, the average Seebeck coefficient obtained is 1.69 $\pm$ 0.08 mV/K. This value

is very close to the one obtained from the unetched substrate (1.71 mV/K).

Characterized NPMs have retained the properties, both in terms of electrical conductivity and Seebeck coefficient, of the substrate from which they have been etched. This result is of great importance since it demonstrates how such a long and aggressive etching process, as the one under which samples have gone, does not affect the unetched part, independently from the membrane thicknesses. Therefore, considering the possibility to perform such etching on large areas and considering its versatility, SaCE is the most suitable way to produce this kind of samples. In fact, by choosing the right etching conditions and the appropriate substrate thickness, it is possible to create a structure that matches the characteristic of the material introduced by Hussein.

4.4 NPM Thermal Properties

NPM thermal conductivity has been measured with the apparatus showed in Figure 4.2. By applying an electrical power to the H block, the sample to be measured has been heated until steady state conditions have been reached. The same electrical power of P = 0.59 W has been applied to all the sample and a different temperature T_H was reached for each sample. With no heat source applied to the system, this evolves analogously to an electrical RC circuit. Therefore, it is possible to claim that $\tau = R_T \times C_T$. Table 4.1 reports the characteristic time constants and the geometrical parameters of the measured samples.
In order to evaluate the parasitic resistance that could come from the system, this has been measured empty. The thermal transient of the measuring system is shown in Figure 4.10. The system has been measured with a piece of bulk silicon. The dimension of the silicon sample are reported in Table 4.1 and its thermal resistance

	l	w	th	τ
System	-	-	-	3366 sec
Al_2O_3	8 mm	8.5 mm	1 mm	1271 sec
Si-bulk	10 mm	8.5 mm	525 μm	211 sec
NPM	9.8 mm	11.7 mm	62 μm	1790 sec

TABLE 4.1: Characteristic time constant and geometrical parameters of the measured samples.

$\Re_{Si}$ has been calculated from the reported silicon thermal conductivity (κ_{TSi} = 148 W/mK) [11]. Therefore, silicon thermal resistance is:

$$\Re_{Si} = \frac{1}{\kappa_{tSi}} \times \frac{l_{Si}}{(w_{Si} \times th_{Si})} = 15.14 K/W$$

System thermal resistance can be calculated by the time constant of Si (τ_{Si}) and of the system (τ_S). It has to be noted that the equivalent electrical circuit, in presence of the sample, is composed by an RC circuit in which the resistance in equal to the parallel between the sample resistance and the system resistance:
In fact:

$$\begin{aligned}
&\tau_S = \Re_S \times C_T \\
&\tau_{Si} = (\Re_{Si} // \Re_S) \times C_T = \frac{\Re_{Si} \times \Re_S}{\Re_{Si} + \Re_v} \times C_T = \frac{\Re_{Si}}{\Re_{Si} + \Re_S} \times \tau_S \\
&\quad \Longrightarrow \ (\Re_{Si} + \Re_S) \times \tau_{Si} = \Re_{Si} \times \tau_S \\
&\quad \Longrightarrow \ \Re_S \times \tau_{Si} = \Re_{Si} \times (\tau_S - \tau_{Si}) \\
&\quad \Longrightarrow \ \Re_S = \Re_{Si} \times \frac{\tau_S - \tau_{Si}}{\tau_{Si}} = 224.2 K/W
\end{aligned}$$

This resistance is parasitic and it is due to undesired thermal bridges. In order to evaluate the accuracy of the system, a piece of polycristallyne alumina with a reported thermal conductivity of around

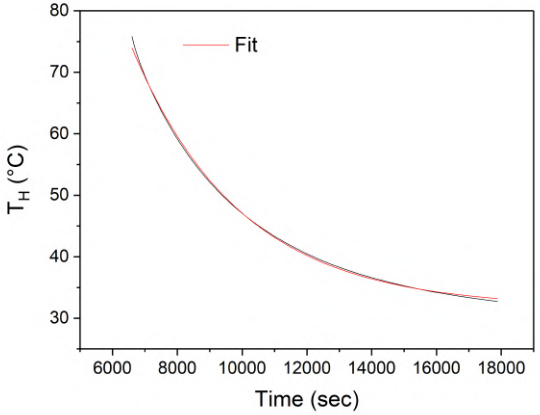

FIGURE 4.10: Thermal transient of the measuring system.

10 W/mK. By knowing $\Re_S$, τ_S and the time constant $\tau_{Al_2O_3}$ of Al_2O_3 sample, it is possible to determine alumina thermal resistance $\Re_{Al_2O_3}$:

$$\begin{aligned}
\tau_{Al_2O_3} &= \frac{\Re_{Al_2O_3}}{\Re_{Al_2O_3} + \Re_S} \times \tau_S \\
&\implies (\Re_{Al_2O_3} + \Re_S) \times \tau_{Al_2O_3} = \Re_{Al_2O_3} \times \tau_S \\
&\implies \Re_{Al_2O_3} \times (\tau_S - \tau_{Al_2O_3}) = \Re_S \times \tau_{Al_2O_3} \\
&\implies \Re_{Al_2O_3} = \frac{\Re_S \times \tau_{Al_2O_3}}{\tau_S - \tau_{Al_2O_3}} = 137.3K/W
\end{aligned}$$

From thermal resistance, alumina thermal conductivity is easily calculated:

$$\kappa_{Al_2O_3} = \frac{1}{\Re_{Al_2O_3}} \times \frac{l_{Al_2O_3}}{(w_{Al_2O_3} \times th_{Al_2O_3})} = 6.78W/(mK)$$

This value is encouragingly close to the reported one.

After having isolated the parasitic contribution to the measurement and after system validation, it is possible to have a precise measurement of a sample of Nanophononic Metamaterial. Numerous attempts have been made for the measure. The main issue is the mechanical fragility of the NPMs. In fact, when samples are squeezed in between the aluminium plaques of the measuring system, the mechanical stress applied on them become too important and the majority of NPMs broke. However, the thermal conductivity of a NPM obtained after 5.5 hours of SaCE ([$AgNO_3$] = 16 mM), with a residual membrane thickness of 62 μm, has been evaluated. NPM morphology is analogous of the ones showed in the previous section and the characteristic time constant of this sample is reported in Figure 4.11.
Following the same line of reasoning followed for Al_2O_3, NPM thermal resistance $\Re_{NPM}$ from the relation:

$$\Re_{NPM} = \frac{\Re_S \times \tau_{NPM}}{\tau_S - \tau_{NPM}} = 254.6K/W$$

Sample geometric parameters, reported in table 4.1, allows to calculate NPM thermal conductivity κ_{NPM}:

$$\kappa_{NPM} = \frac{1}{\Re_{NPM}} \times \frac{l_{NPM}}{(w_{NPM} \times th_{NPM})} = 53.07W/(mK)$$

This value needs to be compared with thermal conductivity of bulk silicon (148 W/m K). NPM has reached a thermal conductivity which is around $\frac{1}{3}$ of the thermal conductivity of bulk silicon. Clearly, given the fact that only one sample has been characterized, this result needs further investigation. Firstly, the system, which is lab-made, needs to be validated with the measurements of other materials with well known thermal conductivity. Different membrane thicknesses needs to be evaluated, in order to understand

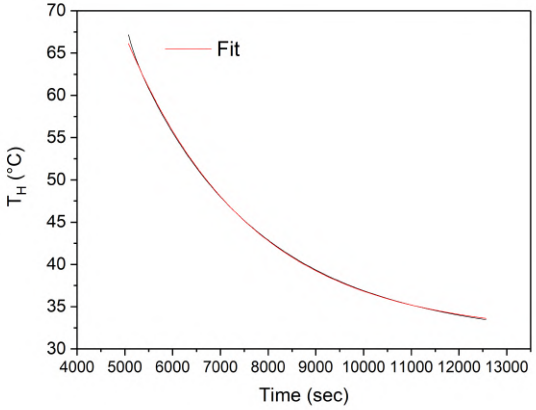

FIGURE 4.11: Thermal transient of a NPM with a residual membrane 62 μm thick.

the dependence between the intensity of the resonance phenomena and membrane thickness. NWs morphology (both in terms of length and diameter) requires more investigation to elucidate their influence on the effect of resonance. Finally, the difficulty to obtain such materials on heavily doped substrates has to be overcome to produce NPM based TEG with high efficiency. This result is of great interest, considering the thickness of the measured NPM. In fact, a membrane of 62 μm could allow a very high power output thanks to its quasi-bulk dimension. Moreover, this measurement shows how the effect of resonance of the nanopillars on which NPM is founded, is present also in such great dimensions (tens of microns). It has to be noted that characterized NPM have retained the electrical properties of the starting substrate. On the other hand, NPM thermal conductivity resulted (for 62 μm thick membrane) to be 36 % of the one of bulk silicon. This demonstrates how NPM offers the great advantage to decouple the electrical and thermal conductivity. The first is in fact controlled by the doping

and the morphology of the membrane while the latter is controlled by the presence of the nanopillars.
A reflection needs to be opened regarding the nature of such a drop of the thermal conductivity. In fact, even if the presence of NW resonance is plausible, many other effects could be present since is sensitive to think that band hybridization would be present only in a small region that contributes to the transport alone, namely at the interface NW/membrane. For instance, part of this κ reduction can be classically explained by heat being trapped in the nanowires, when phonons are considered as particles. In other words, the NWs could act as phonon siphon leaving the base membrane in a state of quasi-thermal silence. This effect is reported in literature by Hussein [6] as well as other authors [12, 13]. Some contribution to the thermal conductivity reduction could possibly come from the nature of NW/membrane interface. In fact, the roughness of this surface could be very beneficial to the phonon scattering [14, 15, 16]. However, also this effect would be confined to the area next to the interface. Given the bulk dimension of the measured membrane, the effect of the roughness can not fully explain such a thermal conductivity reduction. Moreover, the hypothesis that defectivity introduced in the membrane by SaCE it can not be taken into account since both electrical characterization and HR-TEM images have proven that only porosity at the first nanometers of the surface is introduced by the etching. This demonstrates that thermal conductivity reduction is not ascribable to phonon scattering by defect, given the crystalline quality of the membrane.
It is evident that the experimental data collected at this point are not enough to give a full explanation of the measured thermal conductivity. A systematic study involving different membrane thicknesses, NW diameters and lengths, as well as the development of different techniques for NPMs characterization (e.g. thermal scanning microscopy on the membrane cross-section) could have a great impact on the nature of the thermal conductivity drop.

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CHAPTER 5

Silicon Nanowires For Thermoelectricity

As introduced in Chapter 2, one of the most promising method for making silicon a useful thermoelectric material is nanostructuration [1]. In particular, thanks to the thermal conductivity reduction due to phonon scattering at the nanoscale, Si NWs have reached zT values of around 1 at 200 K [2]. Despite the encouraging Si NWs thermoelectric efficiency, the main problem is their integrability in efficient TEGs: there is, in fact, the necessity to create large areas of NWs array, in order to have a satisfying power output. Silver-assisted Chemical Etching offers a practical solution to overcome this issue since it allows to produce large areas of dense silicon NWs through a one-step process [3]. In this chapter the thermoelectric characterization of this kind of arrays will be presented. However, due to the presence of the substrate, parasitic electrical resistances prevent the precise measurement of the nanowire electrical resistivity. Therefore, a structure with dense and very long NWs that allows to avoid substrate contribution will be introduced. Once more, the basis for this structure production is a one-step process as Silver-assisted Chemical Etching.

5.1 Samples Preparation and Characterization

The production of these kind of structures starts from a monocrystalline Si wafer, [100] oriented. Substrates doping type are both p-type (B) and n-type (P) with a reported electrical resistivity between 5 and 10 $\Omega\times$cm as well as heavily doped p-type (B) with a reported electrical resistivity between 0.003 and 0.001 $\Omega\times$cm. Etching experimental steps are as described in the previous chapter: native oxide was removed from substrate surface using HF solution (5% in weight), rinsed with deionized water and then dried with N_2. Etching solutions were prepared by dissolving $AgNO_3$ powders (Roth 99.9999% ROTIMETIC) into HF (Carlo Erba, 39.5% in weight, for analysis, ACS-ISO). Final concentrations are 5 M for HF and 6.25 mM or 16 mM for $AgNO_3$, depending on the cases. NWs were obtained by soaking the cleaned chips into the etching solution in a thermostatic bath (Polystat 36, Fisher Scientific) at a temperature of 10 or 20 °C. At the end of the NWs fabrication, Ag^0 aggregates were removed by oxidizing them with HNO_3 (Merck, 50% vol., 2 minutes). The whole process was carried out in ambient air and light.

Electrical contacts have been prepared by Copper electrodeposition. Beforehand, a layer of 15 nm of Cr plus a layer of 20 nm of Cu have been deposited by thermal evaporation. Cr layer has the function to improve Cu adhesion on Silicon. As thermal evaporation is a directional process, metal is mainly deposited on the top ends of the silicon nanowires. Cu electrodeposition has been performed through an electrolityc cell, schematically shown in Fig 5.1, where only the nanowire forest is in contact with the electrolytic solution through a hole of 4 mm of diameter. Silicon substrate is connected to the cathode of a current generator through a metal plate that clamps the sample at the bottom of the cell toward an O-ring seal. The anode of the current generator is connected to a counterelectrode made of a copper plate 1 mm thick. Cu electrodeposition

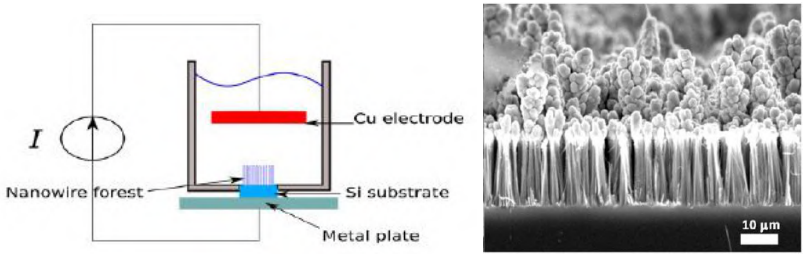

FIGURE 5.1: Schematic of the electrolytic cell utilized for Cu contacts deposition on the left and SEM images of a copper layer grown on the nanowires by electrodeposition in $CuSO_4$:H_2SO_4:H_2O electrolytic solution with I = 25 mA and t = 5 min, on the right [4].

solution is composed by 0.4 M copper sulfate ($CuSO_4$) and 1 M sulfuric acid (H_2SO_4) while the applied current has been 25 mA for 5 minutes. Morphology of deposited Cu contacts is shown in Fig 5.1 [4].

Samples morphological characterization has been performed by Scanning Electron Microscopy (SEM) images using a Zeiss Gemini 500 Field Emission Scanning Electron Microscope equipped with an in lens and a High efficiency Everhart-Thornley (HE-SE2) secondary electron detector.

Nanowires thermal conductivity (k_t) has been determined by measuring its thermal resistance $\Re$ which is related to the thermal conductivity by the geometrical parameters of the sample. It is possible, in principle, to measure the thermal resistance $\Re$ by imposing a known heat flux Q through the sample and then measuring the temperature drop at its ends: $\Re = (T_{Hot} - T_{Cold})/Q$. The apparatus, based on the guarded hot plate technique, is schematically displayed in Figure 5.2. The sample is squeezed between two blocks

(plates) of aluminum, at a constant pressure. The top aluminum block is maintained to a temperature T_H by an electrical (Joule) heater, which is supplied with an electrical power $P_H = V \times I$ where V and I are, respectively, the supplied voltage and current. The cold and the hot blocks will be named C and H and their temperature (T_H and T_C) are measure by RTD (class A Pt 100) temperature sensors, applied at blocks sides. A third aluminium block, named H_{ref}, is placed under the block H and another joule heater applies to H_{ref} block the power $P_{Href} = V \times I$, electronically controlled in order to have less than 0.1 °C of difference between T_H and T_{Href}. In this way, the thermal power exchange between H and H_{ref} can be considered negligible. All measurements are carried out in vacuum (1.3×10^{-3}atm) and a radiation shield has been also applied so that losses due convection and irradiation are minimal. Moreover, a steady state condition is reached during the measurement: once a voltage V_H is imposed to the resistive heater for T_H, the system controls T_{Href} heater in order to maintain the difference T_H - T_{Href} very small for a consedarible amount of time. When the system reached stability, T_H, T_C and the current I_H of the heater T_H have been recorded. In light of that, it is possible to claim that the electrical power $P_H = V \times I$ applied to H block, is the thermal power passing through the sample under measurement. The C block temperature is kept constant by a water circulation. Given the heat power Q that passes through the sample, thermal resistance of the sample $\Re$ can be determined knowing the temperature difference between its extremities. However, it is impossible to make a precise measurement of the temperatures at sample sides, since the sample must be tightly clamped between the H and the C aluminum blocks in order to minimize the thermal contact resistance and to allow the heat flux. Furthermore, it is very difficult to place temperature sensors exactly at the ends of the sample. Therefore, sample thermal resistance has been evaluated as follows. T_H and T_C are different from the temperatures $T_{Hsample}$ and $T_{Csample}$ at

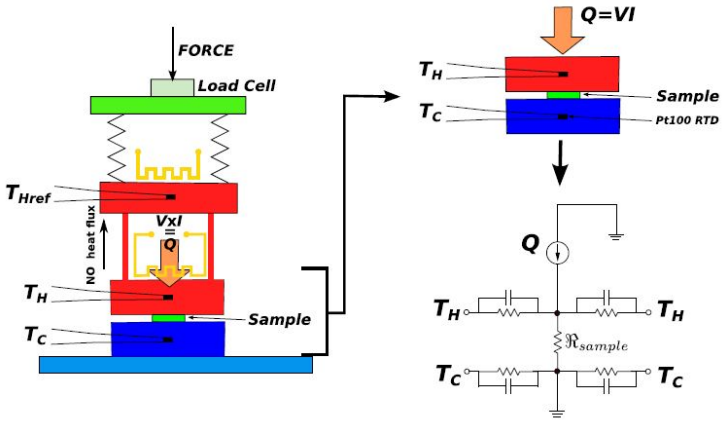

FIGURE 5.2: Scheme of the experimental setup for nanowires thermal conductivity measurements. A sketch of the thermal circuit is shown on the right.

the sides of the sample. The temperature of the two blocks cannot be considered uniform, in particular in the regions closer to the sample, where the heat flux is concentrated. Anyway, the aluminium blocks are intentionally made larger than the sample. Assuming that the walls of the blocks are adiabatic, their temperature in steady state is uniform. Since the temperature sensors for T_H and T_C are placed on the lateral surface of the blocks, the measurement of the two temperatures is very accurate. Therefore, what actually is measured is Q, T_H and T_C, from which is possible to determine sample thermal resistance $\Re$ [5].

Seebeck coefficient and electrical conductivity have been measured simultaneously with the thermal conductivity. The temperature difference has been recorded between the heated top plate and the cooled bottom plate, and the output voltage drop has been recorded by means of a nanovoltmeter (Keithley 2182). Electrical resistance

of the sample has been measured in four contact configuration in which two contacts are used to impose a current, meanwhile the voltage is measured through other two contacts by means of a high impedance voltmeter. Two electrical connections are applied on a side of the T_H aluminium block at the top, the other two are applied to the bottom T_C aluminium block.

5.2 Heavily Doped Silicon NW Arrays

Thermal conductivity of large forests of Si nanowires fabricated on low n-doped substrates (resistivity 1-10 $\Omega\times$cm) has been previously measured, resulting in 4.6 W/m K, which is very small with respect to that of bulk silicon (148 W/m K) [5] . However, Power Factor of a thermoelectric material is fundamental to obtain high thermoelectric efficiency. Therefore p+ nanowires have been produced and characterized [1]. Morphology of these kind of arrays is the one described in Chapter 3 for the heavily doped p-type Silicon NWs (reported resistivity of 0.003-0.001 $\Omega\times$cm), even if Ag^+ has been lowered to 6.25 mM (from 16 mM) in order to have more control to the process and to avoid excessive porosization of the NWs. In fact, while porosity is beneficial for thermal conductivity reduction thanks to phonon scattering at NWs surface, it must not affect electronic transport in the NW. However, the electrical conductivity in heavily doped silicon is only slightly affected by the surface scattering for nanowires larger than 40 nm [6].

5.2.1 Thermal Conductivity Characterization

Figure 5.3 reports measured values of ΔT as a function of the thermal power for Si Nw array 13.5 μm long. The linear fit of this curve gives the thermal resistance $\Re_T$ = 9.20 $\pm$ 0.25 K/W. $\Re_T$ has been measured also for 6.5 μm and 24 μm NW arrays. Then, the product

[1] This Section mostly reports results appeared in S. Elyamny, E. Dimaggio, S. Magagna, D. Narducci, G. Pennelli, *"High power thermoelectric generator based on vertical silicon nanowires"*, Nanoletters, 20, 7, 4748-4753, 2020.

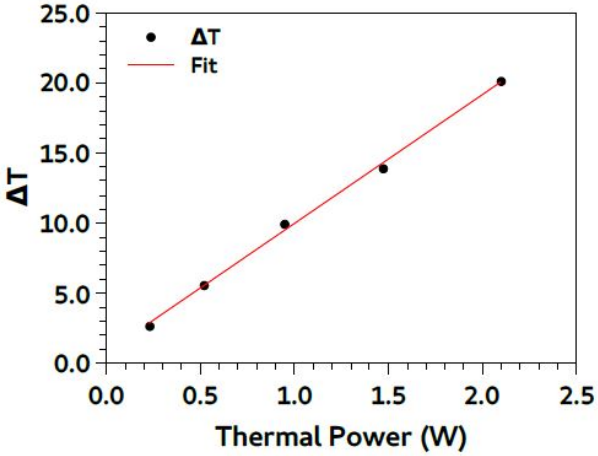

FIGURE 5.3: Thermal conductivity measurement of the 13.5 μm long NW array.

$\Re_T S$, where S is the area of the chip, has been plotted as a function of the nanowire length (L). An accurate geometrical measurement of each chip has been performed both with a caliper and with a calibrated optical microscope used at low enlargement. Let's indicate with $\Re_C$ the contact thermal resistance of each sample. It is possible to assume that the product $\Re_C S$ is the same for all the measured samples. Therefore, $\Re_T$ can be expressed as:

$$\Re_T S = \Re_C S + \frac{1}{\nu \kappa_t} L \tag{5.1}$$

where ν is a coverage factor; the thermal resistance of the nanowire array can be written as $\Re_{NW} = \frac{1}{\nu \kappa_t} L$. Hence, the fitting of the plot of $\Re_T S$ as a function of L gives both $\nu \kappa_t$ and the contact thermal resistance per surface unit $\Re_C S$. Figure 5.4 reports the thermal resistance of p+ SiNW forests of different lengths, multiplied by the surface of each sample. The linear fit is also reported on the graph:

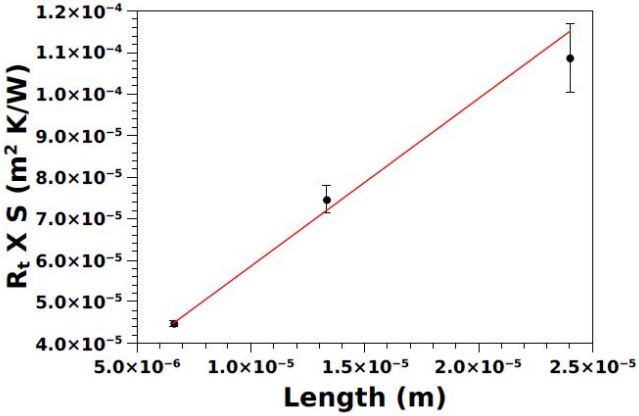

FIGURE 5.4: Thermal resistance, multiplied by the surface, as a function of the nanowire length.

the slope is the reciprocal of the thermal conductivity multiplied by the filling factor ν, which is the ratio between the total cross section of the nanowires and the overall surface of the samples. From the slope, a $\nu k_t = 0.25 \pm 0.02$ W/(m K) is achieved. Filling factor has been estimated from SEM top view images by an image treatment software (ImageJ) through color threshold setting . In this way, only NW apexes have been highlighted and, the ratio between the highlighted area of the image and the total area of the image gives the filling factor ν. Estimated ν is 0.14 ± 0.01. Hence, the thermal conductivity resulted in $k_t = 1.8 \pm 0.3$ W/(m K). The intercept with the vertical axis of the linear fit is the thermal resistance of the contacts, which resulted 1.814×10^{-5} (m^2 K)/W. This result is of great importance since the measured thermal conductivity is really low. In fact, several works reported a low thermal conductivity, measured on single silicon nanowire. In particular, nanowires fabricated by top-down approach and smoothed by thermal oxidation showed a thermal conductivity over 10 W/(m K) [7]. A thermal

conductivity smaller than 10 W/(m K) has been measured on vertical nanowire arrays fabricated by lithography and DRIE (9 W/(m K) [8], 7.5 W/(m K) [9] and 10.1 W/ (m K) [10]). In these cases, the reduction of the thermal conductivity has been ascribed to the roughness resulting from the plasma etching process [10]. Thermal conductivity of SiNW produced by MACE, measured on single nanowire resulted comprised between 4 and 5 W/(m K) [10, 11]. This small value can be explained considering that MACE gives very rough nanowires. In fact, it has been demonstrated, both theoretically and experimentally, that surface roughness is extremely effective in the reduction of the thermal conductivity [12]. Obtained p+ SiNW forests are mainly monocrystalline, as already shown in the previous Chapters, but the surface roughness/surface porosity gives a reduced thermal conductivity. This is fundamental for practical applications, because it will allow to have a significant temperature drop between its extremities.

5.2.2 Electrical and Thermoelectrical Characterization

Seebeck coefficient of p+ doped SiNW forests has been measured simultaneously with the thermal conductivity. Arrays with 6.5 μm, 13 μm and 24 μm long NWs have been characterized. Temperature drop on the contacts has been evaluated from the heat flux and the contact thermal resistance, measured as explained above. Seebeck voltage is due to the effective temperature difference between the ends of the nanowires, which has been determined subtracting the temperature drop on the contacts from the total measured temperature difference. Substrate temperature drop has been considered negligible.
Figure 5.5 shows the Seebeck voltage as a function of the effective temperature drop between the ends of the nanowires for the 13 μm long SiNW array. The slope of the linear fit is the Seebeck coefficient $\alpha = \frac{\Delta V}{\Delta T}$ which was found to be 0.16 mV/K. The linear trend is followed also by the Si NW arrays 6.5 μm and 24 μm long which achieved α values of 0.154 mV/K and 0.179 mV/K respectively.

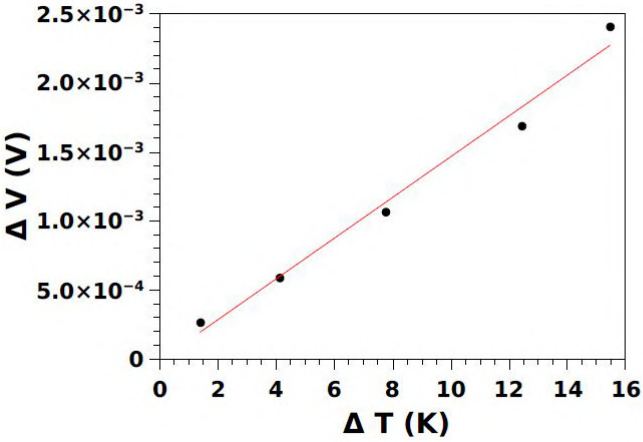

FIGURE 5.5: Seebeck voltage as a function of the temperature difference of the 13 μm long SiNW array, evaluated from the top-to-bottom total temperature difference minus the temperature drop due to the thermal contact resistances.

This values are slightly different from the one obtained from 0.16 mV/K (13 μm long SiNW array) due to the dispersion of the measure, but very close to the ones reported in literature for heavily doped bulk silicon [13, 14].

Figure 5.6 shows a typical IV characteristic measured as previously explained: the current, imposed through one couple of contacts, is reported as a function of the voltage, measured between the other two couple of contacts. The graph shows the electrical conductivity of the 13 μm long, heavily doped SiNW array. The linearity of the curve demonstrates that the contact between electrodeposited copper and top of the Si NWs has a ohmic behavior and no barrier effect is present. Therefore, the electrical resistance, determined by the linear fit of the IV characteristic is equal to 0.093 Ω (S =

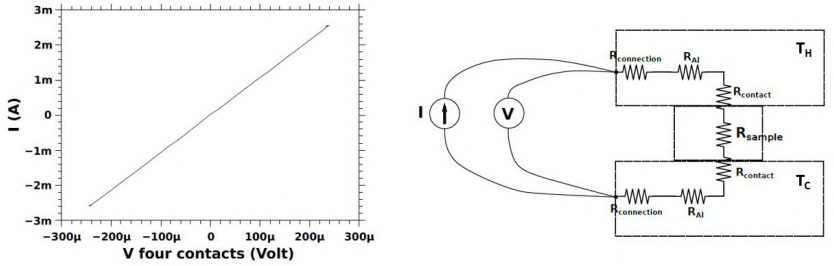

FIGURE 5.6: Electrical conductivity measurement of the 13 μm long SiNW array. On the right, a sketch of the parasitic electrical resistances of the measurement system.

7.7 mm^2). This value, even if small as an absolute value, is quite big if compared with the nominal resistance of the substrate. Indeed, it is also very high in comparison with the resistance that should result from the nominal doping of the nanowire array with a predominantly monocrystalline core. Considering the high doping levels at stake, the parasitic resistances of the system, even if small, have a strong weight in the measurement. It should be underlined that the four contact configuration avoids the resistance of the cables, but not the parasitic resistances due to the connections of the cables to the aluminum blocks. Particularly, parasitic contact resistances comes from the aluminum-top Si NW (electrodeposited copper layer) interface and the interface between the bottom of the wafer and the T_C aluminium block. In fact, the contact resistance due to the interfaces between different materials, such as aluminum and copper (on silicon), can be very unreliable and unreproducible. Hence, the measured resistances, which are all in the range of few tens of mΩ, cannot be ascribed to the Si NW arrays. Moreover, the substrate, even if heavily doped, remains thick with respect to the nanowire length and still determines a resistance several times higher than that of the nanowires. Thus, the measured

resistance should be considered as the entire device electrical resistance, while the resistivity of the nanowires remains uncertain.

Taking into account the measured parameters (Seebeck coefficient, electrical and thermal resistances),it is easy to calculate a zT = $\frac{\alpha^2 \times \sigma}{\kappa} T$ which resulted around 0.8×10^{-3} at room temperature, hence well below expectations. However, considering the high doping value and the principally crystalline core of the nanowires, the electrical resistance should turn out to be very low. If the nominal resistivity of the wafer could be used to estimate zT, a value of 0.15 would be achieved.

5.3 Silicon Nanofelts

As explained above, in order to have a precise measurement of Silicon NWs properties it is necessary to isolate them from all the possible contributions. In particular, the presence of the substrate, when very thick, can have a great influence on the measurements. Thanks to its versatility, SaCE allows to overcome this issue by creating a bulk structure which is composed only by NWs, without the presence of the substrate. This structure has been named nanofelt (NF) [2].

The substrates utilized for the production of these kind of structures have been both p-type (B) and n-type (P), 300 μm thick, with a reported resistivity of 5-10 $\Omega\times$ cm. The choice of such low doped substrates allowed to have more control on the etching process, as explained in Chapter 3, which is crucial for these samples. Ag^+ concentration has been set at 16 mM, the temperature at 10 °C and the time around 15 hours.
Figure 5.7 shows the typical morphology of two NFs, p-type on the upper part and n-type on the lower part. It is notable how, on these

[2]Felt is a textile material that is produced by matting, condensing and pressing fibers together.

kind of samples, the NWs are formed along the whole substrate section. The substrate is etched on both faces and NW arrays of 150 μm are formed on both sides. This dimensions are impressive for one dimensional nanostructures obtained by such an easy and immediate method. Despite the apparent NF fragility, these kind of structures have demonstrated to be mechanically solid, since it has been possible to produce and characterize samples of few mm^2.

In order to measure precisely such structures electrically and thermally, it is necessary to deposit contacts on top of the NWs of both faces. Unfortunately, all the attempts made to deposit contacts by copper electrodeposition have failed, since the porosity of this kind of structures makes the electrolytic solution to pass through the sample, making the electrochemical cell ineffective. In light of that, the measurement has been conducted without deposited contacts and only thermal conductivity has been evaluated, since electrical properties would have been impossible to determine due to the too high contact resistance. The measuring system is the same described above.
Figure 5.8 shows the thermal characterization of a a p-type NF with 150 μm NWs on both faces. The slope of this curve, following the guarded hot plate technique, gives the thermal resistance of the sample. The resulting thermal conductivity of this NF, considering an estimated filling factor of 0.3, is k_t = 13.8 W/(m K). Of course, this value is very high if compared with the one measured on the heavily doped arrays. However, considering the high impact that could come from contact resistance and considering the morphology of this bulk/NW structure, this value is reasonable and not far from the actual NF thermal conductivity. The fact that Si NWs produced by SaCE on low doped substrates are fully crystalline can be greatly beneficial to the power output o a TEG made by such nanostructures. To further improve this aspect, NFs should be etched by heavily doped substrates but, as displayed in Chapter 3, this would lead to porous NWs. Therefore, the mechanical resistance and the

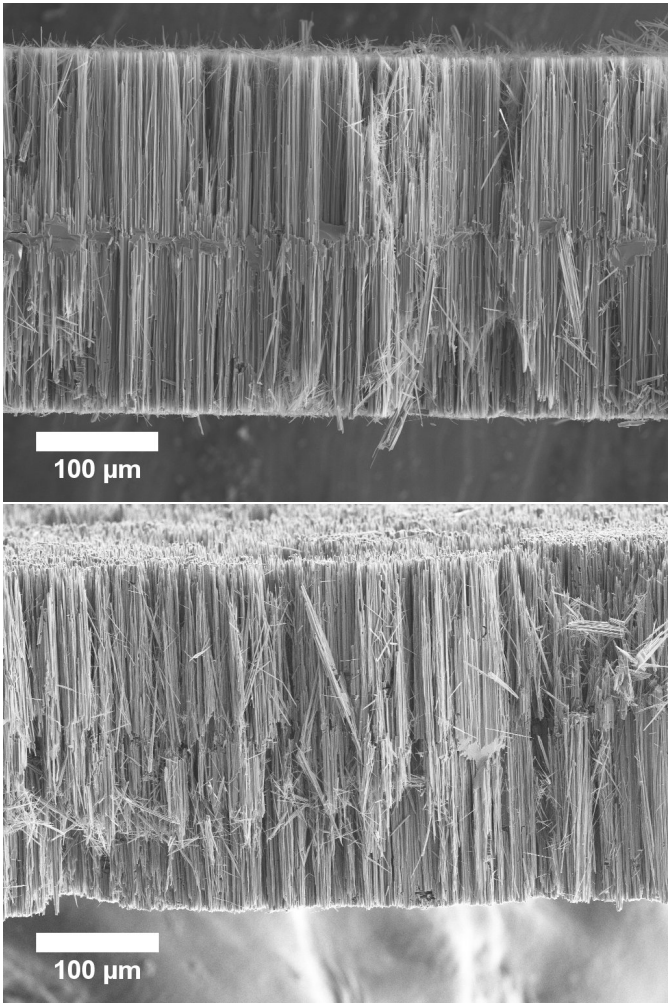

FIGURE 5.7: Morphology of a p-type nanofelt (up) and n-type nanofelt (down) obtained after 15 hours of etching with Ag^+ concentration of 13 mM.

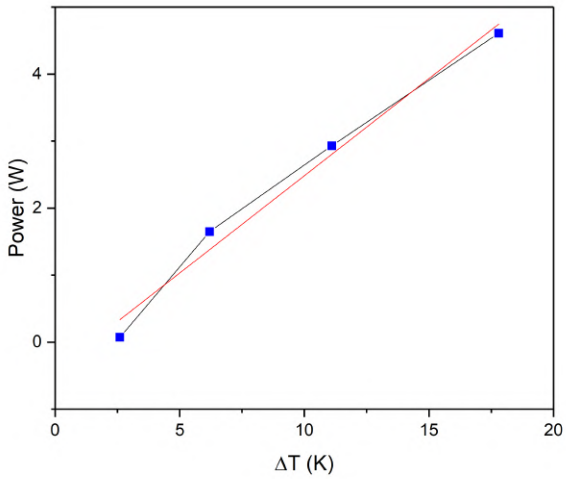

FIGURE 5.8: Thermal conductivity measurement of a p-type NF with 150 μm NWs on both faces.

electrical conductivity would be impacted by the porosity. This issue can be overcome through thermal diffusion doping after NWs fabrication [4, 15]. More experiments are required to characterize Nfs in an accurate way. For instance, it is necessary to think a way to deposit contacts on NWs top in order to have an electrical evaluation. Plus, a calibration curve, as the one reported in Figure 5.4, would allowed to measure precisely contact resistance.
Although these results are preliminary, thanks to the possibility to avoid any contribution of the substrate, NFs are a new type of structure that is worth to further investigate for Si NWs thermoelectric characterization.

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CHAPTER 6

Conclusions

This manuscript was focused on the preparation and characterization of silicon nanostructures for thermoelectric application.

One-step Metal-assisted Chemical Etching was chosen for the silicon NWs production. The results of an extended analysis of the interplay among doping level and type of silicon, nanowire nanomorphology and the parameters controlling the chemistry of SaCE was presented. Specifically, SaCE occurs at the outer substrate surface as a result of Si extrusion by sinking self-propelled Ag particles. Asymmetric momentum transfer from reducing Ag^+ ions forces Ag to penetrate into the Si substrate, causing Si flakes to be exposed at the outer solution-substrate interface where etching actually occurs through either 2- or 4-electron electrochemical oxidation of Si. The region perturbed by the MACE process is set by HF diffusivity. NW surface is found to be either porous (potholed) or crystalline depending on the predominant electrochemical process, while the subsurface is found to be perfectly crystalline. The prevalence of either 2- or 4-electron processes is set by the current density and, therefore, depending on the materials resistivity (but not on its doping type), the voltage sensed widely changes. Two-electron process occurs at low voltages for conductive, heavily doped Si, and causes the formation of superficially potholed NWs. On the

other hand, weakly doped Si are etched with a 4-electron mechanism, leading to fully crystalline NWs.

SaCE was utilized for the production of a recently introduced category of material, the so-called Nanophononic Metamaterial. This material is composed by an array of silicon nanopillars on top of a silicon thin film. NPMs enable local resonance to mix in with conventional phonon transport mechanisms leading to thermal conductivity reduction through group velocity reductions, mode localizations and phonon-vibron coupling across the entire spectrum, differently from conventional technique. This offers the advantage to decouple the electrical conductivity (controlled by the membrane doping and morphology) from the thermal conductivity (controlled by the presence of the nanopillars). NPMs with different membrane thicknesses were electrically and thermoelectrically characterized and their properties were compared with ones of the wafer used as substrate for NPM production. NPMs demonstrated to retain the starting wafer properties, both in terms of electrical conductivity and seebeck coefficient. This result is noteworthy since it proofs that such a long and aggressive etching as SaCE does not modify or alter crystal quality and the properties of silicon.
The thermal conductivity of a NPM with a residual membrane thickness of 62 μm was measured. Preliminar results show a reduction of the thermal conductivity of about $\frac{2}{3}$ compared to bulk silicon. Considering the thickness of the measured NPM, this result is of great interest for the high power output that a NPM-based TEG could reach and also for the depth that the phononic effect of resonance reaches.

SaCE was utilized also for the production of single-leg Si heavily doped NW-based TEG. Si NW arrays were thermally characterized, reaching a thermal conductivity of 1.8 ± 0.3 W/(m K). This value is very small thanks to the roughness of the NWs obtained by SaCE. This allows an efficient phonon scattering at the nanoscale

and leads to a very low thermal conductivity. Thermal conductivity reduction is fundamental for practical applications, because it will allow to have a significant temperature drop between its extremities.
Seebeck coefficient of heavily doped Si NWs was evaluated as well. The measured values were very close to the ones reported in literature. On the other hand, electrical resistivity turned out to be higher than the nominal resistivity from which NWs were produced. In fact, the contact resistance due to the interfaces between the different materials in the measuring system can be very unreliable and unreproducible. Moreover, the substrate, even if heavily doped, remains thick with respect to the nanowire length and still determines a resistance several times higher than that of the nanowires. Thus, the measured resistance should be considered as the entire device electrical resistance, while the resistivity of the nanowires remains uncertain.
A new structure, made exclusively by NWs and free from any substrate, was presented. It was named Si nanofelt (NF) and it was produced again by SaCE. Thermal conductivity of NF was measured and a value of 13.8 W/m K was obtained. Of course this value is much higher than the one obtained from Si Nws arrays. Anyway, due to the experimental impossibility to perform copper contacts electrodeposition, measured thermal conductivity could have a great contribution from contact resistance, impossible to evaluate at this stage. Although these results are preliminary, thanks to the possibility to avoid any contribution of the substrate, NFs are a new type of structure that is worth to further investigate for Si NWs thermoelectric characterization.