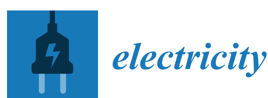

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*Article*

# Design Techniques for Low-Power and Low-Voltage Bandgaps †

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**Abstract:** Reverse bandgaps generate PVT-independent reference voltages by means of the sums of pairs of currents over individual matched resistors: one (CTAT) current is proportional to $V_{EB}$; the other one (PTAT) is proportional to $V_T$ (Thermal voltage). Design guidelines and techniques for a CMOS low-power reverse bandgap reference are presented and discussed in this paper. The paper explains firstly how to design the components of the bandgap branches to minimize circuit current. Secondly, error amplifier topologies are studied in order to reveal the best one, depending on the operation conditions. Finally, a low-voltage bandgap in 65 nm CMOS with 5 ppm/°C, with a DC PSR of −91 dB, with power consumption of 5.2 µW and with an area of 0.0352 mm$^2$ developed with these techniques is presented.

**Keywords:** bandgap; low-voltage; low-power; voltage reference; 65 nm CMOS; trimming; low-current; current-mode; reverse bandgap

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## 1. Introduction

Bandgap (BG) voltage references are widely used in integrated circuits, since each provides a constant voltage, regardless of process, power supply voltage and temperature (PVT) variations. In recent years, the electronics trend has been pushing towards reducing power supplies down to 1.2 V or lower while maintaining or improving measures of performance, such as robustness and current consumption. Thus, voltage-mode BGs cannot be used, since the natural silicon bandgap voltage of 1.25 V would be higher than the supply. For this reason, to avoid switching structure [1,2], current-mode reverse-BGs (R-BG) are typically used [3–8], whose conceptual scheme is shown in Figure 1a. This scheme produces a PVT-independent output voltage $V_{REF}$ by means of the sum of two currents over output resistance $R_3$: $V_T$-based ($V_T = k{\cdot}T/q$) current proportional to absolute temperature (PTAT component, $I_1$) and $V_{EB}$-based current complementary to absolute temperature (CTAT component, $I_2$). $V_T$-based current is multiplied by a constant factor to have the PTAT component be equal to the CTAT one. The summed current flows into a resistor to generate a temperature-independent output voltage $V_{REF}$.

In this paper, the R-BG implementation scheme of Figure 1b is used as the benchmark [9]. The design of said R-BG circuit was analyzed in detail, and optimization guidelines are proposed herein to guarantee overall state-of-the-art (SoA) performance (in terms of a number of parameters; other proposals are focusing on only a few) and industrial yield. As validation, a R-BG circuit was developed in 65nm-CMOS technology to operate with a 1 V supply consuming 5.2 µW with 1% $V_{REF}$ accuracy in the temperature range [−40, 100] °C, and the DC-PSRR was below −91 dB. This performance is guaranteed over

3σ yield for applications in industrial audio products. This device favorably compares with the SoA.

This paper is organized as follows. Section 2 presents R-BG design techniques focusing on bandgap branches, error amplifier (EA) choice and power supply rejection (PSR) optimization. Section 3 shows the actual design of the LV&LP R-BG and Section 4 presents the conclusions.

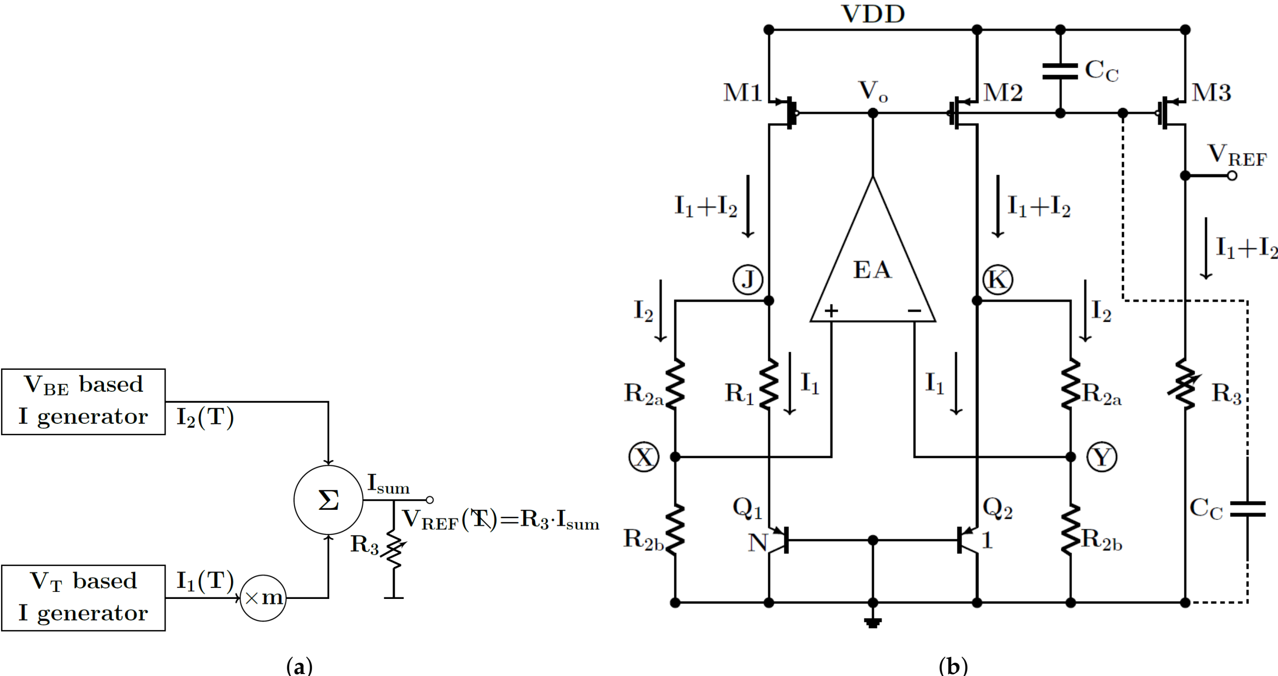



**Figure 1.** (**a**) Conceptual circuit of a current-mode bandgap. (**b**) Low-voltage bandgap schematic. $C_C$ connects $V_o$ with VDD (solid line) or GND (dashed line), depending on the PSR frequency compensation.

## 2. Low-Voltage Bandgap Design

Figure 1b shows the low-voltage (LV) R-BG voltage reference conceptual circuit [9] adopted for discussion. The structure can be divided into two main parts: the BG branches (including Q2 of the single PNP device and Q1 for N PNP devices) and the error amplifier (EA). In the following design, strategies to minimize power consumption—that is, current consumption while operating at LV—are analyzed and optimized. We take into account reliability and performance in the presence of PVT variations for the adopted technology.

As a general guideline for R-BG design, the accuracy is favored over the bandwidth. This leads to using larger devices, since a longer L offers larger output impedance, which translates to higher gain. Moreover, larger devices area-wise (i.e., larger WxL) guarantee fewer device mismatches and lower offsets.

### *2.1. Bandgap Branches*

The current in the R-BG branches is minimized while guaranteeing yield with PVT variations. The minimum current in Q1 and Q2 (they operate with different current densities) is defined from the minimum current per-unit-PNP ($I_\alpha$) in the range where the $\beta$ factor (defined as the ratio between the collector current $I_C$ and the base current $I_B$) is constant for both devices. Therefore, the current in each R-BG branch is defined by the minimum current per-unit-PNP multiplied by the Q1 size, i.e., N.

A key design parameter is the device ratio (N) between Q1 and Q2. For BJT matching purposes, the layout adopts a common-centroid structure, because it averages the geometrical inaccuracies. The value of N follows the equation (with $n$ odd) [10]:

$$N = n^2 - 1. \quad (1)$$

In this way, the current $I_C$ in each bipolar device (Q1 and Q2) is $N \cdot I_\alpha$, and a lower N value reduces power consumption. A higher N value increases the PTAT component by improving the robustness and by reducing the importance of circuit non-idealities (such as opamp offset and component mismatch effects). In fact, the PTAT component has to be larger than the EA offset evaluated as $V_{off} \cdot (1+R_{2a}/R_{2b})$ [10], where $V_{off}$ is the effective EA offset voltage. This is achieved for large N values. However, due to the *ln* (natural logarithm) operation, a significant advantage would require an excessive increase in the N value (and so higher area and higher power consumption). Due to trade-off between power consumption and performance robustness, N = 8 ($n = 3$) is adopted for the common-centroid layout. The current flowing in each PNP (Q1 and Q2) is then $I_1 = 8 \times I_\alpha \cdot (1+\beta)/\beta$. Upon this choice, $R_1$ and $R_2$ (= $R_{2a} + R_{2b}$) can be designed as follows:

$$R_1 = \frac{\Delta V_{\rm EB}}{I_1} = V_{\rm T} \frac{\ln(N)}{I_1}. \quad (2)$$

The value of the temperature-independent constant $m$, defined as $[(\partial V_{\rm EB}/\partial T)/(\partial V_T/\partial T)]|_{300K}$, depends on the technology. Thus, by equating $m$ with $(R_2/R_1) \cdot \ln(N)$, the value of $R_2$ is:

$$R_2 = m \frac{R_1}{\ln(N)}. \quad (3)$$

Thus, the current through $R_2$ is $I_2 = V_{EB2}/R_2 = I_1 \cdot V_{EB}/(m \cdot V_T)$.

$R_2$ is composed of $R_{2a}$ and $R_{2b}$ (Figure 1b). The $R_{2a}$ and $R_{2b}$ partition has to be optimized as a trade-off between two trends: by increasing $R_{2b}$ (reducing $R_{2a}$), the $V_{off}$ output contribution is reduced; by decreasing $R_{2b}$ (increasing $R_{2a}$), the EA input nodes' biases are reduced for $V_X$ and $V_Y$.

In conclusion, the total current in each BG branch (flowing through PMOS current mirrors M1 and M2) is $I_1+I_2$. This current ($I_1+I_2$) is mirrored for the output branch M3. For the defined output voltage $V_{REF,n}$ which is defined as the peak value of the BG curve in nominal condition), $R_3$ should be designed according to the equation:

$$R_3 = \frac{R_2 \cdot V_{\rm REF,n}}{V_{\rm EB} + \frac{R_2}{R_1} \cdot V_{\rm T} \ln(N)}. \quad (4)$$

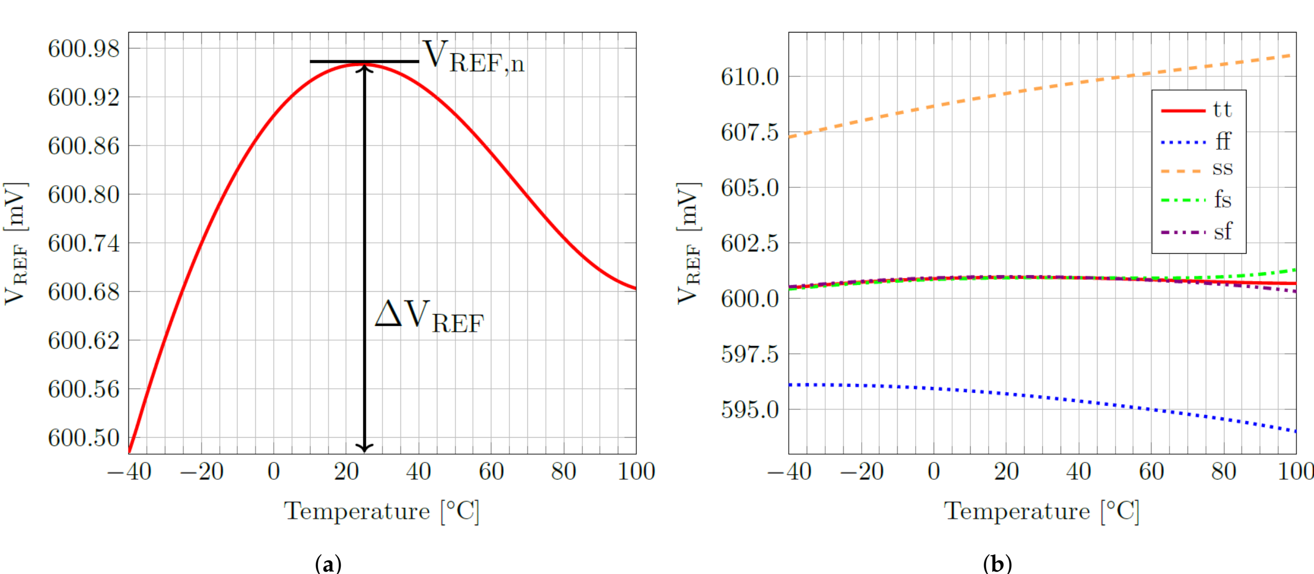



**Figure 2.** (**a**) An example of a BG curve centered at ∼600 mV in a temperature range [−40, 100] °C and a peak at 27 °C. $\Delta V_{REF}$ is defined as $V_{REF,max}-V_{REF,min}$ over the temperature range [−40, 100] °C. (**b**) Worst cases ss (dashes), ff (dots), fs (dash, dot) and sf (dash, dot, dot) are superimposed on the nominal case tt (solid).

Figure 2a presents a typical bandgap curve. It is not flat because the term $(\partial V_{EB}/\partial T)$ is not constant, and it depends on the technology. Flatness is optimized for $m$ calculated at 27 °C (300 K). Its value is usually around −2 mV/°C at 27 °C. On the contrary, the term $(\partial V_T/\partial T)$ is constant with a value of 0.086 mV/°C. The typical slow and fast corners of the BG curve are compared in Figure 2b. As can be seen in **ss** and **ff**, the curve is not centered at 27 °C as in **tt** corner. This is due to the change in the $R_1$ value that is calibrated on the nominal corner.

High accuracy has to be achieved in the current mirror M1/M2–M3. Without any arrangement, different $V_{DS}$ values would result in a mirror error for the current, which should be minimized by using either long L devices or the cascode current mirror, if permitted by the available voltage headroom. To reduce the mismatch between M1, M2 and M3, these devices are designed with large L values.

The ratio between M1/M2 and M3 can be reduced to decrease the power consumption. When the M3 current is reduced by a $\gamma$ factor, the current in the output branch is $(I_1+I_2)/\gamma$, and $V_{REF,n}$ is:

$$V_{\text{REF,n}} = \frac{1}{\gamma} \cdot \left\{ \frac{R_3}{R_2} \cdot \left[ V_{\text{EB}} + \frac{R_2}{R_1} \ln(N) \cdot V_{\text{T}} \right] \right\}. \tag{5}$$

This means that $R_3$ is multiplied by the same $\gamma$ factor, i.e., $R_3^{*}=\gamma \cdot R_3$, where $R_3$ is given by (4). It is important to avoid large $\gamma$ values because $\gamma$ increases the mismatch between M1/M2 and M3.

To improve the current matching between the BG branches and the output branch, a cascode current mirror can be implemented. The cascode current mirror use could be enabled by operating all the transistors in the sub-threshold region, which would result in $V_{GS} < V_{TH}$.

The voltage divider made by $R_{2a}$ and $R_{2b}$ introduces a voltage shift at the input of the error amplifier. This allows proper biasing of the EA differential PMOS input pair, despite the low VDD value.

The minimum VDD for bandgap branches proper operation is given by [10]:

$$\text{VDD}_{\text{minBG}} = V_{\text{X}} + |V_{\text{GS,sth}}| + 2 \cdot V_{\text{DS,sat}}, \tag{6}$$

where $V_{\text{X}}$ is the voltage at X (= Y) node, and $V_{\text{GS,sth}}$ is the sub-threshold region $V_{GS}$. If a cascode current mirror is not used, only a $V_{DS,sat}$ is needed.

## *2.2. Trimming Resistor*

The R-BG was conceived to minimize the effect of PVT variations while not reducing constant deviations (like offset and mismatch), and it produces a $V_{REF}$ constant deviation. Such constant deviations are compensated by digitally-controlled trimming on $R_3$ (used in test bench) in a resistive array whose design is driven by the trade-off between complexity and accuracy (TC is not affected by the trimming circuit). Other trimming implementations (such as changing M3 size) could reduce PSR performance.

The main sources of $V_{REF}$ deviation are: the EA offset ($V_{off}$), the resistor mismatch ($\varepsilon_R$ defined as $\delta R/R$) and the M1/M2–M3 current mirror mismatch ($\varepsilon_M$ defined as $\delta I/I$). $\delta R$ and $\delta I$ are the deviations from R and I, respectively. The contributions of these terms to the $V_{ERR}$ (defined as the deviation from $V_{REF}$) can be written as:

$$V_{\text{ERR}} = V_{\text{off}} \cdot \frac{R_3}{R_1} \cdot \left(1 + \frac{R_{2a}}{R_{2b}}\right) + \varepsilon_R \cdot V_{\text{REF,n}} + \varepsilon_M \cdot V_{\text{REF,n}}, \tag{7}$$

in which the first term on the right-hand side of the equation is called $V_{ERR,PTAT}$. The full scale (FS) trimming correction range is designed to manage such a total error.

Assuming a maximum acceptable error ($\Delta V_{ERR}$) and n bits for controlling the resistive array, the trimming full-scale correction range is $FS_{trim} = \Delta V_{ERR} \cdot 2^n$, which is allocated to be $\pm FS_{trim}/2$ around the $V_{REF}$ nominal value. Then, the design of the R-BG has to optimize the $V_{REF}$ deviation in order to be included in the trimming of the full-scale correction range.

### 2.3. Error Amplifier

The error amplifier (EA, Figure 1b) is committed to force $V_X = V_Y$, to ensure that the residual induced error is lower than the target accuracy. As R-BG produces a DC voltage reference, the main attention is given to static performance (bias, DC-gain, offset) with respect to dynamic performance (bandwidth and slew-rate), which needs to be taken into account for EA design.

#### 2.3.1. EA Bias

The EA bias point has to fulfill the R-BG bias voltage operating point [10] for both input and output nodes for the LV conditions.

For the input nodes, the $R_{2a}$–$R_{2b}$ partition is defined to bias the EA input node close to GND, allowing a PMOS differential pair operation by satisfying:

$$V_{\text{EB}} \cdot \frac{R_{2b}}{R_{2a} + R_{2b}} < \text{VDD} - V_{\text{DS,sat}} - V_{\text{GS}} = V_{\text{in}}. \tag{8}$$

With the same consideration, the minimum $\text{VDD}_{\text{minEA}}$ is [10]:

$$\text{VDD}_{\text{minEA}} = V_{\text{X}} + V_{\text{GS,sth}} + V_{\text{DS,sat}}. \tag{9}$$

For the output node, a proper biasing of M1, M2 and M3 gates requires

$$V_{\text{o}} = \text{VDD} - V_{\text{GS,sth}}. \tag{10}$$

#### 2.3.2. EA DC-Gain Specification

Figure 3a shows the dependence of $\Delta V_{REF}$ on the DC-gain. For instance, a minimum DC-gain of 55 dB is required to have a $\Delta V_{REF}$ lower than 2 mV. Figure 3b depicts the accuracy of the target $V_{REF}$ versus the DC-gain, assuming a nominal target $V_{REF,n}$ of 600 mV. In order to have a constant $V_{REF}$ even in presence of DC-gain deviation (due to PVT) around its nominal value, the minimum DC-gain has to be larger than 75 dB. The resulting $V_{REF}$ is constant, and then compensated by trimming. However, once the trimming is set for a given DC-gain, any further DC-gain deviation (due to PVT) results in residual $\Delta V_{REF}$. This means that the target DC-gain has to be in a region where $V_{REF}$ has flat behavior with respect to DC-gain, in order to avoid accidental $\Delta V_{REF}$, as would occur for low DC-gain; take the value of 50 dB as an example.

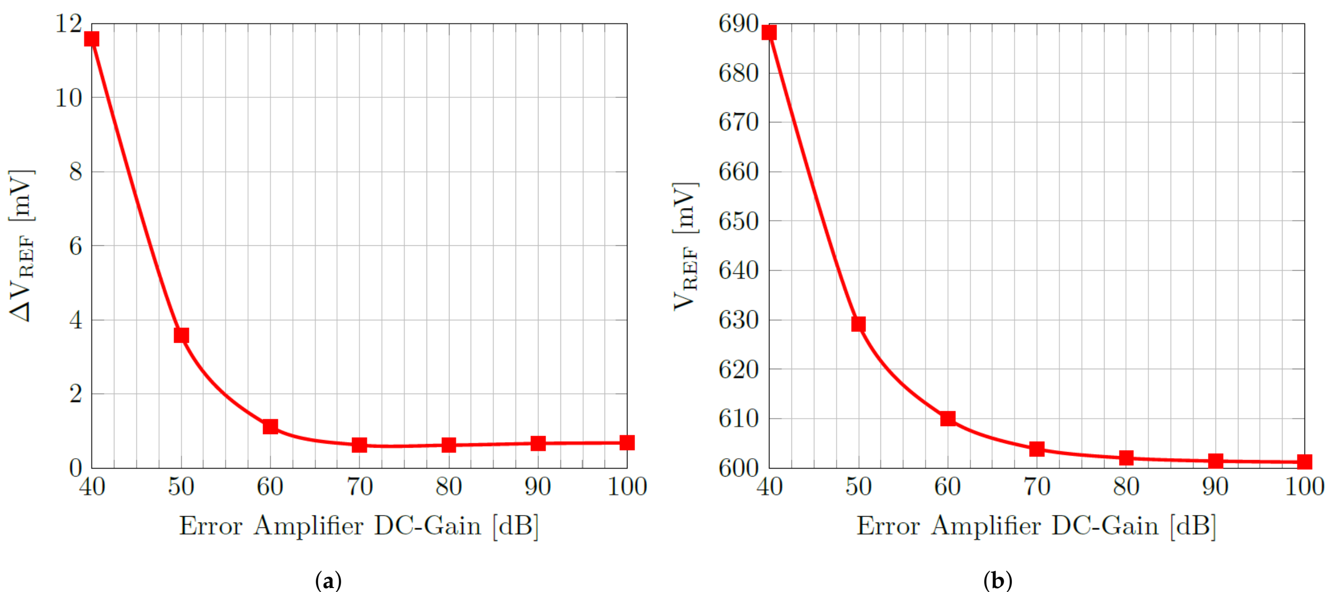



**Figure 3.** (**a**) $V_{REF}$ error versus EA DC-gain. (**b**) $V_{REF}$ value at 27 °C versus EA DG-Gain.

2.3.3. EA Offset Specification

EA offset's ($V_{off}$) effect $V_{REF}$ is given by the $V_{ERR,PTAT}$ term in (7). Typically, $R_{2a}/R_{2b}$ is about 1, and $R_3/R_1 > 1$. Therefore, $V_{off}$ is greatly amplified to $V_{REF}$. However, this $V_{ERR,PTAT}$ is a constant error, and then it is compensated by the trimming operation, limiting the trimming effectiveness range fixed by $FS_{trim}$. Assuming one allocates for $V_{off}$ compensation 50% of the $FS_{trim}$, the specification for the $V_{off}$ is:

$$V_{\text{off}} < \frac{FS_{\text{trim}}}{4} \cdot \frac{R_1}{R_3} \cdot \frac{R_{2b}}{R_{2a} + R_{2b}}. \quad (11)$$

Since $R_1/R_3$ is typically very small, the $V_{off}$ requirement results in very stringent and challenging values (such as $V_{off}$ < 0.5 mV or less).

2.3.4. EA Topology

The above requirements have to be satisfied by the EA design. The required target DC-gain can be achieved by using long devices and/or multistage opamp structures. $V_{off}$ can be reduced (avoiding switching schemes is to be carefully considered) by using large area devices (i.e., large WxL) [11]. In addition, also lowering the current level with MOS in the saturation region would increase DC-gain. Then, the device design can be optimized for low power by operating the transistors in the sub-threshold region, thereby maximizing the intrinsic gain of the transistor (proportionally to $V_A/V_T$, where $V_A$ is the early voltage) for a given current level. Moreover, lower $V_{GS}$ is required, thereby reducing minimum supply voltage and/or enabling cascode structures. Different EA topologies could be compared, as follows [12].

The single-stage operational transconductance amplifier (OTA), the simplest opamp structure (Figure 4a), is widely used for high voltage supplies; nonetheless, its DC-gain is limited to $g_{m,in} \cdot r_{out}$, and it appears insufficiently large to guarantee sufficiently high values—described above. Furthermore, the intrinsic $V_{DS}$ difference in the input devices could introduce systematic $V_{off}$ larger than the requirement. Finally, the request for $V_o = VDD - V_{GS,M1}$ could be critical for this opamp structure. For this reason, other topologies are considered.

Symmetrical OTA, shown in Figure 4b, achieves a low systematic $V_{off}$ since input transistors have the same $V_{DS}$. Moreover, DC-gain ($k \cdot g_{m,in} \cdot r_{out}$, where k is the current ratio between input and output branches) can be higher than fir the single-stage and sufficiently large for the specification. This is at the cost of the extra current of the output branches. The output branch allows only a $V_{DS}$ from VDD to $V_o$. This helps with correct biasing of M1, M2 and M3.

The two-stage Miller OTA (Figure 4c) helps with reaching a higher DC-gain that is given by $A_1 \cdot A_2$ (= $g_{m,in} r_{out,1} \cdot g_{m,out} r_{out,2}$). However, the two-stage structure frequency response requires a large compensation capacitor and a large current in the output stage. For the correct biasing of M1, M2 and M3, the two-stage miller OTA is similar to the symmetrical one.

The folded cascode OTA, as shown in Figure 4d, is very similar to the symmetrical and the two-stage Miller OTAs. Large gain can be achieved using long devices in the output node, and this allows the correct biasing of M1, M2 and M3. Extra cost results from the stability, since a large compensation capacitor from $V_o$ to $V^+$ is needed, with large die area occupancy.

Among the four OTA options, the symmetrical one appears the best choice, and so it could be suggested for high-performance LV R-BGs. The additional current compared to the single-stage OTA is negligible, since it is much lower than the current requested by the BG branches.

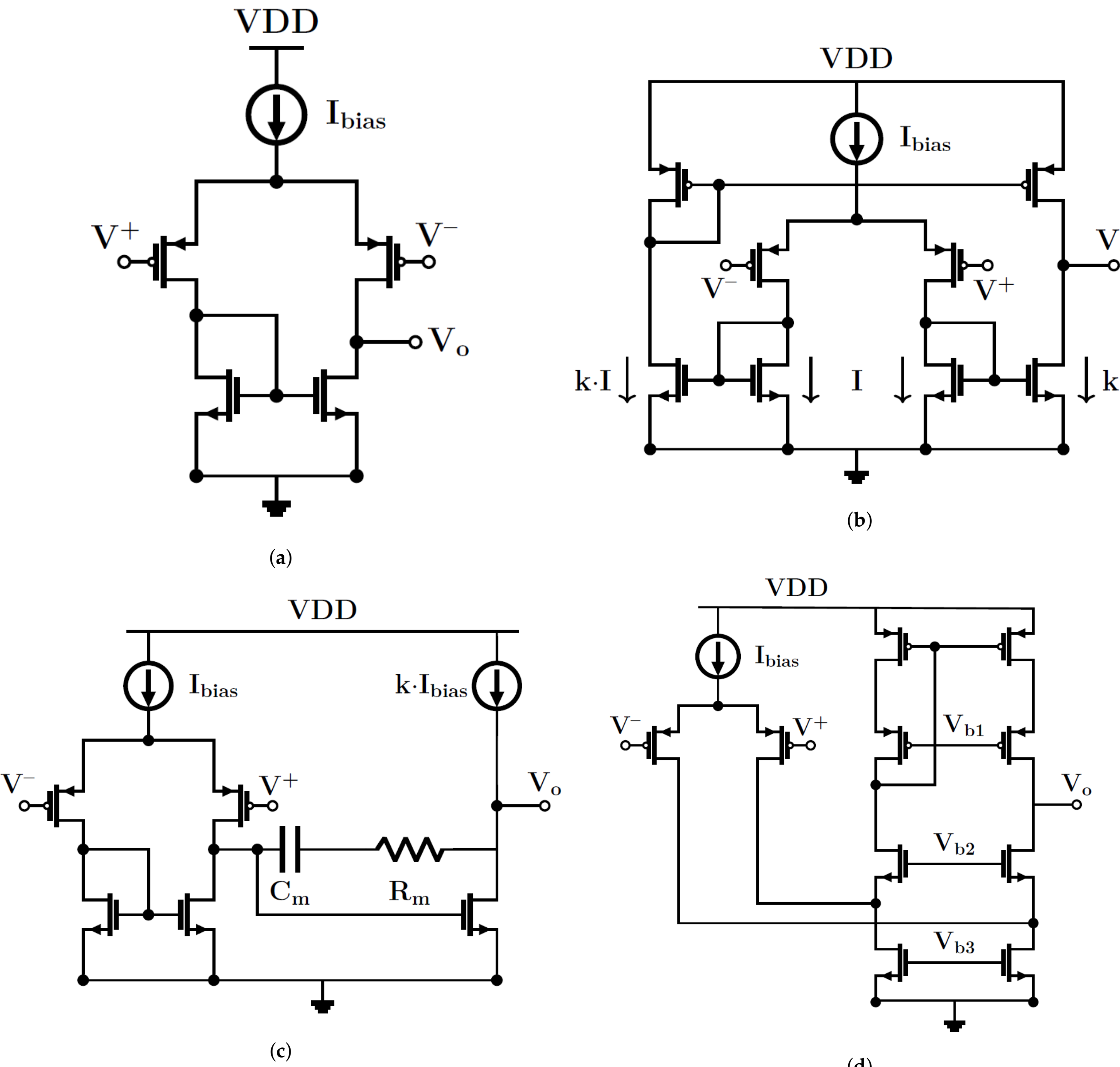



**Figure 4.** (**a**) Single-stage, (**b**) symmetrical, (**c**) two-stage Miller and (**d**) folded cascode OTAs.

### *2.4. Power Supply Rejection*

Power supply rejection (PSR) [13] is a critical parameter, particularly in LV circuits, where any disturber is more important than at high voltages. At low power, the impedance level is higher and so small current errors could result in large voltage errors. For the basic R-BG scheme and assuming the use of a symmetrical EA, the PSR frequency response is shown by the solid line in Figure 5. The DC-PSR value is given by the following equation:

$$\mathrm{PSR_{DC}} = \frac{R_3 \cdot (1 + g_{\mathrm{m,M3}} \cdot r_0)}{R_3 + r_0} \cdot \frac{1}{1 + g_{\mathrm{m,ea}} \cdot r_{\mathrm{ea}} \cdot g_{\mathrm{m,M3}} \cdot (R_{\mathrm{J}} - R_{\mathrm{K}})}, \tag{12}$$

where $g_{m,M3}$ is the transconductance of M3, $r_0$ the output resistance of M3, $g_{m,ea}$ the transconductance of the symmetrical EA ($\mathrm{k}{\cdot}g_{\mathrm{m,in}}$), $r_{ea}$ the output resistance of the EA and $R_J$ ($R_K$) the resistance at node J (K).

PSR with $C_C$ connected from $V_o$ to GND presents poles and zero as follows:

$$z_1 = \frac{1}{r_{ea} \cdot C_C}; \quad p_1 = \frac{1}{(r_0 \parallel R_3) \cdot C_{out}}; \quad p_2 = \frac{g_{m,M3} \cdot g_{m,ea} \cdot (R_J - R_K)}{C_C}. \tag{13}$$

The performance can be improved by increasing current consumption, i.e., reducing the output impedance of the EA. To increase the position of $z_1$, that is, increasing the bandwidth of the DC PSR, it is useful to connect the capacitor $C_C$ from $V_o$ to VDD instead of to GND. With this solution $z_1$ becomes:

$$z_{1c} = \frac{1 + g_{m,M3} \cdot r_0}{r_{ea} \cdot C_C}. \tag{14}$$

Figure 5 (dashed line) displays the effect of $C_C$ connected from $V_o$ to VDD increasing $z_1$ of a quantity $g_{m,M3} \cdot r_0$. The other poles maintain the same values.

Figure 5 shows that without $C_C$ the first zero is shifted to higher frequencies. This is positive, but it reaches worse values at higher frequencies. Due to $z_1$ and $z_{1c}$, which are close to each other, the slope of the PSR is about −40 dB/dec. The zeros are due to the parasitic capacitors. If the application requires a good PSR for a low range of frequencies, $C_C$ could be avoided, with consequent area saving. However, if a good PSR is needed for a high range of frequencies, it is better to place the first zero to a lower frequency. This allows a good PSR in the whole range of frequencies.

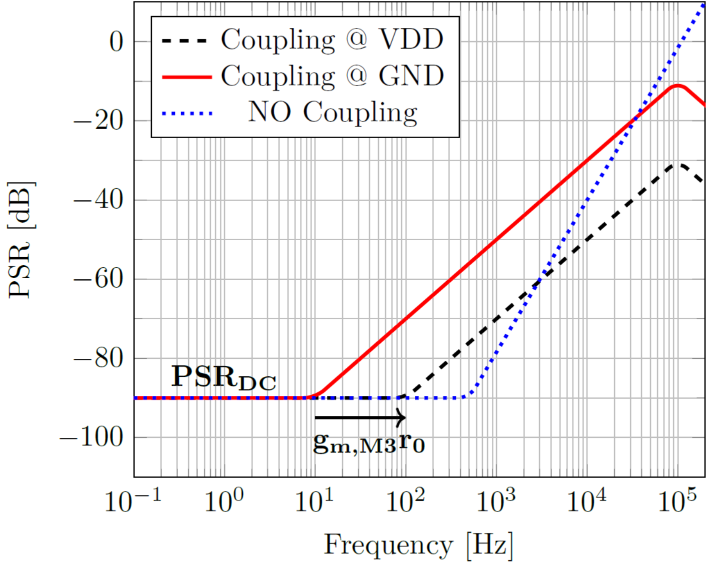



**Figure 5.** Comparison of a PSR typical shape without coupling capacitor $C_C$ (dotted line), with $C_C$ connected from $V_0$ to VDD (dashed line) and GND (solid line). The graph shows that $z_1$ is moved to higher frequencies by a factor $g_{m,M3} r_0$.

## 3. LV-LP BG Design in 65 nm Technology

The design in 65 nm CMOS technology of a LV-LP BG for audio applications based on the previous guidelines is proposed [14]. The developed circuit was fully characterized in the presence of PVT variations, and Monte Carlo simulations were used in post-layout for validation in terms of performance and robustness.

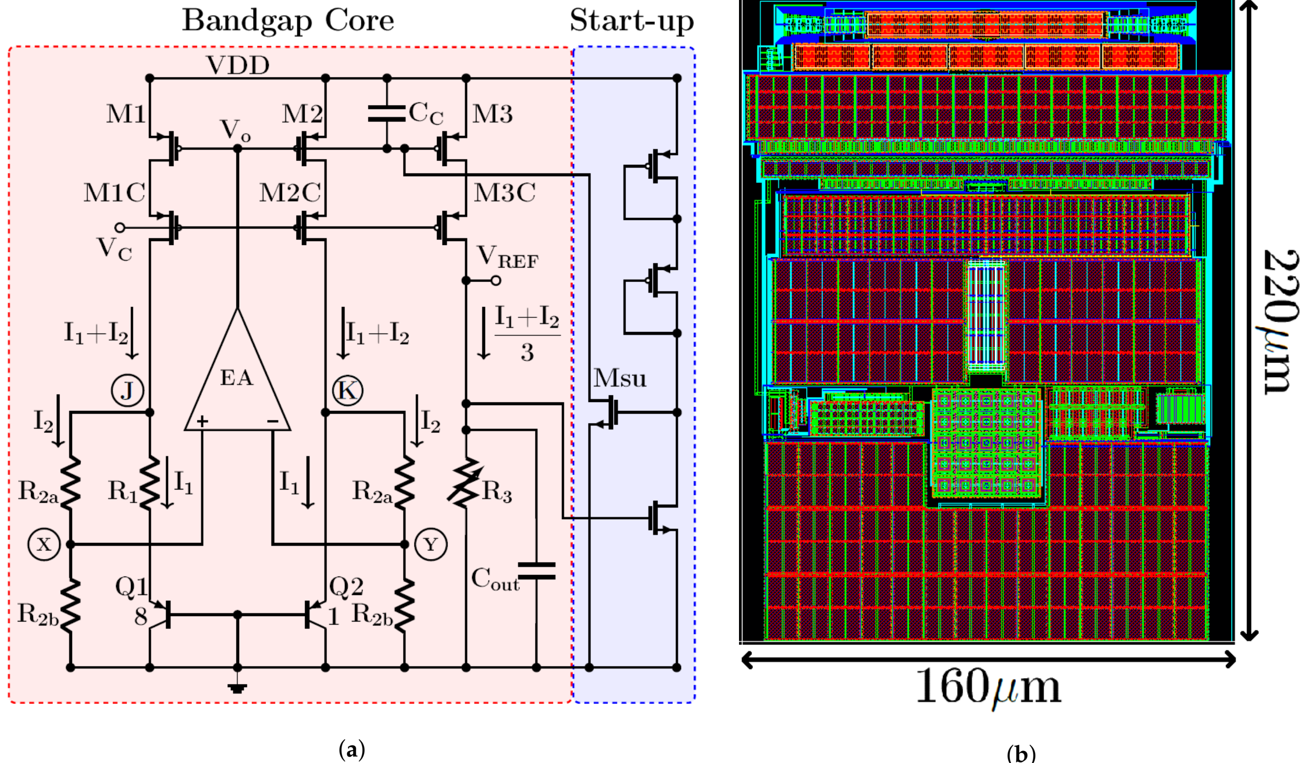
The R-BG is required to operate from the nominal VDD = 1.2 V ± 0.2 V. The R-BG has to provide 600 mV of $V_{REF,n}$ with a 6 mV maximum deviation at 3σ.

### *3.1. Bandgap Branch Design*

Figure 6 shows the developed R-BG structure. As a first step, the parameter N = 8 was adopted as a trade-off between minimum current and large $\Delta V_{EB}$ (2). This means that $\Delta V_{EB}$ = 26 mV·ln(N) = 54 mV, $I_1 = 8 \times I_\alpha \cdot (1+\beta)/\beta$ = 680 nA and $R_1 = \Delta V_{EB}/I_1$ = 81 KΩ. Consequently, from (3), $R_2$ = 790 kΩ ($m \sim$ 20.3). By having $V_{EB}$ = 690.9 mV and setting

$V_{REF,n}$ = 600 mV in (4), the value of $R_3$ is equal to 1170 kΩ with $\gamma = 3$. $R_3$ is a 4-bit trimmable resistor with a trimming range of 5 mV, resulting in $FS_{trim}$ = 75 mV around the nominal $V_{REF,n}$ = 600 mV. The value of $V_{REF}$ can be adjusted by 40 mV above and by 35 mV below (one of the 16 trimming codes is used to not apply any changes). To have enough biasing headroom without increasing the contribution of $V_{off}$ to $V_{REF}$, $R_{2a} = R_{2b}$ = 395 KΩ has been chosen.

All devices operate in the sub-threshold region, minimizing $V_{GS}$ request. Assuming $VDD_{min}$ = 1.0 V, the voltage space for the current mirror (M1–M2) is ($VDD_{min}$–$V_{EB}$) about 350 mV, which allows one to use cascode current mirrors with devices in the sub-threshold region. This optimizes also the output stage (M3) current accuracy.




(**a**) (**b**)

**Figure 6.** The 65 nm bandgap structure (**a**) schematic and (**b**) layout (total area = 0.0352 mm$^2$).

### 3.2. Error Amplifier Structure

As discussed above, a symmetrical EA is used (Figure 7). All transistors operate the in sub-threshold region, and the current mirrors can also be used from $VDD_{min}$ = 1.0 V. $V_{off}$ is reduced to be slightly lower than 0.5 mV by using large-area input devices. In this way, the maximum $V_{ERR}$ due to offset is about 20 mV; i.e., 50% of the $FS_{trim}/2$ is allocated for $V_{off}$ correction.

According to Figure 3, to guarantee a $\Delta V_{REF}$ lower than 1 mV in the temperature range [−40, 100] °C and a maximum trimming range of about 30 mV, EA DC-gain larger than 70 dB is needed. To avoid values that exceed this error during PVT simulations, a gain of 80 dB was chosen. Input stage and output stage currents are in the order of 40 nA each—negligible with respect to the BG branches, as expected. In Figure 8a a pie chart is reported with the power breakdown of the total BG structure. Figure 8b shows the power consumption and the total current of the BG depending on the supply.

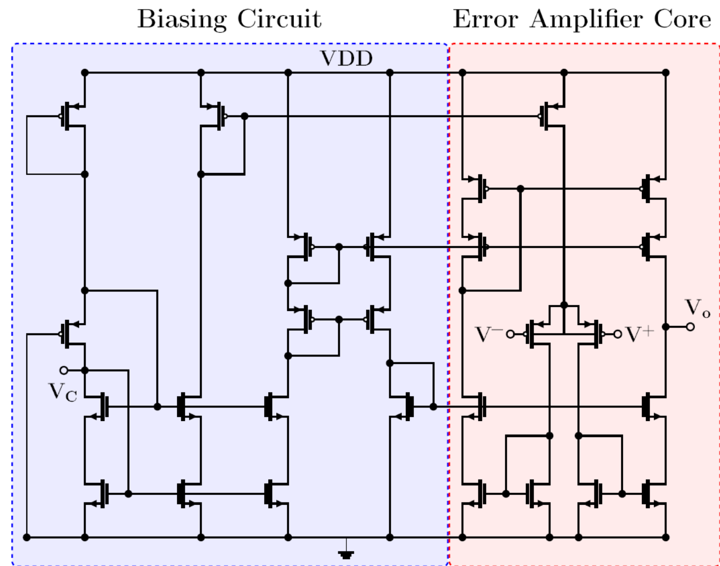



**Figure 7.** Schematic of the error amplifier.

(**a**)

(**b**)

(**c**)

**Figure 8.** (**a**) Power breakdown of the designed circuit. (**b**) Power consumption and total current vs. VDD. (**c**) Start-up transition behavior of $V_{REF}$, $V_o$ and $I_{DS}$ of M3.

### 3.3. Start-Up and Biasing Circuit

The start-up circuit (Figure 6a) is used to guarantee that the BG operates properly. For example, a wrong operating point can occur when no current is flowing in the circuit. During the start-up, transistor $M_{su}$ provides the current to reach the correct operating point. After this has been reached, $M_{su}$ turns-off because its $V_{GS}$ becomes zero. Figure 8c shows the start-up transition behavior of the $V_{REF}$, the EA output $V_o$ and the current flowing in M3 with a supply rise time of 100 µs.

The current consumption of the start-up circuit in the steady state condition is around 400 nA, and it represents the 9% of the total current (Figure 8a). This solution guarantees robust operation.

The biasing circuit is presented in Figure 7. It is used to bias the cascodes in the EA and the current mirror attached to the source of the differential input pair. Furthermore, it biases the BG cascode current mirror composed by M1C, M2C and M3C through $V_C$ (Figure 6a).

### 3.4. PSR Simulation

PSR performance is shown in Figure 9. The position of $z_1$ was shifted one decade higher because the value of $g_{m,M3} \cdot r_0$ was about 10. To save on area, $C_C$ was implemented by using PMOS transistors with the drains and sources connected to VDD and with the gates connected to $V_o$.

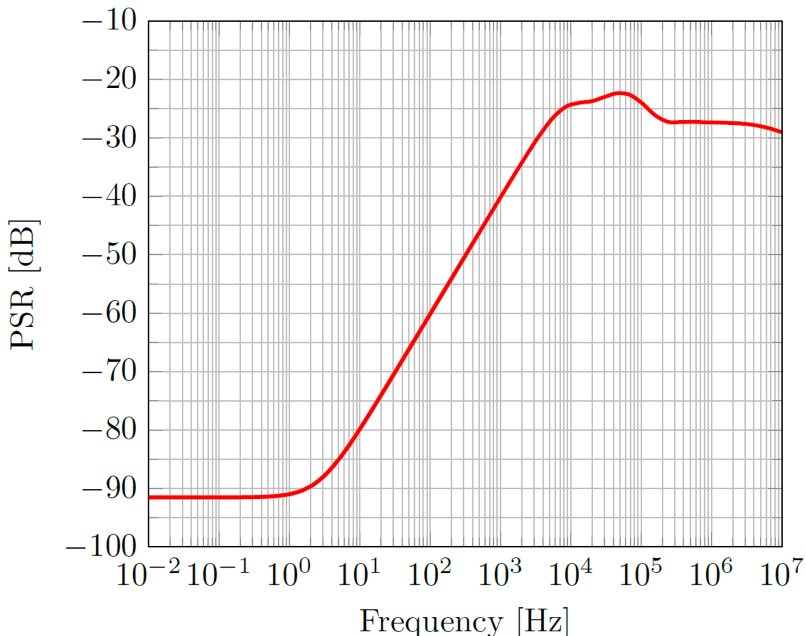
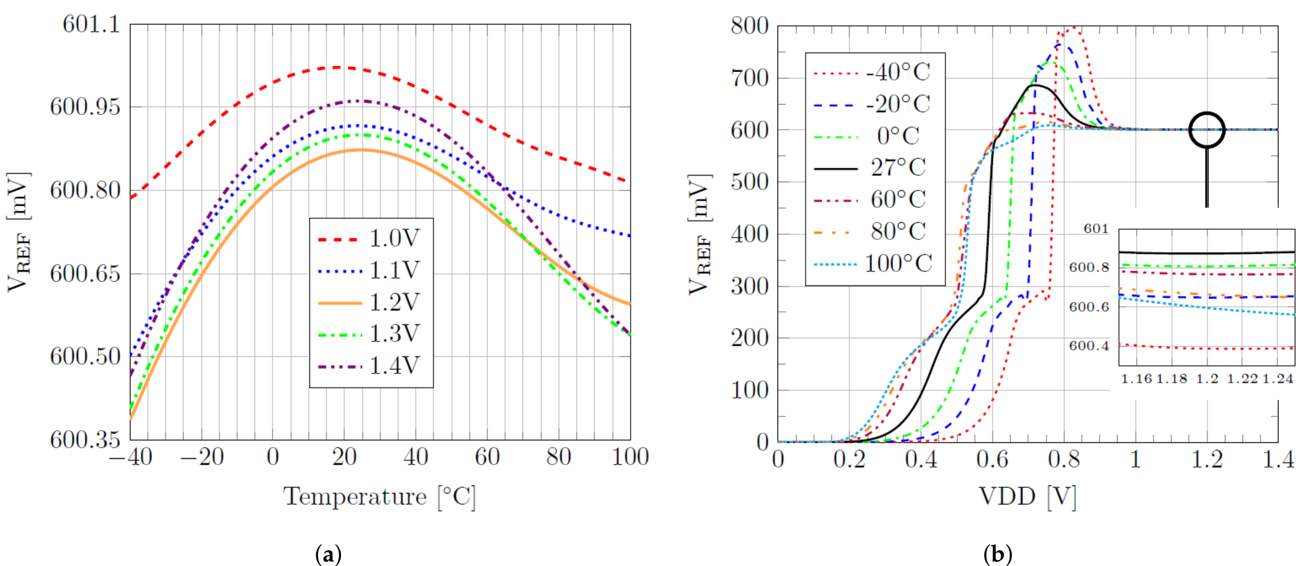



**Figure 9.** The PSR with $C_C$ at VDD post-layout simulation.

### 3.5. DC Simulation

Figure 10a presents the output curvature of the R-BG at different VDD values for the temperature range [−40, 100] °C as required by audio applications. There was a variation of 5 ppm/°C over the temperature range with a minimum value of 600.40 mV and a maximum of 600.87 mV. Hence, the total variation over the range was: $\Delta V_{REF}$ = 0.47 mV.

The dependency of $V_{REF}$ on the supply voltage is shown in Figure 10b. The R-BG properly operated for VDD levels as low as 1 V. The $\Delta V_{REF}$ for $V_{DD}$ between 1.0 and 1.4 V was 0.44 mV.




(**a**) (**b**)

**Figure 10.** Post-layout simulation of (**a**) $V_{REF}$ versus temperature at different VDD and (**b**) $V_{REF}$ versus VDD at different temperatures.

### *3.6. Monte Carlo Simulation*

Based on Monte Carlo simulations (considering a 2000-point simulation), before trimming, the $V_{REF}$ value varies in the voltage range from 575.2 to 630.3 mV with a σ of 7.77 mV. On the other hand, after trimming, the voltage range is reduced: $V_{REF}$ varies from 596.3 to 602.6 mV with a σ of 1.5 mV. This means a variation at 3σ of 1% instead of 4.5% without trimming. Figure 11 shows the histogram collecting simulations at 27 °C, before and after trimming. Moreover, Monte Carlo simulations revealed an EA $V_{off}$ of 471.2 µV at 1σ. This means that $V_{ERR}$ affects $V_{REF}$ for about 15 mV, to be adjusted by the trimming.

Table 1 compares the proposed R-BG performance with the state-of-the-art. The aggressive 5 ppm/°C outperformed SoA BGs with comparable power consumption. Moreover, in Table 2, the simulated performances are presented.

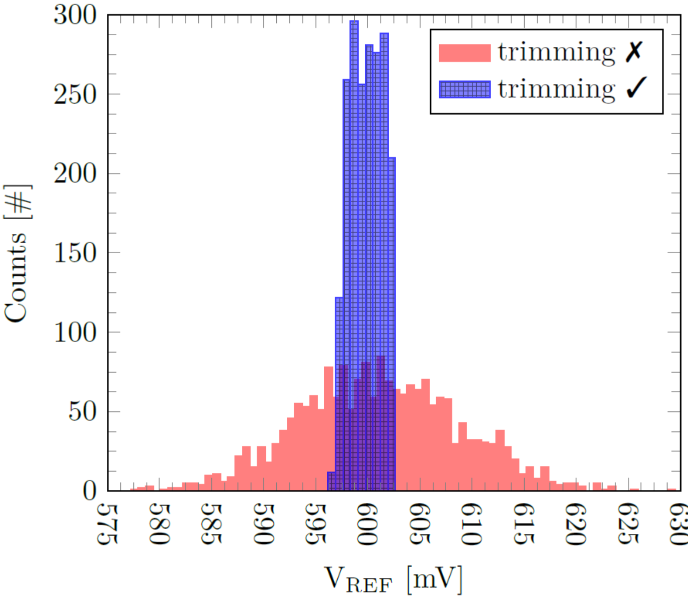



**Figure 11.** Combined histogram of Monte Carlo $V_{REF}$ with (grid) and without trimming (solid) at 27 °C and 1.2 V of VDD.

**Table 1.** Simulated performance compared with other works.

| | [13] S 2016 | [15] M 2016 | [16] S 2018 | [17] S 2014 | [18] M 2020 | [19] M 2016 | [20] M 2013 | This Work S 2020 |
|---|---|---|---|---|---|---|---|---|
| Proc. (nm) [1] | 180 | 65 | 65 | 65 | 65 | 65 | 65 | 65 |
| VDD (V) | 1.1–2.2 | 1.1–1.3 | 1.2 | N.A. | 0.5 | 0.3 | 0.6–1.2 | 1.0–1.4 |
| $V_{REF,n}$ (mV) | 800 | 466 | 730 | ∼441.5 | 495 | 168 | 435 | 600 |
| T. Range (°C) | −40∼125 | −55∼125 | −20∼100 | −45∼120 | −40∼120 | −20∼100 | −40∼125 | −40∼100 |
| P. Cons. (µW) | 19.8 | N.A. | N.A. | 104 | 0.036 | 0.07 | 0.22 | 5.2 |
| TC (ppm/°C) | 9 | 30.9 | 9.8 | 10.65 | 42 | 142 | 30 | 5 |
| PSR DC (dB) | −108 | −61 | −79 | −20.21 | −50 | N.A. | −38 | −91 |
| PSR 10 k (dB) | −68 | N.A. | ∼−30 | −20.21 | N.A. | N.A. | −27.5 | −24.8 |
| Area ($mm^2$) | 0.04 | 0.5 * | N.A. | N.A. | 0.0522 | 0.0053 | 0.024 | 0.0352 |

[1] CMOS process, S simulation, M measurement, * bond pads included, N.A.: Not Available.

**Table 2.** Simulated performance of this work.

| Parameter | Value |
|---|---|
| CMOS process | 65 nm |
| $V_{REF,n}$ | 600 mV |
| $3\sigma_{V_{REF}}$ | 6 mV (1%) |
| Supply Voltage Range | [1,1.4] V |
| Total Current | 4.3 µA |
| Power Consumption | 5.2 µW |
| DC Gain | 79.21 dB |
| EA Input Referred Offset | 471.2 µV (at 1 σ) |
| Temperature Range | [−40,100] °C |
| Temp. Coefficient | 5 ppm/°C |
| PSR DC/1 kHz/10 kHz | −91.0 dB/−52.6 dB/−24.8 dB |

## 4. Conclusions

In this paper, a methodology to design a low-power bandgap was presented. We focused on the component sizing to reduce the current consumption and then covered the design of the bandgap branches and which EA should be used, upon target specifications.

A 65 nm, CMOS, low-power bandgap design with the proposed guidelines was presented and compared to the SoA. The former had a higher PSR, resulted in a superior temperature coefficient and required less power consumption. In comparison with [13], the PSR was worse, but the TC and the power consumption were better. To conclude, this work can be considered a good trade-off between high performance and low power consumption.

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