PROCEEDINGS OF SCIENCE

# A 28 nm Fast Tracker Front-End for Phase-II ATLAS sMDT Detectors

**Alessandra Pipino, Marcello De Matteis, Federica Resta, Luca Mangiagalli[1], Andrea Baschirotto**
*Dept. of Physics "G. Occhialini", University of Milan-Bicocca,*
*Piazza della Scienza 3, 20126 Milan, Italy*
*E-mail:* alessandra.pipino@unimib.it

**Hubert Kroha, Robert Richter, Oliver Kortner**
*Max-Planck-Institute for Physics*
*Föhringer Ring 6, 80805 Munich, Germany*

This paper presents a Fast-Tracker front-end (FTfe) for ATLAS small-diameter Muon Drift Tube (sMDT) detectors of the Phase-II Upgrade HL-LHC. This design addresses the higher rate capability required by sMDT and reduces the dead-time below the maximum drift time, further increasing the efficiency. The front-end ensures a fast baseline restoration with a reset interval of maximum 160 ns, so that the secondary spurious pulses are avoided and the successive muon signals can be detected soon and correctly. The device has been designed in 1V-28nm-CMOS technology; 4.7mV/fC sensitivity and 0.24fC ENC are achieved with a core area of 0.03mm$^2$.

*Topical Workshop on Electronics for Particle Physics (TWEPP2018)*
*17-21 September 2018*
*Antwerp, Belgium*

[1]Speaker





PoS(TWEPP2018)091

## 1. Introduction

The high luminosity and interaction rate of the Phase-II Upgrade HL-LHC (High Luminosity-Large Hadron Collider) imposes challenging requirements for the detectors and the read-out electronics, since a lot of overlapping events per bunch crossing accompany the interesting events. The use of ultra-scaled ICs in the High-Energy-Physics (HEP) experiments allows for read-out systems with higher speed, resolution and smaller area, without compromising target performance like sensitivity, Equivalent Noise Charge (ENC) and peaking time. Moreover, it is possible to exploit the intrinsic radiation hardness of the ultra-scaled technologies [1][2].

The read-out electronics used for muon detection in the current MDT chambers consist of ASD (Amplification-Shaper-Discriminator) blocks to extract charge arrival time and amplitude information, followed by a proper TDC for digital conversion. Secondary spurious pulses (SSPs) cause multiple crossings in the signal tail for each muon track, increasing the data volume to be read. As the storage capability is limited, the read-out system uses small time constants and/or bipolar shaping to cancel the tail, together with additional dead-times (up to maximum drift-time of about 750 ns) to disable the detection of multiple crossings.

The improved small-diameter MDT (sMDT) chambers, for which the proposed front-end has been designed, have 15 mm instead of 30 mm diameter drift tubes, resulting in a shorter maximum drift-time (~180 ns) and, consequently, 10 times higher rate capability. Therefore, less dead-time can be used in the read-out system, even if this increases the pile-up effects of muon signals on top of the undershoot of preceding background pulses.

The Fast Tracker front-end (FTfe) presented in this paper has been designed to exploit the improved efficiency and spatial resolution of the sMDT chambers. Integrated in 28nm-bulk-CMOS technology (one of the first devices for this sector in this node), FTfe is characterized by the selection of useful information only for the primary hit, disabling then the front-end by a reset of the preamplifier, for a short time interval.

## 2. FTfe Architecture

The proposed FTfe architecture, whose block scheme is shown in Figure 1, collects the information of the incoming chamber signals, i.e. arrival time and charge amplitude, through fast and efficient tracking, which consists in:

- event arrival time detection, considering a first threshold $V_{TH1}$ crossing time;
- charge amplitude measurement, using two threshold ($V_{TH1}$ and $V_{TH2}$) crossing times;
- front-end reset, after charge measurement.

In the block diagram of Figure 1, the input current pulse coming from the muon detector is converted into a voltage signal by the Charge Sensitive Preamplifier (CSP), composed by the single-ended opamp and a passive feedback net $C_F$-$R_F$. The CSP output voltage is shaped and amplified by an Active-$G_m$-RC Filter, with unipolar shaping for tail cancellation. The Shaper output is fed into two comparators, which compare it with two different thresholds generated by resistive dividers. The output signal $V_{OUT\_COMP1}$ of the first comparator contains the information about the lower-$V_{TH1}$ crossing time, which represents the charge arrival time. The two signals $V_{OUT\_COMP1}$ and $V_{OUT\_COMP2}$ (corresponding to the higher-$V_{TH2}$) are provided to a Logic block in order to generate the reset and the TIME_DIFF signals. The reset signal controls the switch $S_W$ in

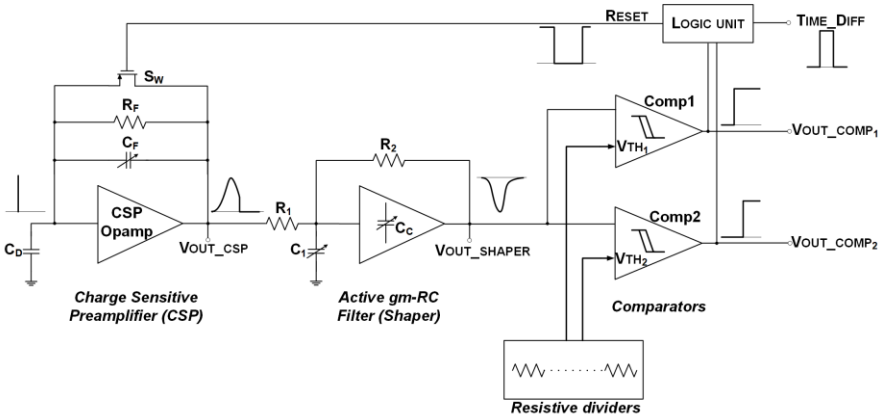


Figure 1. FTfe block diagram.

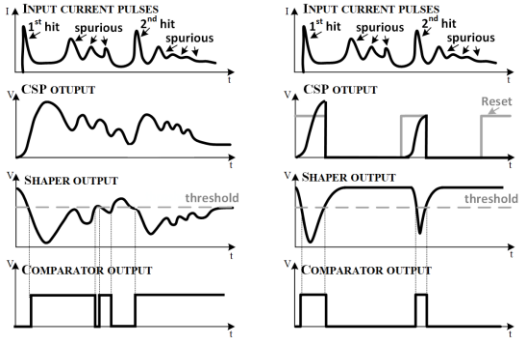


Figure 2. Comparison between the classical read-out system without reset (left) and the proposed FTfe behaviour (right).

Table 1. FTfe specifications.

| Parameter | Value |
|---|---|
| Input charge $Q_{IN}$ | 5-100 fC |
| Detector capacitance $C_D$ | 10 pF |
| Peaking time delay $T_P$ | ≤ 30 ns |
| Sensitivity S | > 4 mV/fC |
| ENC | < 0.5 fC |

Table 2. FTfe specifications distribution.

| | CSP | Shaper |
|---|---|---|
| Peak Amplitude ($Q_{MIN}$-$Q_{MAX}$) | 5–100 mV | 25-500mV |
| Peaking time delay | ≈10 ns | ≈30 ns |
| Output integrated noise | < 400 $\mu V_{RMS}$ | < 2 $mV_{RMS}$ |

feedback to the CSP; when the switch is closed, $C_F$ is discharged and the CSP output is reset to the baseline voltage. During the entire reset interval, the CSP output is insensitive to any signal at the input. As soon as the reset signal is disabled, the front-end returns to detect the next incoming pulses. The TIME_DIFF signal contains the charge information as a measure of the initial slope of the Shaper output, which changes with the charge. In particular, for each hit, TIME_DIFF shows a pulse, whose width corresponds to the difference between $V_{TH1}$ and $V_{TH2}$ crossing times of the Shaper output and changes with the slope. The charge information allows making a time slewing correction.

A simplified timing diagram of the front-end behaviour in response to a typical input current pulse is shown in Figure 2. The case of a read-out system without reset and dead-times (Figure 2, left) is compared to the proposed FTfe system (Figure 2, right). Generic CSP and Shaper output signals are shown, for an arbitrary amount of input charge. At the top of Figure 2, the typical pulse shape, induced by two consecutive muon hits together with their SSPs, is shown. In the read-out system without reset and dead-times, the SSPs are processed by the CSP, the Shaper and the comparator, since the threshold is crossed several times. Moreover, pile-up occurs with the next pulse, which may lead to incorrect amplitude and, therefore, timing information. For this reasons, in the classical read-out system, long fixed dead-times must be used. In the FTfe system, CSP is reset and the SSPs are not processed, neither by the CSP nor by the Shaper. In this way, the Shaper output returns to the baseline faster than in the classical case and the front-end is able to process the next signal soon. The target specifications considered only to validate the Fast Tracking idea are summarized in Table 1. Starting from these requirements, the main characteristics as voltage

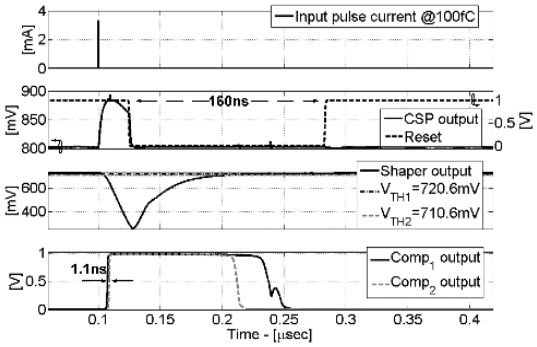


Figure 3. CSP, Shaper, Comparators and Reset signals at 100fC input charge (post-layout simulation).

peak, peaking time delay and noise have been distributed among the front-end building blocks, i.e. CSP and Shaper, as shown in Table 2.

## 3. FTfe Performance Results

The presented FTfe prototype has been integrated in 28nm-CMOS technology with 0.03mm$^2$ area, suitable for multi-channel devices. The front-end operates with 1 V supply voltage and consumes 1.9 mA (shared as 1.2 mA in the CSP, 0.5 mA in the Shaper, 0.1 mA in each comparator). Transient noise post-layout simulations are shown to demonstrate FTfe functionalities (these nodes are not externally available in the prototype). The muon detector is modelled with a current pulse generator in parallel to $C_D$. The input current pulse amplitude is fixed as $Q_{IN}/Q_{TIME}$, where $Q_{TIME}$ is very short and equal to 30 ps and $Q_{IN}$ is the input charge which can assume values from 5 fC (166 μA) to 100 fC (3.3 mA). In Figure 3 input current pulse, analog signals (CSP and Shaper outputs with threshold voltages) and digital signals (Reset and Comparators outputs) are reported for maximum charge. The CSP output amplitude voltage is equal to 82.6 mV, with a baseline voltage equal to 802.4 mV and peaking time delay of 11 ns. At the Shaper output, the peak amplitude is 469.6 mV, with a baseline voltage equal to 725.6 mV and a peaking time delay of 28 ns. Voltage thresholds very close to the baseline have been used in order to detect the crossings also for the minimum charge. In particular, $V_{TH1}$ and $V_{TH2}$ are set to -5m$_{VDC}$ and -15m$_{VDC}$ respectively from the Shaper signal baseline. As shown in Figure 3, at maximum charge the slope is very steep and the two comparators switch with a delay of 1.1 ns relative to each other, which represents the TIME_DIFF pulse width. At minimum charge, when the slope is soft, the TIME_DIFF pulse width is larger and equal to 9 ns. Notice that the reset interval starts soon after the comparators switching, and its length is 160 ns for maximum charge. When the reset signal becomes low, the CSP output signal is restored to the baseline voltage.

In order to validate the front-end, post-layout simulations and lab measurements with two consecutive hits are performed, reading the first comparator output. Figure 4 and Figure 5 show the generated input signal, the CSP output with the reset and the first comparator output, in post-layout simulation and measurement, respectively. In the measurement plots, the input signal is reported as a voltage signal taken on the PCB after an input network and capacitance $C_D$, where the two steps correspond to the two close-by hits. The input network influences the CSP and Shaper behaviour and indeed ToT and reset interval are larger than the expected values seen in simulation. However, this measurement confirms that the CSP output signal returns to baseline when the reset is low and, during the reset interval, the front-end does not read any incoming hit. Only the primary pulse is read, as seen in the simulation of Figure 4 (2$^{nd}$ diagram from the top).

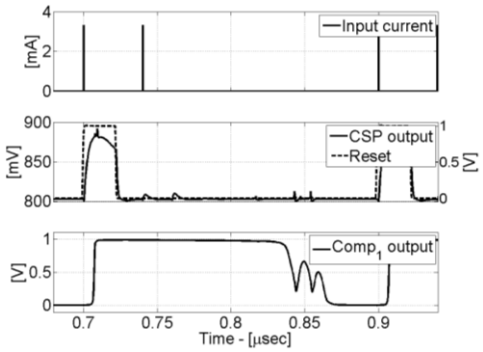


Figure 4. FTfe post-layout simulation with several pulses.

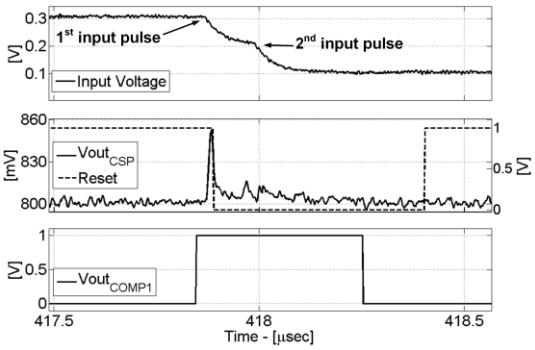


Figure 5. FTfe measurement with two consecutive pulses.

## 4. Conclusions

Post-layout simulations validate the proposed architecture, with interesting performance parameters like peaking time delay of 28 ns, sensitivity of 4.7 mV/fC and ENC of 0.24 fC, all measured at the Shaper output. The resulting dead-time of maximum 160 ns is less than the maximum drift-time, in line with the sMDT requirements. Preliminary measurements are promising and confirm the expected front-end operation.

## Acknowledgment

This activity is within the INFN ScalTech28 project.

## References

[1] S. Mattiazzo, et al., *Total Ionizing Dose effects on a 28 nm Hi-K metal-gate CMOS technology up to 1 Grad*, Journal of Instrumentation, 2 February 2017

[2] Zhang, Chun-Min, et al., *Characterization of gigarad total ionizing dose and annealing effects on 28-nm bulk MOSFETs*, IEEE Transactions on Nuclear Science, 64.10 (2017): 2639-2647.

[3] Aad, Georges, et al., *The ATLAS experiment at the CERN large hadron collider,* Journal of Instrumentation, 2008, 3.8: S08003-S08003.

[4] De Matteis, M., et al., *Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC*, Journal of Instrumentation, 11.02 (2016): C02087.

[5] De Matteis, Marcello, et al., *An Eight-Channels 0.13-μm-CMOS Front End for ATLAS Muon-Drift-Tubes Detectors*, IEEE Sensors Journal, 17.11: 3406-3415.

[6] W. Riegler et al., *MDT Resolution Simulation Frontend Electronics Requirements*, ATL-MUON-97-137, CERN, 1997.

[7] C. Posch, E. Hazen, and J. Oliver, *MDT-ASD User's Manual*, ATL-MUON-2002-003, CERN, 2007.

[8] H. Kroha et al., *New High-Precision Drift-Tube Detectors for the ATLAS Muon Spectrometer*, Journal of Instrumentation, 12 (2017) C06007.

[9] O. Kortner et al., *Precision Muon tracking Detectors and Read-out Electronics for Operation at Very High Background Rates at Future Colliders*, Nuclear Instrum. and Methods, A 824 (2016) 556-558.

[10] S. D'Amico and A. Baschirotto, *An active-Gm-RC continuous-time biquad low-pass cell*, Electronics, Circuits and Systems, 2003. ICECS 2003. Proceedings of the 2003 10th IEEE International Conference on., Vol. 2. IEEE, 2003.