

# PCMC DC-DC Converter Development Methodology by Means of dSPACE

Osvaldo Gasparri<sup>1(⊠)</sup>, Roberto Di Lorenzo<sup>1</sup>, Paolo Del Croce<sup>2</sup>, and Andrea Baschirotto<sup>1</sup>

<sup>1</sup> University of Milan Bicocca, Milan, Italy o.gasparri@campus.unimib.it <sup>2</sup> Infineon Technologies Austria AG, Villach, Austria

Abstract. This work describes the development methodology of an electronic device. All the phases, starting from the definition of the specifications up to the fabrication of the device, will be explained using the evolution of a project aimed at developing a high-performance DC-DC converter for LED driver application as a use case. The project involves teams and experts from the technology department, the product development and the fabrication. It is therefore important to have an efficient process flow, ensuring the optimal communications and information transmission between the teams. In addition, the project here presented introduces a novelty regarding the concept phase. The use of a rapid control prototyping tool, called dSPACE, guarantees the feasibility of a concept circuit before proceeding directly with the design phase, avoiding time-wasting. In fact, the mentioned emulator allows the preliminary evaluation of the circuit in ideal conditions and, subsequently, a more real study on hardware.

Keywords: Methodology · DC-DC Converter · dSpace · Simulink · Concept

## 1 Motivation

The aim of this work is to make the development process of an industrial microelectronic device that starts from the definition of the specifications and ends with the product fabrication, more efficient. To do this, it is important to operate within a well-defined workflow between the different teams involved, each of which will mainly work on a specific phase of the project. The clear definition of the process phases, together with the clear transmission of the project information/results between all the involved teams, by means of digital twins, guarantees the continuity of the chain, improving efficiency and minimizing troubles. Each step involves the use of dedicated software that will return a digital file in a special format, subsequently used as input for the next step. The result is a digital chain in which the composition rings and junctions are already defined from the beginning.

Each process step is explained here using the evolution of a Buck DC-DC converter as a use case. Since, for the specific microelectronic case, circuit design is usually the longest and most problematic phase, it is convenient to exploit a concept phase where the architecture of the entire circuit is identified and validated in advance. This is what

the environment dSPACE does through the mixed implementation between software (Simulink) and hardware (a dedicated board), returning a block scheme of the prototype circuit to be designed.

The developed methodology intends to be valid for any other device to be realized, improving production efficiency.

## 2 Methodology Description

The chapter explains the digital phases of the development process one by one. Figure 1 shows a flowchart of the development process leading to the production of a generic circuit. The process has a well-defined chronological sequence. Each step involves experts of specific teams, working on specific software. Furthermore, each block of the chain is connected to both the previous and the next. This connection (arrows, in Fig. 1) could be a simple passage of information, such as a file containing the dataset, or it could be a very complicated file in a special format containing the circuit design/layout. These files are the single source of truth for the teams concerned (also spelled out in Fig. 1). In fact, in each new step, the starting point is the file returned from the previous phase, regardless of what happened before or how. Digital twins are used to efficiently switch from one step to another without discontinuity or troubles.

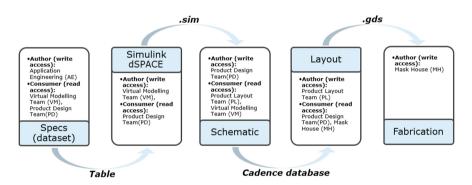


Fig. 1. Development methodology

Once the workflow is clear, it is necessary to define the project and its application. In the automotive industry any electronic device works with the car battery, whose voltages range from 7–8 V to >27 V due to cold-cranking and load dump. However, to avoid damages to such devices, their supply source should be stable and consistent with their datasheets. A Buck DC-DC Converter could be used to reduce the value of a voltage/current supplied as an input. In addition, a control circuit is used to make its output equal to the desired value. The controlled DC-DC Converter is then placed between the battery and the electronic device to ensure correct operation. In the case considered, the device is the LED for street lighting.

Every project starts with the definition of the specifications: this happens e.g. in a meeting with all the experts from the teams involved. The list of specifications, or

dataset, contains the key features of the circuit to be designed. These can be circuit technical specifications, such as the value of the DC-DC output current, or costumer requirements such as economic or temporal aspects. Note that the product price influences the technical specifications. Since the silicon prize is 0.01–0.02 €/mm² (depending on the technology), the area of the chip must be minimized. Consequently, the most complex circuit topologies could already be discarded because they would be too bulky. In the meantime, it is important to guarantee high efficiency of the circuit: the best solution will be chosen in terms of efficiency/price ratio.

The specification list will then be placed in a database or in a read-only file stored on a corporate server. Only employees within the project have the right of access to open the file and read the dataset at one time. In the event that a specification changes (e.g. if the concept circuit test through dSPACE shows a discrepancy between a specification and a technology limit), the data will be modified or updated. So all the colleagues will only see the updated data. This avoids problems related to bad communications between teams. Table 1 shows the DC-DC Converter dataset. The parameters are initially listed and are no longer changed. Only their values can change.

	•	•
Parameter	Measure unit	Value
Switching frequency	kHz	<400
Input voltage range	V	[7,26]
Inductance	μН	<40
LED peak current	A	<3.5
LED ripple current	A	[2.6,3.4]
LED mean current	A	$3 \pm 5\%$

**Table 1.** List of specifications (dataset)

This first phase returns a string of numbers/ranges obtainable from the Table, namely:

$$\{400, [7, 26], 40, 3.5, [2.6, 3.4], [2.85, 3.15]\}$$

This string will be the input for the concept phase of the main-block-circuit. Note that the product price is not directly part of that dataset. However, some specifications may indirectly bring this information: for example, the inductance value is limited to  $40~\mu H$ . A higher value would result in a more expensive coil and a higher area occupation. On the other hand, a higher inductance value would lead to a more accurate led driver: in fact the inductance is inversely proportional to the current ripple (Everett 1999; Zainal 2003). The lower the ripple, the closer the output current to the mean value desired by the LED, allowing it to operate safely. Finally, technology also influences the specifications: the higher the switching frequency, the higher the power consumption but, at the same time, the higher the accuracy. A compromise must be found.

The concept phase, aimed at finding the optimal solution, begins now. First of all, researchers and product development experts study the state of the art for a first

analysis of all possible solutions. At the same time, the rules that describe the circuit operation must be deduced. For the reader, the DC-DC Converter can be represented by a black box (consisting of a transistor, an inductor etc.). (Mike 2011) provides the proper schematic. Its role is simple: whatever changes from the output, the circuit must guarantee a fixed current to the output load (the LED). This is done by turning a switch (the transistor) on and off repeatedly (at 400 kHz). In this way, the current supplies to the output rises and falls very quickly, obtaining an almost constant value (Everett 1999). However, a DC-DC Converter alone cannot be insensitive to external perturbations: it needs a "control loop". By reading the output current value, the control loop is able to determine when it is time to turn the switch on and off, making the current as close as possible to the desired value. Here is an example of how the control loop might work: reads the output current; compares the current with the peak current specification; turns the switch off if the output current exceed this value; waits 1/400 kHz before turning the switch back on. This is how the so-called "Peak Current Mode Control (PCMC) DC-DC Converter" works.

Obviously, there are many other control loop solutions (Lloyd 1985, Frank 2007). The concept phase must filter the best solutions, simulate them and compare their results. This is made with a first high-level simulation in ideal conditions of the solutions found. The high-level concept circuit is created using the MATLAB's Simulink software. Here a circuit appears like a set of blocks connected together. The blocks can be predefined (logical operators, counters, registers, etc.) or can be programmed using MATLAB to perform the desired function. It is therefore possible to simulate any type of circuit. The PCMC DC-DC Converter has the block representation of Fig. 2.

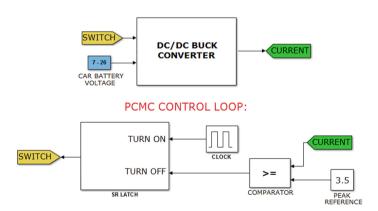


Fig. 2. Simulink block approach of the controlled DC-DC Converter

Simulation's plots and data are the feedback to understand the suitability of the solutions. If unsatisfactory, the circuit can be easily adjusted or upgraded. In fact, from the PCMC loop (Fig. 2, lower side), many other solutions can be obtained (Osvaldo 2019). For example, the clock that decides when to turn on the switch can be replaced

with another comparator: if the current drops below a lower value (e.g. 2.6 A), the switch is turned on. The Hysteretic Current Mode Control (HCMC) is thus obtained which accurately controls the current ripple. While, for better control of the average current value the Average Current Mode Control (ACMC) can be obtained (Lloyd 1999).

After a first screening of the solutions and their simulations, the test on hardware is the next step: no longer in ideal condition, but this time also considering all the parasitic elements that could affect the efficiency/operation of the circuit. The rapid control prototyping tool called dSPACE comes into play (dSpace 2011). dSPACE takes the Simulink file as an input. In fact, this emulator contains an FPGA module (programmable via Simulink) on which the Simulink circuit is downloaded, after having been automatically translated and coded in VHDL. So the emulator dSPACE becomes the desired circuit to be tested. For example, it can be used to test all the DC-DC control loops once at a time. The DC-DC Converter (Fig. 2, upper side) is instead incorporated in a Printed Circuit Board (PCB). Connected to the PCB output there is the LED. In this way, the test takes into account the actual behavior of the switch and the LED. Figure 3 shows the prototype.

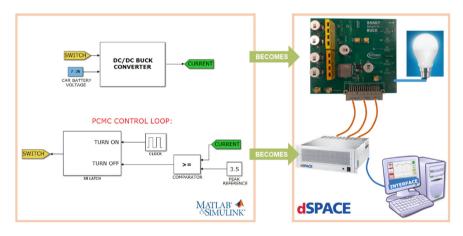


Fig. 3. Set-up. From Simulink (left) to dSPACE (right)

dSPACE contains a PowerPC that deals with little time-demanding calculations and interfacing with the rest of the modules. It also provides real time communication with the host PC. This means that, both before and during the test, the user can manage everything with a Graphic User Interface (GUI), easily created using the dedicated software Control Desk. Here, the user can directly enter specifications string returned from the first phase (from Table 1) and run the circuit testing. Figure 4 shows the scheme of the laboratory environment, relating to the DC/DC use case. The results obtained in the concept phase are then presented to the AE/PD experts, who will decide among the chosen solutions the optimal one with which to proceed to the design phase.

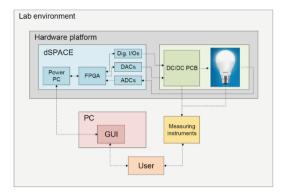


Fig. 4. Scheme of the Laboratory environment

The .sim file from the concept phase is the input for the design phase in which the Simulink blocks will be designed at transistor level. This is accomplished by creating a schematic in Cadence, software of Virtuoso. This is the most critical phase. Many difficulties can arise. Every single component is simulated by varying the process, temperature etc., to ensure the correct circuit operation even in the worst situation. Once the circuit is designed, the schematic file is given to the layouter who will draw the layout. The.gds file returned will then be the input for the fabrication phase. Figure 5 shows these latter phases. However, before obtaining the final product, the chips must be tested in laboratory to verify their operation, robustness etc. Sometimes there are errors or inaccuracies that make it necessary to modify the schematic. The process restarts from the design phase by creating a loop. It will take a long time for the chip to work properly, in line with the specifications and ready to be sold.

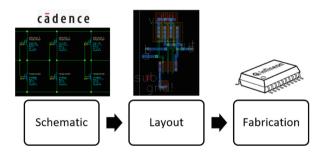


Fig. 5. Final development phases

#### 3 Results

This section is reserved to show the results of the concept phase for the PCMC DC/DC converter LED driver, both during the Simulink simulation and the dSPACE test, using the set-up of Fig. 3. Figure 6 shows the circuit operation during a Simulink simulation.

At one point, an abrupt change in the voltage of the car battery was simulated: the output current was changed accordingly. Worst conditions simulations allow to understand the robustness of the circuit.

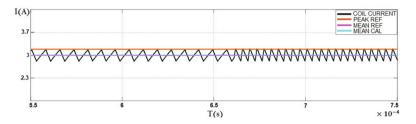


Fig. 6. Output current waveform from Simulink simulation

After a first screening of the simulated solutions, dSPACE is used to test their behavior no longer in ideal condition. As shown in Fig. 3, the basic DC-DC Converter circuit becomes a PCB, while the control loops are downloaded one by one into the FPGA of dSPACE.

Through a GUI, Fig. 7, users controls the operation of the system. In particular, some circuit specifications can be set. It is also possible to set an upper limit for voltage and current against over-current and over-voltage. Waveforms, e.g. the output current, can be directly displayed on the computer together with other parameters, such as the input voltage from the car battery. However, for better precision, the oscilloscope is used. Figure 8 shows all waveforms of interest from scope, which also provides the peak, the ripple, the mean and the switching frequency values. Note that, in this case, the output current sensing is made through a 0.5  $\Omega$  resistance. Therefore, all those values in the low bar of Fig. 8 relating to a current signal, but displayed in Volts on the scope, should be divided by 0.5  $\Omega$ , to obtain the respective in Amps. For example:  $I_{max} = 1,65 \text{ V}/0,5 \Omega = 3,3 \text{ A}$ . The results from Simulink and dSPACE can be then compared to evaluate the impact of the parasitic elements and the presence of the LED on the response of the system.

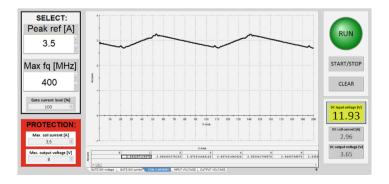


Fig. 7. Graphic User Interphase (GUI) during circuit testing

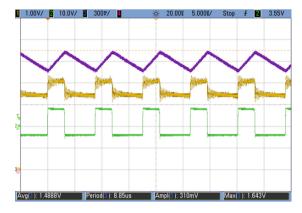


Fig. 8. From scope: current (violet); output voltage (yellow); switch activity (green)

# 4 Discussion/Implications

The results of the simulated and tested solutions will be presented and discussed before the experts. A table resuming the pros and cons of all the topologies will be the tip of the scale to choose the optimal solution on which to continue further development. Table 2 is the example in the case of the DC-DC Converter, in which many control loops have been tested and compared. The PCMC was preferable over the HCMC and ACMC. Subsequent improvements led to the PCMC with Slope Compensation and the final optimal concept renamed Variable off Time PCMC (Osvaldo 2019).

Parameter	HCMC	ACMC	PCMC	PCMC + SC	VoT-PCMC
Loop simplicity	++	_	++	+	+
Regulation Precision	_	+	_	_	++
Noise immunity	_	++	_	_	++
Reference perturbation	_	++	+	+	+
Line perturbation	+	+	+	+	++
Rapidity	++	_	++	++	++
Sampling advantages	_	_	++	++	++
Stability	++	++	_	++	++
Improvement available	_	_	++	_	_

Table 2. Pros and cons of the screened solutions

The VoT-PCMC Simulink file becomes the input of the delicate design phase. During Simulink's ideal simulations no problems arise (since the limiting factor is the computer hardware). While, during the dSPACE test phase, the efficiency of the circuit could be significantly reduced. In fact, the dSPACE platform has intrinsic delays that may lead to systematic errors. The source of these delays lies in the Analog to Digital Converter (ADC). This is used for instance for reading the output current (analog signal)

and for translating it into a digital signal to be used later to make comparisons/turn the switch on and off. Delays could lead to wrong system states. However, once the error source is known, problems can be avoided.

## References

dSpace: Hardware Reference, FPGA DS5203, PPC DS1005, datasheet (2011)

Rogers, E.: Understanding Buck Power Stages in Switchmode Power Supplies, Texas Instruments (1999)

Xi, F.: Design of DC-DC Converters, October 2007, IEEE SSCS Dallas Chapter (2007)

Dixon Jr., L.H.: Closing the feedback loop. Texas Instruments (1985)

Dixon, L.: Average Current Mode Control of Switching Power Supplies. Uni-trode (1999)

Wens, M., Steyaert, M.: Design and Implementation of Fully-Integrated Inductive DC-DC Converters in Standard CMOS, Chapter 2, 2011th edn. Springer, Heidelberg (2011)

Gasparri, O.: Variable off-Time Peak Current Mode Control (VoT-PCMC) as method for average current regulation in Buck Converter Drivers, November 2019. Genova, ICECS (2019)

Salam, Z.: Power Electronics and Drives, Chapter 3, UTM-JB (2003)

**Open Access** This chapter is licensed under the terms of the Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/), which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license and indicate if changes were made.

The images or other third party material in this chapter are included in the chapter's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the chapter's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder.

