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INTEGRATED READOUT SYSTEMS FOR PARTICLE DETECTORS

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Experience is what you get
when you didn't get what you wanted.
- Randy Pausch

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Abstract

Increasing demand for high rate detectors in modern High Energy Physics experiments is generating many technological challenges. In particular, developments in particle detector technology increased requirements on electronic readout systems and fostered research on integrated readout systems. As a widely used technology, CMOS integrated circuits are a common choice for readout chip.

In this thesis some of the major challenges in detector readout are analyzed while reporting novel experimental results on an existent prototype. A new readout system, exploiting a new double threshold signal processing technique, is also presented.

The first part of this thesis presents experimental results obtained with GEMINI chip, a readout chip for Triple-GEM detectors fabricated in CMOS 180 nm. After an analysis of major challenges in Triple-GEM readout, results from chip characterization are presented. On detector tests are also reported describing methodologies developed specifically for this system. Furthermore, results from an irradiation test of GEMINI are presented, with an analysis of TID effects on Time-over-Threshold performance.

The second part of this thesis presents a new readout chip, FTfe, designed in CMOS 65 nm process. This readout system has been specifically designed for Muon Drift Chambers taking advantage of the know-how acquired during experimental work on GEMINI. After a theoretical analysis of the signal processing technique proposed, the implementation of FTfe is presented in detail. Results from transistor level simulations are eventually presented.

Introduction

Particle detectors readout development is a research branch that acquired growing importance in High Energy Physics experiments. Depending on detector operating principle outputs generated can be very different. For this reason, Application Specific Integrated Circuits (ASICs) are often developed for specific types of detectors. Architectures of readout chips are designed to exploit detector advantages and to face challenges they pose, as high rate requirements and radiation damage. Physical interfacing with detector may also be challenging for variability of electrical characteristics and interaction with high voltage systems.

In this, thesis, some of the critical aspects in detector readout are analyzed also reporting experimental results and proposing a new readout system. This document is divided in two parts: the first describes experimental results obtained during the work on GEMINI chip, a readout system for Triple-GEM detectors; some critical aspects in GEM readout will be also analyzed. The second describes the design of a new readout system, Fully Differential Fast Tracking front end, that greatly benefitted from the experience acquired from the work on GEMINI chip.

Part I

Triple-GEM detectors readout: GEMINI chip

Chapter 1

GEMINI a readout ASIC for Triple-GEM

1.1 Triple-GEM detectors

The Gas Electron Multiplier (GEM) is a particle detector based on gaseous ionization invented at CERN in 1997 [1]. Versatility and reduced cost made this technology an interesting option for many experiments and fostered research both on detector and readout electronics. Operating principle of GEM and Triple-GEM detectors will be described in the next sections where the main challenges in readout development will also be illustrated.

1.1.1 Operating principle

As reported in [1] and [2] a GEM is made of two copper layers separated by a 50 μm thin foil of kapton. The surface is perforated with holes with a diameter between 50 μm and 70 μm that act as electron multiplication channels. A high voltage difference applied on the two metallic sides creates an electric field in the order of 10^5 V/m into the holes. The whole structure shown in Figure 1.2 is mounted inside a gas chamber where electrons generated by gas ionization are drifted towards the GEM using a low electric field. Then, high field inside the holes accelerates the incoming electrons generating new electrons in the gas. This

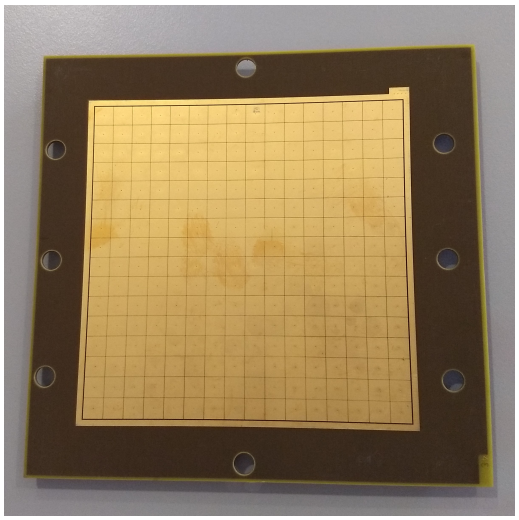


Figure 1.1: Picture of a board with Triple-GEM pads.

multiplication effect allows to obtain a gain in the order of 10^3 on the signal generated by the first ionization. Eventually, electrons moving towards anodes induce signal with a phenomenon first reported in [3] and formalized by Ramo in [4]. A picture of pads used is shown in Figure 1.1. Production of GEM foils can take advantage of techniques developed for Printed Circuit Boards (PCB). This is a great advantage in terms of cost and ease of manufacturing. Thanks to the pitch of about 100 μm between GEM holes [1], spatial resolution is good and allows a variety of applications as shown in [5]. Their structure also make them suitable for irregularly shaped detectors and for wide area detectors.

Triple-GEM

The idea of assembling multiple GEM grids to obtain large amplification was considered since the beginning and early studies of detectors with three GEM layers showed the advantages of this solution in terms of gain and ions suppression [6], [7], [8]. As reported in [9] a Triple-GEM is built using three GEM grids positioned between anode and cathode as shown in Figure 1.3. The cathode is designed considering the particular application and type of particles to be detected, while the readout layer can be implemented with microstrips or with metal pads, as reported in [10] and [11].

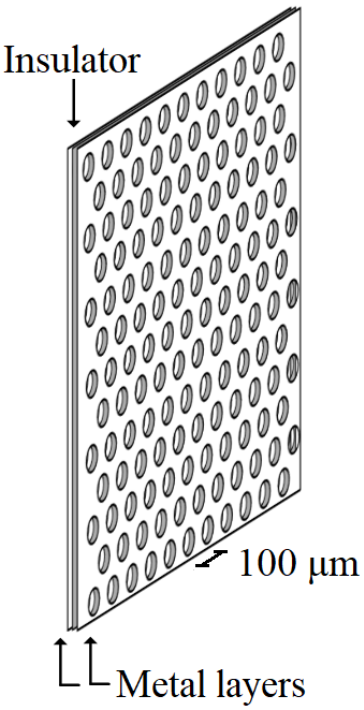


Figure 1.2: Illustration of GEM structure.

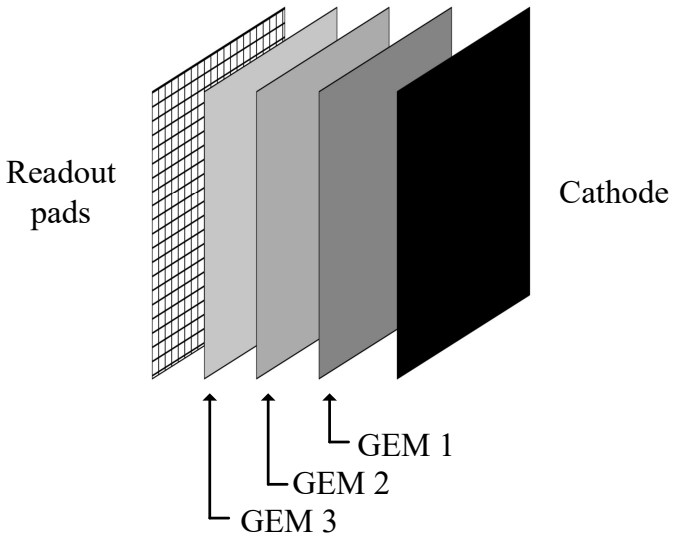


Figure 1.3: Structure of a Triple-GEM.

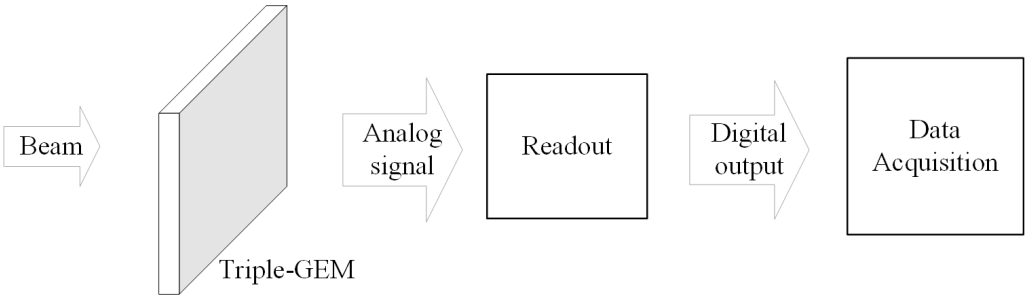


Figure 1.4: Diagram of a typical readout and data acquisition system.

1.1.2 Challenges in Triple-GEM readout

As shown in the diagram of Figure 1.4, acquisition of signals from Triple-GEM requires the processing of analog signals generated by the detector. Readout systems used for this task interface directly with detector back plane and generate digital outputs that can be elaborated and stored by a data acquisition system. The characteristics of Triple-GEM detectors creates new challenges for the readout systems. These challenges can be divided in three different categories:

- Spatial resolution, theoretically limited only by electrons diffusion and by holes geometry to the order of $10^{-4}m$, is practically limited by size and placement of anodes. When high spatial resolution is required, it is necessary to read many anodes in parallel with space effective solutions. On the other side, using big anodes means more capacitance at readout input with consequent constraints in readout channel design.

- High rate capabilities of Triple-GEM detectors obviously requires proper readout rate. Fast signal processing is needed to manage count rates that can reach $10^6 \frac{counts}{s \cdot mm^2}$. Adequate output interfaces are also required to communicate with data acquisition systems.

- The possibility of designing Triple-GEM detectors in various shapes and size to adapt to peculiar experimental conditions has a direct effect on anodes electrical characteristics. Anodes designed to cover an irregular area may have different capacitance and connections length with a relevant variation from initial specifications.

Considering a simplified case it is possible to analyze some important trade-offs in the choice of anode structure and their impact on readout performance. Considering a detector with homogeneous incident radiation, and ignoring border effect, as long as readout pads are much bigger than GEM holes the rate of events detected per channel C can be written as:

$$C = A \times R \tag{1.1}$$

where A is pad area and R is the rate of events detected per unit of area. Hence, pads area variations are directly related to the required readout rate. Consequently, for a give event rate, readout electronics maximum rate generates a constraint on maximum pad size. On the other hand, minimum pad size is limited by readout system volume and interconnections between pads and readout.

1.1.3 State of art in Triple-GEM readout

Early applications of GEM detectors used readout systems designed for other purposes chosen to fit the requirements of each experiment. An interesting example is reported in [12], where a CCD is used for GEM readout. Detectors developed for imaging applications in medical field have also been used to exploit GEM high spatial resolution, as reported in [11].

Wide area detector used modular solutions, as reported in [9]. Here, CARIOCA chip [13] is used to readout a Triple-GEM. This ASIC, originally developed LHCb muon system wire chambers, is an Amplifier-Shaper-Discriminator that integrates 8-channels with a common programmable threshold and maximum rates higher than 10^7 events per second.

Increasing use of GEM detectors created a new research branch dedicated to custom readout systems, that could exploit the advantages of this technology. An ASIC specifically designed for a GEM detector is reported in [14]. Here, the circular detector used has a maximum event rate of 30 kHz per channel, that allows to output digital data of each event frame with LVDS standard and a 50 MHz clock. Other developments reported in [15] show improved performance in

terms of readout frequency, 60 kHz, and further integration with digital systems for Time to Digital Conversion.

1.2 GEMINI chip

GEMINI chip was developed by the Microelectronics group at University of Milano - Bicocca. It was specifically designed for Triple-GEM detectors, to exploit the advantages of this technology. ASIC architecture will be illustrated in the next sections, while data obtained during various tests will be illustrated in the next chapter.

1.2.1 Chip architecture

GEMINI [16] is an integrated readout system that features 16 channels programmable with a I2C interface. As shown in Figure 1.5, the I2C interface is used to program 16 9-bit DACs used for threshold setting. An internal calibration system, controlled by the I2C interface, allows to adjust automatically C_F value for all channels with respect to CMOS process variations with a precision of 5 %.

Each channel has two inputs, referred as *in* and *Vref* in the diagram, that are respectively connected to detector output and to a voltage reference of 1 V. 16 LVDS outputs allow for fast interfacing with Data Acquisition systems, while analog signal is available for testing purposes from one pin for each channel.

1.2.2 Channel architecture

Each channel is constituted by a Charge Sensitive Preamplifier (CSP), that integrates current pulses coming from the detector and generates a voltage signal. The following Discriminator compares CSP output with the threshold programmed on channel DAC. Digital output is generated by an LVDS driver while an analog buffer allows to acquire CSP output for testing purposes.

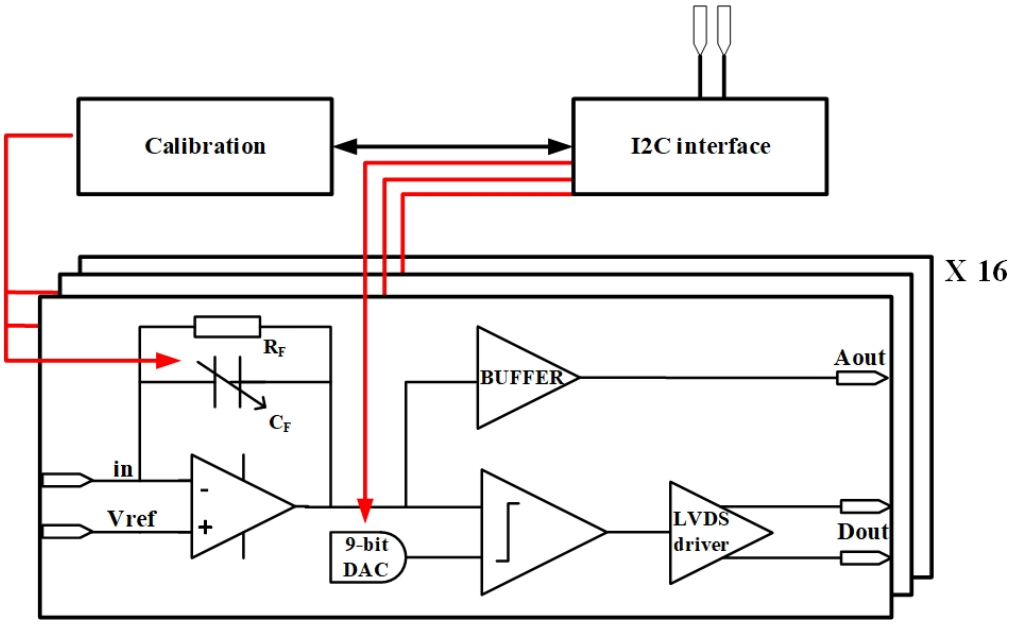


Figure 1.5: Diagram of GEMINI architecture with block diagram of internal channels.

Time-over-Threshold

Time over Threshold technique is commonly used in particle physics experiments, as reported in [17] and [18]. It is used by GEMINI to encode information on input charge in digital output. The principle of this technique consists in comparing an incoming signal with a fixed threshold and produce information on Time over Threshold. As illustrated in Figure 1.6, different input signals compared to a fixed threshold generate different ToT values. On the other hand, different threshold values can affect significantly ToT obtained from the same input, as shown in Figure 1.7.

For these reasons, it is necessary to extrapolate a calibration curve with known inputs and a fixed threshold before each measurement. During data analysis it will be necessary to use corresponding calibration curves to calculate input charge from each ToT value, knowing threshold value used.

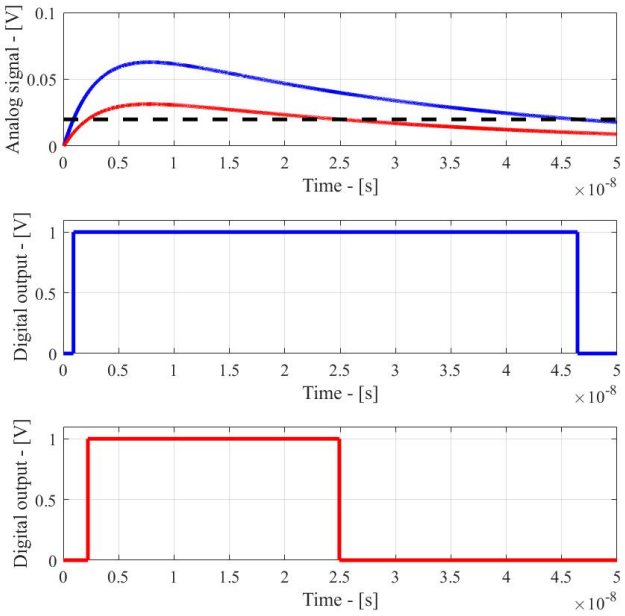


Figure 1.6: Time over Threshold variation for different inputs. Dashed black line shows the threshold compared to inputs in red and blue. Digital outputs resulting from the comparison with the threshold are shown in corresponding colors.

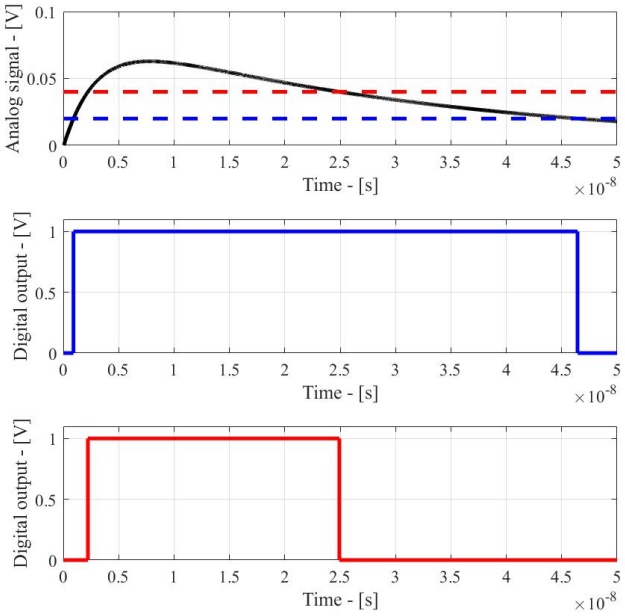


Figure 1.7: ToT variation for different thresholds. Black line shows an analog signal compared to threshold shown with dashed lines. Digital outputs resulting from the comparison with the thresholds are shown in corresponding colors.

Chapter 2

Tests on GEMINI chip

This chapter describes results obtained during testing activities with GEMINI chip. Results from test bench characterization will be presented in section 2.1. In section 2.2 various tests performed on detector are described, while in section 2.3 an analysis of the effect of ionizing radiation on GEMINI ToT performance is presented.

2.1 GEMINI characterization

Characterization of GEMINI chip on test bench is a fundamental step to understand its behaviour in the final application. This allows to analyze device performance in a controlled environment before mounting it on detector. The following sections will describe the setup used for characterization and key results obtained and published in [19].

2.1.1 Test setup

The test setup used to acquire data for GEMINI characterization is illustrated in Figure 2.1. Samples tested were mounted on a GEMINI 16D, a module designed at INFN laboratories in Frascati to mount GEMINI on detector. The name of this module, comes from the possibility of reading 16 channels in parallel, thanks to a single GEMINI chip.

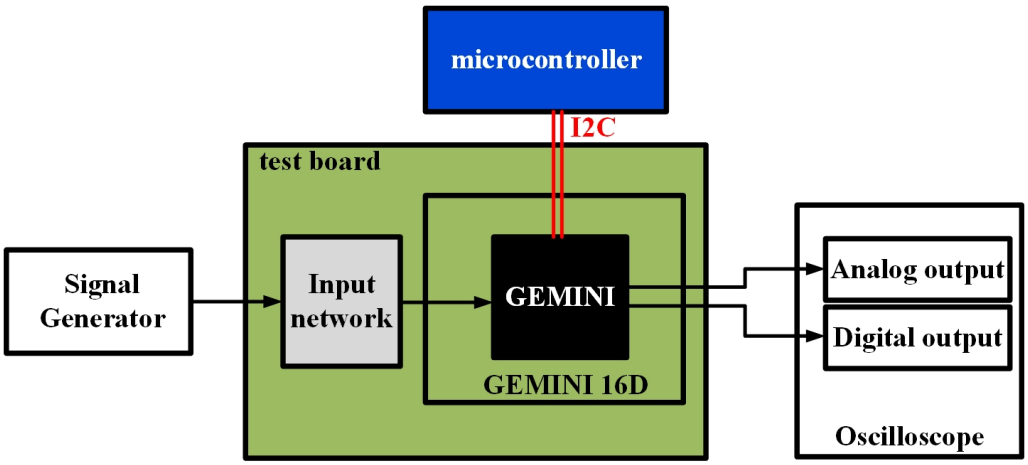


Figure 2.1: Diagram of measurement setup used for GEMINI characterization. A complete GEMINI 16D module was plugged on a test board to test the chip with references integrated in the module.

For the characterization, GEMINI 16D module was mounted on a test board, that allowed to feed controlled signals to GEMINI inputs. To emulate detector electrical characteristics and convert input voltage steps in current pulses, an ac coupled passive network was integrated on the test board. For each edge in voltage signal a current pulse was fed to GEMINI input. Amount of charge in each pulse could be controlled through the amplitude of the input voltage signal.

Analog and digital outputs of GEMINI 16D were read with a digital oscilloscope to acquire voltage waveforms that could be analyzed to verify chip response to known inputs.

2.1.2 Pulse amplitude

Charge Sensitive Preamplifier (CSP) response can be monitored thanks to the analog output buffer. In particular, it is important to verify that CSP output peak value varies linearly with input charge. Non-linearity in CSP response would result in signal distortion and loss of information.

Figure 2.2 shows a plot of peak values of analog output signal for different input charge values. A linear relation between input charge and analog output peak is clearly visible in the whole input range. A linear fit of data gives a R^2 value of 0.9999. In particular, there is not evident output saturation in the input

range specified.

2.1.3 Time over Threshold

Figure 2.3 shows Time over Threshold curves obtained with different threshold values. Each curve was obtained acquiring ToT values for multiple inputs with a fixed threshold value. Here, it is possible to observe dependency illustrated in Figure 1.7. For the same input values a higher threshold value gives lower ToT values, while worsening the error propagation from ToT value to input charge. This can be visualized from the reduced slope of the characteristic curve.

In order to use GEMINI for ToT measurements with Triple-GEM it will be necessary to extrapolate a calibration curve that takes into account both detector response and chip response, as shown in section 2.2.3.

2.2 On detector measurements

This section illustrates results obtained during experimental activities on Triple-GEM detectors equipped with GEMINI readout. The aim of these activities is to evaluate chip performance on detector after characterization on test bench.

2.2.1 Test with induced signal

This test was necessary to evaluate if GEMINI could meet the maximum count rate requirement of 5 Mcps when connected to detector pads. A particular experimental setup was used to induce a known signal on detector pads. Thanks to the small distance between the last GEM grid and detector pads (few millimeters), it was possible to induce signal on readout pads injecting voltage signals on GEM contacts. Indeed, each falling edge of a voltage signal induces a current with the same polarity of a real signal on readout pads. Thanks to the AC coupling between input signal and readout it was possible to use a voltage signal with ladder shape to induce a series of pulses of the same polarity.

Monitoring GEMINI analog output allowed to evaluate channel response to high rate signals. In Figure 2.4 a plot of a signal acquired from GEMINI

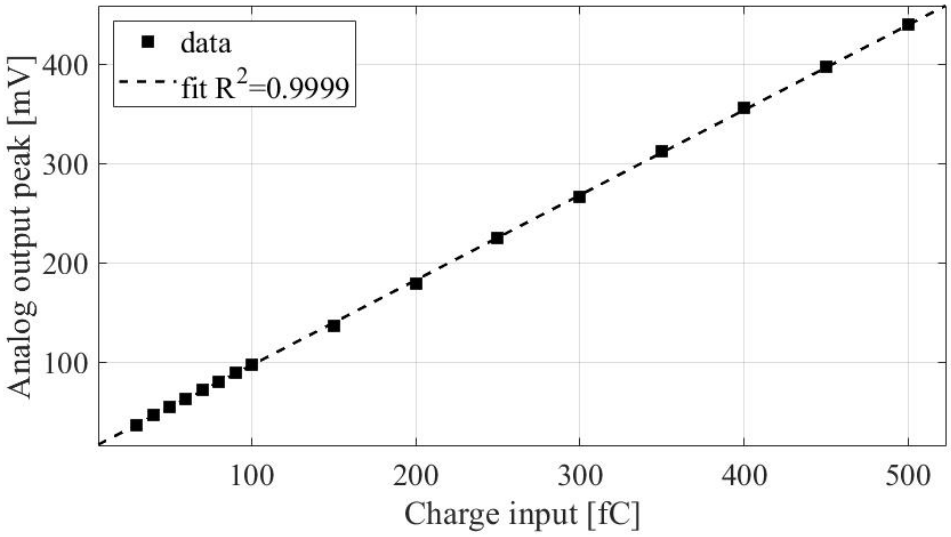


Figure 2.2: Analog output peak amplitude variation vs input charge variation measured on test bench.

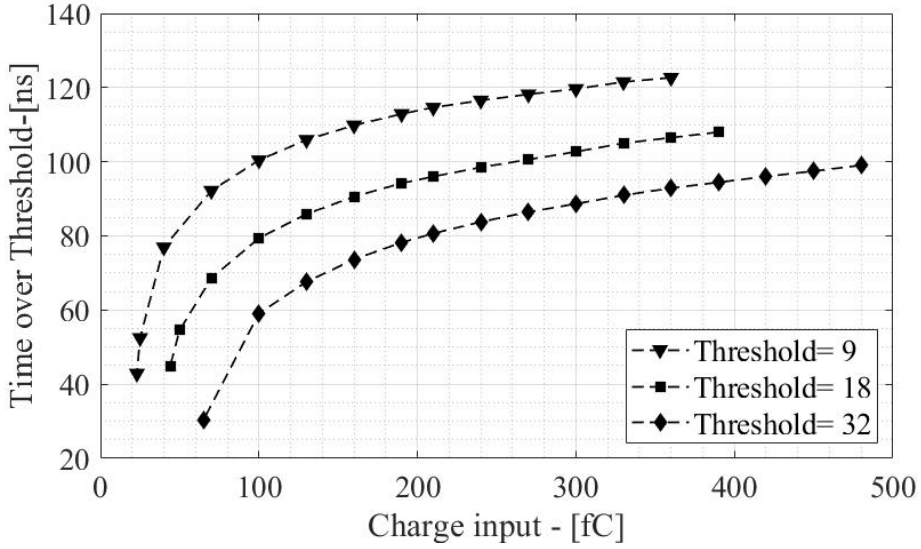


Figure 2.3: ToT curves obtained with three different threshold values on test bench.

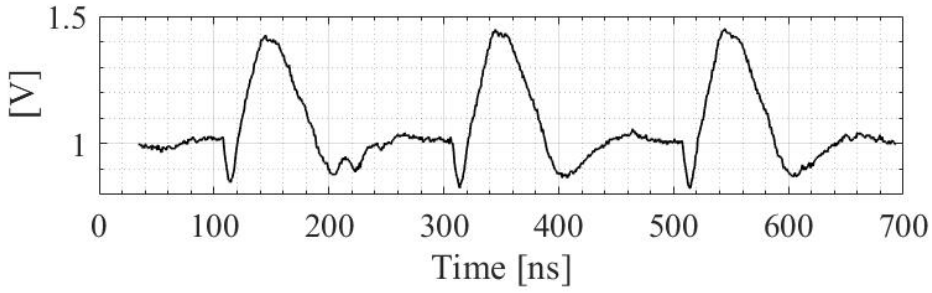


Figure 2.4: Voltage signal acquired from GEMINI analog output connected to Triple-GEM for maximum rate testing.

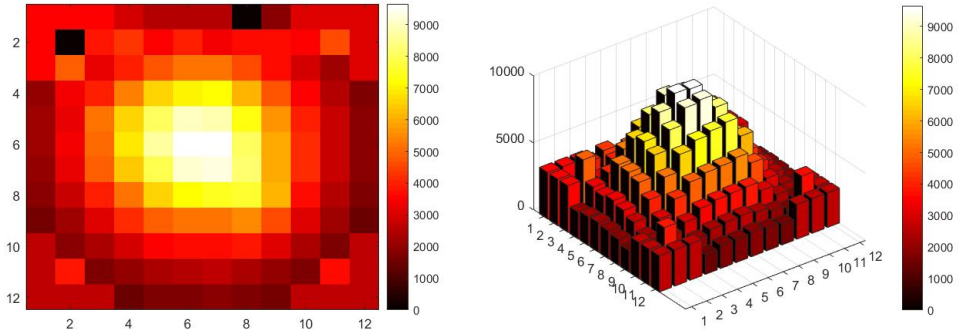
analog output is shown. The plot shows that readout time for a peak of nearly maximum amplitude (maximum output swing is 500 mV) is short enough to guarantee complete baseline restoration in about 180 ns. Indeed, pulse height and duration of the second and third pulse are consistent with the first one. This result demonstrated the capability of meeting rate requirements of 5 Mcps in a real setup.

2.2.2 Test with Fe55 source

This test deals with the counting performance of GEMINI. The aim of was to verify the correct operation of the ASIC channels with real input signals. For this test a small Triple-GEM detector was used. Eight GEMINI chips were used for readout, for a total of 128 channels. The structure of readout pads covering detector back plane was characterized by a central matrix of square pads of 8 mm x 8 mm, with four corner pads three times bigger than central pads. Programming of GEMINI and acquisition of digital outputs was done using a custom board with on-board FPGA developed by Nuclear Instruments. The detector, filled with a gas mixture of Ar and CO_2, was exposed to X radiation emitted by a Fe55 sample with an activity of 370 kBq.

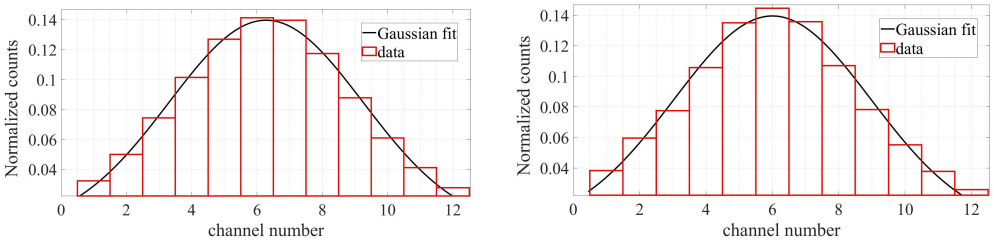
Figure 2.5a shows a map of events counted by each channel during data acquisition. Emitting source position is clearly visible, confirming the correct operation of GEMINI chips in event counting for imaging application. Bigger pads in the corners show higher counts due to the bigger area and for geometrical

effects at detector corners. Bar plot shown in Figure 2.5b helps to visualize counts distribution over detector channels. Here it is possible to observe a ratio of about 5 times between counts in central region and in border regions. As shown in Figure 2.6a and Figure 2.6b histograms of channels crossing detector center can be fitted with a gaussian distribution. This confirms the absence of artifacts in source imaging and gives positive indications on readout performance.



(a) **(b)**

Figure 2.5: (2.5a) Map of a Fe55 source obtained using the setup described. (2.5b) Bar plot of counts acquired from a Fe55 source using the setup described.



(a) **(b)**

Figure 2.6: Histograms of counts in horizontal (2.6a) and vertical (2.6b) sections crossing detector center.

2.2.3 Tests with other sources

Further tests were carried using a new setup with a Time to Digital Converter, to digitalize ToT information. This allowed to match information on counts with information on input charge for each event detected. In this situation it

was possible to analyze charge distribution over the input range values and use GEMINI programmable thresholds to ignore low energy events.

To apply this method to physics experiment it is necessary to define a correspondence between ToT values and input charge. ToT values calculated by GEMINI are not only related to chip response, but also related to detector response and readout pads physical configuration. For this reason, calibration curves are extracted from each experimental setup using a known source. Figure 2.7 shows two calibration curves extracted for two different threshold values.

Figure 2.8 shows data obtained observing the emission of a Mo target irradiated with X-rays. The input charge displayed on the horizontal axis is calculated for ToT value using the calibration curves of Figure 2.7. Vertical axis represents counts per second for each bin, bin width was defined by ToT resolution (2 ns). The plot shows two series of data, in black data acquired with a low threshold (100) and in red data acquired with a higher threshold (350). Data are not normalized to highlight reduction of counting rate with threshold increase. Indeed, event filtering at readout stage can reduce drastically requirements on data rate at acquisition level. From Figure 2.8 it is possible to observe from the red series that higher threshold used allowed to reduce background around 100 fC. Thanks to this, it is possible to identify a peak in Mo emission around 120 fC, while ignoring emission peaks at lower charge given by the activation of materials used in the experimental setup.

2.3 Radiation Hardness

2.3.1 Motivation

The integration of GEMINI chips in Triple-GEM detectors modules is a key factor to exploit this technology. However, a strong integration with the detector means also an exposure to incident radiation. Performance degradation of semiconductor devices due to radiation damage is a well known problem and multiple studies on this subject showed the effects on integrated circuits performance [20], [21], [22]. Radiation damage can be divided in the following

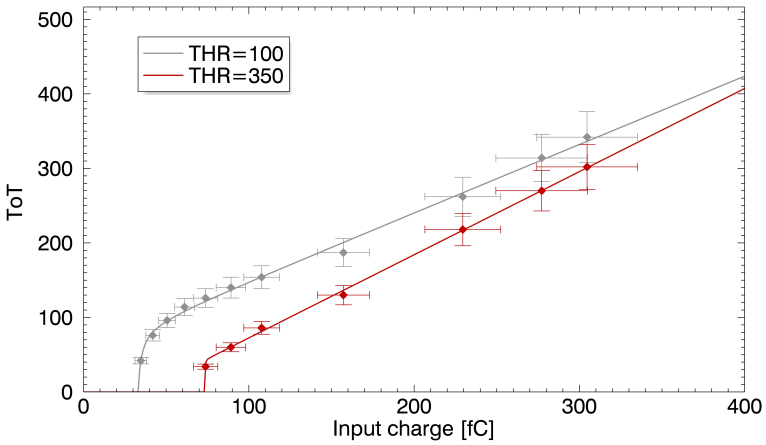


Figure 2.7: Calibration curves extracted from a setup with a Triple-GEM and GEMINI chips.

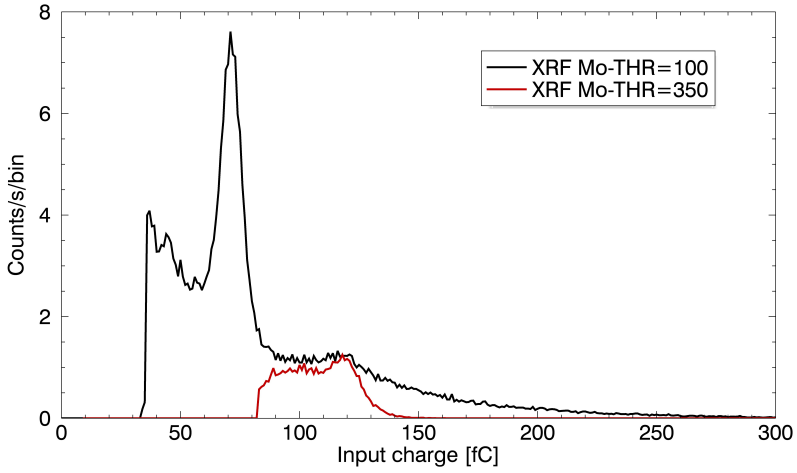


Figure 2.8: Emission spectrum of a Mo target irradiated with X-rays. Black line represents data obtained with threshold 100 set on GEMINI, while red line represents data obtained using threshold 350.

categories:

- **Single Event Effects (SEE)**: Effects generated by a local interaction of incident radiation with the silicon substrate. Some of the effects are glitches, alteration of digital registers content or activation of parasitic devices that draw destructive substrate currents. Single Event Effects are analyzed observing error and failure rate of devices while irradiated.

- **Total Dose Effects**: Cumulative damage due to interaction with ionizing radiation. One of the most relevant effects is charge trapping in gate oxide, that determines variations of threshold voltage. Total dose effects are often analyzed using the Total Ionizing Dose (TID), the total dose of ionizing radiation received by the device under test.

In this test effects of 20 Mrad TID on GEMINI Time over Threshold performance will be analyzed, in order to evaluate long term effects during chip operation in harsh environment.

2.3.2 Methodology

To assess the radiation hardness of an integrated circuit it is necessary to compare its performance before and after being irradiated. However, the evaluation of performance degradation strictly depends on the particular application. For this reason, a custom testing procedure was designed for GEMINI. This procedure aims at verify the overall performance of GEMINI channel collecting Time-over-Threshold (ToT) outputs generated from a known input. Comparison of distributions of ToT values obtained from the same input for different values of TID allows to understand the effect of radiation damage on system performance and evaluate potential corruption of output data. The key aspects of the procedure can be summarized in the following points:

- **Constant X-ray flux**: The device is irradiated with an X-ray beam of constant intensity, previously characterized, centered on chip die. Chip performance can be measured multiple times during irradiation to obtain

measurements at different TID values. Every TID value reported is referred to dose on the whole chip die.

- **Controlled Input**: Input signal is generated from memorized presets that allow to reproduce the same inputs at various TID values.
- **Acquisition of ToT values**: ToT values generated by GEMINI are digitilized and collected to obtain histograms of ToT values distributions.

2.3.3 Experimental Setup

The experimental setup employed for this test used many parts of the custom Data Acquisition system designed for the integration of GEMINI chip. Figure 2.9 shows a block diagram of the whole setup. A signal generator controlled via a USB interface and a passive network are used to generate signals that mimic those generated by a Triple-GEM detector. GEMINI chips under test are mounted on a 64D board, capable of hosting 4 chips for a total of 64 channels. The X-ray source used had a beam centered on one chip die and allowed a dose rate of about 3 Mrad/h.

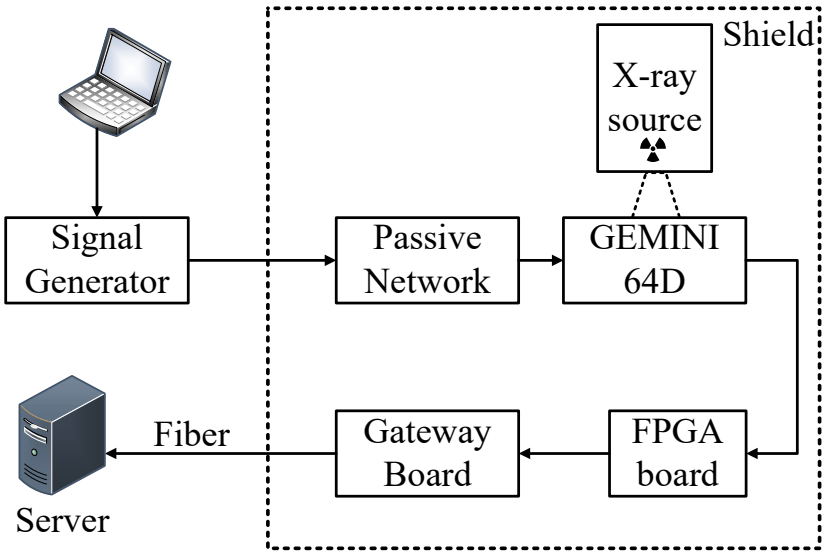


Figure 2.9: Block diagram of the experimental setup used for irradiation tests.

2.3.4 Data Analysis

Figure 2.10 shows three plots of ToT histograms obtained from three different inputs. Each plot compares the distribution obtained before irradiation (0 rad), with the one obtained after irradiation up to 20 Mrad TID. The three input presets were selected to generate different ToT distributions that could give insight on the behaviour of GEMINI with structured energy spectra. In particular, Figure 2.10a, shows an histogram obtained with preset named *Preset 1*, which generates a single peak at 130 ns. A qualitative comparison of the histograms in Figure 2.10a obtained before irradiation (blue line) and after (orange line) shows that deviation of average value is comparable with peak width. In Figure 2.11a average ToT at different TID is shown with error bars defined by peak standard deviation. Here, it is possible to see a gradual increase of ToT average value with TID. However, difference between ToT average at 0 rad (dashed line) and at 20 Mrad is less than the standard deviation.

ToT distributions comparison

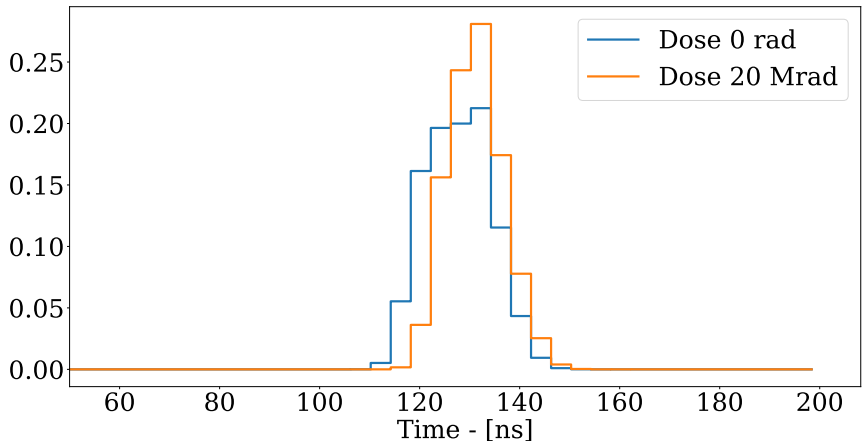
ToT distributions before and after irradiation can be tested with a paired t-test to assess if the variation is statistically significant. In this analysis normalized values of ToT values occurence will be compared. This test allows to understand if two samples have been extracted by two populations with different mean value. The procedure is divided in five steps:

1. calculate the difference between each pair of two observations. In this case the difference d_i will be calculated for each ToT value subtracting relative frequence before irradiation x_i to relative frequency after irradiation y_i.

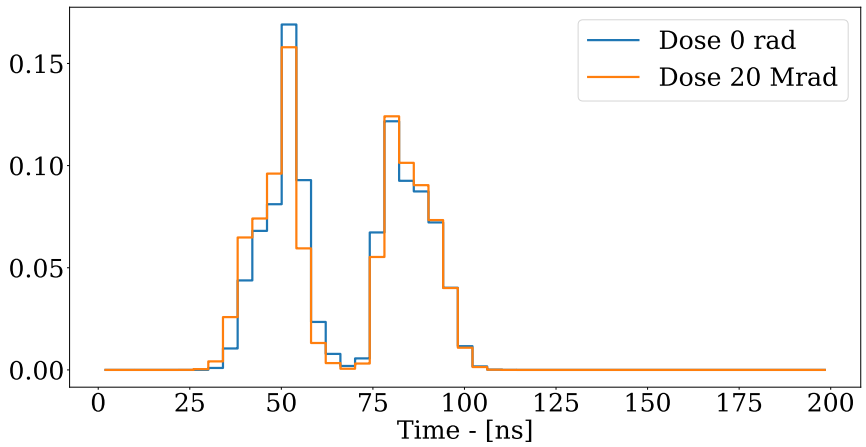
2. calculate the mean difference computing $\overline{d}$.

3. calculate the standard deviation of the mean difference $S_{\overline{d}} = \frac{s_d}{\sqrt{n}}$ where s_d is the standard deviation of differences and n the number of pairs.

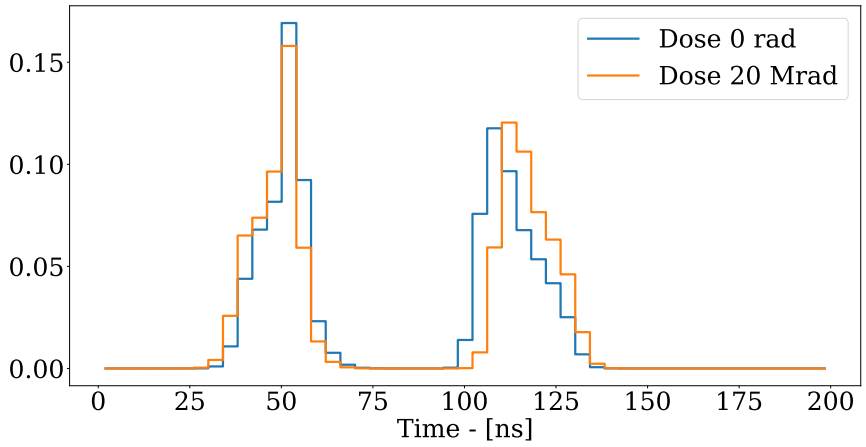
4. calculate the t statistic $t = \frac{\overline{d}}{S_{\overline{d}}}$



(a) Preset1

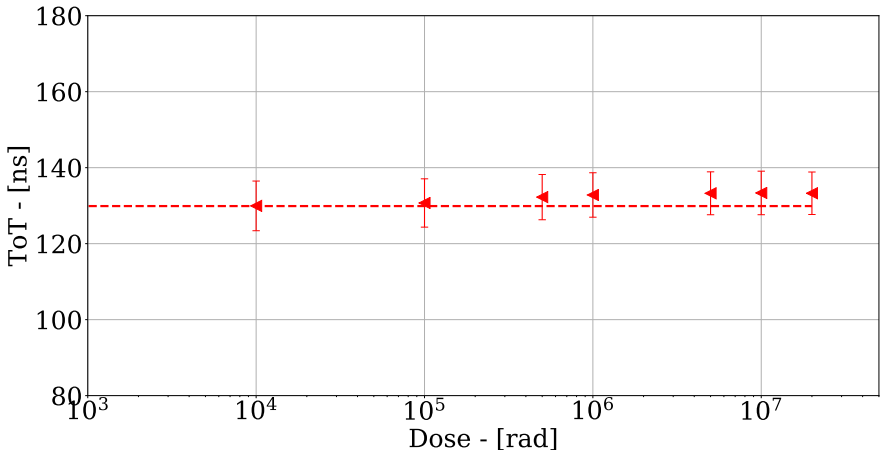


(b) Preset2

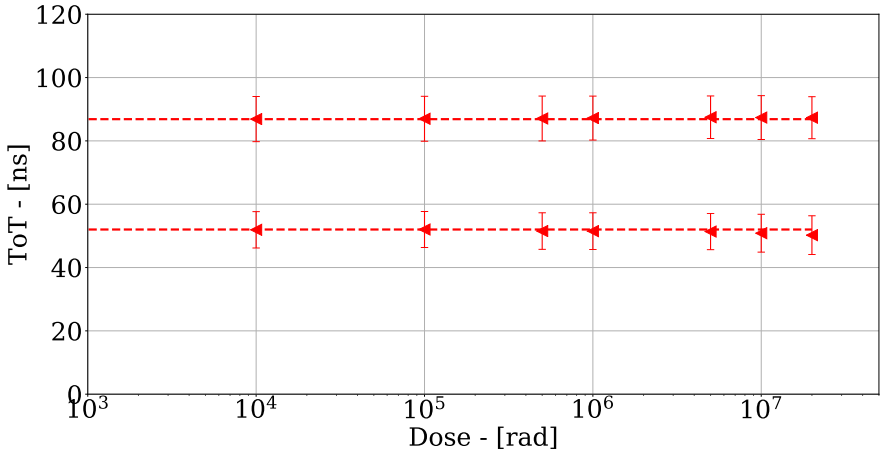


(c) Preset3

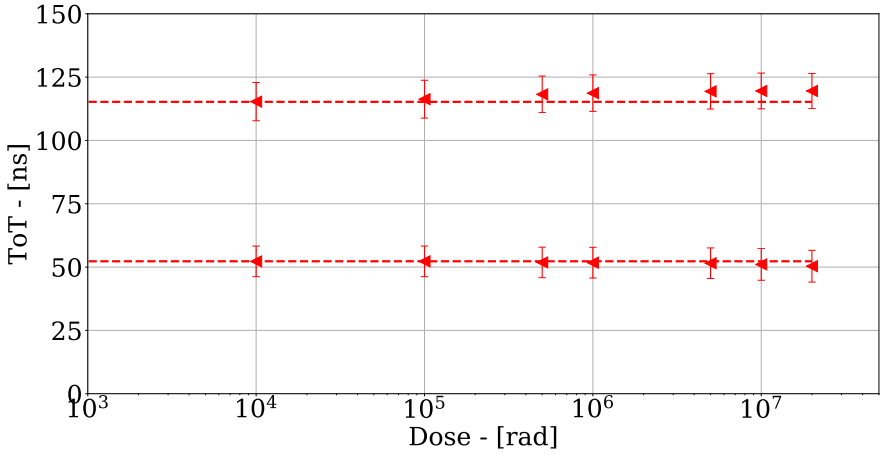
Figure 2.10: ToT Histograms.



(a) Preset1



(b) Preset2



(c) Preset3

Figure 2.11: ToT variation vs Dose.

Input	t-score	p-value
Preset 1	2.0445e-16	0.9999
Preset 2-1	1.1368e-15	0.9999
Preset 2-2	8.1861e-16	0.9999
Preset 3-1	2.6581e-16	0.9999
Preset 3-2	-3.3514e-16	0.9999

Table 2.1: Outputs of the paired t-test executed to compare ToT distribution before irradiation and after irradiation for each input.

5. compare t value to the t-distribution with $n-1$ degrees of freedom. To reject the null hypothesis of the two samples coming from the same population a significant difference from such distribution is needed.

Table 2.1 shows the outputs obtained from this analysis performed using scipy implementation of paired t-test [23]. Peaks detected with Preset 2 and Preset 3 were analyzed separately to operate on distributions that could be approximated to the normal distribution. Very low t-scores with high p-values obtained indicate that the hypothesis of the two samples being extracted from the same population can't be rejected. Hence, there is not a statistical basis to state that ToT distribution after irradiation is different than before.

Part II

MDT detectors readout: FTfe chip

Chapter 3

An analog signal processing technique for MDT detectors readout

3.1 Monitored Drift Tubes readout in ATLAS

The Monitored Drift Tubes (MDT) [24] are detectors employed in the Muon Spectrometer of ATLAS experiment for momentum measurements. The MDT chambers are arranged in three cylindrical layers along the trajectory of the track, allowing to determine particle momentum from track's curvature in magnetic

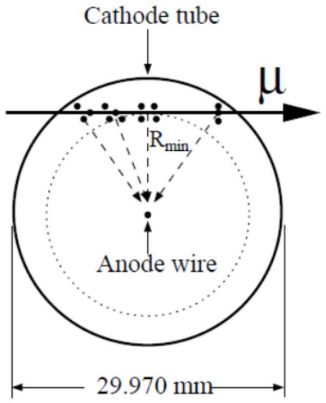


Figure 3.1: Illustration of MDT section.

field inside ATLAS. Each element is made of a 30 mm diameter aluminium tube pressured with a gas mixture of Ar/CO2 at 3 bar. Traversing charged particles create electrons in the tube due to Argon ionisation. Electrons drift towards a gold-plate tungsten-rhenium anode wire with 50 um diameter, kept at a potential of 3080 V. Moving charge multiplied by avalanche effect induces a current on the anode wire, which is detected by the front-end electronics. This, measures arrival time and ionisation charge of the hit. The overall signal generated by a charged particle hit is the sum of the currents induced by all ions and electrons generated. Signal generation is illustrated in Figure 3.1, in a cross section view of a tube. Drift radius of each signal generated can be calculated from drift time measurement but the exact relation between radius and drift time (r-t relation) depends also on temperature, pressure, magnetic field and total hit rate in the tube. Hence, these parameters are monitored with high precision during operation and used for calibration.

The main task of the readout electronics is to detect arrival time and charge for every hit, facing with the expected high hit rate due to LHC bunch crossing frequency of 40 MHz. Only the first current pulse generated, given by ion clusters near the anode, is used for track coordinates computation. However, following pulses generated by ionizations further from the anode, will generate a sequence of pulses. To avoid multiple threshold crossings and reduce volume of output data, a programmable dead-time is used in current MDT readout system, the ASD chip [25].

3.2 FTfe analog signal processing

The signal processing technique here analyzed is based on developments of concepts described in [26]. This section analyzes the signal processing technique while its implementation in a fully differential Fast Tracking front end will be described in the next chapter

Fast Tracking front-end analog signal processing is based on extraction of input charge information from signal slope. Signal generated integrating one input

current pulse is compared with two thresholds. As shown in the following, time interval between the two threshold crossings ($Time_{DIFF}$) encodes information on signal slope and, consequently, on input charge. Performing signal processing on the first signal edge allows to ignore following spourius signals and reset the whole readout channel to reduce baseline restoration time. This technique has the advantages of:

- being insensitive to signal baseline variations, as long as the baseline is lower than thresholds. This advantage comes from the use of only slope information.
- extracting information on the first event ignoring sequent events. This results in strong pile-up rejection capabilities.

However, there are some challenges in the use of this technique:

- resolution on input charge depends on resolution in Time to Digital Conversion (TDC). Hence, frontend design will have a constraint coming from TDC resolution.
- relationship between input charge and output time $Time_{DIFF}(Q_{in})$ is not linear and depends on readout characteristics.

3.3 Extracting information from signal slope

Dependency of $Time_{DIFF}$ from input charge is a key point for the application of this technique. A possible approach is to compute the impulse response function of the circuit $f_{circuit}(t)$ and find values of t such that:

$$f_{circuit}(t) = THR \tag{3.1}$$

This procedure is possible with a numerical approach but it is not always possible to find an analytic expression of $f^{-1}_{circuit}$. For this reason, an approximate relation can be interesting. Furthermore, a simple expression can be used efficiently for online data processing and processing of big datasets.

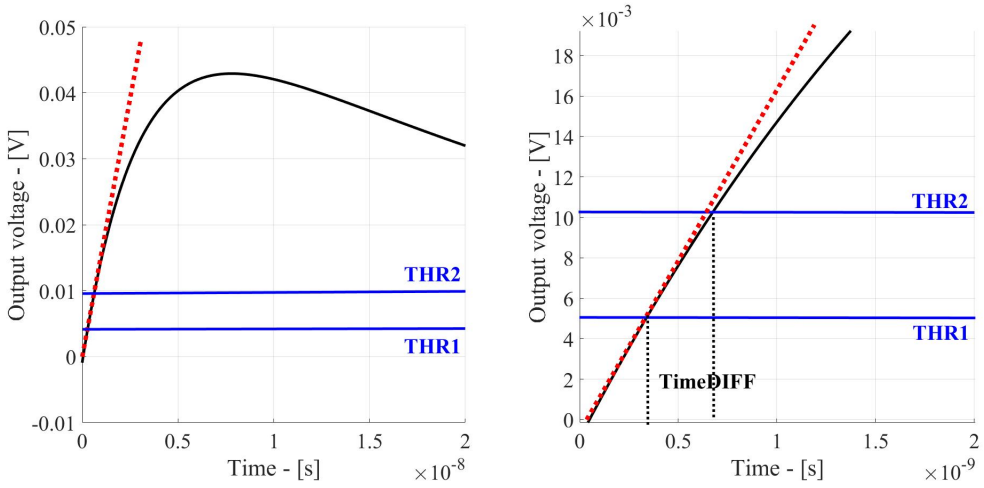


Figure 3.2: (a) Illustration of linear approximation adopted. Black solid line, signal processed; Red dashed line, linear approximation; Blue solid lines, thresholds. (b) Detail of linearization shown in (a).

A fundamental assumption in the following steps is that THR_2 and THR_1 are always small compared to response function variations, as illustrated in Figure 3.2a. In this situation, we consider a linearization of input signal expressed as:

$$y = A(Q_{in}) \cdot t + B \tag{3.2}$$

where dependency from Q_{in} comes from circuit transfer function. Threshold crossing time t_i can then be calculated from equation 3.2

$$t_i = \frac{(THR_i - B)}{A(Q_{in})} \tag{3.3}$$

and time difference can be written as:

$$Time_{DIFF}(Q_{in}) = t_2 - t_1 = \frac{(THR_2 - THR_1)}{A(Q_{in})} \tag{3.4}$$

To write an approximate dependency of A from Q_{in} some assumptions on circuit topology are needed. In the following section, a topology commonly used for current pulses readout will be presented. In this context $Time_{DIFF}(Q_{in})$ will be

calculated.

Charge Sensitive Preamplifier

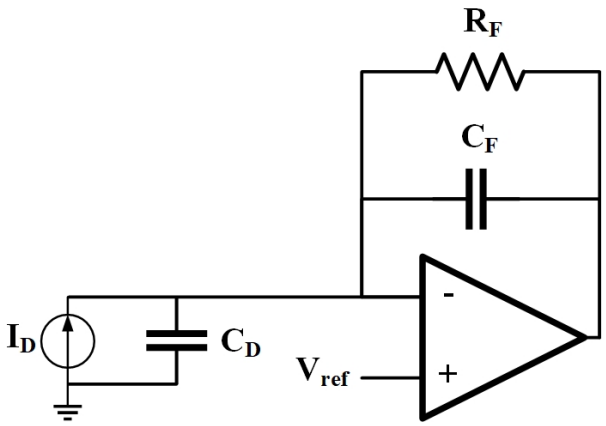


Figure 3.3: Scheme of a Charge Sensitive Preamplifier.

The Charge Sensitive Preamplifier (CSP) is a topology widely used in detector readout. As shown in Figure it exploits a closed loop amplifier with a feedback capacitor C_F and a feedback resistor R_F. The detector is modeled in this scheme as a current generator with capacitance C_D. The transfer function of an ideal CSP with infinite open loop gain can be written as:

$$\frac{V_{out}}{I_D} = -\frac{R_F}{(1 + s\,C_F\,R_F)} \tag{3.5}$$

Its response to an ideal pulse, that approximates response to detector output, can be written as:

$$V_{out}(t) \approx -\frac{Q_{in}}{C_F}\, e^{-\frac{t}{C_F R_F}} \tag{3.6}$$

Considering finite amplifier gain and detector capacitance the transfer function depends on many circuital parameters. As reported in [27], where amplifier gain is expressed as $g_m\,R_L >> 1$ and $R_F \approx R_L$, transfer function can be approximated with:

$$T_{CSP}(s) = -\frac{R_F\ (s\,\tau_z - 1)}{(s\,\tau_0 + 1)\ (s\,\tau_1 + 1)} \tag{3.7}$$

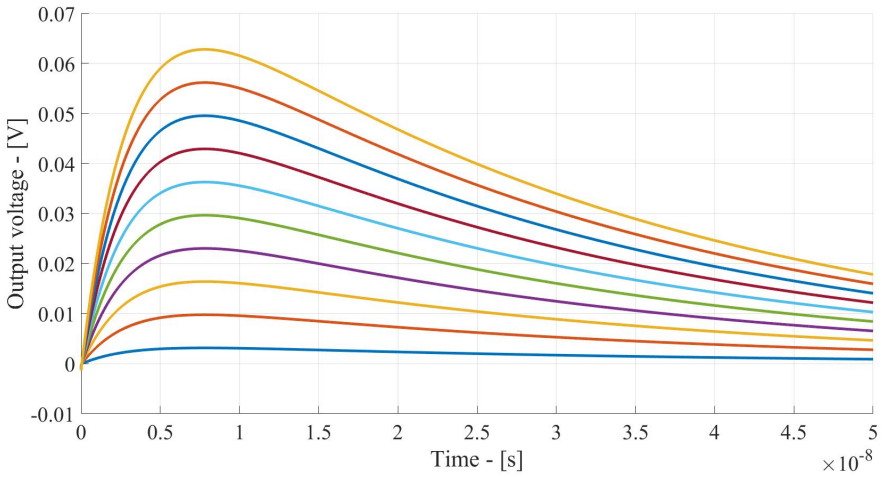


Figure 3.4: Waveforms calculated from CSP transfer function for various input charge Q_{in}

where:

$$\tau_z = \frac{C_F}{g_m} \tag{3.8}$$

$$\tau_0 = \frac{C_D}{g_m} \tag{3.9}$$

$$\tau_1 = C_F\, R_F \left(1 + 2\,\frac{C_D}{C_F\, g_m\, R_L}\right) \tag{3.10}$$

Impulse response calculated from equation 3.7 is shown in Figure 3.4 for multiple inputs. Peak value can be written as:

$$V_{peak} = \frac{Q_{in}\, R_F}{\tau_0 + \tau_1} \tag{3.11}$$

an peaking time can be written as:

$$t_P = \frac{\tau_0\, \tau_1}{\tau_1 - \tau_0} log\left(\frac{\tau_1}{\tau_0}\right) \tag{3.12}$$

Calculation of $Time_{DIFF}$

As expected from stability theory, equation 3.12 shows that peaking timedepends only on circuit time constants. Considering also equation 3.11, an expression for $A(Q_{in})$ can be written approximating CSP output to a triangular signal, with

peak value V_{peak} and peaking time independent from input charge Q_{in}.

In this approximation, signal slope must be inversely proportional to Q_{in} for constraints coming from equation 3.12 and equation 3.11. $A(Q_{in})$ can then be written as:

$$A(Q_{in}) = \frac{1}{a \cdot Q_{in}} \tag{3.13}$$

This simple relation can be easily applied to more complex systems just changing the value of a. The error in this approximation will depend on the specific transfer function. Using equation 3.13 and equation 3.4 the following relation can be written:

$$Time_{DIFF}(Q_{in}) = \frac{(THR_2 - THR_1)}{a \cdot Q_{in}} \tag{3.14}$$

- The linear approximation brings to bigger errors for small input values. This can be explained considering that signal amplitude is proportional to Q_{in} while threshold values are fixed. For this reason, very small input values may invalidate the assumption of thresholds much smaller than signal amplitude.

- Fixing resolution on $Time_{DIFF}$, resolution on Q_{in} calculated from equation 3.14 varies over the input range.

Figure 3.5 shows in black squares $Time_{DIFF}$ data obtained comparing waveforms shown in Figure 3.4 with two thresholds at 1 mV and 2 mV. These values are computed using the exact circuit response function. The solid red line shows the fit of equation 3.14 with free parameter a. Some interesting aspects of this technique can be observed from this plot Application of this methodology to a more complex system allows to evaluate its effectiveness. Figure 3.8 shows response curve of a system composed by a CSP followed by a single pole shaping stage as shown in Figure 3.6. Its transfer function can be written as:

$$T_{CSP\,SH}(s) = -R_F \frac{(1 - s\,\tau_z)}{(s\,\tau_0 + 1)\,(s\,\tau_1 + 1)} \frac{-G_{SH}}{(s\,\tau_{SH} + 1)} \tag{3.15}$$

where G_{SH} is the DC gain of single pole shaper and with:

$$\tau_z < \tau_0 < \tau_1 < \tau_{SH} \tag{3.16}$$

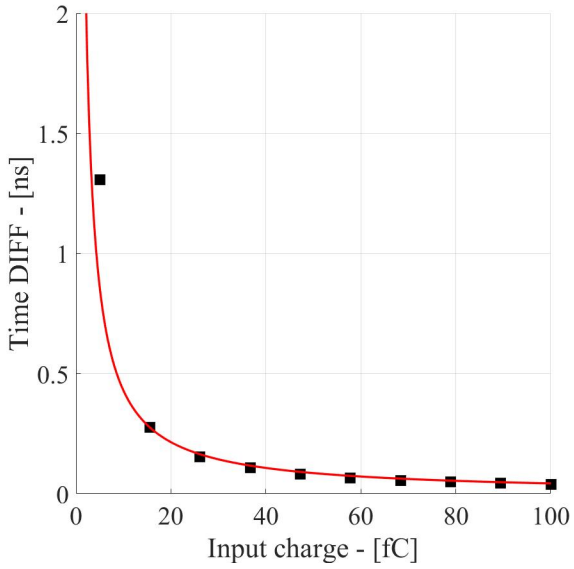


Figure 3.5: Time DIFF values obtained from waveforms of Figure 3.4 using thresholds at 1 mV and 2 mV are shown with black squares. Fit with function shown in equation 3.14 is shown in red.

Fitting of output $Time_{DIFF}$ with expression 3.14 is shown in Figure 3.8. The good approximation of the curve confirms the approximations made.

3.4 Strategies for threshold setting

From the analysis presented in the previous sections it is possible to synthesize a strategy for threshold setting based on the following observations:

- Value of $\delta THR = THR_2 - THR_1$ must be optimized with respect to the range of $Time_{DIFF}$ values required for Time to Digital Conversion (TDC).

  Minimum $Time_{DIFF}$ will be obtained with maximum input

  Maximum $Time_{DIFF}$ will be obtained with minimum input.

- Signal amplitude for minimum input is the main constraint an threshold value.

A possible strategy to identify a convenient threshold configuration for a given system, can then be described in the following steps:

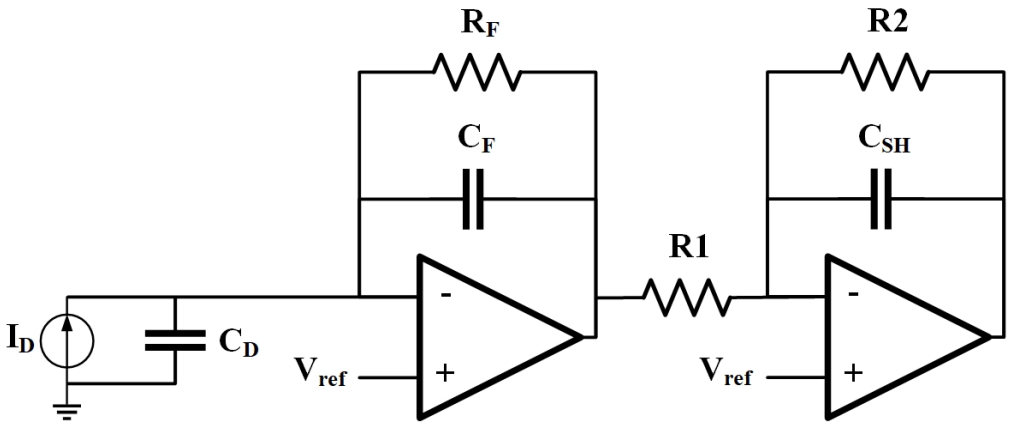


Figure 3.6: Schematic of a readout system composed by a CSP and a single pole Shaper.

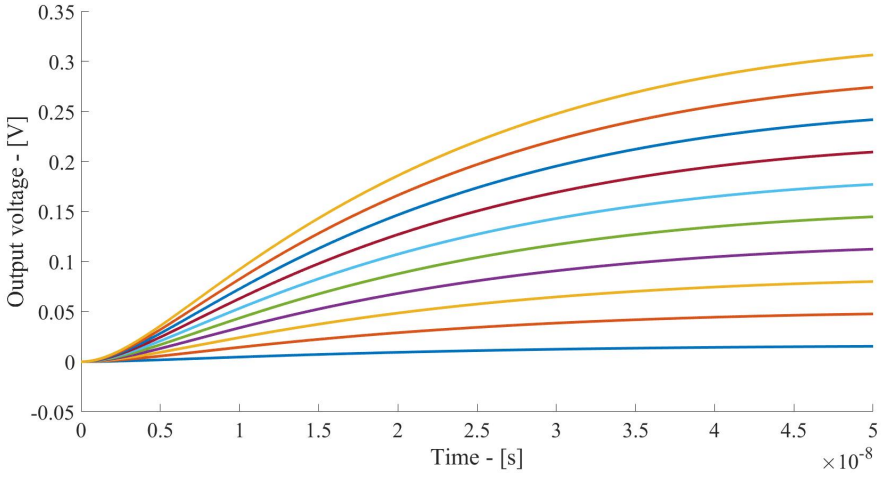


Figure 3.7: Waveforms calculated from transfer function of a CSP with a single pole shaping stage for various input charge Q_{in}

1. test with maximum input and set thresholds to obtain a $Time_{DIFF}$ that meets TDC specifications.

2. check for minimum input detection for thresholds set.

3. if minimum input is not detected it is necessary to repeat the procedure with lower thresholds.

Additionally, it is possible to extend the usable range of thresholds adding some digital logic. In principle, if a signal reach the first threshold but not the second, an infinite $Time_{DIFF}$ would be created. Adding a counter to the system it is

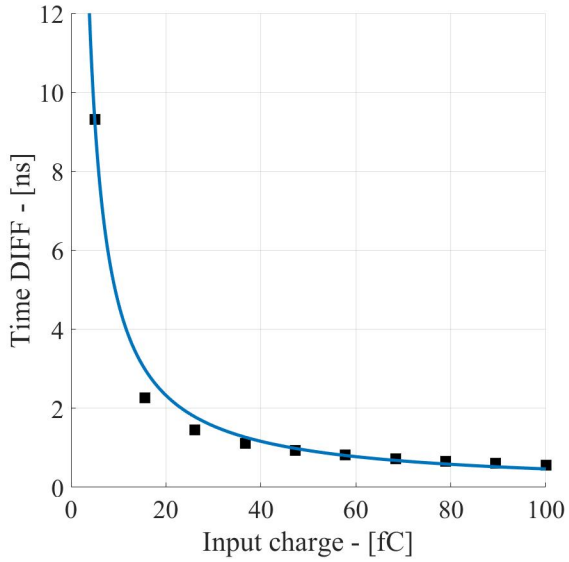


Figure 3.8: Time DIFF values obtained from waveforms of Figure 3.7. Fit with function shown in equation 3.14 is shown in blue.

possible to limit $Time_{DIFF}$ duration, and generate a known value when an output is too long, assuming that only the first threshold is reached. In this way, signals smaller than THR_2 will be detected as a value at the beginning of the scale, while loosing the requirements on THR_2. Information on implementation of this solution and many other aspects of FTfe prototype will be described in the next chapter.

Chapter 4

FTfe Design

The Fully differential Fast Tracking front end (FTfe) here presented is a readout system designed to develop the concept first reported in [26]. In the following sections, structure of the readout channel designed will be described, motivating design choices and explaining circuit operation.

4.1 Channel architecture

A simplified schematic of FTfe channel is shown in Figure 4.1. The analog signal processing is performed by a fully differential structure constituted by a CSP and a single pole shaping stage. Analog signal produced is fed to two comparators coupled in ac, and compared to differential thresholds generated by on-board DACs. Digital signals produced are elaborated by an asynchronous logic unit. In order to reduce substrate noise, the whole system uses only asynchronous logic that does not require an internal clock. For channel simmetry a dummy capacitor, matching detector Capacitance C_D, is connected to positive input.

Every time an event has been read the logic unit starts the reset phase, that reset every component of signal processing chain. In the following sections, the implementation of each block will be described and its reset method will be shown.

Requirements of input range from 5 fC to 100 fC, input impedance of 120 Ω and detector capacitance up to 60 pF were cosidered in the design.

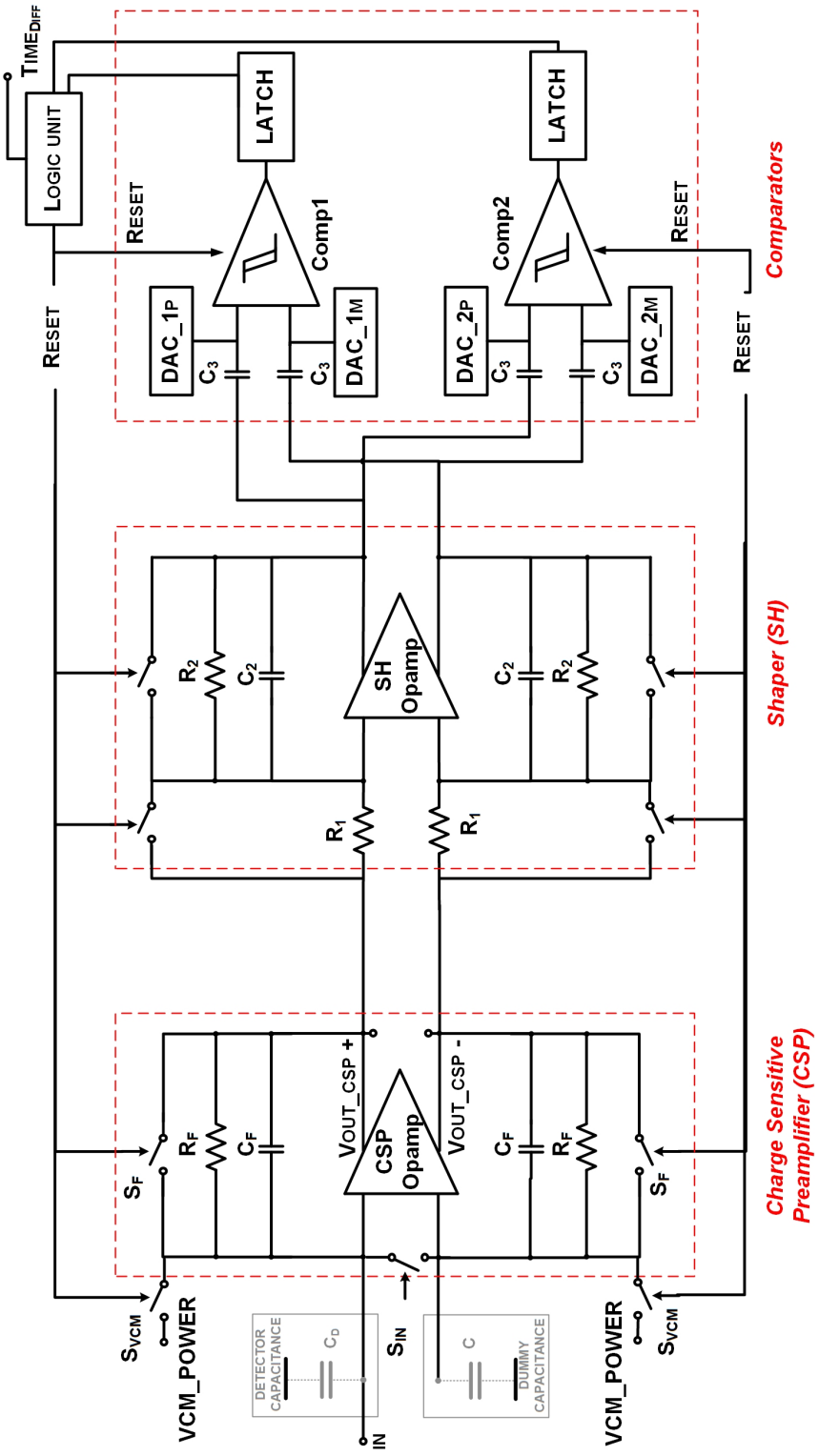


Figure 4.1: FTfe simplified schematic.

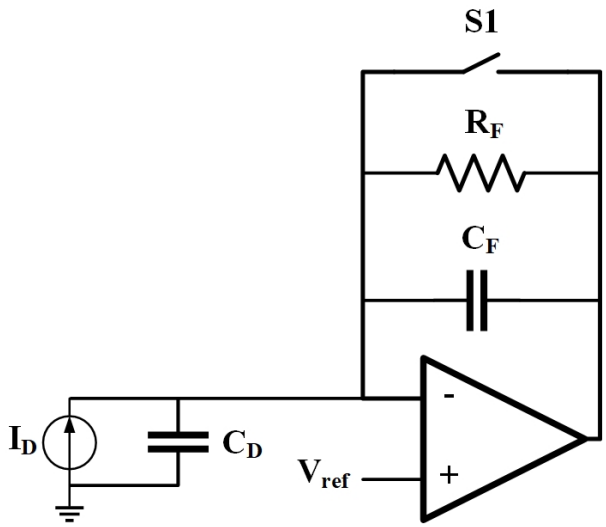


Figure 4.2: Scheme of CSP

4.2 Charge Sensitive Preamplifier

Fully differential CSP implementation shown in Figure 4.1 reads from negative input the single ended current signal generated by the detector and produces a differential voltage signal at its output. Low frequency gain is 87 dB and C_F capacitor has been implemented with a 5-bit programmable array to allow CSP calibration for process variations compensation and frequency response optimization due to C_D variations. Its operation can be analysed more easily starting from the single ended implementation depicted in Figure 4.2. When switch S1 is open, the stage operates as shown in the previous chapter. When S1 il closed, the amplifier is in buffer configuration. A fast closing of S1 during current pulse integration makes the voltage at output node go immediatly to Vref voltage, drastically reducing baseline restoration time. Furthermore, current pulses during reset are not integrated.

The critical aspect of this system is that closing S1 connects the output node directly to C_D, that can be as big as 60 pF. This, raises instability problems during reset phase that have to be correctly addressed during design phase.

The criticity of single ended CSP reset is also present in the CSP fully differential implementation in Figure 4.1. However, a more complex reset strategy

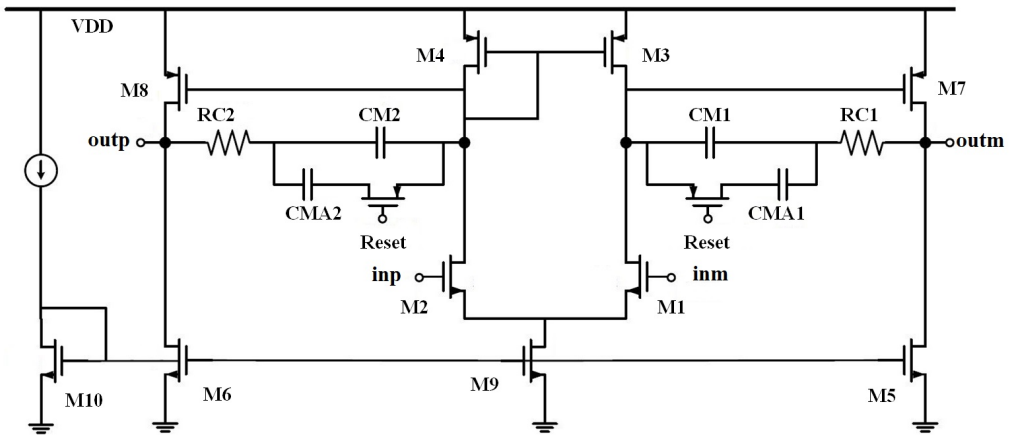


Figure 4.3: Scheme of OpAmp used.

is here implemented, to guarantee stability in every state of channel operation. A key feature is the variable compensation opamp implemented.

4.2.1 OpAmp

To ensure stability in every phase of circuit operation a multi-phase reset has been implemented. The opamp used in the CSP, and in the Shaping stage, is a compensated two stage fully differential amplifier, shown in Figure 4.3. It features a variable compensation consituted by an always active compensation CM1-2 and additional capacitors CMA1-2 activated during reset phase to ensure stability.

To reduce noise for following comparison, M1 and M2 have a g_m of $25mAV$. OpAmp low frequency gain is 50 dB and it is biased with a reference current of $400\mu A$ for a total power consumption of $10.66mA$.

4.2.2 Reset state

To guarantee stability in the whole reset cycle, the feedback switch S_F is closed only after activation of additional compensation. Figure 4.4 shows reset signals generated at the beginning of reset phase. CC signal, controlling OpAmp compensation, is activated immediatly after reset, togheter with the SIGNAL IN signal, that closes S_{VCM} switches to null input signal. FB signal activates

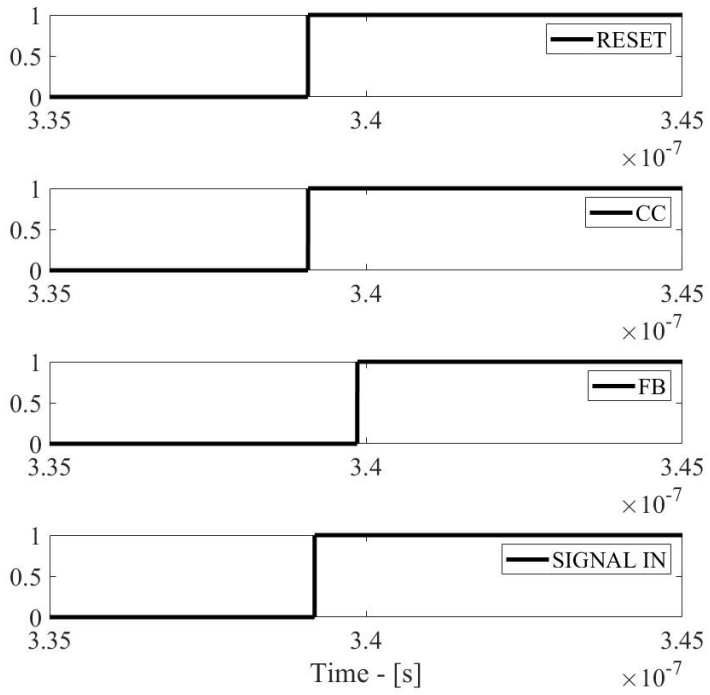


Figure 4.4: Diagram of reset phases at reset beginning.

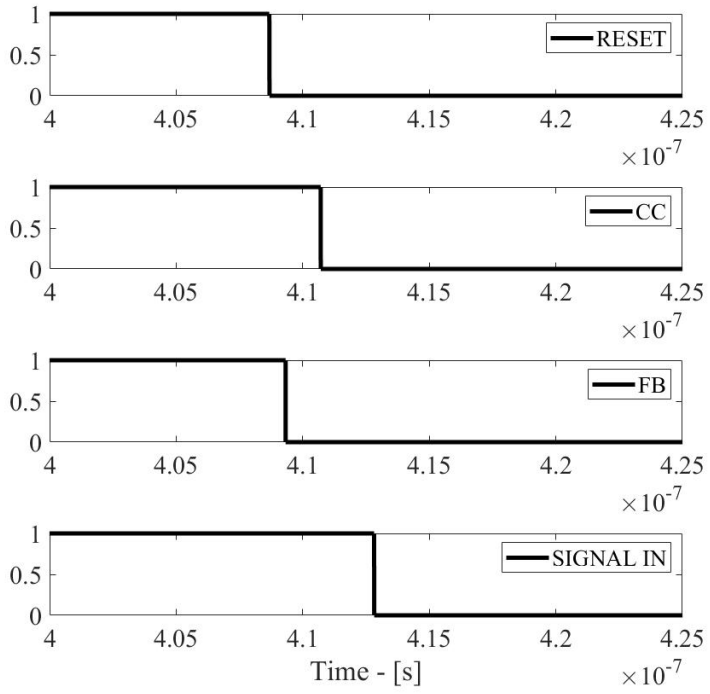


Figure 4.5: Diagram of reset phases at reset ending.

feedback switch with a delay that guarantees complete activation of additional compensation before reset. Furthermore, FB controls switch S_{IN} that allows to balance CSP inputs without requiring high currents from S_{VCM} switches.

Signals controlling reset ending are shown in Figure 4.5. Immediatly after the end of RESET signal, FB signal becomes 0, ans S_F is opened. Back to the CSP configuration the additional compensation is deactivated by the CC signal. SIGNAL IN keeps S_{VCM} activate for a short period after reset, to ensure that charge injection from switches does not generate signal at channel input.

4.3 Shaper

The Shaping stage shown in Figure 4.1 is implemented with the same OpAmp used for the CSP. Shaper Transfer function can be approximated to a single pole system with a time constant given by $1/(2\,\pi R_2 C_2)$. Low frequency gain can be approximated to the ratio R_2/R_1. Values of R_2,R_2,C_2 were chosen to have 30 dB gain and unity gain at 170 kHz.

C_2 was implemented with a 4-bit programmable capacitive array, to allow Shaper calibration for mitigation of process variations effects.

4.4 Comparison Stage

The comparison stage, shown in Figure 4.6, processes Shaper output. Comp1 and Comp2 are two stage comparators used to compare the analog signal to two different thresholds and generate outputs Q_1 and Q_2 stored in two resettable latches. Thanks to capacitors C_3 it is possible to bias the two inputs of each comparators at different voltages to apply a threshold for event detection. Hence, each channel has 4 Digital to Analog Converters (DACs) that generate a programmable voltage at comparators inputs. As shown in Figure 4.7, DACs are implemented with a topology based on two resistors strings. MSB decoder controls the strings with coarse resolution, while LSB decoder controls the finer resolution string for a total of 8-bit resolution. Full scale is fixed at 70 mV by design.

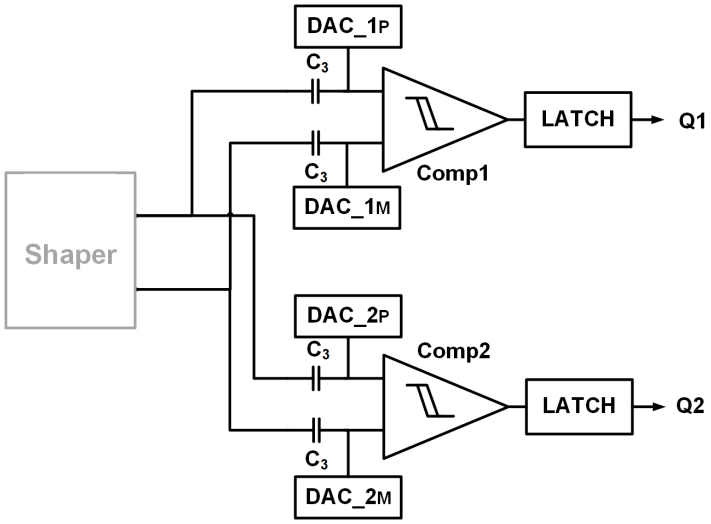


Figure 4.6: Schematic of Comparison stage.

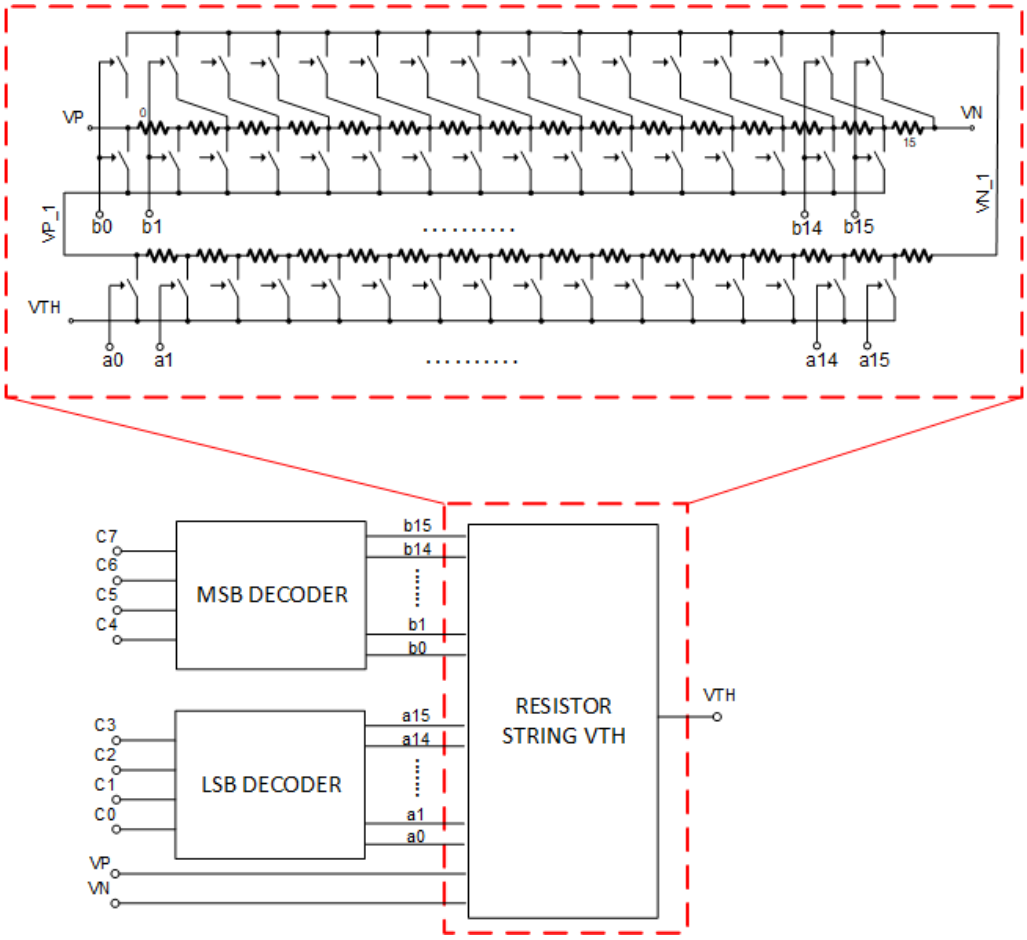


Figure 4.7: Scheme of DACs used for threshold generation.

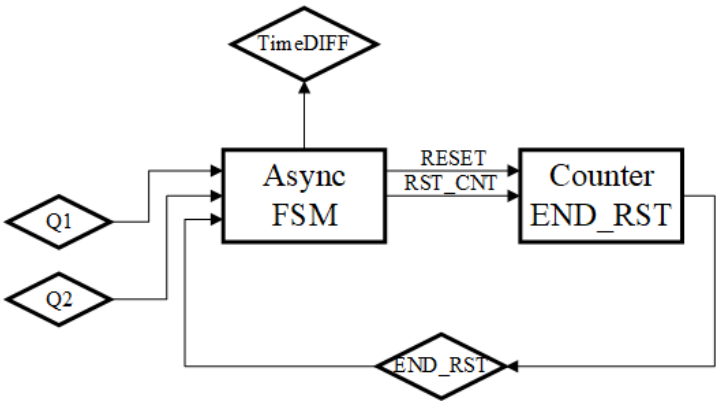


Figure 4.8: Logic Unit diagram.

4.5 Logic unit

FTfe channel operation is controlled by a Logic Unit that triggers channel reset when an event has been completely processed. A diagram of the Logic Unit is shown in Figure 4.8. Comparators outputs Q_1, Q_1 are input signal for an Asynchronous Finite State Machine (AFSM), that triggers the beginning of the reset phase and generates $Time_{DIFF}$ signal. The Counter END_RST block determines duration of reset phase and sends an END_RST signal to the AFSM that determines reset phase ending. This counter is implemented without a clock signal and measures time thanks to voltage increase on a capacitor connected to a current source. This counter can be programmed with 4-bit resolution between 80 ns and 200 ns

4.5.1 Async FSM

The Asynchronous Finite State Machine is here described. Its internal states are represented in Figure 4.9. Each internal state can be represented with the following expressions:

$$A_{n+1} = \sum s_A + A_n \cdot \sum \overline{r_A} \tag{4.1}$$

where A_n are states of single bit register storing machine state and s and r are set signal and reset signal for the cell. The 4 four state machine can then be

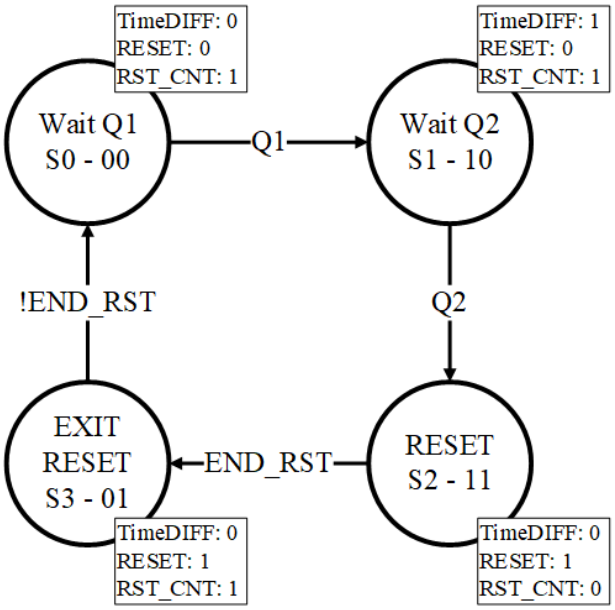


Figure 4.9: FSM diagram.

described with two bits named A and B, whose states are given by:

$$A_{n+1} = s_0 \cdot Q1 + A_n \cdot \overline{(s_2 \cdot \text{END\_RST})} = \overline{\text{B}} \cdot Q1 + A_n \cdot \overline{(\text{B} \cdot \text{END\_RST})} \quad (4.2)$$

$$B_{n+1} = s_1 \cdot Q2 + B_n \cdot \overline{(s_3 \cdot \overline{\text{END\_RST}})} = A \cdot Q2 + B_n \cdot (A + END\_RST) \quad (4.3)$$

Outputs can be obtained from each state with the following Table:

s	A	B	$TimeDIFF$	$RESET$	RST_CNT
s_0	0	0	0	0	1
s_1	1	0	1	0	1
s_2	1	1	0	1	0
s_3	0	1	0	1	1

$$TimeDIFF = A \cdot \overline{\text{B}} \quad (4.4)$$

$$RESET = B \quad (4.5)$$

$$RST\_CNT = \overline{\text{A} \cdot \text{B}} \quad (4.6)$$

To address the problem of single threshold crossing, when only the first threshold is crossed, further logic is added outside the Logic Unit. When $Time_{Diff}$ signal

is started, arriving at state S1, an analog counter similar to the one used to determine threshold duration is activated. If a Q2 signal arrives before end of counting the counter is reset and $Time_{Diff}$ signal ended. If counting ends before detecting a Q2 signal $Time_{Diff}$ output signal is ended with a duration equal to counting time. This counter can be programmed with 4-bit resolution between 10 ns and 50 ns.

Chapter 5

FTfe Simulations

In this chapter results from transistor level simulation of FTfe channel are presented. First, some results from simulations of fundamental blocks will be presented. After that, results of simulations to verify full channel functionality will be presented.

5.1 Analog processing

A simulation of CSP transfer function is shown in Figure 5.1. 87 dB DC gain and unity gain frequency confirms correct operation, while operation of 5-bit calibration system is verified in maximum and minimum capacitance setting, plotted with dashed lines. Shaping stage transfer function simulated is instead shown in Figure 5.2. 30 dB DC gain given by resistor ration is confirmed in simulation, togheter with expected bandwidth. Transfer functions for maximum and minimum capacitance values are also shown with dashed lines.

5.2 DAC

Simulations performed to assess DAC operation consider also mismatch effects, that can have important effects on its operation. To ensure DAC linearity two quantities are considered: Differential Non Linearity and Integral Non Linearity.

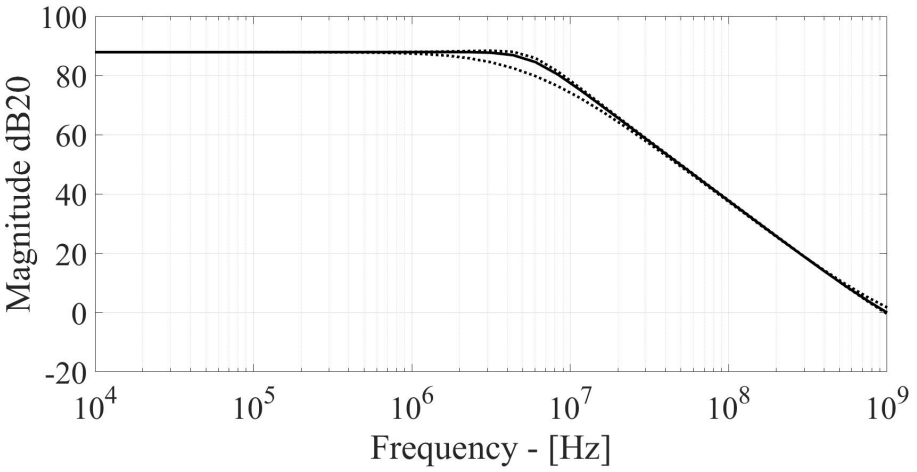


Figure 5.1: CSP transfer function calibration.

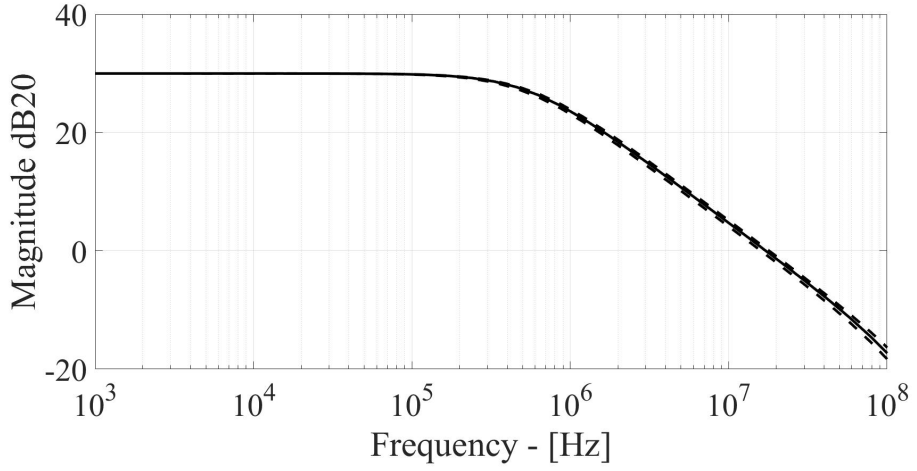


Figure 5.2: SH transfer function.

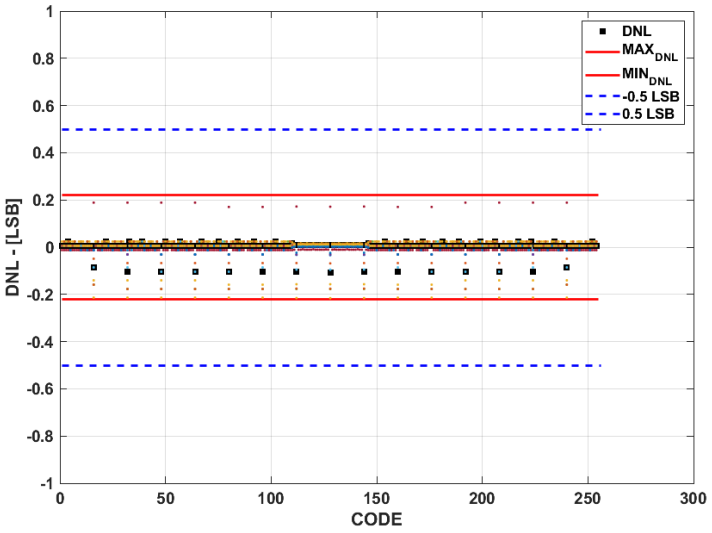


Figure 5.3: DAC DNL evaluated in Montecarlo simulations.

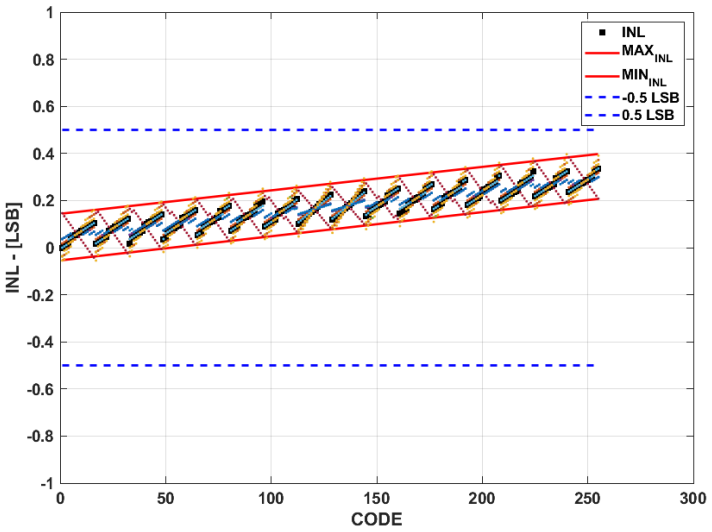


Figure 5.4: DAC INL evaluated in Montecarlo simulations.

The first can be computed with the formula:

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{LSB} - 1 \tag{5.1}$$

that takes into account the difference between adiacent output values in DAC output scale. For proper operation DNL should be smaller than half of LSB. The second evaluates the difference of output voltage in units of LSB.

$$INL(i) = \frac{V_{outIdeal}(i) - V_{outReal}(i)}{LSB} \tag{5.2}$$

Data obtained from DNL and INL calculation of DAC output in Montecarlo simulations are shown in Figures 5.3 and 5.4 respectively.

5.3 Transient simulations

In Figures 5.5 and 5.6 output from two full channel schematic simulations are shown. The first shows response to maximum input signal of 100 fC, the second response to minimum input of 5 fC. In both plots input current pulse is shown at the top, right below differential signal at CSP output is shown. In the third subplot, SH response is shown, followed by the TimeDIFF calculated and start of following reset. In both cases the channel processes correctly input signal and is able to reset completely CSP and SH outputs.

With this threshold configuration a TimeDIFF of about 3 ns was obtained with maximum input, while 20 ns was obtained with the minimum.

5.4 TimeDIFF vs Qin curve

Analyzing outputs of multiple simulations it is possible to observe $Time_{DIFF}$ variation in Q_{in} range. Some points extracted in Post-Layout simulations are shown in Figure 5.7. Here, error bars estimated from expected noise performance dominated by CSP g_m, are also shown. Solid red line shows a fit with equation 3.14, that approximates the real curve.

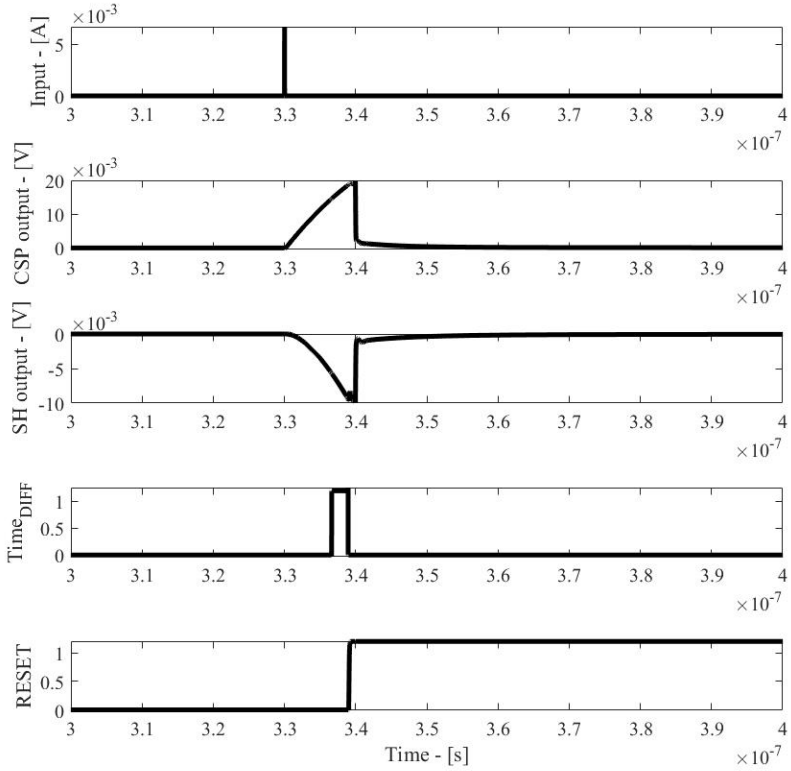


Figure 5.5: Full Channel simulation with 100 fC input.

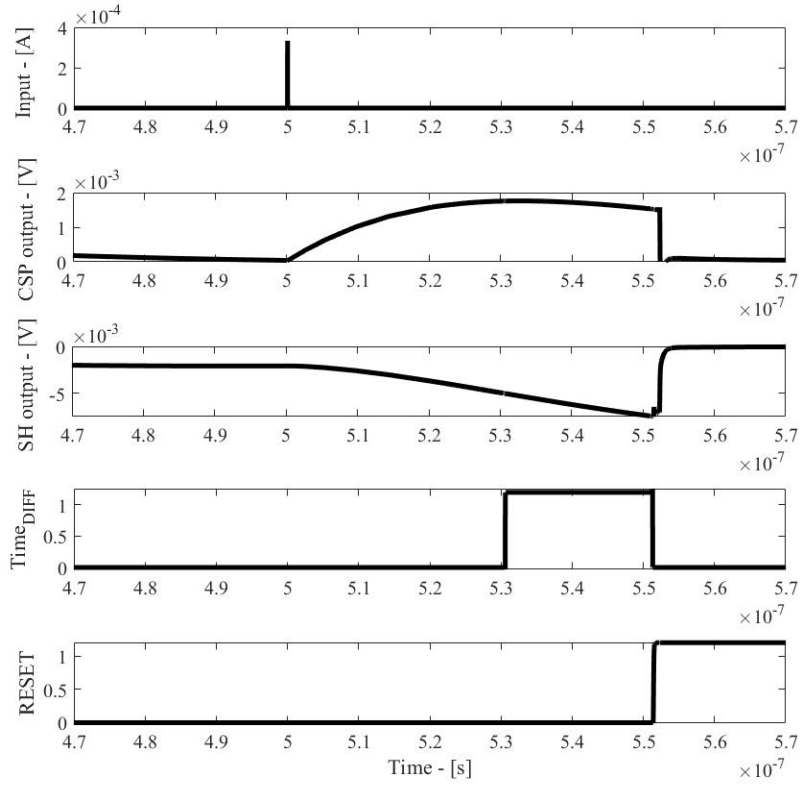


Figure 5.6: Full Channel simulation with 5 fC input.

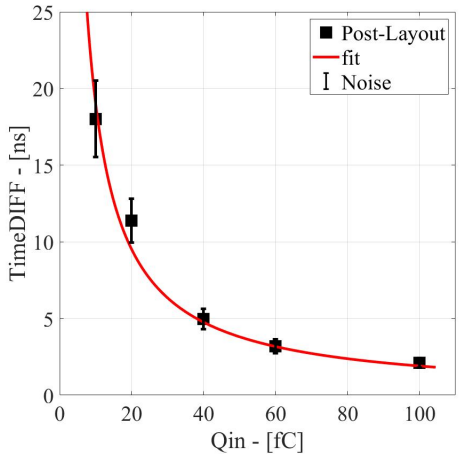


Figure 5.7: TimeDIFF values obtained in Post-Layout simulations. Error bars are estimated from expected noise performance.

Chapter 6

Conclusions

In this thesis, some of the major challenges in the development of CMOS integrated circuits for high rate gaseous particle detectors were analyzed. Critical aspects of Triple-GEM detectors readout were analyzed and experimental results obtained with GEMINI chip were reported. Data collected showed that GEMINI meets the maximum count rate requirements of 5 Mcps on detector and Time over Threshold and imaging tests gave promising results. Furthermore, effects of ionizing radiation on readout performance were analyzed using experimental data obtained with an custom built irradiation setup. Analysis of data collected gave no evidence of a significant variation in Time over Threshold response with a 20 Mrad TID.

A new signal processing technique for high rate readout was also analyzed. Thanks to a two threshold system, information on input charge is acquired on signal rising edge, allowing to reset the readout channel before complete processing of input signal. An approximated model for charge estimation from data obtained was presented. A Fully Differential Fast Tracking frontend, implementing the technique described, was presented. Channel performance was simulated and results from simulations of most critical blocks were presented. Fabrication of a 4-channel prototype in planned for the end of 2019.

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Milano, October 2019 Luca Mangiagalli