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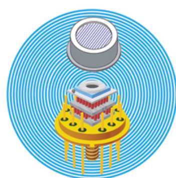
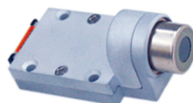

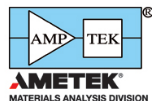

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Solving the critical thermal bowing in 3C-SiC/Si(111) by a tilting Si pillar architecture

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The exceptionally large thermal strain in few-micrometers-thick 3C-SiC films on Si(111), causing severe wafer bending and cracking, is demonstrated to be elastically quenched by substrate patterning in finite arrays of Si micro-pillars, sufficiently large in aspect ratio to allow for lateral pillar tilting, both by simulations and by preliminary experiments. In suspended SiC patches, the mechanical problem is addressed by finite element method: both the strain relaxation and the wafer curvature are calculated at different pillar height, array size, and film thickness. Patches as large as required by power electronic devices (500–1000 μm in size) show a remarkable residual strain in the central area, unless the pillar aspect ratio is made sufficiently large to allow peripheral pillars to accommodate the full film retraction. A sublinear relationship between the pillar aspect ratio and the patch size, guaranteeing a minimal curvature radius, as required for wafer processing and micro-crack prevention, is shown to be valid for any heteroepitaxial system. © *2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* https://doi.org/10.1063/1.5019325

I. INTRODUCTION

In Ref. 1, a new architecture for exceptionally efficient compliant substrates in the epitaxial growth of several-microns-thick Ge layers on Si (001) is proposed. Deep reactive ion etching of the Si substrate by the Bosch process allows for the realization of microns-tall Si pillars, arranged in dense square arrays with a lateral size of some hundreds of micrometers. Subsequent Ge deposition by low energy plasma enhanced chemical vapor deposition provides self-aligned prismatic Ge crystals on the Si pillar top, spaced a few hundreds of nanometers for a vertical growth lasting tens of micrometers.[2,3] Merging of the Ge crystals into a suspended Ge patch on the pillar array was obtained and theoretically analyzed, both by subsequent and prolonged thermal annealing,[4] or by growth at higher temperatures.[5] The principle of such an approach was also proven for standard Ge deposition in a thermal CVD apparatus[6] and for cubic 3C-SiC/Si (001) and (111).[7–9] Heteroepitaxial growth on Si pillars was also demonstrated for other systems, e.g., GaAs/Si[10] and GaAs/Ge/Si[11] or GaN/Si.[12]

A detailed analysis of the elastic properties of the Ge/Si(001) system by Finite Element Method (FEM) simulations and experimental Raman, photoluminescence, and X-ray diffraction measurements was presented in Ref. 1, showing that the lateral tilting of the Si pillars (as tall as 8 μm) gives rise to a full thermal strain relaxation in the epitaxial layer (as thick as 6–8 μm), particularly for squared patches as small as 100 μm in size. In that paper, the possibility to achieve elastic compliance by exploiting the effective tilting of pillars due to their high aspect-ratio was outlined by a simple analytical model. However, on the one hand Ge is elastically softer than Si and, on the other hand, very few applications require suspended Ge films as thick as several micrometers, and Ge patches as large as some 500–1000 μm. The latter conditions are usually required in heteroepitaxial systems for power electronic applications, where GaN and 3C-SiC are presently the most important competitors.[13,14] The second one is more compatible with standard Si-semiconductor processing and more environmental-friendly than the former one. Nevertheless, it exhibits a large lattice misfit with Si ($\sim$23%) and tougher elastic properties than GaN. The latter issue is a critical point, as, differently from the Ge case, thermal bowing of the substrate is usually very large,[16,17] particularly for the (111) wafer orientation, since the misfit in the thermal expansion coefficients amounts to $\sim$8% at room temperature.[15] Extended wafer cracking easily occurs on Si(111), the more interesting orientation for defect reduction,[18,19] even after just a few SiC micrometers have been deposited. Such a large bowing for the (111) orientation is due to the incomplete plastic relaxation of the lattice misfit by extended defects (despite their lower density with respect to the (001) orientation),[18] and it results in a tensile stress contribution at high temperature (the opposite for the Ge/Si system), which adds to the tensile thermal contribution during cooling down to room temperature. Therefore, a

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larger effective thermal strain should be obtained with respect to other systems and, along with the remarkable stiffness of the SiC elastic constant, it makes such a system a very good candidate for thermal strain reduction by a tilting pillar architecture, as also indicated by preliminary SiC deposition experiments reported here (see also Ref. 9).

The relevance of the substrate bowing in 3C-SiC/Si systems requires an extension of the modeling presented in Ref. 1, where the relationship between the patch size and the pillar height is addressed. Here, we present targeted FEM calculations providing an in-depth analysis of the role played by the pillar architecture in mitigating thermal stress in both the film and the substrate. In particular, by suitably relating the wafer bowing to the residual strain in the film, we show that for large patch sizes the bowing may be doctored if a proper pillar aspect ratio is selected, according to a very general sublinear relationship of pillar height and patch size. The origin for such an effect is analyzed in terms of the maximum pillar tilting at the patch edges. A confirmation of the model prediction is provided by analyzing preliminary experimental samples grown on both planar and patterned substrates. We finally show that the large misfit (both thermal and lattice-originated) and the stiff elastic constants provide for 3C-SiC a small increase in the wafer bowing with film thickness, at variance with the case of Ge/Si(001) and cubic GaN/Si(001), as calculated for comparison.

II. METHODS

A 1 mm thick Si(111) substrate is considered here, patterned in square patches of micrometer-sized pillars, as sketched in Fig. 1(a). Different geometries were considered by varying the patch size L (100–1500 μm), as well as the micrometric height h and base width w of the pillars, while a constant spacing of 2 μm is set between the pillars. The separation between different patches is fixed to 8 μm. A continuum SiC epitaxial layer is positioned on top of the pillars, with thickness in the range of 1–25 μm.

An initial (unrelaxed) tensile strain ε_0 is imposed on the SiC region, corresponding to the residual strain present at room temperature in a flat epitaxial 3C-SiC layer after the growth. More precisely, ε_0 results from both the contributions of residual lattice misfit, a highly defective interface region, and the thermal coefficient mismatch between the two materials, as a byproduct of the complex mechanisms of defect generation and redistribution during the whole sample processing.[15,18,20–22] As such, the actual value of ε_0 is in general dependent on the peculiar growth processing and cannot be set *a priori*.[23,24] In the present calculations, we assume a value of 0.3%, according to unpublished experimental measurements of planar SiC/Si(111) films (see also the *a posteriori* confirmation in the case reported in Sec. III B), despite the ideal estimation of the thermal mismatch contribution alone, based on thermal coefficients at usual deposition temperature [some 1300–1400 °C (Ref. 20)] would result in 0.1%.

The commercial code COMSOL Multiphysics® was adopted for the numerical solution of the partial differential equations of mechanical equilibrium, thus providing the relaxed strain field ε. For the sake of accuracy, an optimized mesh, finely refined in the region of the Si pillars, as sketched in Fig. 1(c), has been used in the calculations. The zero-displacement Dirichlet boundary condition is imposed at the bottom of the substrate, while the zero-stress Neumann boundary conditions are set at all free surfaces. Si and 3C-SiC were treated as elastically isotropic materials, with Young's modulus Y_{Si}=170 GPa and Y_{SiC}=600 GPa and Poisson ratio ν_{Si}=0.26 and ν_{SiC}=0.18, according to the literature values for (111)-oriented substrate.[25,26]

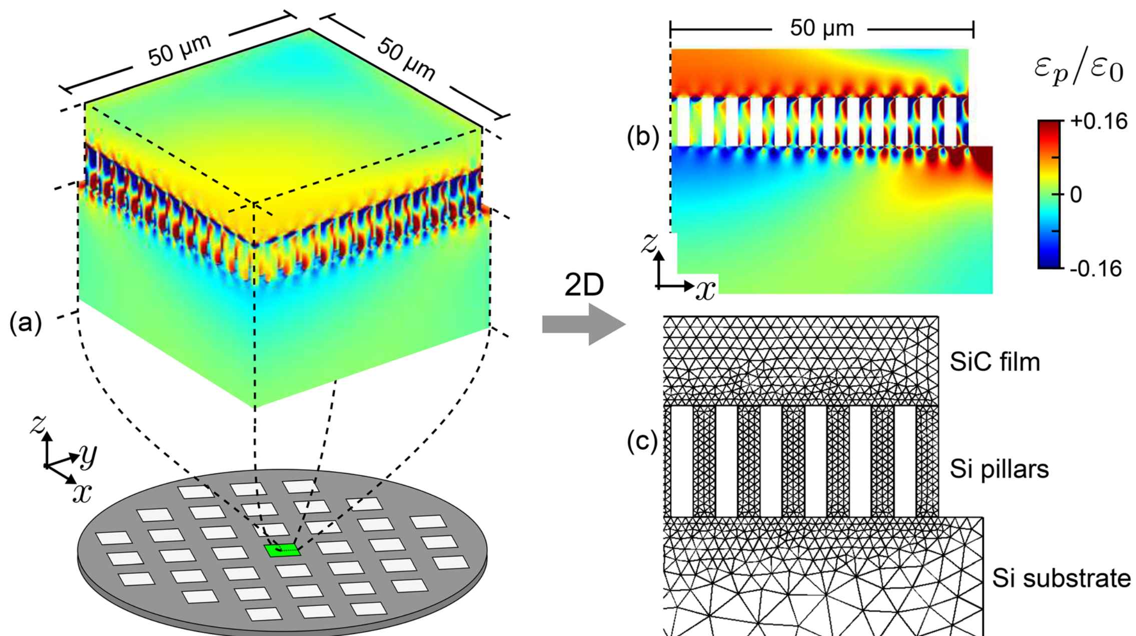

FIG. 1. Comparison of strain relaxation of an 8 μm SiC film on a 100 μm large patch of Si pillars on Si substrate for both 3D (a) and 2D (b) geometries. 8 μm tall pillars of base width 2 μm are considered. A single patch, corresponding to a central one in the wafer patterning, sketched in the figure [panel (a)], is considered. Only a quarter (half) sector of the 3D (2D) patch is reported. The color map shows the in-plane strain ε_p corresponding to $0.5(\varepsilon_{xx} + \varepsilon_{yy})$ in the 3D case and to ε_{xx} in 2D. A coarsened representation of the triangular mesh used for the 2D FEM calculations is also reported in panel (c).

Simulations were performed in both 3D and 2D, the latter one corresponding to an array of infinite ridges. However, 3D simulations are possible only in the case of a single patch as small as 100 μm, due to high computational cost, while in 2D multiple patches can be considered, up to a lateral size L = 1500 μm. In Fig. 1, we show color maps of the in-plane strain obtained by FEM calculations in both 3D [panel (a)] and 2D [panel (b)] for a single 100 μm wide patch, with periodic conditions applied only at the vertical sides of the substrate region, below the pillared single patch. Moreover, by exploiting the squared symmetry of the patch, just a quarter of the structure was considered in the 3D case, and one half in the 2D case. In the 3D structure, the strain relaxation in the film is obtained for both the ε_{xx} and ε_{yy} components, particularly effective close to the edges of the patch, while in the 2D case the relaxation concerns just the ε_{xx} component and the ε_{yy} value is set to zero. By a full numerical comparison, it comes out that the 2D simulation provides a reasonable representation of the central slice of the actual 3D structure, still overestimating the average residual strain over the entire SiC patch by approximately a factor 2. This overestimation essentially comes out of the larger elastic stiffness in the bending of a continuous Si ridge (as for our 2D pillar calculations) with respect to a row of pillars, where voids are intercalated between them. Moreover, the initial setting $\varepsilon_{yy} = 0$ in the 2D calculations, rather than the actual value obtained by solving the full 3D mechanical problem, causes a minor additional overestimation of ε_{xx}, also guaranteeing a safe overestimation of the wafer curvature with respect to the 3D case since the two are linearly related, as will be discussed further on. To quantify this difference for the more technologically relevant case of larger patches, we have considered a test case for a patch of 1000 μm in the x direction, periodic by 10 μm in the y direction, both by 2D ridges and the actual pillared substrate, as in the 3D case of Fig. 1. We see that the overestimation in residual strain decreases to a factor 1.1, indicating a reduction of the 2D/3D discrepancy with increasing residual strain. Based on these considerations, in the following of the paper, we only report results of 2D pillar calculations (shortly addressed as "pillars"), allowing us both to consider the system-scale commonly interesting in applications and to supply useful quantitative information, but for a maximum factor 2 at very low bowing cases. This overestimation safely compensates possible increases in the experimental bowing, as produced by some unpredictable SiC deposition on pillar sidewalls and at the bottom of Si trenches. On the other hand, the reduced 2D tilting does not allow us to correctly predict the actual stress within the pillars, which is larger, and hence a possible breaking of the peripheral pillars for some critical geometries: an issue which is, however, not hindering any application. According to the previous comparison between 2D and 3D results, we estimate that for patches as large as 500–1000 μm, a pillar height beyond 15 μm, usable for technological applications, guarantees a tilting angle sufficiently small to stay within the failure critical stress [$\sim$7 GPa (Refs. 27 and 28)]. As a confirmation, preliminary experiments reported in this paper demonstrate that no mechanical ruptures are visible at an optical microscope.

Two different approaches can be exploited in order to associate the residual strain after the elastic relaxation with the corresponding bowing of the substrate. In the first case, a sequence of consecutive patches along the substrate surface is taken into account, as illustrated by the black contour in Fig. 2(a) for six 1000 μm-sized patches, mimicking the whole wafer patterning. On the one side of the chain (left in the figure), a free surface is assumed, corresponding to the border of the wafer, while on the other side (right) symmetry conditions are applied, as corresponding to the wafer center. In this way, the substrate bowing is directly provided by the displacement field resulting from the FEM solution of the mechanical equilibrium problem. In particular, this is shown in Fig. 2(a) where the bent structure obtained by the displacement field (amplified by a factor 100 to make it more evident) is reported. The vertical component of the displacement is also highlighted by the color map. An enlarged view of a portion of the wafer surface around the boundary between two patches is also shown to indicate the local deformation at the surface. Due to the computational cost, even in 2D, this approach is only viable when considering a small number of patches (<10), not representative of real wafers as large as 100 or 150 mm.

The second approach is then introduced to overtake such limitations, by providing an approximated evaluation of the substrate bowing for more realistic sizes. Only a single patch is taken into account in the FEM calculation, imposing periodic boundary conditions as done for Fig. 1. This is a reasonable simplification when focusing on one of the patches at the

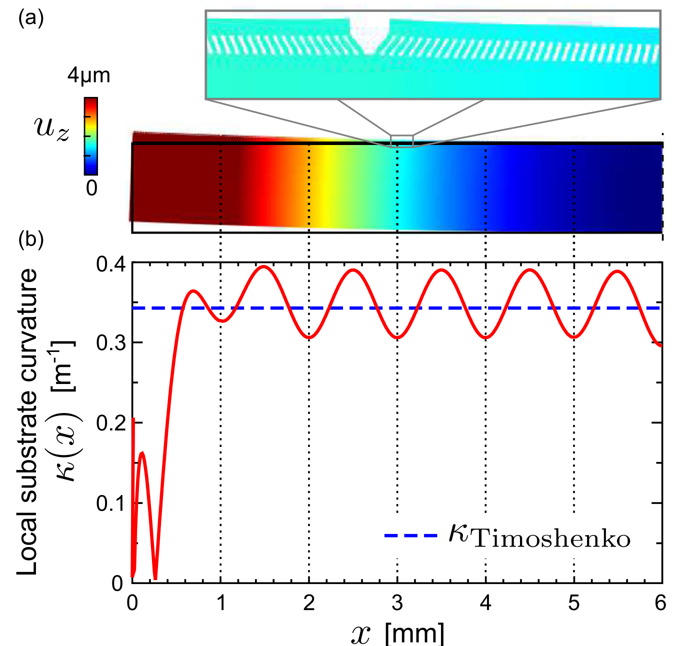

FIG. 2. Solution of the mechanical equilibrium problem for a sequence of 6 consecutive 1000 μm-sized patches. Pillars are 8 μm tall and 2 μm large in base, the SiC film is 8 μm thick, and the substrate is 1 mm thick. In panel (a), the undeformed geometry is traced by the black contour while the deformed geometry as obtained after strain relaxation by FEM is given in color (displacements are amplified by a factor 100). The color map reports the vertical displacement values. An enlarged view of the region between two patches is also shown. In panel (b), the substrate curvature directly computed from the simulation (red continuum line) is compared with the value obtained by the analytical Timoshenko formula (dashed blue line).

center of the wafer, confined among other tens in all directions. In order to convert the strain field computed by the FEM calculation into a value of substrate curvature κ (or curvature radius R_κ), we then assume that the system behaves in the same way for a bilayer structure, as if the pillars were not present, still with a film residual strain as the average calculated with the pillar architecture $\langle\varepsilon_{xx}\rangle_{film}$. In this case, we can make use of the analytical Timoshenko formula[29] for planar bilayers

$$\kappa = R_\kappa^{-1} = \frac{6(1+m)^2}{(h_{Si}+h_{SiC})\left[3(1+m)^2+(1+mn)(m^2+m^{-1}n^{-1})\right]} \times \langle\varepsilon_{xx}\rangle_{film}, \quad (1)$$

where h_{Si}=1 mm is the Si substrate thickness, h_{SiC} is the SiC film thickness, $m = h_{Si}/h_{SiC}$, and $n = Y_{Si}/Y_{SiC}$.

The analogy of the actual system with the simpler case of a bilayer can be qualitatively inferred by noting how the deformed geometry in Fig. 2(a), as computed on a coarse scale, follows a smooth bowing line while only magnifying the view that it is possible to recognize a fine structure affected by the actual pillar patterning. For a more quantitative validation of our approximation, the plot in Fig. 2(b) provides a comparison between the local curvature computed at the bottom of the substrate, by the full calculation based on the first method, and the estimate provided by the Timoshenko formula, following the second approach. Excluding the behavior obtained in correspondence of the first patch, strongly influenced by the presence of the lateral free surface, an oscillating trend is recognized, with a maximum value of curvature below each patch, i.e., where the film is actually present, and minima in between them, i.e., where the stressor is absent. Interestingly, starting from the third patch toward the wafer center, the amplitude of the oscillations tends to stabilize and the average value looks well comparable to the estimate provided by Timoshenko formula using the film strain on a single patch as prescribed in the second approach. All results in this paper are then obtained by exploiting this second, simplified approach.

III. RESULTS AND DISCUSSION

A. Predictions for 3C-SiC/Si(111)

Following the methodologies outlined in Sec. II, we now analyze the impact of different geometries on the reduction of the substrate bowing. Notice that the patch and pillar sizes considered here are fully within the limits of the current lithography processes, so that realistic predictions can be obtained.

First, we studied the impact of the patch lateral size. Figure 3 shows two cases, 200 μm [panel (b)] and 1000 μm [panels (d) and (e)] in patch lateral sizes, for SiC thickness of 8 μm. For comparison, we include in the figure also the case of the corresponding finite patch directly deposited on the flat substrate [mesas, panels (a) and (c), respectively]. Notice that, for sake of scale, the 200 μm systems are displayed entirely, while the 1000 μm cases are displayed in one half. The color

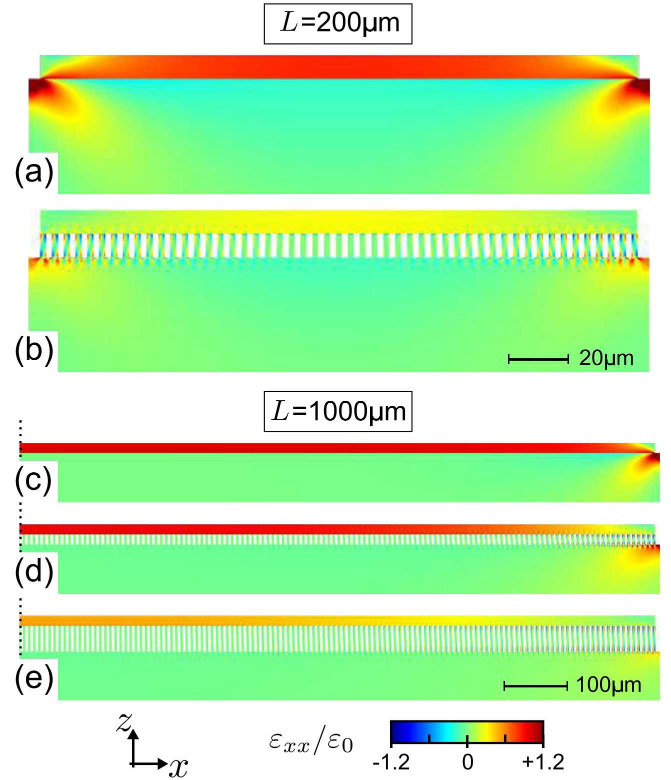

FIG. 3. Comparison of in-plane ε_{xx} strain maps between a SiC mesa [(a) and (c)] and a SiC film suspended on a Si pillar patch on Si [(b), (d) and (e)], for two different sizes L = 200 μm and L = 1000 μm (half is shown). For all cases, the underlying Si substrate is 1 mm thick, while the SiC film is 8 μm thick. Si pillars have a base width of 2 μm and are 8 μm tall in the simulations reported in panels (b) and (d), while h = 20 μm in panel (e).

mapping reports the relevant in-plane strain component ε_{xx} with respect to the full strain value (0.3%). In panels (b) and (d), the Si pillars are 8 μm in height and 2 μm in base, the same as reported in Ref. 1 for the Ge/Si(001) system. According to the latter work, we see here that, in the case of the 200 μm patch, the strain relaxation provided by the pillar architecture with respect to the mesa [panel (a)] is very large. However, as we move to the more interesting patch size of 1000 μm [panel (d)], the additional strain relaxation with respect to the mesa (c) is limited to a small area of few tens of micrometers, close to the patch edges. If the pillar height is increased to 20 μm, still with the same base, we see in panel (e) that the compliance effect turns out to be relevant across the whole patch.

Actually, the average strain relaxation in the 8 μm SiC film with respect to the patch size for different pillar heights (still 2 μm in base) is quantitatively addressed in Fig. 4. Starting with the case of the mesa (h = 0), for small pillar height, the residual strain readily saturates to the planar one with increasing patch size, while relevant relaxations (60%–80%) can be obtained for h = 20 μm even for device-oriented patches as large as 600–1000 μm. At such pillar heights, the trend of the curve with patch size is also different, similar to the initial part of the one for h = 10 μm, where the free tilting of the pillars is complete, as we will see in the following.

According to the obvious observation that the compliance effect increases with pillar aspect ratio (h/w), even a

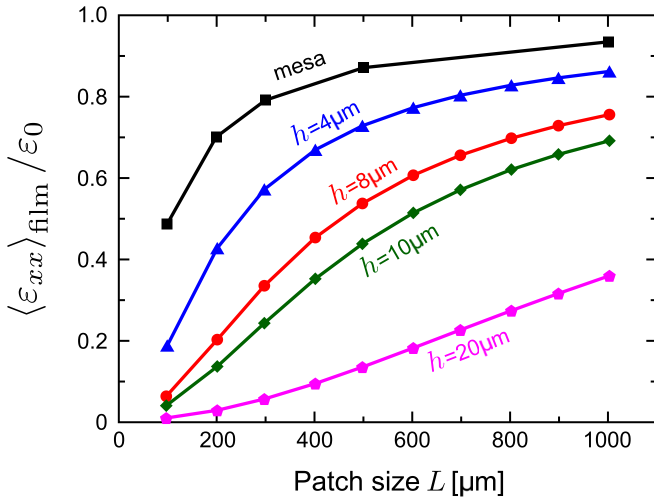

FIG. 4. Comparison of the strain relaxation in the film for different patch sizes L and pillar heights h. The limiting case of a mesa structure is also reported. All cases refer to an 8 μm thick SiC film and 2 μm large pillars. The strain is obtained as the average of the ε_{xx} component within the SiC film region.

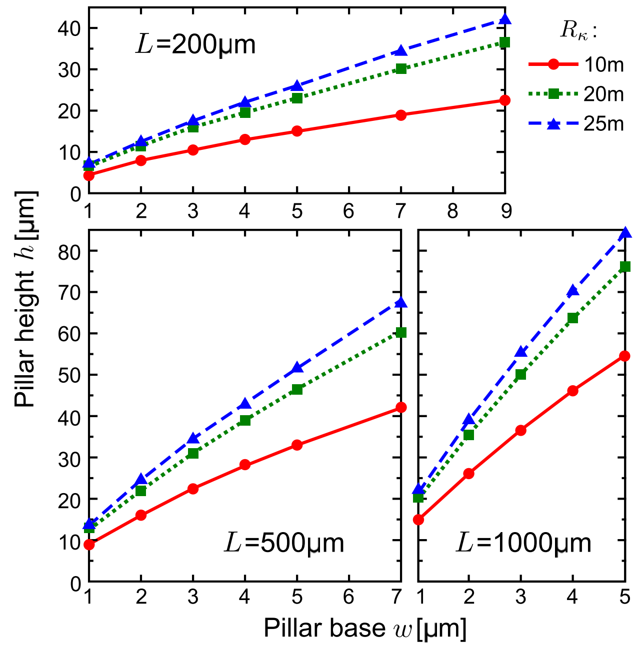

FIG. 5. Critical curves of pillar height h and base width w resulting in given values of curvature radius R_κ = 10, 20, and 25 m. Each plot corresponds to a different patch size L = 200, 500, and 1000 μm. In all these simulations, the SiC film thickness is equal to 8 μm.

variation of the pillar base influences the strain relaxation in the film and, consequently, the curvature of the substrate. Actually, the full scaling with pillar sizes should include also the thickness of the film. Here we prefer to focus on a given SiC thickness of 8 μm and to provide pairs of (h, w) for different patch sizes, such that the curvature radius remains larger than a critical value. In particular, we selected three values for the curvature radius R_κ that are technologically relevant for wafer manufacturability in size of 4 in. and 6 in.: 10, 20, and 25 m. In Fig. 5, we report in three different panels (patch size of 200, 500, and 1000 μm) pairs of (h, w) providing the same critical radius. Realistically speaking, in order to have a curvature radius of 25 m and patches of 1 mm in size, one needs to carve pillars as deep as 40 μm, 2 μm in width and 2 μm in spacing: these are still reasonable dimensions and aspect ratios for a Bosch etching process. For computational limits, the (h, w) ranges that we could explore in simulations are different for the different patches, being limited in the largest one. Obviously, if a full size scaling of the system would have been performed, the h(w) curves would result in straight lines.

If we aim at understanding the reasons why large patches display an unrelaxed area close to the center, if the pillar aspect ratio is not sufficiently large, we need to get deeper in the description of the mechanism allowing for pillar compliance. As described in Ref. 1 for the Ge/Si case, the key point is that the lateral tilting of the pillars is in turn produced by the pillar free rotation, as provided by the curl of the displacement field in the whole pillar. In Fig. 6, the curl of the displacement calculated by FEM for h = 8 μm and w = 2 μm is reported in a color mapping for three patch sizes, where the deformation of the whole structure (amplified by a factor 10) is also visible. This quantity directly indicates the rotation extent around the *y* component (perpendicular to the figure plane). It is interesting to note two issues: the first one is that in the case of the 200 μm patch (the one with the largest strain relaxation) all the pillars but the central one are rotated, while several ones for the 500 and 1000 μm case are not rotated in the central area. The second feature is that the rotation of the peripheral pillars is approximately the same for 500 and 1000 μm patches, despite that the larger patch would require a larger peripheral retraction of the film, and in turn, a larger rotation. Therefore, it appears that the reason why the central pillars

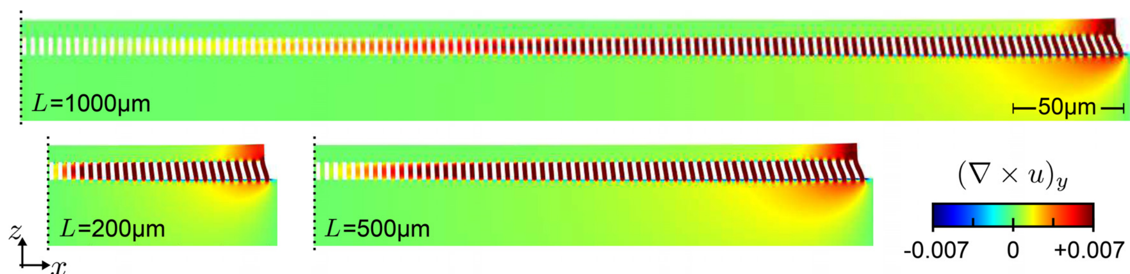

FIG. 6. Color map of the rotation component of the displacements for patches of three different sizes L = 200, 500, and 1000 μm (half is shown). Si pillars are 8 μm tall and have a 2 μm large base. The SiC film is 8 μm thick. The geometry is distorted according to the computed displacement field (magnified by a factor 10).

are not sufficiently rotated and, hence, the overlaying film is not sufficiently relaxed, is the frustrated rotation of the peripheral ones, occurring beyond an elastic maximum which depends on the pillar aspect ratio.

In Fig. 7, we report a detailed and quantitative analysis that better describes this concept. For patch sizes L ranging from 100 up to 1500 μm, we plot the rotation around the y axis for each pillar, from the edge towards the center of the patch. It is evident that for small patches the rotation scales linearly with pillar position, a feature that guarantees full strain release, as the tilting and the film retraction should also scale linearly. On the contrary, for larger patches, the rotation decay with pillar position is progressively nonlinear and, correspondingly, the rotation of the more peripheral pillars in the different patches gradually converges to a maximum value, which is essentially the same for 500, 1000, and 1500 μm in patch size. This means that in large patches the mechanical resistance of the pillars against rotation actually balances the contraction force provided by the film. The inset shows the rotation of the peripheral pillars as a function of the patch size for different pillar heights and base widths. With respect to the usual case of h = 8 μm w = 2 μm, we see that by doubling h (black circles), the rotation is larger and the saturation value is delayed to larger patches. On the contrary, the blue triangles correspond to the case of doubling w with respect to the case reported by the black curve, i.e., the same aspect ratio as for the red curve. In this case, the rotation is inhibited by the larger base, and the saturation for larger patches approximately occurs as in the case of the red curve. Actually, the free rotation of the peripheral pillar for a given height h strongly depends on width: as a classical beam pinned at one end, the lateral displacement of the opposite end under a constant tangential force depends on w, as shown in Ref. 1 for the Ge/Si case. For such a reason, the onset of peripheral rotation, and in turn of the strain relaxation in the film, suddenly occurs in a limited w range, as reported in Fig. 8.

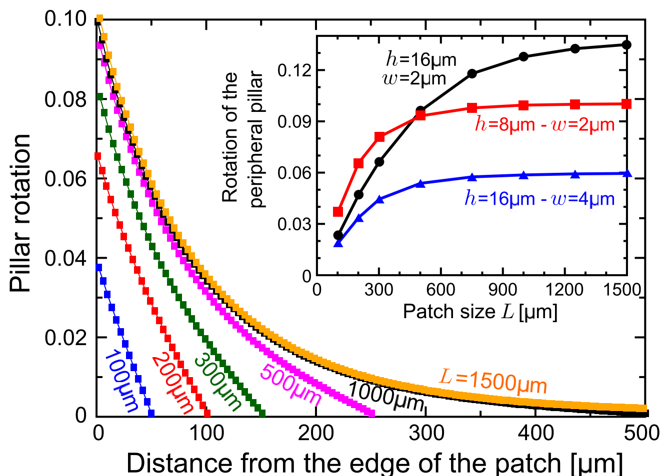

FIG. 7. Rotation of each pillar inside a patch, for different patch size L. Each point corresponds to a pillar from the peripheral one toward the patch center. Si pillars are 8 μm tall and have a 2 μm large base. Inset: rotation of the most peripheral pillar as a function of the patch size. Curves obtained by doubling the pillar height h and the base width w are reported. All results are obtained for a SiC film thickness of 8 μm.

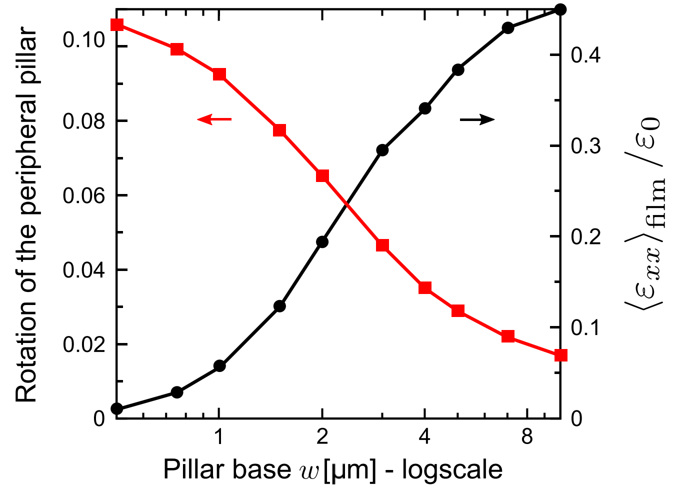

FIG. 8. Dependence of the rotation of the external pillar (left axis) and of the average film strain (right) on the width of the pillar base. The SiC film is 8 μm thick, and the pillars are 8 μm tall.

B. Experimental confirmation for planar and patterned 3C-SiC/Si(111)

In order to test the validity of our theoretical predictions and to offer a proof of the efficacy of the tilting pillar architecture in solving the issue of thermal bowing, preliminary experiments were performed. 3C-SiC/Si(111) samples were grown for both planar and pillar-patterned substrates on 4 in. wafers in a hot-wall CVD reactor (ACISM10) with a large reaction chamber. The standard growth process consists of six steps: bake out, first ramp up, carbonization, second ramp up to the 3C-SiC growth temperature, and SiC deposition. The bake out was done at 500 °C under high vacuum (about 10^{-4} mbar). After a quick H_2 etching of the Si surface, the ethylene (C_2H_4) gas was introduced in the reaction chamber and the temperature was increased up to 1140 °C, to initiate the carbonization. When carbonization finished a second ramp up increased the temperature up to 1370 °C, which is the standard temperature to grow 3C-SiC. The deposition of the 3C-SiC epitaxial layer was then performed by letting C_2H_4 flow into the chamber together with trichlorosilane (TCS). A growth rate of 3 μm/h was set and the samples were prepared for thicknesses roughly ranging from 1 to 21 μm, by regulating the duration of the deposition from 1 to 7 h. The actual thickness for the planar substrates was then checked by Fourier Transform Infrared (FTIR) spectrometer (QS2200 Nanometrics), by analyzing the reflectance spectra of the SiC layer. Substrate bowing was measured by using a Nomarski Differential Interference Contrast (NDIC) microscope (Nikon Eclipse L200). By tuning the focus on the film surface, we measured the z-axis value at five points (center, east, north, west, and south) on the wafer and then we estimated the bow as the variation between the maximum and minimum z-axis values.

A nearly crack-free epitaxial SiC layer (cracked area below 10%) was obtained on a planar substrate (800 μm in thickness) only for a thickness of 1 μm, resulting in a large wafer curvature (7.6 m radius). By exploiting the Timoshenko formula [Eq. (1)], with our estimation of 0.3% in thermal

strain for the SiC layer, we obtain a curvature radius of 10 m. This is quite a good agreement, by considering also the experimental (unexpected) evidence that a progressive crack density (for 2 and 4 μm deposition, we have cracked areas of 50% and 80%, respectively) increases the bowing, progressively beyond the Timoshenko prediction. If the SiC film thickness is virtually increased to 10 and 21 μm for a substrate as thick as 1 mm (experimentally impossible because of full wafer fragmentation in the growth chamber), the Timoshenko prediction for the curvature radius would be 1.8 and 0.9 m, respectively.

On the other hand, a thick SiC film was successfully grown on a pillar-patterned substrate as thick as 1 mm. As schematized in Fig. 9(a), hexagonal patches sized $\sim$100 μm, composed of hexagonal pillars of different width w and spacing d, were defined on the wafer, according to the crystal symmetry of the (111) plane. The patches, covering the full wafer, display different pillar base size and spacing, in order to preliminarily investigate the suspended SiC film formation by different geometries, in a single growth run and under the same growth conditions of the planar case. In Figs. 9(b)–9(d), we show top-view Nomarski images of a 21 μm thick SiC sample on 20 μm tall Si pillars, for three different pattern geometries. In panels (b) and (d), the pillars have a base width of 3 and 10 μm, respectively, and a spacing of 3 μm, resulting in a partially coalesced film with some remaining holes between the pillars. On the contrary, in panel (c), a base width of 5 μm with a pillar spacing of 2 μm is found to result in a continuous film. The analysis of additional samples with SiC thicknesses of 3, 6, and 12 μm shows that, for this geometry, a connected SiC pillar network is formed already at 12 μm. This allows us to estimate an effective thickness of the continuous film approximately ranging from 10 to 20 μm, depending on the patch configuration. It is not possible to perform reliable simulations with such a large variation of pillar geometry across the wafer, but still bowing measurements demonstrate that the sample displays a satisfactory curvature radius (approximately 16 m), at least one order of magnitude larger than the one expected for the corresponding planar configuration. More importantly, the film is unbroken and crack-free, in contrast to any one grown to the same thickness on a planar substrate. Also, pillars remain intact for any pattern, indicating that stresses are lower than the failure threshold.

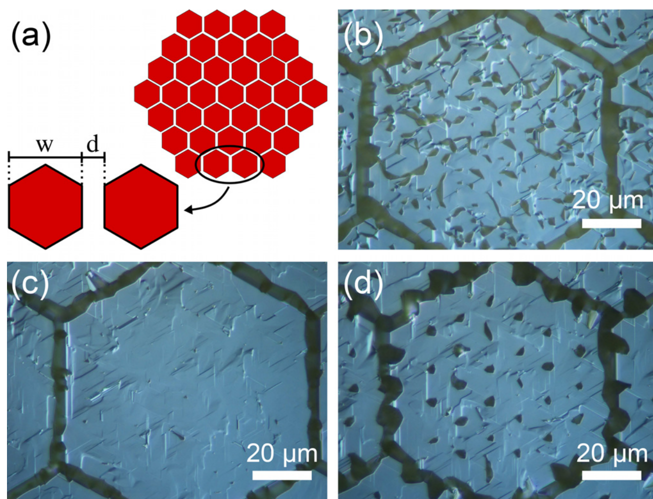

FIG. 9. (a) Scheme of the pattern composed of hexagonal Si pillars with base width w and pillar distance d for a single patch. Top views by a Nomarski microscope of L = 100 μm patches after deposition of 21 μm SiC on 20 μm tall Si pillars with (b) w = 3 μm and d = 3 μm. (c) w = 5 μm and d = 2 μm. (d) w = 10 μm and d = 3 μm.

This preliminary result provides a qualitative, still neat, demonstration of the efficacy of the tilting pillar architecture in doctoring the problem of substrate bowing by minimization of the thermal stresses. Additional experimental work is now in progress to obtain a full wafer covering with patches, as large as 500 μm, bearing a fully continuous suspended SiC layer, in order to characterize the film for device fabrication.

C. Predictions for other epitaxial materials on Si(111)

In Sec. III A, we focused on the mechanism of thermal strain relaxation (and, in turn, reduction of wafer bowing) made possible by exploiting the Si pillar architecture, just considering a SiC film with a thickness of 8 μm. We now want to investigate more explicitly the role played by the film itself when considering different film thicknesses and materials, such as cubic GaN and Ge.

In Fig. 10, we plot the variation of the curvature radius R_κ as a function of the film thickness for a pillar height h = 8 μm and patch size of 1000 μm: we see that there is no variation between 8 and 20 μm in thickness, mostly explained by the interplay of the elastic constants and the residual strain in the Timoshenko formula. Actually, if the ones for cubic GaN/Si(001) (softer film) and Ge/Si(001) (even softer than Si) are taken, we see that a different behavior occurs. In particular, for Ge we used the same parameter reported in Ref. 1, while for a cubic GaN we choose the parameter Y = 181 GPa and ν = 0.352, as reported in Ref. 30, and ε_0 is calculated simply as the thermal strain due to the difference in the thermal expansion coefficient with Si. In the latter case, we considered a deposition temperature of 900°, which is a reasonable average between the different values reported in literature, for different deposition techniques. Regarding the thermal expansion coefficients, we use here $5.59 \times 10^{-6}\,°C^{-1}$ for GaN[31] and

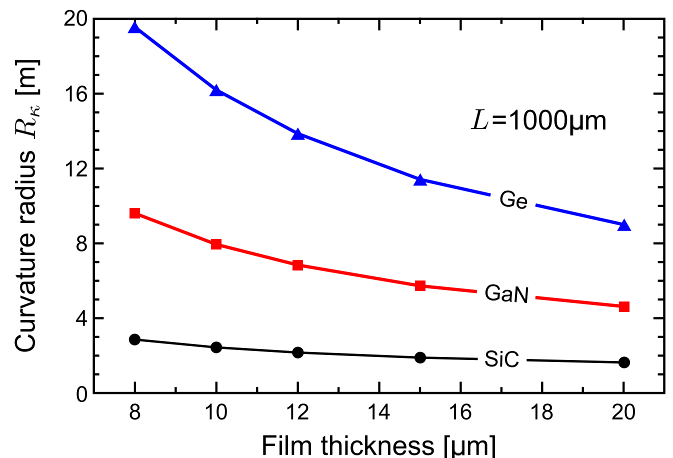

FIG. 10. Variation of the curvature radius R_κ as a function of the film thickness for three different materials: 3C-SiC as discussed in this work, Ge as in Ref. 1, and GaN based on literature values.[30,31] Pillars are 8 μm tall and 2 μm large, and a patch of L = 1000 μm is considered.

$2.6 \times 10^{-6}\,^{\circ}\mathrm{C}^{-1}$ for Si.[32] ε_0 turns to be 0.196%. The results are reported by the red and blue curve in Fig. 10, showing that the SiC case is a fortunate one, being nearly independent of the film thickness.

Finally, with the same input parameters for the three materials, we plot in Fig. 11 the pillar height with respect to the patch size in order to have a curvature radius R_κ larger than 25 m. The film thickness is set to 15 μm, while the base of the pillars is 2 μm. It can be observed that, even if the three materials have different elastic properties, the curves are ordered following the strain values that are to be relaxed, e.g., highest strain ε_0 is present in SiC so that the tallest pillars are needed for a relaxation rate to get the target curvature radius. Notice that the functional behavior is equal for the three systems. In particular, the discrete values for the different patches have been interpolated with the following function: $\frac{h}{w} = A + B\left(\frac{L}{1000\,\mu m}\right)^C$ and the fitting parameters are reported in Table I. Actually, the leading parameter C is surprisingly similar in all the three cases, demonstrating that the mechanism underlying the compliant role of the pillar architecture is general and the concept has a wide applicability.

IV. CONCLUSIONS

The present paper indicates that the substrate bowing (and cracking) by thermal misfit between a stiff and thick film, such as cubic 3C-SiC for power electronics, and a Si substrate can be doctored by a tilting pillar architecture. This occurs for continuous SiC patches on finite pillar arrays, provided a suitable aspect ratio for the micrometric pillars is selected, according to the patch size, still within the actual limits of silicon substrate lithography. Such a mechanism is shown to be effective particularly for the SiC(111) orientation, which is promising in terms of defect density, still quite critical (few micrometers in deposition) for wafer cracking, in the planar configuration. Due to the fact that most of our simulations are actually performed for infinite ridge arrays, rather than actual pillar arrays, safely predicting an overestimation of the substrate curvature, more experimental investigations are needed to bring the patterning geometry to the optimal configuration for device fabrication on sufficiently large and thick SiC patches. Still, our concept is sound, as demonstrated by the preliminary experimental data reported here. The sublinear relationship between the ridges aspect ratio and the patch size is demonstrated to be generally applicable to any heteroepitaxial system, and to be determined by a maximum lateral tilting value for the peripheral structures in a patch. Our approach can then be used for the very practical purpose of estimating the optimal pillar aspect ratio to comply with the critical bowing required for the applications. Our findings can also be applied to the case of thick films wafer-bonded on a patterned substrate, where the problem of extended defect nucleation in the formation of the suspended patch by the lateral epitaxial growth on pillars is not present.

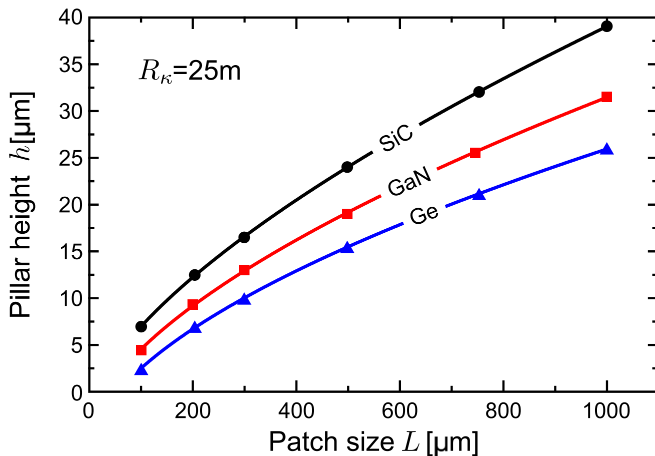

FIG. 11. Critical curves of pillar height h and base width w resulting in a curvature radius $R_\kappa = 25$ m. Three different materials are compared: 3C-SiC as discussed in this work, Ge as in Ref. 1, and GaN based on literature values.[30,31] Simulation values plotted as points in the graph are interpolated by a function $\frac{h}{w} = A + B\left(\frac{L}{1000\,\mu m}\right)^C$, with the fitting parameters reported in Table I. Pillar base is 2 μm.

TABLE I. Parameters for the fitting curves in Fig. 10 for $\frac{h}{w} = A + B\left(\frac{L}{1000\,\mu m}\right)^C$.

	A	B	C
SiC	−0.9 ± 0.14	20.4 ± 0.13	0.65 ± 0.01
GaN	−2.0 ± 0.3	17.7 ± 0.3	0.61 ± 0.02
Ge	−2.9 ± 0.3	15.9 ± 0.3	0.57 ± 0.02

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