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INNOVATIVE ANALOG AND MIXED-SIGNAL SOLUTIONS FOR PRECISE MEASUREMENT OF ELECTRICAL QUANTITIES IN POWER TRANSISTORS

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Contents

List of Figures

List of Tables

Glossary

ADC An analog-to-digital converter (ADC, A/D, or A-to-D) is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal.

DAC A digital-to-analog converter (DAC, D/A, D2A, or D-to-A) is a system that converts a digital signal into an analog signal.

PCB A printed circuit board (PCB) mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate. Components (e.g. capacitors, resistors or active devices) are generally soldered on the PCB.

ECU In automotive electronics, Electronic Control Unit (ECU) is any embedded system that controls one or more of the electrical system or subsystems in a transport vehicle.

ESD Electrostatic discharge (ESD) is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown.

EMI Electromagnetic interference (EMI), also called radio-frequency interference (RFI) when in the radio frequency spectrum, is a disturbance generated by an external source that affects an electrical circuit by electromagnetic induction, electrostatic coupling, or conduction.

BCD BCD technology incorporates analog components (Bipolar), digital components (CMOS) and high-voltage transistors (DMOS) on the same die.

LSB In a binary number, the LSB is the least weighted bit in the group. Typically, the LSB is the furthest right bit. For an ADCor DAC, the weight of an LSB equals the full-scale voltage range of the converter divided by 2^N, where N is the converter's resolution.

DNL Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.

INL The INL in DACs, it is a measure of the deviation between the ideal output

value and the actual measured output value for a certain input code. In ADCs, it is the deviation between the ideal input threshold value and the measured threshold level of a certain output code.

FSM Finite-State Machines (FSM) are sequential circuit used in many digital systems to control the behaviour of systems and data-flow paths..

MSB In a binary number, the MSB is the most weighted bit in the number. Typically, the MSB is the left-most bit.

Abstract

This thesis presents the development of a mixed-signal multi-functional system for automotive applications and, in particular, for high-side current measurements, open-load detection and thermo-electrical stress protection.

The system is composed of a tracking ADC featuring a triple-ranged resolution (coarse, fine and finest) in order to adapt to the system requirements and optimize the design in terms of area.

The coarse range, designed for the full-scale input values [0 A:100 A], has a 5 b resolution and it is used for the stress detection feature. The fine and the finest ranges are used for lowest input current values [0 A:14 A] where more accuracy is required.

Moreover, the system implements two protections functionalities: it is capable to detect a possible load detachment by processing the current measurements and it is able to estimate the wire temperature by digitally processing the ADC output and to signal if the cables heat up dangerously.

The current monitoring and the protection feature are extremely important as a reliable and embedded system enables the car manufactures to design the vehicles harness more efficiently, by reducing the copper cables diameter, and therefore to save costs.

Preface

In this thesis a multi-functional system for current measurements and thermo-electrical stress for automotive applications is presented and in this Preface the structure of the manuscript is described.

Chapter 1 introduces the electronics in automotive as a field which is becoming in these years as one of the most interesting with regard to the market and the research. A brief overview on the challenges the designers have to overcome when working in this context is given, as the automotive is one of the most harsh in terms of temperature, vibration and electro-magnetic pollution. Moreover this thesis project application background is given by going through the aim of the work and its motivation, describing briefly the main problem and the possible solution.

In Chapter 2 the system requirements are described. First some remarks on the design specification within the automotive electronics are given. Then the requirements on the three main system functionalities to be implemented (namely the current measurement, the open-load detection, and the thermo-electrical stress protection) are presented and discussed.

In Chapter 3 the concept of the multi-functional system implementing current measurements, open-load detection and thermo-electrical stress protection is presented.

The following Chapters describes the steps leading to the transistor level implementation. The flow used in this work is the following: Chapter 5 presents a 5 b ADC, implemented in order to gain familiarity with the used technology so to understand its characteristics when used for an high-precision signal processing blocks.

Once the 5 b ADC has been design and validated, the 8 b ADC presented in Chapter 6 has been implemented for the purpose of increasing the system accuracy and fulfil the accuracy requirements.

Afterwards the entire 10 b ADC described in Chapter 7 has been built together with the open-load detection.

Finally in Chapter 8 the block used for the temperature estimation and thermo-electrical stress protection is presented. This last part is more related to the logics design and the implementation of the digital algorithms.

Chapter 1

Introduction

1.1 Electronics in automotive

The first commercially successful example of an electronics system available on a car was the 1930 Galvin brothers' expensive $130 unit (a Model A Deluxe coupé cost $540) vacuum-tubes car-radio, which also was the first product to wear the Motorola name [1].

The development of semiconductors after WWII greatly expanded the use of electronics in automobiles, with solid-state diodes making the automotive alternator the standard after about 1960 [2].

In 1978 for the first time a microprocessor appeared on a car. The Cadillac Seville introduced a "trip computer" based on a 6802 microprocessor which was able to display mileage and other information [3].

In the following years more electronic systems entered the car for different purposes, such as engine optimization (e.g. fuel injection), comfort (e.g. air conditioning), safety (e.g. ABS), entertainment and driver information (e.g. GPS). These functionalities are controlled with embedded systems called Electronic Control Unit (ECU). An ECU is usually composed of one or more microprocessors, possibly memories, is able to process input signals into output signals and to communicate with other ECUs [4].

In recent years, ECUs were increased in their capabilities and are able to perform more complex and critical operations where the driver allows the electronic systems to, partially or totally, take over the control of the vehicle (e.g. adaptive cruise-control, auto-parking, etc.). Some modern cars contain up to 90 ECUs, 170 sensors, more than 15 million lines of code, and a few kilometres network with more than 1000 connection point [5], [6].

It is then clear that the growth rate of electronics within automobiles increased considerably in the years and, even if the price of chips continuously decreases, it

is unsurprising that the electronics share of the total car cost is predicted to reach 35% in 2020 and 50% in 2030, as shown in the graph in Figure 1.1 [7].

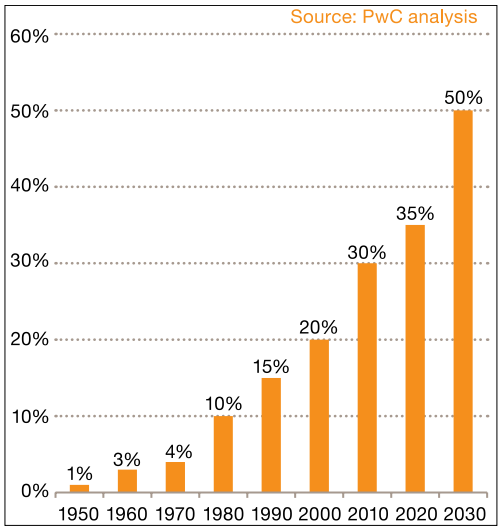


Figure 1.1: Growth in semiconductor content per vehicle (% of total car cost)

1.2 Design in automotive electronics

The automotive electronic systems present significant differences with respect to commercial electronics. For instance, the supply is provided by the car battery, the distribution of the ECUs system is all over the car body, and the safety requirements are more stringent for automotive applications.

The typical lead-acid battery nominally provides 14 V. However the supply voltage to the ECU's shows a large variation: typically 5 to 60 V and it is polluted by various interfering signals. Moreover 14 V batteries would not be able to supplies new high-power applications in the car considering the stringent emission requirements. Therefore supplementary new 48 V lithium-ion batteries have being developed especially for the mild-hybrid-vehicles market which is expected to increase in China and EU from 450.000 units in 2016 to 12.8 milions in 2032 [8]. This battery voltage is less polluted and the maximum ECU supply voltage is in both cases quite comparable. Internal in the ECU, standard low voltages are used for the high complexity signal processing micro-controllers and memories but the ASICs at the borders of the ECU must cope with the high voltages and disturbances on their supply pins, communication pins, sensor inputs and actuator outputs [4].

In order to have the ECU's as close as possible to the sensors, they are distributed all over the car-body and the network connecting them is prone to Electrostatic dis-

charge (ESD) and Electromagnetic interference (EMI). It is not possible to shield the connections because of the extra-weighting and costs therefore the automotive electronics must deal with ESD and EMI by design, whereas commercial systems operate in much cleaner environments. The proximity of the ECU's to the sensors increases speed and accuracy, but exposes these units to higher temperature (upto 150° in the engine compartment or more if the ECU's are closer to the exhaust) pushing thus the design in terms of reliability.

1.3 Automotive technology

Automotive electronics brings together two worlds which are apparently far, that is power electronics and accurate signal processing. As mentioned earlier, the typical lead-acid battery nominally provides 14 V and it is often supported with an auxiliary 48 V lithium-ion battery. On the other end, the ECU's distributed all over the car-body are required to precisely and fast process the signals coming from the sensors; such operation may not be performed with high-voltage devices (especially for speed, costs, and power reasons) but need to be preformed by low-power IC. In this scenario, since the middle eighties [9], a new technology emerged: the BIPOLAR-CMOS-DMOS (BCD) process (Fig. 1.2).

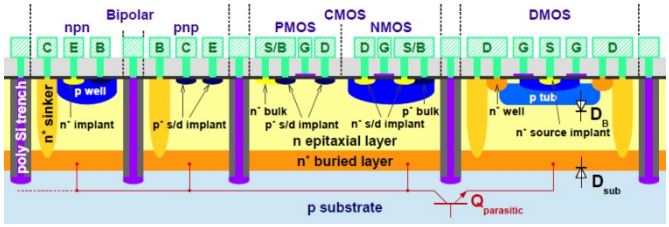


Figure 1.2: BCD technology

BCD is a family of silicon processes, each of which combines the strengths of three different process technologies onto a single chip: Bipolar for precise analog functions, CMOS (Complementary Metal Oxide Semiconductor) for digital and analog design, and DMOS (Double Diffused Metal Oxide Semiconductor) for power and high-voltage elements. This combination of technologies brings many advantages: improved reliability, reduced electromagnetic interference and smaller chip area.

Regarding the BCD process in automotive applications, an important trend [10]–[12] is to decrease the process expenses, and ultimately reduces the prices for end customers. Furthermore, several studies [10]–[12] address the need of increasing the technology robustness with respect to the electrical stress. In fact, all integrated power-transistors have to be robust against high energetic pulses. In some

applications these devices may be connected directly to the cable harness within cars and so demanding ESD-requirements have to be fulfilled. Moreover, because of the harsh, high-temperature environments, a robust low-voltage CMOS platform is needed. For these reasons it is important not only to ensure the circuits functionalities by technology, but also by design, implementing solutions which allows monitoring, and possibly detecting critical events that could damage devices under severe electrical stress.

The primary demand for robustness and the tendency to reduce fabrication-related costs make the BCD within the automotive environment a power-optimized technology which is not specifically tailored for high-accuracy signal processing blocks (as ADCs). For instance, some technologies are not featured with elements such as MIM or MOM capacitors therefore all the mixed-signal processing needs to deal, if required to [13], with non-linear elements like MOSFET caps in order to provide the desired performances. For these reasons, designing with a BCD power-optimized technology with the automotive environment presents new challenges for mixed-signals designers which are required to explore new solutions.

1.4 Motivation

1.4.1 Application background

This research project is focused on *high-side* load switch applications for automotive electronics. By definition, an high-side load switch is a device controlled by an external enable signal, and connects or disconnects a power source (battery or adaptor) to a given load. Compared to a low-side load switch, a high-side switch sources current to the load, while the low-side type connects or disconnects the load to ground, and therefore sinks current from the load [14].

The high-side load switch is showed in Fig. 1.3 and usually consists of the following three elements:

1. A pass element, which is essentially a transistor. It typically is an enhancement-mode MOSFET. The pass element operates in the linear region as a switch to pass the current from the power source to the load.
2. A gate-control block, which drives the voltage gate of the pass element switching it ON or OFF.
3. An input logic block, whose main function is to interpret the enable signal and trigger the gate control block, to switch the pass element ON and OFF [14].

The pass element is the most fundamental part of the high-side switch. The most frequently looked at parameters, especially the resistance of the switch while it is

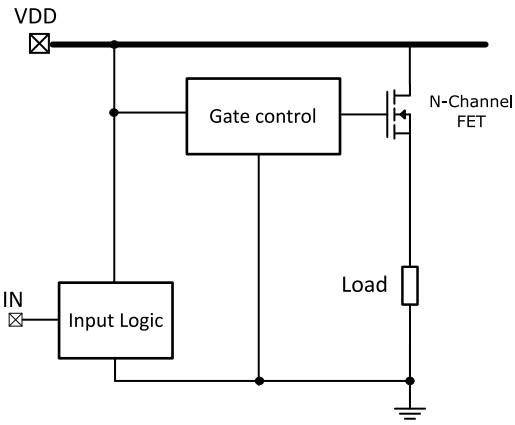


Figure 1.3: An N-Channel FET high-side load switch

ON ($R_{\mathrm{DS,ON}}$), are directly related to the structure and characteristics of the pass element.

The N-Channel FET uses electrons as the majority carriers, which have higher mobility than holes, the majority carriers in the P-Channel FET. This means that, with the same physical dimensions, the N-Channel FET has higher transconductance than the P-Channel FET, which translates to lower drain-source resistance during the ON state, or $R_{\mathrm{DS,ON}}$.

Typically, the $R_{\mathrm{DS,ON}}$ of the N-Channel FET is two to three times lower than that of a similar-sized P-Channel FET, thus a higher I_{DS} by a similar factor. This also means that, for the same $R_{\mathrm{DS,ON}}$ and I_{DS}, the N-Channel FET typically requires less silicon, and therefore has lower gate capacitance and threshold voltage than the P-Channel FET.

1.4.2 Aim of the work

In the automotive electronics, high-side switches are required to safely drive high currents into complex (resistive, inductive and capacitive) grounded loads in compliance with the harsh car environment. This requires both a robust, low on-resistance power switch and accurate analog circuitry for diagnostic, protection and control functions.

This work deals with the design of a multi-functional system for measurement of the current flowing through the high-side switch and the load, and thermo-electrical stress detection, whose purpose is increasing the system reliability by design. In fact wires might be damaged if their temperature, because of the Joule's effect, rises above a certain threshold. If a system that efficiently monitor the wire temperature is implemented, then car cables size may be reduced as they are

not required to compensate with robustness (i.e. larger diameters) to the current measurement/monitoring inaccuracy. An idea on how much car manufacturers might save by using smaller cables is given by the following quote referring to Fig.1.4 by Peter Guest, Bentley Bentayga product-line director: *"The harness is delivered on a pallet that's basically the size of the car"*

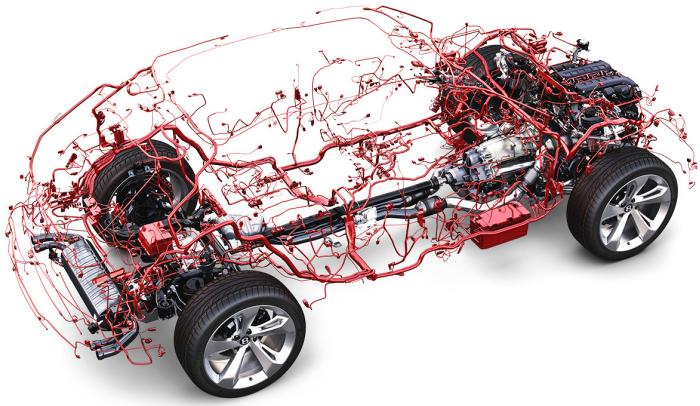


Figure 1.4: Bentley's complete wiring harness. Source: `https://www.motor1.com/`

1.4.3 The problem

The expected load current I_{load} flowing through switch and a load, which is to be measured, is composed of:
1) dummy loads currents - typically from 0 mA to 200 mA
2) load current - typically from 400 mA to 100 A

In case of the load detachment, the current flowing through the switch would be given only by 1). By measuring the I_{load}, the system shall be able to detect the detachment event and signal it. It is clear that, compared to the 100 A full-scale value, the differentiation between the open-load current $I_{\text{load,OL}}$ and the minimum open-load current $I_{\text{load,min}}$ is very difficult as these currents are relatively close.

With the information gotten with the current measurement, the system is required to estimate the temperature variation due to the Joule's effect in the cable and to shut-off the system whenever a too fast (according to the wire specifications) temperature rise is detected. This protection would allow the car manufacturers to reduce the harness diameters which are currently over-sized for the robustness' sake and, therefore, reduce significantly the production costs.

1.4.4 Possible solution

An effective way to carry out the current measurements within this environment is passing to the digital domain. For a current sensing, this involves implementing a system that first maps the analog input current to an analog voltage—since it is easier dealing with voltages than currents [15]—and then performs an Analog-to-Digital conversion. Moreover, for cost reduction, power devices and the ADC have to be realized in the same chip.

Increasing system integration and miniaturization of high-and-low power semiconductors allow finding solutions which monolithically combine high-voltage devices and low-voltage circuitry. As mentioned in Section 1.3, from the technological point of view the best candidate is the BCD technology (Fig. 1.2), even if, within the automotive environment, it is usually power-optimized and not specifically tailored for high-accuracy signal processing blocks (as the ADC).

Next chapter goes in detail through the system requirements, covering the specifications and the design constraints.

Chapter 2

System requirements

2.1 Introduction

In this Chapter the system requirements are described. First some remarks on the design specification within the automotive electronics are given. Then the requirements on the current measurement, the open-load detection, and the thermo-electrical stress protection are presented and discussed.

2.1.1 Automotive electronics requirements

As first remark this design shall fulfil all the following specification within a six sigma yield and in a $[-40\,°C : 150\,°C]$ temperature range, which is typical for any automotive applications

The six sigma concept requires that each process element and each part necessary for the product have a defect rate of no more than 3.4 PPM (parts per million). The underlying assumption is that the variations occurring in all the parameters associated with these process elements and parts follow a normal statistical distribution function and that the specification limits are situated six sigma away from the process average [16].

The $[-40\,°C : 150\,°C]$ temperature range takes into account a possible cold car start within the most frigid environment (such as mountains roads or tundras), and the hot engine compartment or the chassis near the breaks. This standard is defined within the 1994 AEC Q100 specification by the Automotive Electronics Council (AEC)[1], which is an organisation based in the United States that sets qualification standards for the supply of components in the automotive electronics industry.

[1] AEC homepage: `http://www.aecouncil.com/`

2.1.2 Current measurements requirements

The measurements system shall operate on the input current I_{load} which ranges from 0 A to 100 A. The system requirements globally regarding the current measurements are hereby enlisted:

1. Monotonic A-to-D conversion
2. Accuracy:
   i. ±8% at 10 A, more relaxed for higher values
   ii. ±8% at 100 A for the over-current detection
   iii. Additional detectable I_{load} values at 100 mA, 200 mA, and 300 mA
3. Conversion time (from start of conversion signal) : 90 µs

In particular, regarding the open-load detection feature the requirements are the following:

4. Externally selectable leakage currents detection thresholds:
   i. 20 mA ± 8 mA
   ii. 60 mA ± 8 mA

Monotonicity

An ADC is monotonic if, for increasing analog input, the digital output code increases and vice-versa. Monotonic behavior does not guarantee that there will be no missing codes. Monotonic behaviour is an especially important characteristic for ADCs used in feedback control loops since non-monotonic response can cause oscillations in the system [17].

A non-monotonic ADC transfer function would be missing a lower code until the higher code is converted (assuming linearly increasing input voltage). Fig. 2.1 shows a 3-bit ADC conversion plot with a missing code caused by a non-monotonic conversion.

Accuracy

ADCs are usually referred as having n-bit resolution, which often is misunderstood to mean accuracy.

The resolution of an ADC is defined as the smallest change in the value of an input signal that changes the value of the digital output by one count. For an ideal ADC, the transfer function is a staircase with step width equal to the resolution. However, due to system non-idealities, the transfer function's response will have a larger deviation from the ideal response.

Fig. 2.2 shows a 3-bit ideal conversion plot (black line). For a given analog input value a_0 with an ideal A-to-D conversion the ideal digital output would be marked

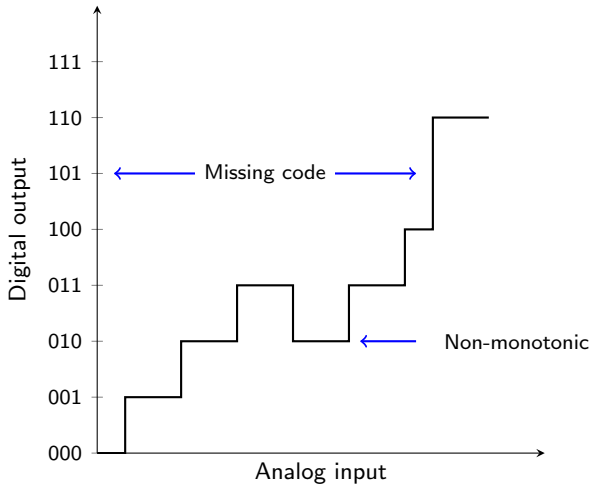


Figure 2.1: Non-monotonic 3 b A-to-D conversion, Source: `http://microchipdeveloper.com/adc:adc-monotonicity`

by the black spot. The red 'cloud' around this spot is the deviation from the ideal output. The smaller this cloud the better the accuracy.

Resolution does not imply accuracy nor does accuracy imply resolution, however an ADC accuracy cannot exceed the Least Significant Bit (LSB) size. Therefore accuracy sets the minimum resolution, i.e. the maximum acceptable quantization error.

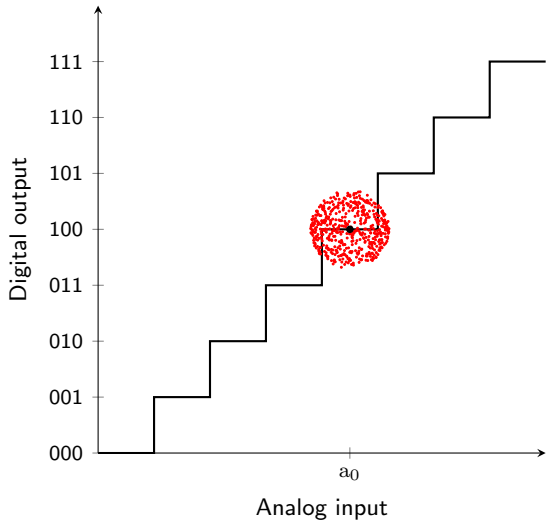


Figure 2.2: 3 b ADC conversion plot. The black dot is the ideal A-to-D conversion of a_0. The red cloud represents the conversion inaccuracy.

Quantization error is the difference between the analog signal and the closest available digital value at each sampling instant from the ADC. Quantization error also introduces noise, called quantization noise, to the sample signal. The higher the resolution of the ADC, the lower the quantization error and the smaller the quantization noise. The relationship between resolution (in bits) and quantization noise for an ideal ADC can be expressed as *Signal to Noise* $(S/N) = -20 \cdot \log(1/2^n)$, where n is the resolution of the ADC in bits.

Applications determine if missing codes are allowed and degree of accuracy required, which usually is uniform for all of the inputs values. However in this project different levels of accuracy are required for different input ranges. This characteristic will be exploited for a more efficient design.

Timing

The requirement regarding the timing in Point 3 determines the maximum time frame for the signal to be delivered at the output since the start of conversion signal, which is external to the system. This Point influences several aspects within the design, such as the type of architecture or the clock frequency, as explained in Chapter 5.

Open-load detection

The open-load detection feature is required in order to signal a possible load detachment from the wire where I_{load} is flowing. This functionality shall be activated whenever a current smaller the one LSB is detected. In this case, the system is required to distinguish if the current is indeed 0 A or larger than a programmable open-load currents. In the latter case the I_{load} current is due only to dummy loads, as mentioned in Subsection 1.4.3.

The threshold current used to detect the possible open-load is required to be externally selectable between two values which depends on the application.

2.1.3 Thermo-electrical stress protection

As mentioned in the introductory Chapter, the wire harness costs are a very important entry in the car bill of materials. An effective wire protection implementation would therefore enable the OEM to reduce the wire size. Such system would compensate to a decreased physical robustness with a reliable temperature estimation monitor [19].

The system is required to provide a thermo-electrical stress protection by detecting a critical temperature rise in the wire carrying I_{load}. The heat-up to be estimated is

due to the Joule's effect caused from the flowing current. In particular the system shall be able to:

1. select among three critical temperature rises ΔT_c, i.e. 15 °C, 25 °C and 35 °C
2. estimate the temperature behaviour according to five different kind of wires, which differ thermo-geometrically.

The wire current-temperature-time relationship is expressed by (2.1) [21].

$$\Delta T(t) = \frac{I_{\text{load}}(t)^2 \cdot \alpha}{A} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \tag{2.1}$$

where ΔT [K] is the temperature variation, t $[s]$ is the time, α $\left[\text{K} \cdot \text{m}^2/\text{A}^2\right]$ is parameter depending on the thermal characteristic of the wire, A $\left[\text{mm}^2\right]$ is the wire section and τ $[s]$ is the thermal time constant. The five wires characteristics are reported in Table 2.1.

Table 2.1: Wires characteristics

Wire	α $\left[\text{mK} \cdot \text{m}^2/\text{A}^2\right]$	A $\left[\text{mm}^2\right]$	τ $[s]$
1	175.50	0.35	14
2	154.05	0.5	18.1
3	136.50	0.75	23.2
4	128.70	1	27.5
5	118.95	1.5	33.9

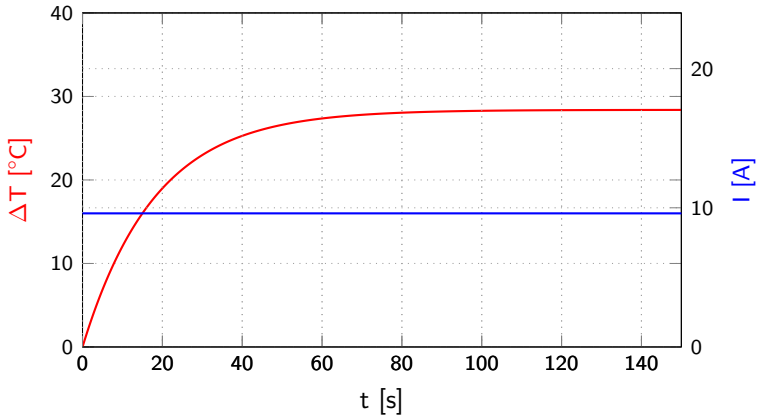
Fig. 2.3a plots the ΔT characteristic for Wire 4 with a constant input current $I = 10\,\text{A}$, whereas Fig. 2.3b plots the characteristic with a toggling input between 0 A and 12 A [19], [20]. As expected from (2.1), the behaviour of the curves is anti-exponential and, with a constant current, they would eventually reach an asymptotic value.

Fig. 2.4 shows the time vs. current characteristics for the five different wires, where ΔT_c has been set at 25 °C. These plots show for how long the different wires may sustain a current value before the protection shall be enabled. From Fig. 2.4 it could be noticed that the wires can sustain the lowest current values for infinitive time but then, after a certain wire-specific current-threshold, this time rapidly decays. Moreover, according to Table 2.1, the larger the wire the more current can be sustained for a longer time.

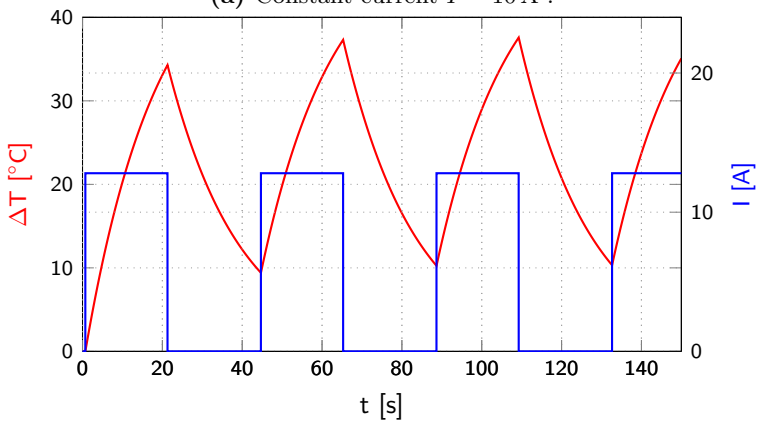
2.1.4 Design constraints

Constraints are the rules or limitations through which design is conceived and created. These limitations can be self-imposed, conceptual necessities, client directives, cost influenced, etc.

The constraints of this project are hereby enlisted:



(a) Constant current $I = 10\,\mathrm{A}$.



(b) Toggling current.

Figure 2.3: Temperature variation vs. time wire characteristics [19], [20].

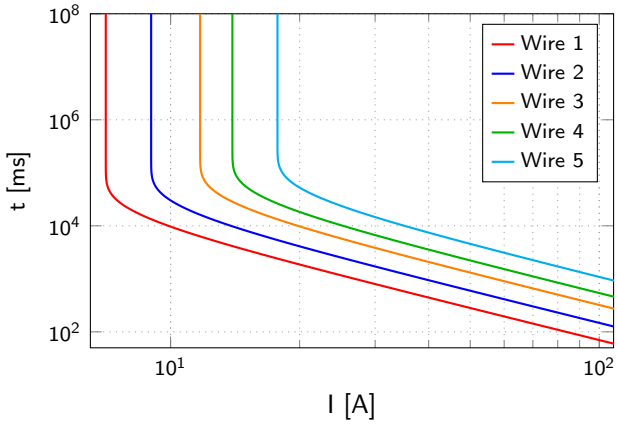


Figure 2.4: Time vs. current wire characteristics with $\Delta T_c = 25\,^{\circ}\mathrm{C}$ [20], [22].

- Typical voltage supply: $3.15\,\mathrm{V} \pm 10\%$
- Data rate, i.e. what is the I_{load} expected reading-request frequency: [10-100 KHz]
- The input signal is expected to vary slowly
- Digital output to be provided in parallel (it would be nice to have also a corresponding analog output)
- Accuracy of the reference voltages/currents vs. Process, Voltage and Temperature (PVT) variations:
  - Voltage:
    - $\pm 2\%$ vs. Temperature
    - $\pm 5\%$ vs. Process
  - Current:
    - $\pm 2\%$ vs. Temperature
    - $\pm 4\%$ vs. Process
- Available clock: $5\,\mathrm{MHz} \pm 20\%$
- Power transistor (high-side switch) on-resistance $R_{on} = 3\,\mathrm{m}\Omega$ @ 300 K
- Accuracy should be achieved without a trimming process.

These design constraints are typical for an electronics design for the automotive application. It is worth remarking on the last point that it implies avoid the use of memories for the trimming as they could be impractical for a BCD power-optimized technology, especially in terms of area usage on the chip.

Chapter 3

Concept

3.1 Introduction

In this Chapter the concept of the multi-functional system implementing current measurements, open-load detection and thermo-electrical stress protection is presented.

From the introductory Chapter it is clear that the design ought to be based on an ADC, especially considering that the output data need to be processed in order to get the temperature estimation.

The selection of an ADC is a critical process as it involves e deep understanding of the system requirements in order to find the better tailored solution for the specific application. There are plenty of converters available in literature and the process of selection can be simplified by means of a check-list, organized by importance. The check-list used in this design is the following:

1. What is the required level of system accuracy?
2. How many bits of resolution are required?
3. What is the nature of the analog input signal?
4. How fast must the converter operate (conversion speed)?
5. What are the environmental conditions?
6. What type of digital output format is required?
7. What are the timing conditions?

This list needs to be checked considering both the requirements (Section 2.1.2) and the design constraints (Section 2.1.4).

3.1.1 System accuracy and resolution

Based on the accuracy requirements provided in Subsection 2.1.2 Point 2iii the resolution should be set to measure the lowest current value 100 mA. Considering that the full scale is 100 A this would lead the ADC number of levels N to be

$N = 100\,\text{A}/100\,\text{mA} = 1000$, which would require a resolution n of *at least* 10 b.

A first trivial approach is to use a full 10 b ADC. However this solution would provide a large accuracy also where not required by the specification at the cost of a large sizes [23]. Another approach is a logarithmic-scale ADC which would provide higher resolution only on the lowest values. A drawback of this implementation is that it would require a non-linear ADC which also could only be implemented at the cost a of high area consumption [24].

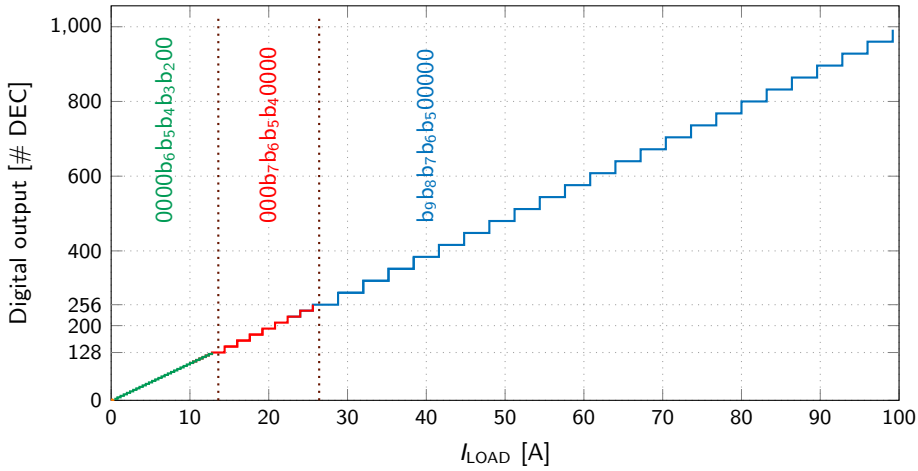
With a more careful requirements analysis, it could be noticed that the current measurement functionality requires ±8% accuracy around $I_{\text{load},5} = 5\,\text{A}$, which is in terms of absolute error ±0.25 A. For $I_{\text{load}} = 100\,\text{A}$ the required accuracy is again ±8% which is in terms of absolute error ±8 A. On the other hand, the 100 mA resolution level is required only for $I_{\text{load}} = [0\,\text{mA} - 400\,\text{mA}]$ but not necessary for higher current values.

These accuracy specifications differences imply different quantization levels according to the value of I_{load}, allowing therefore not using a full 10 b ADC for the measurements but rather having different resolutions for different I_{load}. In particular it is reasonable to address around $I_{\text{load},5}$ approximately ±2.5% budget for the quantization error, which leads to 8 b resolution (with respect to the full scale) for $I_{\text{load}} = [1\,\text{A} - 13\,\text{A}]$. For larger values this specification may be relaxed, leading to 5 b for $I_{\text{load}} = [13\,\text{A} - 100\,\text{A}]$. On the other hand for the lowest current values $I_{\text{load}} = [0\,\text{mA} - 400\,\text{mA}]$ the resolution with respect to the full scale is set to 10 b. To summarize:

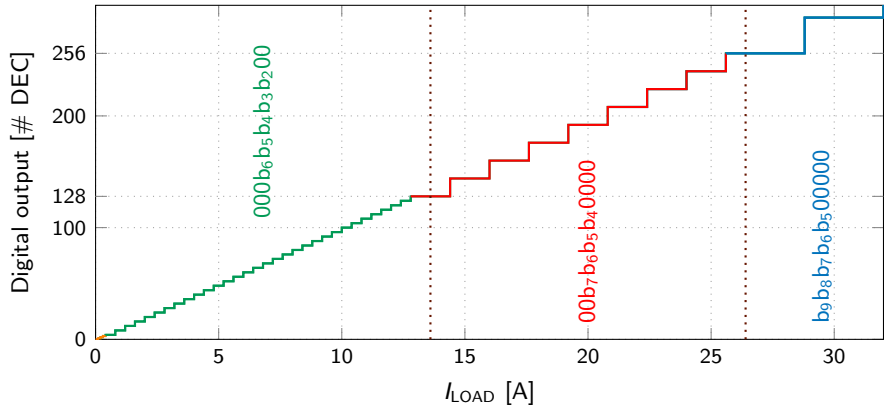
- 10 b (finest) resolution for $I_{\text{load}} = [0\,\text{mA} - 400\,\text{mA}]$
- 8 b (fine) resolution for $I_{\text{load}} = [1\,\text{A} - 13\,\text{A}]$
- 5 b (coarse) resolution for $I_{\text{load}} = [13\,\text{A} - 100\,\text{A}]$

This concept is depicted in Fig. 3.1, where in Fig. 3.1a the conversion plot for the full I_{load} range is shown, in Fig. 3.1b for $I_{\text{load}} = [0\,\text{A} - 30\,\text{A}]$ and in Fig. 3.1c for $I_{\text{load}} = [0\,\text{A} - 1.2\,\text{A}]$. The coarse resolution is represented by the blue line, the fine one by the green line and the finest one by the orange one. There is also an intermediate range between the the fine and the coarse resolution introduced because a 10% quantization error would affect the system when switching between 5 b and 8 b resolutions due to the abrupt transition. The middle steps go from $I_{\text{load}} = 12.8\,\text{A}$, corresponding to the digital output word 128 (in decimal) to $I_{\text{load}} = 25.6\,\text{A}$, corresponding to 256 with 7 b resolution. In this way the quantization errors at both the switching values are reduced from 10% to 5.6%.

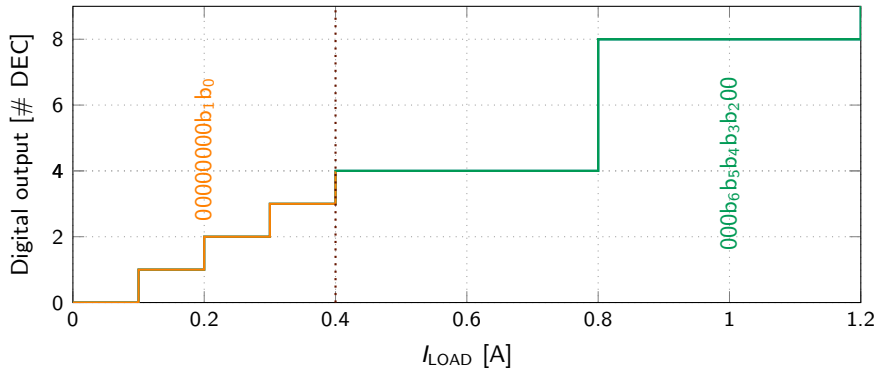
The transition values have been designed to use at most 5 out of 10 bits available at each range. In fact, in the first range the 2 LSB's are used, in the second and the last range 5 bits and in the intermediate one 4 out of 8. This solution allows



(a) I_{load} full input range $[0\,\text{A} - 100\,\text{A}]$.



(b) I_{load} zoomed-in range: $[0\,\text{A} - 32\,\text{A}]$.



(c) I_{load} range further zoomed-in range: $[0\,\text{A} - 1.2\,\text{A}]$.

Figure 3.1: Triple-ranged ADC concept plot.

reducing the logics complexity as digital operations operate at most on 5 bits as well as relaxing the analog design as explained in Chapter 4.

3.1.2 ADC topology choice

This Section goes through the most common ADC architectures available in literature which are analysed according to the most relevant aspects of the applications and the design environment. The different topologies considered are listed in the first column of Table 3.1 [25].

The ADC choice must take into account the characteristic of the input signal and the required output format. Section 2.1.4 provides information on the input signal, in particular:

1. Data rate, i.e. what is the I_{load} expected reading-request frequency: [10-100 KHz]
2. The input signal is expected to vary slowly
3. Digital output to be provided in parallel (it would be nice to have also a corresponding analog output)

Generally every ADC is able to provide an analog output if cascaded with a DAC. However the digital-to-analog converter can be embedded in the tracking ADC without the need of additional blocks, simplifying therefore the system.

The system needs to be robust as it operates in an automotive environment, which is polluted with various interfering signals, as reported in Section 1.2. The input signal needs then to be filtered from unwanted signals. Both the [25] and the tracking ADC (explained in Section 3.2) topologies can provide such a feature built in the system.

The topology choice must consider that the used technology is not specifically tailored for high-accuracy applications. In this scenario it is preferable to use a Nyquist sample frequency ADC (SAR, the pipeline and the tracking ADC's) instead of an oversampling ADC ($\Sigma\Delta$ ADC) which would requires the internal blocks, like operational amplifiers and comparators to operate at much higher frequencies than the Nyquist counterparts, pushing consequently the internal blocks speed specifications. Moreover a relatively simple solution in terms of analog and digital blocks is preferable. In this regards the tracking ADC is the most convenient as it is the less demanding in terms of internal block complexity. In fact it only requires a current steering DAC, a comparator and an up/down counter.

The above-mentioned considerations are summarized in Table 3.1. It could be noticed that for this application the best candidate is the tracking ADC, which working principle is explained in the next Section.

Table 3.1: ADC's comparison matrix

ADC Topology	Criteria			
	Analog output	Input filtering	Sampling frequency	Semplicity
SAR	+	−	+	+
ΣΔ	+	++	−	−−
Pipeline	+	−	+	+
Tracking	++	++	+	++

3.2 Tracking ADC

3.2.1 General counter ADC

The counter-type ADC typical scheme is shown in Fig. 3.2. The counter is reset with the DAC output zero. With *In* non-zero the comparator produces an output to open the AND gate, the counter counts clock pulses and the DAC gives output which increase by one counter. The process continues until the DAC output equals *In*, at which instant the comparator output flips and close the AND gate, the counter is reset to zero and the N-bit counter output is stored in the register. The DAC output increase at each step is given by the ADC LSB, which depends on the number of bit *N*. The number of counts is proportional to *In* and for every sampling interval the DAC output follows a ramp fashion [26].

Fig. 3.3 shows the counter ADC conversion waveforms, with the input on the top (blue line) and the digital output on the bottom (red line). The golden line is the counter output which is reset and stored in the register when the DAC output equals the input *In*. The time between updates (new digital output values) changes depending on how high the input voltage is. For low signal levels, the updates are rather close-spaced. For higher signal levels, they are spaced further apart in time

The counter-ADC is fairly simple to design because of its less complexity. However

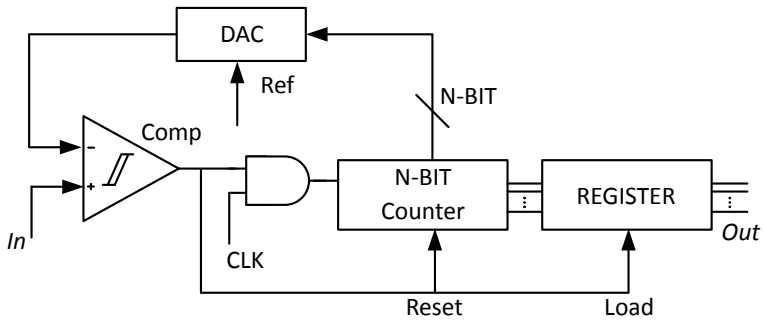
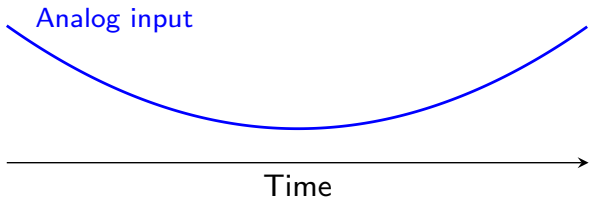
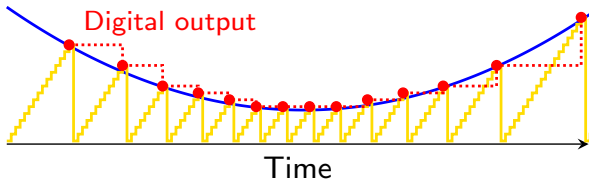


Figure 3.2: Scheme of the counter-type ADC.



(a) Analog input.



(b) Digital output

Figure 3.3: Counter ADC conversion waveforms [27].

it is disadvantageous because every time the counter has to start from zero and the output rate is not regular.

3.2.2 Tracking ADC description

In counter type ADC, the counter goes to zero for every conversion which is a disadvantageous with respect to high conversion time.

In this application the input analog signal is continuous in amplitude with respect to time and the difference between the two sampled analog values is expected to be small. Therefore, in order to speed-up the conversion, after the first analog sample (when the DAC output equals the input *In*) the counter has to be stopped there instead of being reset. This can be achieved if in place of a regular "up" counter driving the DAC , the circuit uses an up/down counter. The counter is continuously clocked, and the up/down control line is driven by the output of the comparator. So, when the analog input signal exceeds the DAC output, the counter goes into the "count up" mode. When the DAC output exceeds the analog input, the counter switches into the "count down" mode. Either way, the DAC output always counts in the proper direction to *track* the input signal [27].

The tracking ADC typical scheme is shown in Fig. 3.4. It could be noticed that no shift register is needed to buffer the binary count at the end of a cycle. Since the counter's output continuously tracks the input (rather than counting to meet the input and then resetting back to zero), the binary output is updated with every clock pulse.

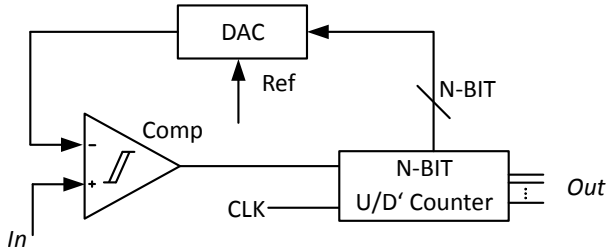
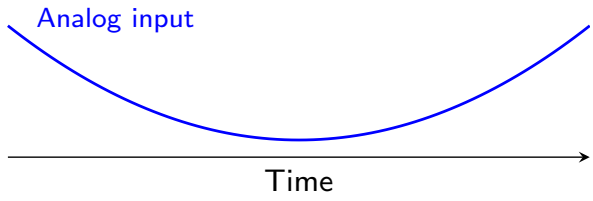
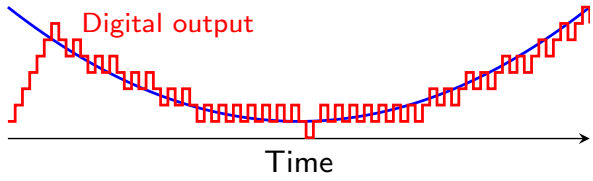


Figure 3.4: Scheme of the tracking ADC



(a) Analog input.



(b) Digital output

Figure 3.5: Tracking ADC conversion waveforms [27].

An advantage of this converter circuit is speed, since the counter never has to reset. Fig. 3.5 shows the counter ADC conversion waveforms, with the input on the top (blue line) and the digital output on the bottom (red line).

The update time is much faster with respect to the basic counter-type ADC (Fig. 3.2), expect for the beginning where the DAC needs to match the analog and output rate change is identical to the counter-type. Also, with no shift register in this circuit, the binary output would ramp up rather than jump from zero to an accurate count.

The major drawback to this ADC design is the fact that the binary output is never stable: it always toggles between counts with every clock pulse, even with a perfectly stable analog input signal. This phenomenon is informally known as

bit bobble, and it can be problematic in some digital systems. However in the application of interest this is not an issue as an averaging is performed on the output, halving therefore the quantization error.

Considering the conversion waveform in Fig. 3.5b, the tracking ADC would be suitable with the characteristics of the input signal, especially knowing that it is expected to vary slowly and this converter would be able to nicely follow (*track*) it.

In case of an interfering pulse appearing at the input, the ADC would reject it as it is not able to follow such a fast signal. This characteristic make this ADC topology inherently robust against this type of external interferers.

The generic scheme proposed in Fig. 3.4 needs to be adjusted according to the fact that the input signal is a current and that a normal up-down counter would not be able to provide the triple-ranged conversion characteristic depicted in Fig. 3.1.

Next Section describes the conversion block which is the base of the multi-functional system.

3.3 ADC concept

Fig. 3.6 shows the ADC base on which the multi-function concept is built. The input current I_{load} is flowing in the right-hand branch throw the Power Resistor (PT), which is part of an high-side load switch architecture (Fig. 1.3). On the left-hand branch there is a PT scaled replica, smaller by a factor $1/20\,\text{k}$; both transistors are kept in linear region by the Gate Driver. Because of the sizes scaling, the PT replica on-resistance R_{s} is $20\,\text{k}$ times larger than the PT resistance R_{l}. The relationship between the currents and the voltages is described by Equation (3.1a) and (3.1b).

$$V_{\text{l}} = V_{\text{DD}} - I_{\text{load}} \cdot R_{\text{l}} \tag{3.1a}$$

$$V_{\text{s}} = V_{\text{DD}} - I_{\text{sense}} \cdot R_{\text{s}} \tag{3.1b}$$

According to Equations (3.1a-3.1b), if $V_{\text{l}} = V_{\text{s}}$ then the current I_{sense} is a scaled-down by a factor $20\,\text{k}$ replica of the current I_{load}. The scaling is implemented because it is not possible to process I_{load}, which ranges form $0\,\text{A}$ to $100\,\text{A}$, directly within low-power CMOS circuitry. With the given $20\,\text{k}$ ratio, I_{sense} range reduces to $[0\,\text{mA} : 5\,\text{mA}]$ which is much easier to handle.

Referring to Fig. 3.6, the loop composed of the comparator (Comp), the ADC

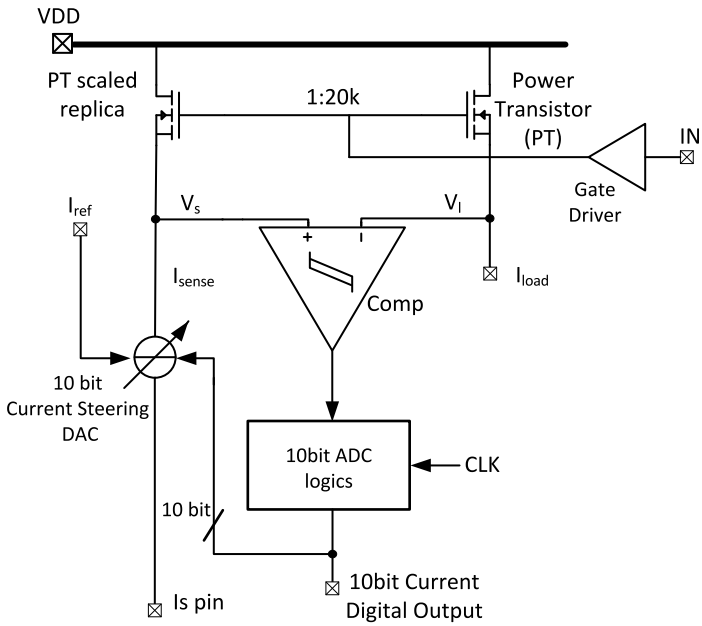


Figure 3.6: Scheme of the basic ADC concept.

logics and the current steering DAC serves the purposes of indirectly compare and equal (considering the scaling factor) the two currents by means of the voltages V_s and V_l. According to Equations (3.1), if $V_\mathrm{s} > V_\mathrm{l}$ then I_sense needs to be increased and vice-versa. The comparator output is fed into the 10 b ADC logics, which is based on an up/down counter. The logic drives the current steering DAC (i.e. a digitally controlled current source with an external reference current I_ref) which adjust I_sense by one current step at each clock (CLK) period. Since the system is following the input analog signal, this loop implements a tracking ADC solution.

Considering $R_\mathrm{l} = 3\,\mathrm{m\Omega}$, and $V_\mathrm{DD} = 3\,\mathrm{V}$, the relationship between the currents and the voltages ranges is:

$$I_\mathrm{load} = [0\,\mathrm{A} : 100\,\mathrm{A}] \quad \mapsto \quad V_\mathrm{s} = [3\,\mathrm{V} : 2.702\,\mathrm{V}] \tag{3.2a}$$

$$I_\mathrm{sense} = [0\,\mathrm{mA} : 5\,\mathrm{mA}] \quad \mapsto \quad V_\mathrm{l} = [3\,\mathrm{V} : 2.702\,\mathrm{V}] \tag{3.2b}$$

V_l and V_s ranges are equals as the currents scaling is inversely proportional to the resistances scaling.

Referred to the V_DD, the voltage range becomes:

$$V_\mathrm{s,l,DD} = V_\mathrm{DD} - V_\mathrm{s,l} = [0\,\mathrm{mV} : 298\,\mathrm{mV}] \tag{3.3}$$

An important feature of this concept is the possibility to have both a digital and

an analog representation of the input signal. The output binary code is provided directly by the up-down counter. The analog output can be read at the I_s pin as a quantized and scaled-down version of I_{load}. This would allow a front-end having more flexibility—and possibly a control feedback with a double-checking—when reading the data provided by the converter.

3.4 Open-load feature

The open-load detection functionality shall be activated whenever a possible current smaller the minimum measurable value by the ADC (i.e. the LSB) is detected. In this case, the system is required to distinguish if the current is indeed 0 A or larger than a programmable open-load currents. In the latter case, the system shall output the open-load event. The system that implements this feature should be following the operations depicted in the flow charts in Fig. 3.7.

The diamond-shaped blocks represent a decision, which is basically a comparison between a value processed by the system and a reference. The rectangle-shaped blocks indicate a specific value setting. For the sake of simplicity, the controls performed by the logics (i.e. overflow control and different resolution driving) are omitted.

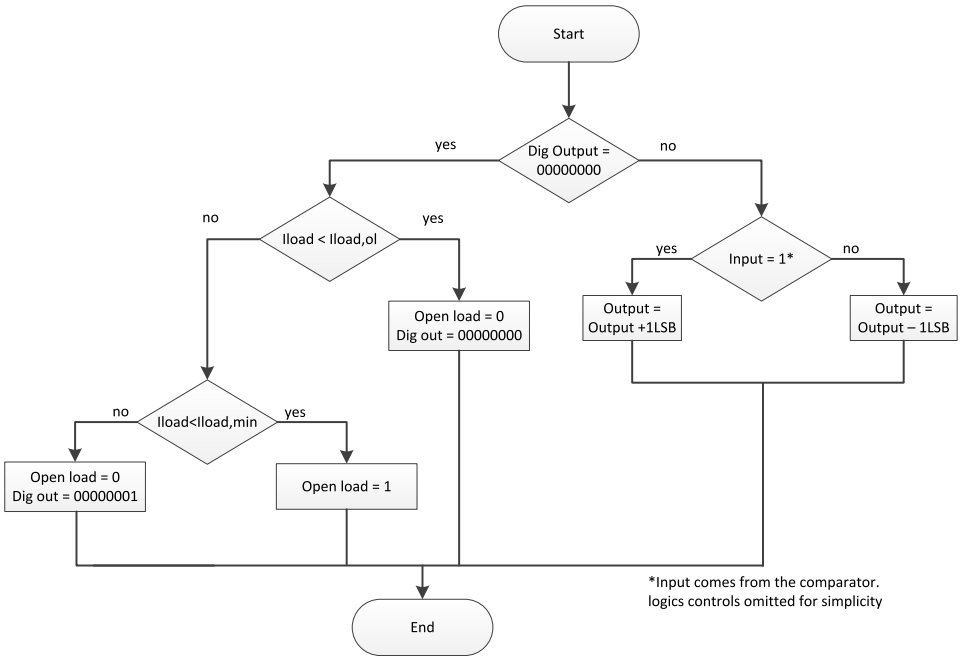


Figure 3.7: System flow chart.

In the first place, the system needs to digitally check if the binary output coming from the ADC is 0. If not (right-hand path), then the system follows up with the normal tracking conversion by processing the output of the comparator with the up/down converter. If yes (left-hand path), the open-load detection is activated. The comparator check if I_{load} is smaller than the open-load threshold current $I_{\text{OL,th}}$. If yes, than there is no open-load current therefore the digital output is indeed 0. Else, the I_{load} is compared with a reference equal to the minimum possible load-current value. If $I_{\text{load}} < I_{\text{load,min}}$ then the load-current is between the threshold and the minimum possible load-current and therefore the open-load is detected, otherwise the I_{load} is at least larger than $I_{\text{load,min}}$, and therefore the digital output is set to 1. The last comparison might appear redundant as it has already been checked if I_{load} was smaller than $I_{\text{load,min}}$, however since the very first comparison until the last one the input current might have been changed. Therefore the double-check is a safe way to avoid false positives.

Considering the two possible open-load currents $I_{\text{load,OL}}$ to be $20\,\text{mA} \pm 8\,\text{mA}$ and $60\,\text{mA} \pm 8\,\text{mA}$ it is reasonable to the the set the threshold currents $I_{\text{OL,th}}$ as defined in Equations (3.4).

$$\begin{aligned} I_{\text{load,OL1}} = 20\,\text{mA} \quad &\mapsto \quad I_{\text{load,th1}} = 10\,\text{mA} \\ I_{\text{load,OL2}} = 60\,\text{mA} \quad &\mapsto \quad I_{\text{load,th2}} = 50\,\text{mA} \end{aligned} \tag{3.4}$$

3.5 System concept

Fig. 3.8 shows the scheme of the full system concept. With respect to Fig. 3.6, the blocks implementing the open-load detection (in red) and the temperature estimation (in orange) have been added.

Referring to the flow chart in Fig. 3.7, during the normal current measurement operation (right-hand path) only the black blocks are used and the switch Sw is in position b. In particular, the 20 K ratio transistors are used to compare V_{s} and V_{s} and D1 is used to generate the quantized I_{sense} current. Moreover during this phase, the temperature is continuously estimated by a digital block (orange) by processing 5 out of the 10 bit provided by the ADC. This operation is better explained in Chapter 7.

During the open-load detection operation, the switch Sw is in position a. In this phase I_{load} needs to be compared with one of the two thresholds defined in Equations (3.4). Comparing such small currents might prove challenging in terms of design if using D1, especially considering the level of resolution required (theoretically 10 mA over the full-scale 100 A would require 5000 quantization levels, i.e. a 13 b ADC). It is obvious that this kind of resolution is not needed for all of the input

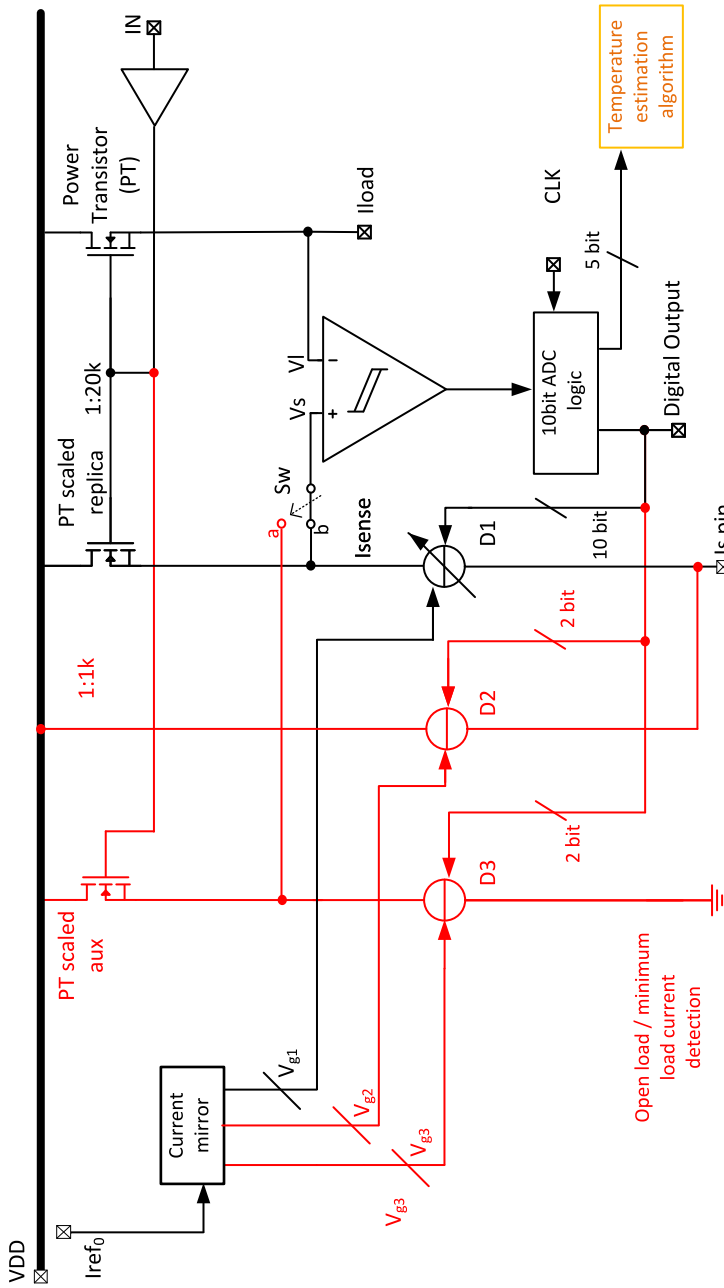


Figure 3.8: Scheme of the full munti-functional system. Based on [28].

range, therefore the same considerations described Section 3.1.1 apply. However in this instance the current that D1 would generate is not a scaled-down replica of I_{load}, but rather a scaled-down version of the threshold currents $I_{\text{OL,th}}$. This means that the current flowing into the I_s pin would not represent the current I_{load} and this shall be avoided as it would provide incorrect information to a possible read-out system connected to this pin.

A possible solution is to use two auxiliary DACs, namely D2 and D3, both digitally driven and activated only on the open-load detection operation.

D3 is designed to provide the three possible currents used for the two comparisons on the left-hand path of Fig. 3.7: the two $I_{\text{OL,th}}$ and $I_{\text{load,min}}$. Since the possible currents are three and an enable bit is necessary, this DAC needs to be controlled by 2 bit provided by the ADC logics.

D3 is connected on the top-side to an auxiliary scaled-down power transistor with a 1 k ratio with respect to the the main PT. This is solution is adopted in order to relax the DAC design for the currents comparison as larger currents are generally less sensitive to variations (this is clear if one thinks to two current mirrors with the same sizes: the one with lower current exhibits the smaller overdrive voltage, and therefore it is more sensitive to the transistors threshold-voltage spread). With this solution the current to be provided by D3 are 10 µA, 50 µA and 100 µA instead of 0.5 µA, 2.5 µA and 5 µA.

On the bottom-side D3 is connected to a ground-related pin so to have the current generated by this DAC not flowing into the I_s pin.

The DAC D2 activates only when an open-load current in indeed detected and its function is to provide to the I_s pin a scaled-down by 20 K version of the current flowing on the I_{load} side. Since this DAC is not used to perform any comparison, it is not required to be as accurate as D3 and therefore its design may be relaxed. When enabled, it generates one of the two programmable open-load current down-scaled by 20 K , i.e. either 0.5 µA or 2.5 µA. D3 requires 2 b to be driven: one for the current selection and one for the enable.

In the next Chapter the transistor level design is presented, showing the methodology used starting from the system model and the block specifications definition.

Chapter 4

System level design

4.1 Introduction

The system design includes the steps that lead to the transistor level implementation. The flow used in this work is the following: first a 5 b ADC has been implemented in order to gain familiarity with the BCD technology so to understand its characteristics when used for an high-precision signal processing blocks. It should be noticed that a 5 b ADC cannot possibly fulfil the system accuracy specifications, as its quantization error alone around 10 A is approximately 12%.

Once the 5 b ADC has been design and validated, an 8 b ADC has been implemented for the purpose of increasing the system accuracy and fulfil the accuracy requirements for $I_{\text{load}} = 10\,\text{A}$. Finally the entire 10 b ADC has been built together with the open-load detection and temperature estimation features. This last part is more related to the logics design and the implementation of the digital algorithms.

4.2 Development of the 5b ADC

The concept used for the 5 b ADC is the same as the one shown in Fig. 3.6, with the only difference being the resulting resolution (5 b instead of 10 b). Every block in the scheme needs to be specifically designed in a way to meet the overall objective. Therefore in the first place the specifications for each functional blocks in the system must be developed.

A typical flow chart of the design process of an individual block is shown in Fig. 4.1. The process is iterative and the larger the number of the blocks the more cycles might be needed. Similar considerations and steps are used to the design of the 8 b and the 10 b ADC.

The system design starts with an estimation of the suitable specifications for the individual blocks. Then the proper implementation is selected for each of them

among the different solutions present in literature, modifying it if necessary. The next step is to verify if the blocks meet the individual specifications earlier set. If they do they are combined together into the system, else the previous two steps need to be retaken. The system performance are then tested and compared with the overall requirements. If they are satisfied the system is completed, otherwise the individual blocks have to be modified or redesigned.

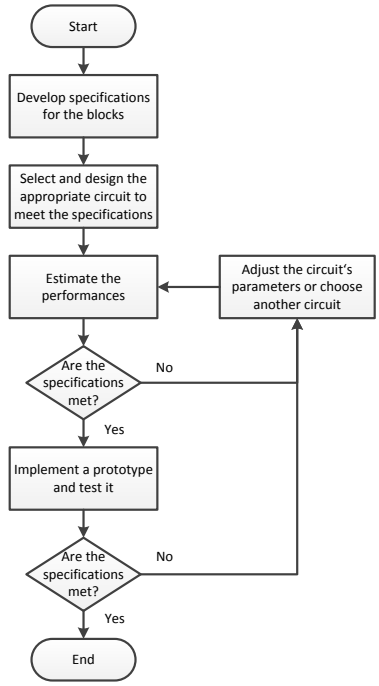


Figure 4.1: Flow chart of the design process [29].

4.2.1 Considerations on the external blocks

The develop of the specifications for the blocks must consider non-idealities affecting the system, which can lead to deteriorated performance if not understood and taken into account early in the design.

The main external non-idealities (i.e. the ones that cannot be reduced by design but can only be carefully taken into account) are due to spread in the geometrical scaling ratio K between the power transistor ant its smaller replica and to the references drift. Usually they are not dependent on the input value, therefore they would not produce non-linear error but rather DC ones, i.e. gain error, off-set error and full-scale error, which is the combination of the two.

Equation (4.1) describes the typical transfer function of the ideal (error-free) ADC

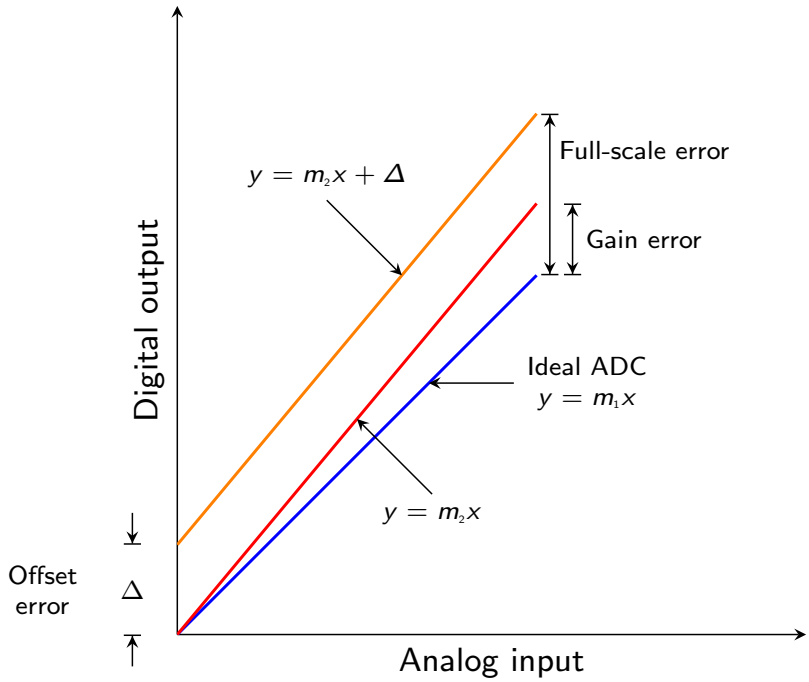


Figure 4.2: Off-set, gain and full-scale errors.

[30], plotted in blue in Fig. 4.2, where the input is V_{in}, the digital output is a Code, the reference is defined as V_{ref} and the number of bit is N:

$$\text{Code} = V_{in} \cdot \frac{2^N}{V_{ref}} \tag{4.1}$$

This equation demonstrates that the ADC output code is directly proportional to the analog input voltage and inversely proportional to the voltage reference. Equation (4.1) also shows that the output code depends on the number of bits (the converter resolution).

If the off-set error is introduced into the transfer function, Equation (4.1) can be rewritten as:

$$\text{Code} = (V_{in} - \Delta) \cdot \frac{2^N}{V_{ref}} \tag{4.2}$$

where Δ is the input off-set voltage of the ADC.

The gain error is equal to the difference between the ideal slope from zero to full scale and the actual slope from zero to full scale. If the impact of only the gain error (no off-set-voltage error) on an ADC is considered, Equation (4.1) can be

rewritten as:

$$\text{Code} = V_{in} \cdot \frac{2^N}{V_{ref}\,(1 - G_e)} \tag{4.3}$$

where G_e is the gain expressed according to Fig. 4.2 as:

$$G_e = \frac{m_2 - m_1}{m_1}$$

From Equation (4.3) it can be seen that the gain-error factor adds to the initial accuracy of V_{ref}. The output code is inversely proportional to the combination of the voltage reference plus the gain error.

Equations (4.2) and (4.3) can be combined to show the final transfer function:

$$\text{Code} = (V_{in} - \Delta) \cdot \frac{2^N}{V_{ref}\,(1 - G_e)} \tag{4.4}$$

According to Equation (4.4), a drift on the references (V_{ref} in this case) produces a gain error.

The error on the ratio K can be seen as current mismatch error between the power transistor and its scaled-down replica. Ideally the two devices work in linear region and $I_{\text{sense}} = I_{\text{load}}/K$, with

$$I_{\text{load}} = \mu\, C_{ox} \frac{W}{L}\,(V_{GS} - V_{th})\,V_{DS} = c\,(V_{GS} - V_{th})\,V_{DS} \tag{4.5}$$

where μ is the carriers mobility, C_{ox} is the oxide capacitance, W and L are the transistors width and length, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, V_{DS} is the drain-source voltage and $c = \mu\, C_{ox} W/L$.

The main sources of mismatch between two transistors are typically due to sizes (W and L) and threshold voltage (V_{th}) spreads. To model these effects, Equation (4.5) can be rewritten as:

$$I_{\text{load}} = c\,\delta_c\,(V_{GS} - (V_{th} + \varepsilon_{th}))\,V_{DS} \tag{4.6}$$

where δ_c represent the sizes mismatch and ε_{th} the thresholds spread. Equation (4.6) can be rearranged as:

$$I_{\text{load}} = c\,(V_{GS} - V_{th})\,V_{DS}\,\delta_c - c\,(\delta_c\,\varepsilon_{th})\,V_{DS} \tag{4.7}$$

The gain error is due only by δ_c ($G_e = \delta_c$), whereas the off-set error is due to both δ_c and ε_{th} ($\Delta = -c\,(\delta_c\,\varepsilon_{th})\,V_{DS}$). The off-set error is non-linear as it depends also on the drain-source voltage. However for the used BCD technology it has been

measured to be negligible, therefore the only effect of the K mismatch is a linear gain error.

4.3 Blocks specifications

Referring to Fig. 3.6, the remaining source of non-idealities other than the K ratio and the references are the DAC and the comparator, whose specifications can be set and implemented by design.

4.3.1 Comparator

The comparator input off-set specification depends on the LSB. Considering the $N = 5\,\mathrm{b}$ resolution and the input full-scale FS to be 100 A, the current LSB on the I_{load} side is:

$$\mathrm{LSB_{IL}} = \frac{FS}{2^N - 1} = \frac{100\,\mathrm{A}}{31} = 3.2\,\mathrm{A}$$

whereas on the I_{sense} side it is down-scaled by 20 K to $\mathrm{LSB_{IS}} = 160\,\mu\mathrm{A}$. According to Equation (3.3), this leads in the voltage domain $\mathrm{LSB_V} = 9.6\,\mathrm{mV}$

The maximum voltage off-set affecting the comparator shall produce an error negligible with respect to the voltage least-significative bit, setting the maximum off-set $V_{\mathrm{os}} \ll 1\ \mathrm{LSB_V}$ around $100\,\mu\mathrm{V}$ to be accomplished within the automotive specifications, i.e. with a $6\,\sigma$ yield and with the temperature ranging from $-40\,^{\circ}\mathrm{C}$ to $150\,^{\circ}\mathrm{C}$.

The comparator IP was already developed by Infineon. The block was designed with an auto-zero scheme, ensuring a 0 V mean input off-set and $27\,\mu\mathrm{V}$ random input off-set at $6\,\sigma$. It is driven with a 625 kHz clock and the current consumption is $80\,\mu\mathrm{A}$. This clock frequency is also the driving the ADC logics and the DAC, as these blocks are synchronised.

4.3.2 DAC

In the following section are described the general specifications which shall be taken into account when designing a DAC [31].

Resolution The DAC resolution is the number of bits used to generate the analog output. For this first design it is set to 5 b.

Conversion Rate Conversion rate is the speed at which a DAC can produce repetitious data conversions at the output. In this case it shall be 625 kS/s

Monotonicity Monotonicity is the ability of the output signal to change in the same direction, or to preserve state for every increase/decrease in the input signal. A monotonic DAC has an analog output that never decreases with an increasing decimal value corresponding to the digital input code, and conversely.

This design shall ensure the overall conversion monotonicity, therefore the DAC is required to provide a monotonic conversion.

Linearity The static behavior of a DAC is described by its transfer characteristic. Static specs can be considered to the DAC's distortion performance at low frequencies. Static DAC performance is characterized by DNL and INL. DNL is a measure of the deviation between the analog output levels corresponding to two successive (in binary value) input codes from the ideal one-least-significant bit step, i.e., DNL expresses the difference between the actual step size and the ideal least-significant-bit step size. It must be noted that one LSB step size corresponds to the minimum voltage or current that a DAC can resolve. INL is a measure of the deviation of the DAC output from the output provided by an ideal straight-line transfer characteristic. INL can also be defined as the accumulated DNL errors. The ideal straight line can be drawn as an endpoint line, passing through the zero and full-scale points (for an N-bit DAC, endpoints are usually given as the analog outputs matching with code 0 and $2^N - 1$), or as a best-fit line to the DAC's actual transfer characteristic. Both DNL and INL are measured in the unit of LSB size. Non-ideal output of a 3 b DAC, illustrating DNL and INL, is shown in Fig. 4.3

For this design the absolute value of the INL shall be set to be smaller than 0.5

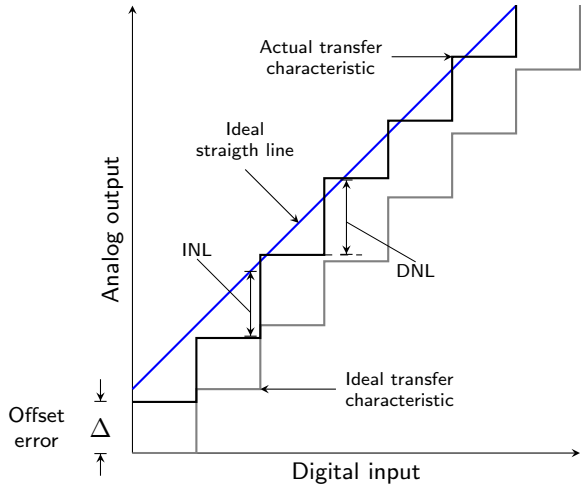


Figure 4.3: Transfer characteristic of a 3 b DAC, illustrating Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) [31].

LSB, as this condition guarantee the DAC monotonicity.

Off-set and gain error For the off-set and gain error, similar considerations to what described in Section 4.2.1 and depicted in Fig. 4.2 apply. These two effects shall be minimized so to fulfil the DAC accuracy requirements, i.e. for this design the shall produce an error smaller than the 3%.

Settling Time The settling time is the time it takes for the analog output to settle within ± 0.2 LSB accuracy of the final value. In this design, the settling time shall be smaller than 1/6 of the clock period, i.e. 0.3 ns.

Chapter 5

Transistor level design of the first ADC prototype

5.1 Transistor level design of the 5b DAC

As stated in the previous Chapter, in the first place a 5 b ADC has been implemented in order to gain familiarity with the BCD technology so to understand its characteristics when used for an high-precision signal processing blocks. The main focus is to design a suitable DAC for the ADC, as the comparator has been already delivered by Infineon.

The current-steering DAC architecture can be implemented using either binary weighted, thermometer-coded (unary) implementations or an hybrid solution.

Thermometric DAC 's uses a single-current element for each quantizations step. They are simple to design and inherently monotonic [25]. However they are not optimal from the area occupation point of view, as they require a decoder between the ADC logics (the u/d counter) and the DAC, which converts thermometer to binary code. The implementation of the digital circuit for the decoder is not efficient in terms of area with the BCD power-optimized technology, therefore implementations including thermometer code should be avoided.

Binary weighted DAC's group current elements into binary multiples that are turned on or off directly with the input bits. This eliminates the decoder required in thermometric DAC's. However, binary DAC's still often use individual unit current sources to make up the larger binary units for matching purposes. Nonetheless in terms of area this solution is estimated to be the most convenient.

The binary DAC is shown in Fig. 5.1. On the left-hand side is placed the Main Cell, which is supplied with the external reference current I_{ref}. On the right-hand side, there are the binary weighted cells driven by the word $b_{0..4}$ provided by the ADC logics. The converter requires N current sources, each twice as much as the

former, with the value of the largest current source equal to $I_{\mathrm{MSB}} = (2^N - 1)I_{\mathrm{LSB}}$ where I_{MSB} and I_{LSB} are the current outputs steered by the most- and least-significant bits, respectively. It should be noted that in Fig. 5.1 $I_{\mathrm{LSB}} = I_{\mathrm{u}}$. The output current for the N-bit binary-weighted current steering is given as:

$$I_{\mathrm{sense}} = I_{\mathrm{u}} \sum_{k=1}^{N} b_k 2^{k-1} \tag{5.1}$$

The matching between current sources affects both INL and DNL. Modeling each current source as a Gaussian random variable [23] with mean I_{u} and variance σ^2, in a full binary architecture the DNL, normalized to the LSB for each transition ($k = 1, ..., 2^N - 1$) between successive codes, is a random variable with variance dependent on k and with a maximum value equal to [32]:

$$\sigma^2_{\mathrm{DNL,\ LSB,\ MAX}}(k) = 4 \cdot 2^N \frac{\sigma^2}{I_{\mathrm{u}}^2} \tag{5.2}$$

in correspondence with the mid-code transition, which is the most critical one in terms of monotonicity [25].

The INL normalized to the to the LSB for each transition ($k = 1, ..., 2^N - 1$) is equal to [32]:

$$\sigma^2_{\mathrm{INL,\ LSB}}(k) = \frac{k\left(2^N - 1 - k\right)}{(2^N - 1)} \frac{\sigma^2}{I_{\mathrm{u}}^2} \tag{5.3}$$

which is maximum for the mid-code. In these expressions the DNL and INL are gain-error and offset-error corrected.

In order to choose the maximum value of variance allowed for the unit current source the INL and DNL yield, defined as the probability that the values of INL(k)

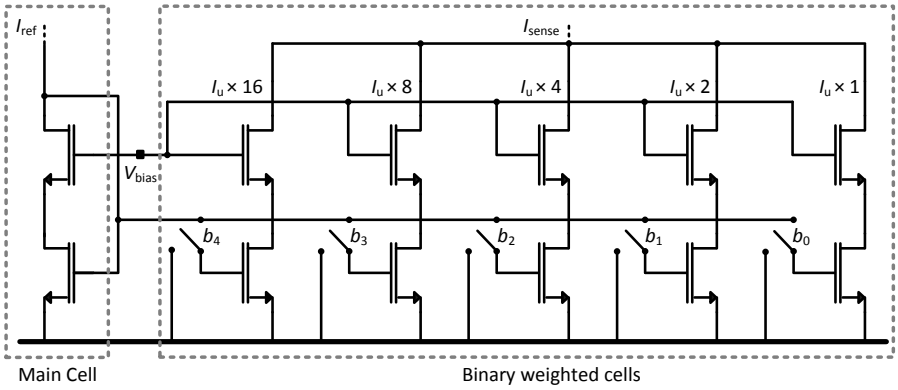


Figure 5.1: Transistor level 5 b DAC.

and DNL(k) are less then 1 LSB for each k, is considered.

The maximum relative variance σ^2/I_u^2 of the unit current source can be obtained with Monte-Carlo simulations in order to have a $6\,\sigma$ yield for both the INL and the DNL. The relative variance of a unit current source (implemented with a MOS transistor in saturation region) depends on its dimensions (W and L) according to the Pelgrom's model [33]:

$$\frac{\sigma^2}{I_u^2} = \frac{1}{WL}\left(A_\beta^2 + \frac{4A_{Vth}^2}{V_{ov}^2}\right) \tag{5.4}$$

where V_{ov} is the overdrive voltage of the transistor, A_β and A_{Vth} are constants typical of the technology used. For a given V_{ov}, the maximum value of the relative variance fixes the minimum area for a unit current source.

The mid-code transition occurs when the 5 b DAC digital input switches from $b_{15} = [01111]$ to $b_{16} = [10000]$, which on the I_{sense} side correspond to the quantized currents levels $I_{sense,15} = 2.40\,\text{mA}$ and $I_{sense,16} = 2.56\,\text{mA}$. In order to have the desired INL and monotonicity for the DAC with the required yield, the I_{sense} standard deviation σ at $I_{sense,15}$ and $I_{sense,16}$ shall be smaller than $\pm 0.5\,\text{LSB}/6$.

5.1.1 Current mirror topology choice

The choice of the topology for the current mirrors composing the DAC needs first of all to consider where it is connected and supplying the current. Referring to the basic concept shown in Fig. 3.6, the DAC is on top connected to the V_s pin whose voltage domain is [3 V : 2.702 V] (defined in Equation (3.2b)) and on bottom to the I_s pin, which is at ground.

The V_s node is a signal node therefore it is necessary to have an high impedance node for the DAC to be insensitive to this node voltage variation. This leads to have a n-MOS based current sources structure, where the high-impedance drain terminals are connected to V_s.

The single-transistor current mirror is still sensitive to the V_{DS} variation due to the channel-length modulation second order effect. Cascoding can be used minimize this effect and to increase the output impedance. In terms of biasing and transistors' operating region this is feasible as the minimum voltage head-room at the node V_s is 2.7 V and the threshold voltages are around 0.8 V.

The wide-swing cascode current mirror [34] has been implemented. It has been preferred with respect to the classical cascode because it features better mismatch performances. In fact, all the transistors sizes and currents being equal, in the wide-swing cascode mirror the drain voltages at the bottom transistors (Fig. 5.1) are one threshold voltage lower than the normal cascode ones, therefore; although

the V_{DS} variation is equal relative terms, in absolute values it is less significant. This allows minimizing the current mismatch due to possible different channel-length modulation effects in the mirror. The downside of this implementation is the necessity to have an additional biasing voltage V_{bias}.

5.1.2 Current mirror dimensioning

The transistors dimensioning has been carried out by optimizing the trade-off area-mismatch expressed by Equation (5.4). The binary cells have been designed based on a single unit able to generate the current I_{u} and each cell multiplicity varies according to its binary weight. This leads having the cell corresponding the LSB (digitally driven by b_0) composed by one unit, the cell for the second-LSB by two units, and so on. For matching purposes the single unit and the main cell transistors have the same size therefore $I_{\text{u}} = I_{\text{LSB}} = I_{\text{ref}}$, setting the reference current at 160 µA.

All of the cells have the following transistors sizes:

- Bottom: $W/L = 12\,\mu\text{m}/4.8\,\mu\text{m}$
- Cascoded: $W/L = 12\,\mu\text{m}/1.2\,\mu\text{m}$

The cascoded devices are four times shorter than the bottom ones in order for them to have twice the transconductance and increase the overall output impedance R_{out} given by:

$$R_{\text{out}} = r_{ds,1} + r_{ds,2} + g_{m,2}\, r_{ds,1}\, r_{ds,2} \tag{5.5}$$

where r_{ds} is the transistors output resistance, g_m is their transconductance and the subscripts 1 and 2 identify respectively the bottom and the cascoded MOS's. The resulting overdrive voltages are $V_{ov,1} = 700\,\text{mV}$ and $V_{ov,2} = 350\,\text{mV}$.

5.1.3 Simulations results

The DAC's layout has bee drawn and the Montecarlo (MC) Post-Layout Simulations (PLS) results are reported in Table 5.1, with different temperature value (it could be noticed that the worst case is with the temperature Temp. $= -40\,^{\circ}\text{C}$). The Bit column represents the digital word driving the DAC expressed in decimal. The values in the mean and σ columns are obtained with the MC analysis and they are compared with the ideal values. The last column represents 6 times the standard deviation normalized to the I_{sense} least significant bit $\text{LSB}_{\text{Is}} = 160\,\mu\text{A}$. It could be noticed that the mean values are in all cases very close to the ideal ones.

Regarding the monotonicity as stated in Section 5.1 the most critical transition is the major-carry transition, that is when switching from bit number 15 to 16. If this transition results in a non-ambiguous conversion, then the monotonicity is

ensured for all of the input-scale. It may be observed the $6 \times \sigma$ values normalized to the LSB to be less than 0.5 LSB. This means that these two values would never overlap ensuring therefore the conversion monotonicity.

Table 5.1: MC PLSs results of the 5 b DAC.

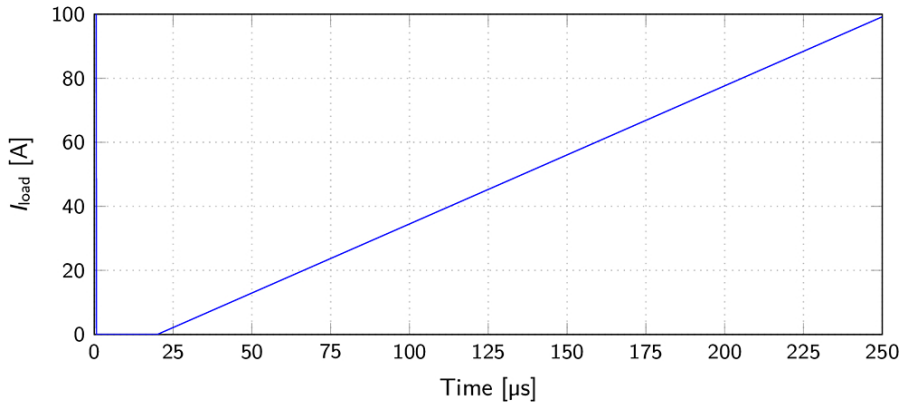
Bit DEC.	Temp. [°C]	Mean [A]	σ [A]	Ideal Value [A]	$6 \times \sigma$ [# of LSB's]
1	−40	1.61E-04	8.06E-07	1.60E-04	0.03
	27	1.61E-04	6.56E-07		0.02
	150	1.60E-04	5.16E-07	(LSB)	0.02
2	−40	3.50E-04	1.36E-06		0.05
	27	1.61E-04	6.56E-07	3.20E-04	0.04
	150	1.60E-04	5.16E-07		0.03
4	−40	3.21E-04	2.42E-06		0.09
	27	3.21E-04	1.96E-06	3.20E-04	0.07
	150	3.21E-04	1.53E-06		0.06
8	−40	1.29E-03	4.59E-06		0.17
	27	1.28E-03	3.74E-06	6.40E-04	0.14
	150	1.28E-03	2.91E-06		0.11
15	−40	2.41E-03	8.40E-06		0.32
	27	2.41E-03	6.85E-06	2.40E-03	0.26
	150	2.40E-03	5.32E-06		0.20
16	−40	2.56E-03	9.09E-06		0.34
	27	2.55E-03	7.44E-06	2.56E-03	0.28
	150	2.55E-03	5.79E-06		0.22

After these analyses, the complete system has been implemented by adding to the layout the logic circuits and the auto-zeroing comparator.

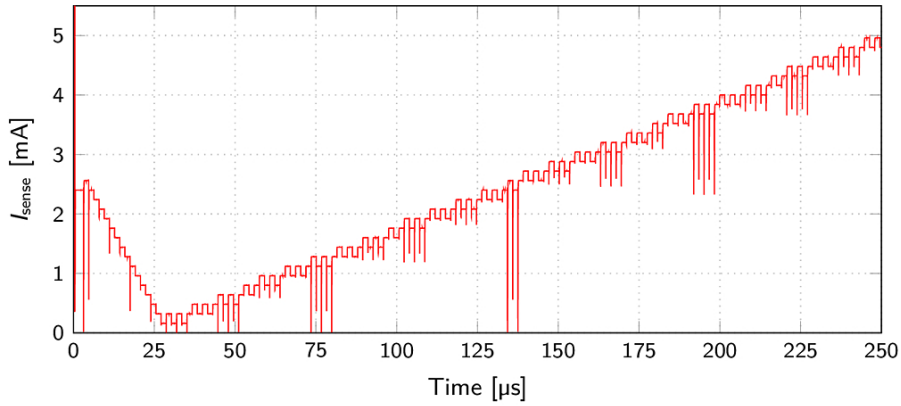
The logics block performs two operations: it implements the 5 b up/down counter whose starting digital value is set to the mid level value $b = 01111$ and it divides the input external clock at 5 MHz as the auto-zeroing comparator needs a driving clock at 625 kHz. The digital block has been implemented in VHDL code and its layout has been automatically synthesized and routed with some specific tools provided in the technology design kit.

A transient analysis has been performed by applying a full-scale input current ramp at the V_l node (Fig. 5.2a). The resulting current flowing into the I_sense node is plotted in Fig. 5.2b. In fig. 5.2c the voltages at the nodes V_s and V_l are shown. At the beginning the conversion starts from the mid-scale values and the system increases the current on the node I_sense (or equivalently it decreases the voltage on the node V_s) by one LSB per clock period until it catches up with the input value. After this point the system starts tracking the load current.

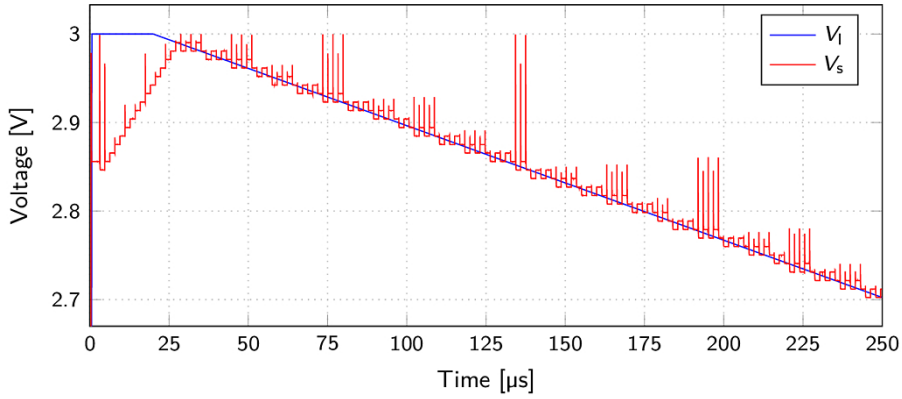
The spikes present in the conversion at each transitions may be unacceptable



(a) Current input I_{load}.



(b) Current output I_{sense}.



(c) Voltage input and output.

Figure 5.2: Input and output characteristics of the 5 b ADC.

in some applications, e.g. in audio systems where they would translate in some audible clicks. In this case however they are negligible as the analog output is only read around the middle of the clock period and not ad the edge of the transitions.

Fig. 5.3 plots the system characteristic in the voltage domain whit a full-scale input sinusoid at 2.5 kHz. As expected from the previous simulations, the system is able to follow the input tone.

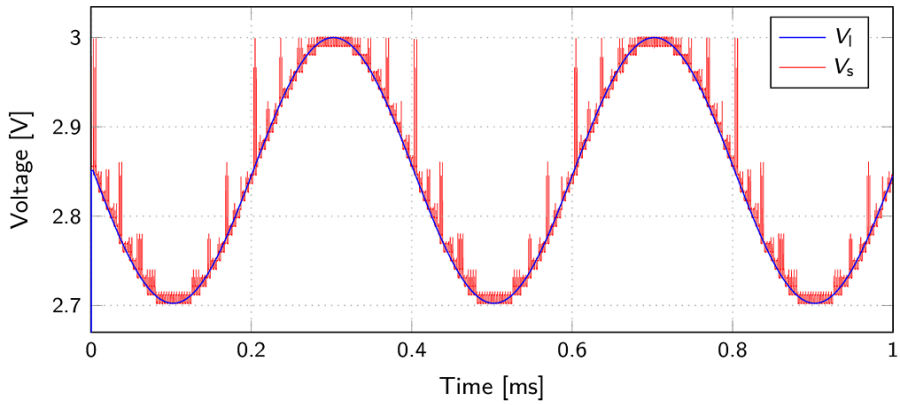


Figure 5.3: Full-scale sines analog input and output characteristics. Input frequency = 2.5 kHz.

Fig. 5.4 plots in the voltage domain the settling time analysis. According to the specification, the output should settle at its final value ±0.1 LSB within 300 ns. The simulation has been performed considering the worst case scenario, i.e. by setting −40 °C environment temperature and by choosing the technology slow corner. Moreover the input has been set around the value corresponding to the major-carry transition, i.e. with the largest number of transistors turning on and off at the same time. The obtained settling time is around 200 ns which satisfies the specification.

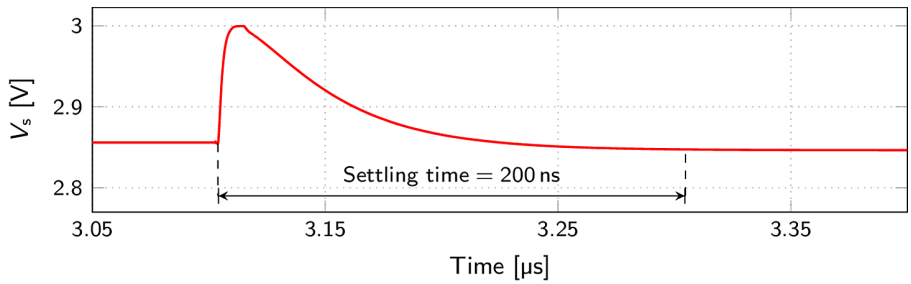


Figure 5.4: Settling time analysis.

5.2 Measurements

The 5 b tracking ADC has been taped-out and a 20 pins ceramic package are used for measurements.

In order to perform the measurements, a PCB has been designed (Fig. 5.5). The external signals provided to the boards are the supply voltage and the ground, the clock and the V_I input signal. The outputs are the 5 b digital word generated by the up/down counter and the V_s node. The reference and biasing currents are locally generated by means of variable resistors whose values is trimmed until the wanted currents are obtained. The enabling and resetting signals can be controlled with some switches soldered on the PCB.

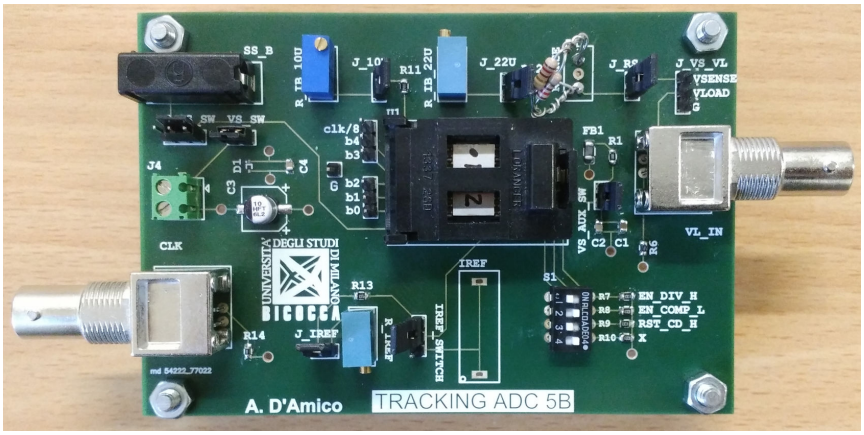
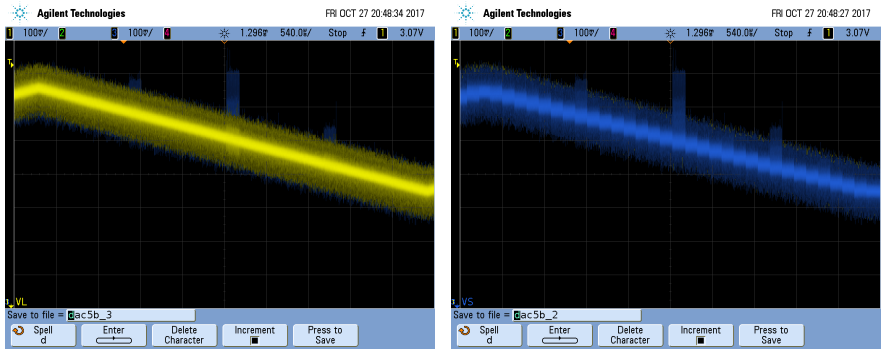


Figure 5.5: PCB for the 5 b ADC measurements.

Measurements have been performed by applying at the V_I input a full-scale ramp ranging from 3 V to 2.7 V, by measuring the V_s pin and reading the 5 b digital output.

Fig. 5.6 shows two screen-shots of the oscilloscope measuring the input ramp (Fig. 5.6a) generated by an arbitrary waveform generator and the output signal (Fig. 5.6b). It could be noticed V_s following the input slope, confirming what observed in the simulations results (Fig. 5.2c).

Fig. 5.7 shows the digital output of the system, read by a logic analyser. The red line is the output digital buffer converted in the decimal scale. The blue line is the V_I voltage which is referred to the voltage supply V_DD for an easier comparison. A portion of the plots is zoomed-in in order to note the digital toggling (*bit bobble*) when the variation on the input side is less than one LSB. From this measurement the monotonic characteristic of the conversion is observed as the output binary word (beside the inherent toggling) increases with the input voltage. Moreover,



(a) Input signal at V_I. **(b)** Output signal at V_s.

Figure 5.6: Oscilloscope measurements.

the A-to-D conversion covers the full-scale.

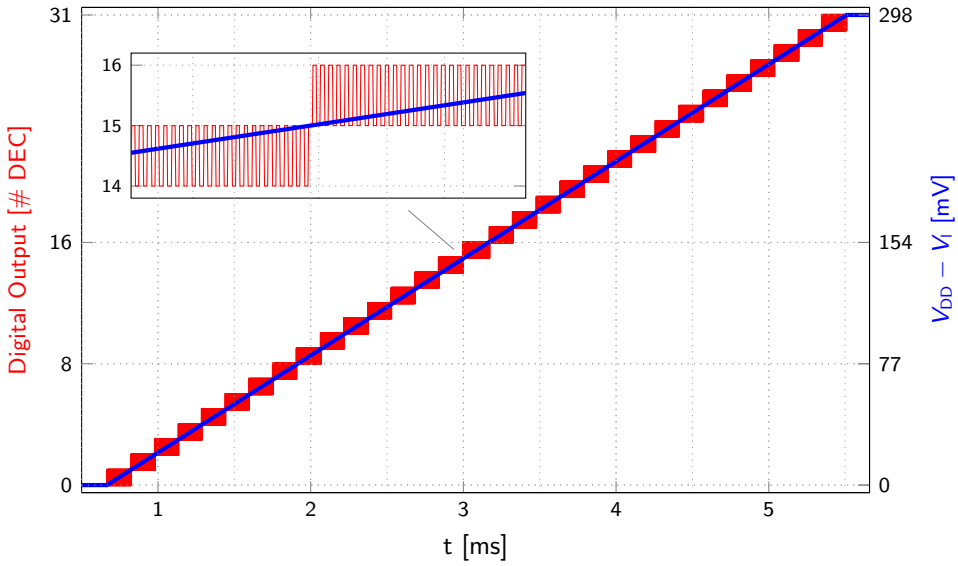


Figure 5.7: Digital output analysis.

Chapter 6

8b ADC design

6.1 8b ADC Concept

After the 5 b ADC design and validation, an 8 b ADC has been implemented for the purpose of increasing the system accuracy and fulfil the accuracy requirements for $I_{\text{load}} = 10\,\text{A}$, but excluding the requirements for the $[0\,\text{mA} - 300\,\text{mA}]$ range, which have been addressed in Chapter 7.

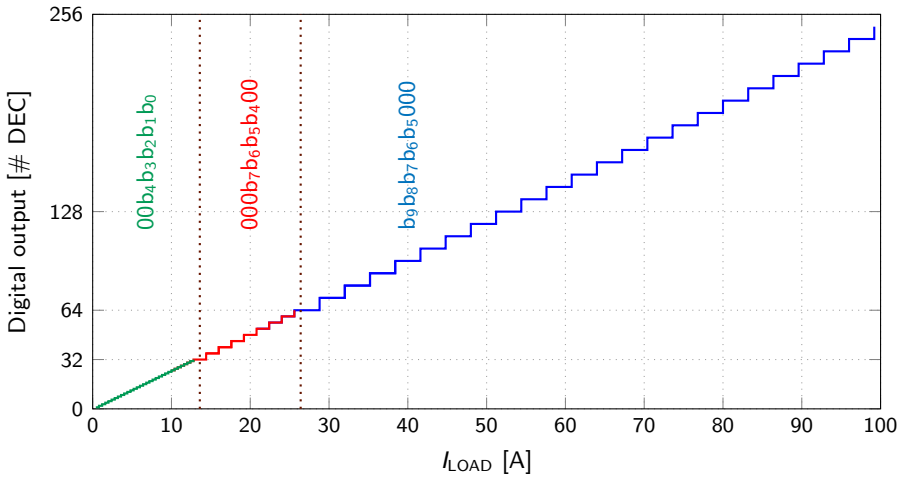
The system design has been carried out in order to exploit the specifications reported in Chapter 2. Two resolutions requirements are present: 5 b for the full range input $I_{\text{load}} = [0\,\text{A} - 100\,\text{A}]$ which are used for the stress-detection feature, and 8 b resolution around $I_{\text{load}} = 10\,\text{A}$. A first trivial approach is to use a full 8 b ADC. However this solution would provide a large accuracy also where not required by the specification at the cost of a large sizes. In fact both of the possible implementations, thermometric and fully-binary weighted, would use large area as they need to be implemented with $2^8 = 256$ matched devices for the DAC [23].

The solution presented in this work consists of a double-ranged ADC which provides the required resolution only when necessary. The core block is represented by the 5 b ADC developed in Chapter 5. Beside it, an additional 3 b ADC has been inserted which works only for limited input values, i.e. $I_{\text{load}} = [0\,\text{A} - 12.4\,\text{A}]$. Within this range, the 3 b and 5 b ADC operate jointly and thus the resolution provided by the system is 8 b.

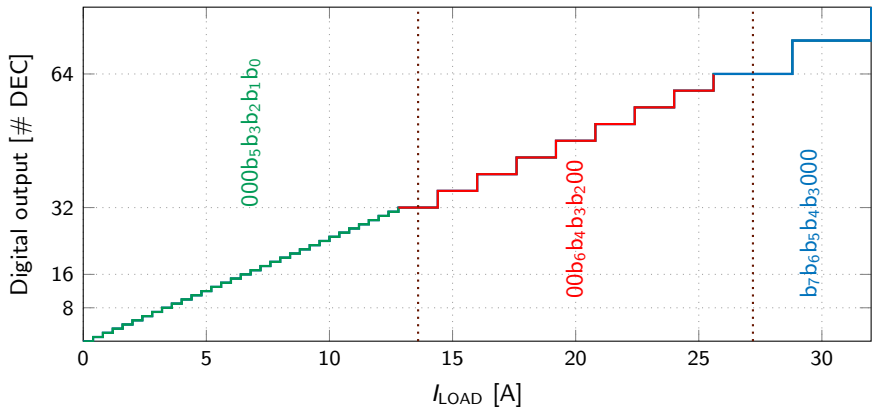
The multi-resolution concept is depicted in Fig. 6.1, where in Fig. 6.1a the conversion characteristic for the full I_{load} range is shown, in Fig. 6.1b for $I_{\text{load}} = [0\,\text{A} - 30\,\text{A}]$. The coarsest resolution (5 b) is represented by the blue line and the finest one (8 b) by the green line. There is also an intermediate area between the two ranges introduced to reduce the 10% quantization error at the ranges transition. The middle steps go from $I_{\text{load}} = 12.8\,\text{A}$, corresponding to the digital output word 32 (in decimal) to $I_{\text{load}} = 25.6\,\text{A}$, corresponding to 64. In this way the quantization

errors at both the switching values are reduced from 10% to 5.6%. The transition values have been designed to use at most 5 out of 10 bits available at each range as could be noticed by the zeros in the three plot labels. This solution allows reducing the logics complexity as digital operations deal only with 5 bits as well as relaxing the analog design.

With respect to a full 8 b converter, which needs $2^8 = 256$ devices for the DAC, the used solution makes use of $2^5 + 2^3 = 40$ devices, saving therefore around 85% of the area.



(a) I_{load} full input range [0 A − 100 A].



(b) I_{load} zoomed-in range: [0 A − 32 A].

Figure 6.1: Double-ranged 8 b ADC concept plot.

Table 6.1 shows for each of the output digital word (expressed both in decimal and binary) the corresponding analog output I_{sense}, the I_{load} value and voltage V_{s} values (expressed both absolutely and referred to V_{DD}). The middle horizontal

Table 6.1: 8 b conversion table

# bit [DEC]	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	I_{load} [A]	I_{sense} [µA]	V_s [V]	$V_{DD} - V_s$ [mV]
0	0	0	0	0	0	0	0	0	0	0	3	0
1	0	0	0	0	0	0	0	1	0.4	20	2.9988	1.2
2	0	0	0	0	0	0	1	0	0.8	40	2.9976	2.4
3	0	0	0	0	0	0	1	1	1.2	60	2.9964	3.6
4	0	0	0	0	0	1	0	0	1.6	80	2.9952	4.8
5	0	0	0	0	0	1	0	1	2	100	2.994	6
6	0	0	0	0	0	1	1	0	2.4	120	2.9928	7.2
7	0	0	0	0	0	1	1	1	2.8	140	2.9916	8.4
8	0	0	0	0	1	0	0	0	3.2	160	2.9904	9.6
9	0	0	0	0	1	0	0	1	3.6	180	2.9892	10.8
10	0	0	0	0	1	0	1	0	4	200	2.988	12
11	0	0	0	0	1	0	1	1	4.4	220	2.9868	13.2
12	0	0	0	0	1	1	0	0	4.8	240	2.9856	14.4
13	0	0	0	0	1	1	0	1	5.2	260	2.9844	15.6
14	0	0	0	0	1	1	1	0	5.6	280	2.9832	16.8
15	0	0	0	0	1	1	1	1	6	300	2.982	18
16	0	0	0	1	0	0	0	0	6.4	320	2.9808	19.2
17	0	0	0	1	0	0	0	1	6.8	340	2.9796	20.4
18	0	0	0	1	0	0	1	0	7.2	360	2.9784	21.6
19	0	0	0	1	0	0	1	1	7.6	380	2.9772	22.8
20	0	0	0	1	0	1	0	0	8	400	2.976	24
21	0	0	0	1	0	1	0	1	8.4	420	2.9748	25.2
22	0	0	0	1	0	1	1	0	8.8	440	2.9736	26.4
23	0	0	0	1	0	1	1	1	9.2	460	2.9724	27.6
24	0	0	0	1	1	0	0	0	9.6	480	2.9712	28.8
25	0	0	0	1	1	0	0	1	10	500	2.97	30
26	0	0	0	1	1	0	1	0	10.4	520	2.9688	31.2
27	0	0	0	1	1	0	1	1	10.8	540	2.9676	32.4
28	0	0	0	1	1	1	0	0	11.2	560	2.9664	33.6
29	0	0	0	1	1	1	0	1	11.6	580	2.9652	34.8
30	0	0	0	1	1	1	1	0	12	600	2.964	36
31	0	0	0	1	1	1	1	1	12.4	620	2.9628	37.2
32	0	0	1	0	0	0	0	0	12.8	640	2.9616	38.4
36	0	0	1	0	0	1	0	0	14.4	720	2.9568	43.2
40	0	0	1	0	1	0	0	0	16	800	2.952	48
44	0	0	1	0	1	1	0	0	17.6	880	2.9472	52.8
48	0	0	1	1	0	0	0	0	19.2	960	2.9424	57.6
52	0	0	1	1	0	1	0	0	20.8	1040	2.9376	62.4
56	0	0	1	1	1	0	0	0	22.4	1120	2.9328	67.2
60	0	0	1	1	1	1	0	0	24	1200	2.928	72
64	0	1	0	0	0	0	0	0	25.6	1280	2.9232	76.8
72	0	1	0	0	1	0	0	0	28.8	1440	2.9136	86.4
80	0	1	0	1	0	0	0	0	32	1600	2.904	96
88	0	1	0	1	1	0	0	0	35.2	1760	2.8944	105.6
96	0	1	1	0	0	0	0	0	38.4	1920	2.8848	115.2
104	0	1	1	0	1	0	0	0	41.6	2080	2.8752	124.8
112	0	1	1	1	0	0	0	0	44.8	2240	2.8656	134.4
120	0	1	1	1	1	0	0	0	48	2400	2.856	144
128	1	0	0	0	0	0	0	0	51.2	2560	2.8464	153.6
136	1	0	0	0	1	0	0	0	54.4	2720	2.8368	163.2
144	1	0	0	1	0	0	0	0	57.6	2880	2.8272	172.8
152	1	0	0	1	1	0	0	0	60.8	3040	2.8176	182.4
160	1	0	1	0	0	0	0	0	64	3200	2.808	192
168	1	0	1	0	1	0	0	0	67.2	3360	2.7984	201.6
176	1	0	1	1	0	0	0	0	70.4	3520	2.7888	211.2
184	1	0	1	1	1	0	0	0	73.6	3680	2.7792	220.8
192	1	1	0	0	0	0	0	0	76.8	3840	2.7696	230.4
200	1	1	0	0	1	0	0	0	80	4000	2.76	240
208	1	1	0	1	0	0	0	0	83.2	4160	2.7504	249.6
216	1	1	0	1	1	0	0	0	86.4	4320	2.7408	259.2
224	1	1	1	0	0	0	0	0	89.6	4480	2.7312	268.8
232	1	1	1	0	1	0	0	0	92.8	4640	2.7216	278.4
240	1	1	1	1	0	0	0	0	96	4800	2.712	288
248	1	1	1	1	1	0	0	0	99.2	4960	2.7024	297.6

lines mark the change of resolution, similarly on what shown in Fig. 6.1 by the colors.

6.2 Development

The 8 b ADC is developed starting from the 5 b ADC designed in the previous Chapter and adapting the block specifications to the new requirements. Fig. 6.2 shows the 8b ADC concept. The same design considerations made in 3 applies also in this case.

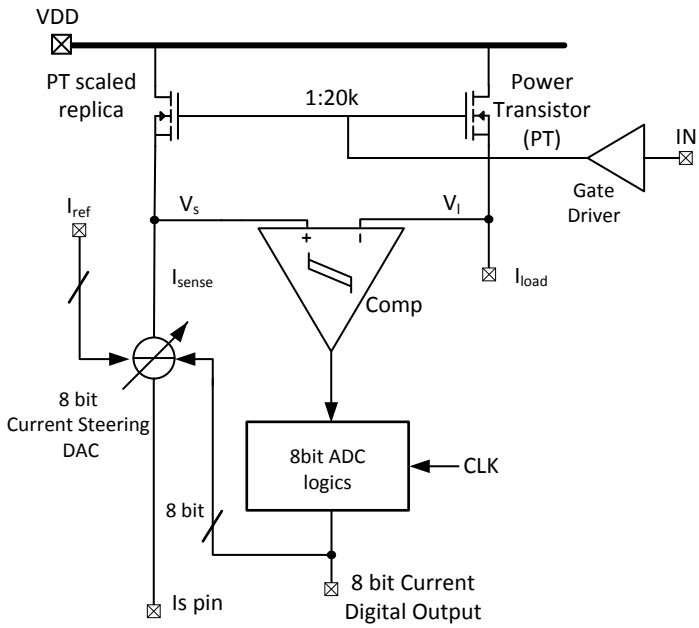


Figure 6.2: Scheme of the 8b ADC concept [28].

6.2.1 Block specifications

Comparator

The comparator input off-set specification depends on the LSB. Considering the $N = 8$ b resolution and the input full-scale FS to be 100 A. The LSB on the I_{load} side is $\text{LSB}_{\text{IL}} = 400\,\text{mA}$ which, according to Equation (3.1),in the voltage domain maps to $\text{LSB}_{\text{V}} = 1.2\,\text{mV}$. The comparator off-set shall therefore be negligible with respect to this value. The Infineon's comparator IP used in the previous scheme provides a 0 V mean input off-set and 27 µV random input off-set at $6\,\sigma$ and therefore can be used again.

DAC

The DAC general specifications reported in Section 4.3.2 shall be satisfied, except the resolution which has to be increased and designed around the concept presented in Section 6.1.

6.2.2 Transistor level design

The main focus is to design a suitable current steering DAC able to provide the required resolution. The core of the block is the DAC implemented for the 5b ADC which still operates with the full-scale input and then add a second DAC which operates for $I_{\text{load}} = [0\,\text{A} - 12.4\,\text{A}]$, corresponding to the two first sections of Table 6.1.

Fig. 6.3 shows the concept of the 8b current steering DAC built with the parallel of the already designed 5b converter and a new 3b one. The 8b driving the current sources are generated by the ADC logic which. A reference current is required for each sub-converter.

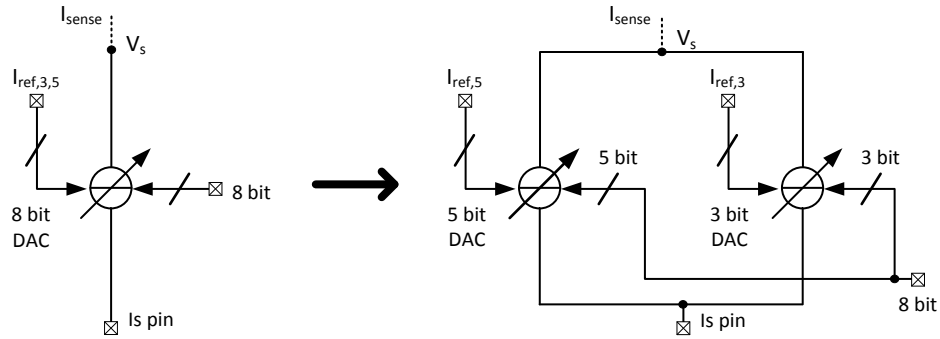


Figure 6.3: 8b current steering DAC concept.

The circuital solution used to implement the 3 b DAC is the same as the one adopted for the 5 b DAC (Fig. 5.1 and it is shown in Fig. 6.4.

Regarding monotonicity this solution needs a more careful design with respect to the 5 b DAC as the most critical points are represented by the transitions between the two DAC's i.e. when passing from bit number 7 to bit 8 and the major carry transition for both the 3 b and the 5 b DAC.

The supplemental 3 b DAC has been designed matching the 5 b DAC with its cells identical to the previous ones and having the following transistors sizes:

- Bottom: $W/L = 12\,\mu\text{m}/4.8\,\mu\text{m}$
- Cascoded: $W/L = 12\,\mu\text{m}/1.2\,\mu\text{m}$

The reference current I_{ref} has been set at the LSB value (20 µA), which is eight

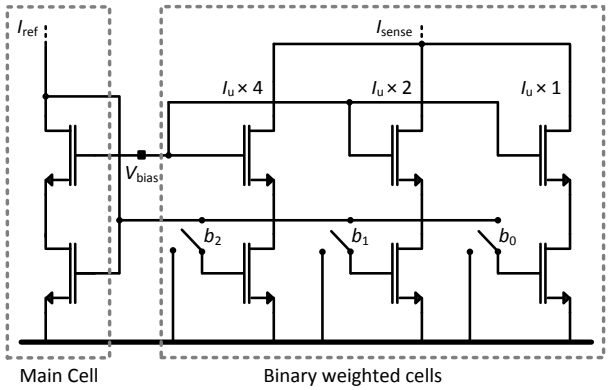


Figure 6.4: Transistor level 3 b DAC.

time smaller than the 5 b DAC one. Given the same transistors sizes, this current is expected to produce overdrive voltages which are $\sqrt{8}$ times smaller than the other converter (reported in Section 5.1.2) and, in fact, the simulated values for the bottom and cascoded devices are respectively $V_{ov,1} = 260\,\text{mV}$ and $V_{ov,2} = 140\,\text{mV}$.

According to Equation (5.4), the 3 b DAC is affected more than the 5 b counterpart by mismatch because of the smaller overdrive voltages. This aspect has been thoroughly taken into account when sizing the transistors.

6.3 Simulation results

The DAC's layout has bee drawn and the Montecarlo (MC) Post-Layout Simulations (PLS) results at $-40\,°\text{C}$ temperature (worst case) are reported in Table 6.2.

Table 6.2: MC PLSs results of the 8 b DAC.

Bit DEC.	Mean [A]	σ [A]	Ideal Value [A]	$6 \times \sigma$ [# of LSB's]
1	2.03E-05	2.40E-07	2.00E-05 (LSB)	0.07
2	4.05E-05	8.43E-07	4.00E-05	0.13
3	6.08E-05	1.81E-06	6.00E-05	0.18
4	8.09E-05	3.14E-06	8.00E-05	0.24
7	1.42E-04	8.85E-06	1.40E-04	0.38
8	1.61E-04	5.61E-06	1.60E-04	0.21

The mean values are very close to the ideal one and sigma results are slightly worse (as expected) than the 5 b DAC. Nevertheless, monotonicity is ensured both within the for the 3 b DAC considering the major carry transition from bit number 3 to 4 and for the DAC switching from bit 7 to 8 as for both of the cases the $6 \times \sigma$ spread is less than 0.5 LSB's.

After these analyses, the complete system has been implemented by adding to the layout the logic circuits and the auto-zeroing comparator.

The logic block performs two operations. It divides the input external clock at 5 MHz as the auto-zeroing comparator needs a driving clock at 625 kHz and it implements the 8 b up/down counter which drives the DAC according to the three possible ranges shown in Table 6.1. In fact, for each of these ranges, the counter increase or decrease is different as it transitions from ± 1 to ± 4 to ± 8. The digital block has been implemented in VHDL code and its layout has been automatically synthesized and routed with some specific tools provided in the technology design kit.

A transient analysis has been performed by applying a full-scale input current ramp at the V_l node (Fig. 6.6a). The resulting current flowing into the I_sense node is plotted in Fig. 6.6b.

In fig. 6.7a the voltages at the nodes V_s and V_l are shown. At the beginning the conversion starts from the mid-scale values and the system increases the current on the node I_sense (or equivalently it decreases the voltage on the node V_s) by one LSB per clock period until it catches up with the input value. After this point the system starts tracking the load current. In Fig. 6.7b the plots are zoomed-in and the transitions among the three resolutions ranges are clearly visible happening around 130 µs and 200 µs. Fig. 6.7c shows the voltage characteristics further zoomed-in on the finest resolution range.

Fig. 6.8a shows the system voltage characteristics when full-scale sine at 1 kHz is applied at the input node, whereas 6.8b shows the characteristics whit an input sine covering only the values in lowest range (corresponding to $I_\mathrm{load} = [0\,\mathrm{A} - 12\,\mathrm{A}]$). As expected from the previous simulations, the system is able to follow the input tones.

6.4 Measurements

The 8 b tracking ADC has been taped-out and a 20 pins ceramic package has been used for measurements.

In order to perform the measurements, a PCB has been designed (Fig. 6.5). The external signals provided to the boards are the supply voltage and the ground, the clock and the V_l input signal. The outputs are the 8 b digital word generated by the up/down counter and the V_s node. The reference and biasing currents are locally generated by means of variable resistors whose values is trimmed until the wanted currents are obtained. The enabling and resetting signals can be controlled with some switches soldered on the PCB.

Figure 6.5: PCB for the 8 b ADC measurements.

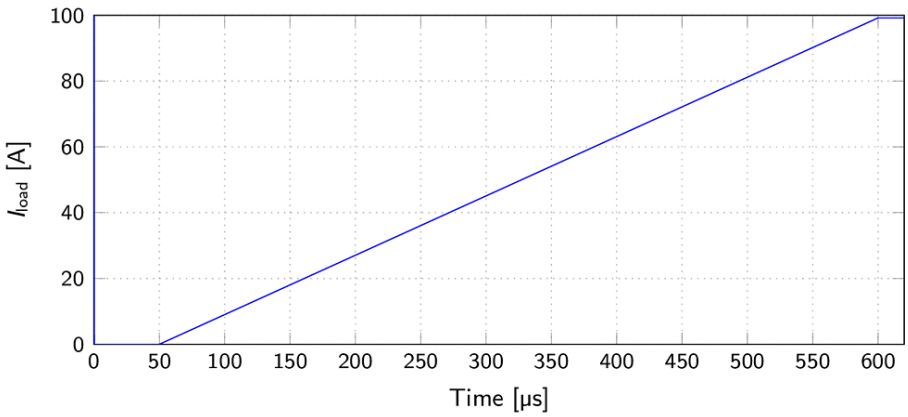
Measurements have been performed by applying at the V_I input a full-scale ramp ranging from 3 V to 2.7 V, by measuring the V_s pin and reading the 8 b digital output.

Fig. 6.9 shows three screen-shots of the oscilloscope measuring at the V_I node the input ramp (yellow line) sourced by an arbitrary waveform generator and the output signal at the V_s node (blue line). In Fig. 6.9a the full-range ADC dynamic is shown.

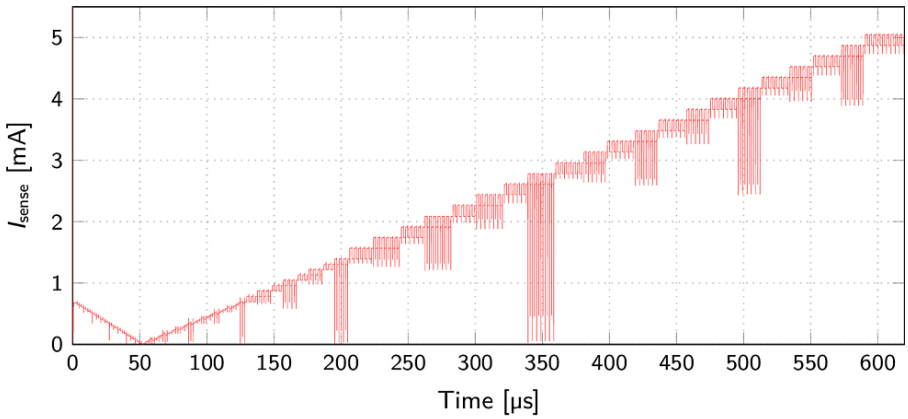
Fig. 6.9b shows the zoomed-in screen-shots from the oscilloscope, where the change of resolution from the coarser resolution in third range to the fine resolution in the second range can be observed. Fig. 6.9c shows the transition from the fine resolution to the finest one.

The plots in Fig. 6.10 show the digital output of the system, acquired with a logic analyser. The red line is the output digital buffer converted in the decimal scale. The blue line is the V_I voltage which is referred to the voltage supply V_DD for an easier comparison. In particular Fig. 6.10a shows the full-range input-output characteristics, Fig. 6.10b the transition from the coarse resolution range to the fine one and Fig. 6.10c from the fine to the finest one.

The quantization error has been calculated as the difference between two lines: the the ideal A-to-D conversion (best-fit) line connecting 0 and the full scale value in the red plot in Fig.6.10 A-to-D conversion characteristic (red line). The best line fit has been divided in the same number of quantization levels as the one listed in Table 6.1, with each interval spaced according to the different resolutions. Fig. 6.11 plots the quantization error expressed as number of LSB's (chosen according the resolution range) vs. the ADC output code expressed in base-ten and it can be observed to be always less than 0.5 LSB's.

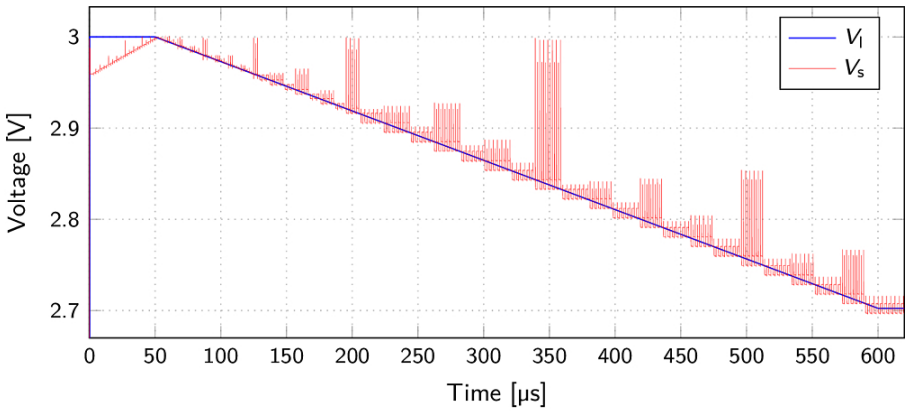


(a) Current input I_{load}.

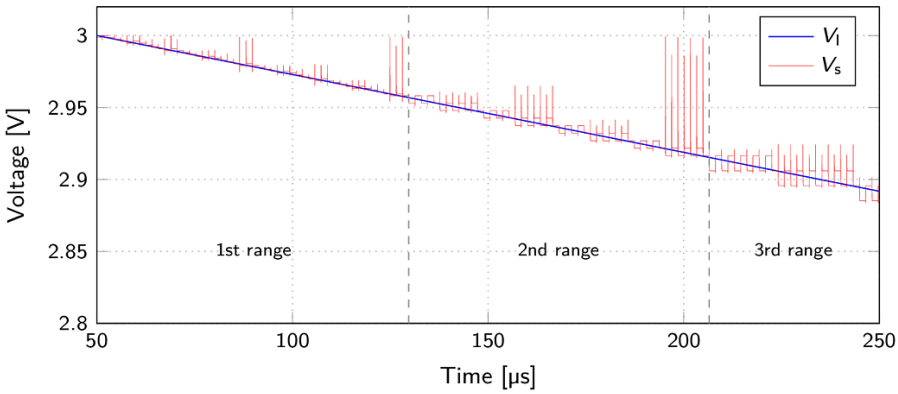


(b) Current output I_{sense}.

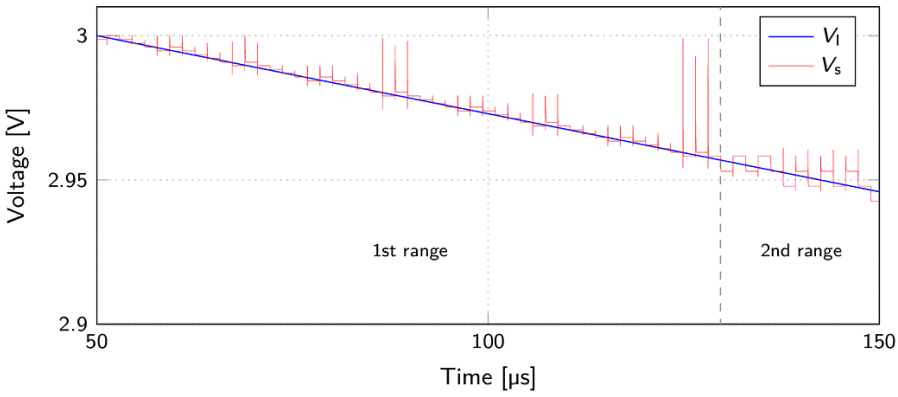
Figure 6.6: Input and output current characteristics of the 8 b ADC.



(a) Voltage input and output.

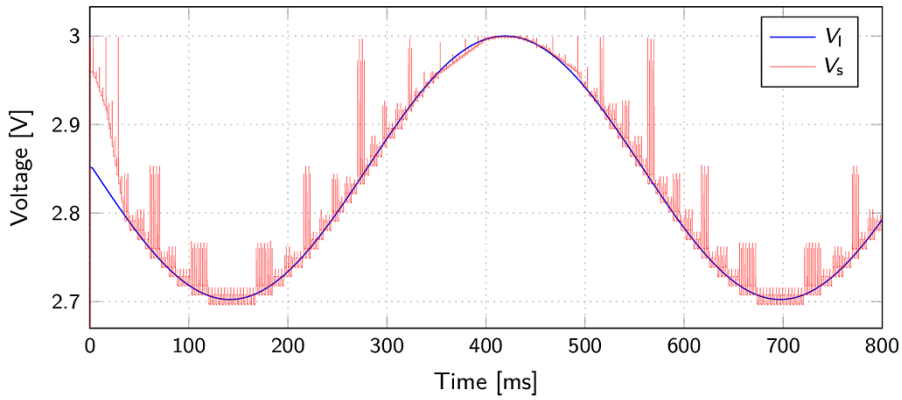


(b) Voltage input and output zoomed in.

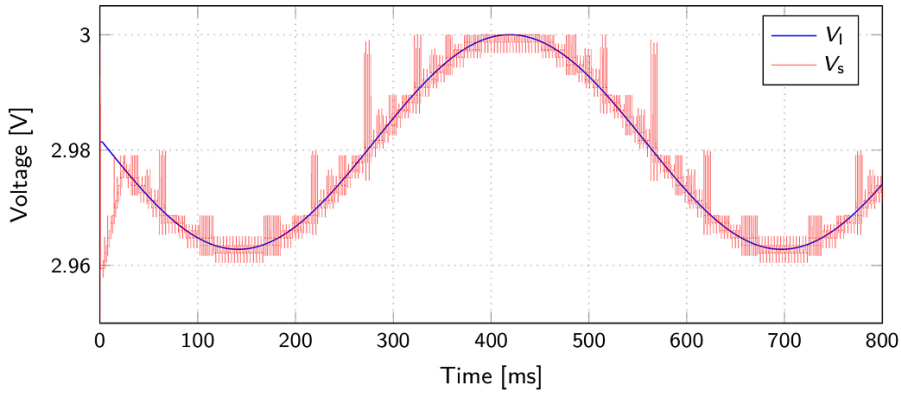


(c) Voltage input and output further zoomed in.

Figure 6.7: Input and output voltage characteristics of the 8 b ADC with a ramp.

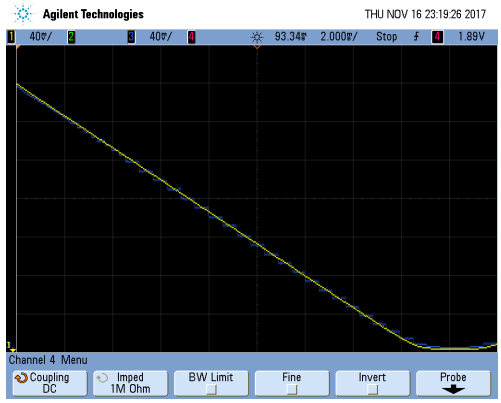


(a) Full-scale amplitude sine.

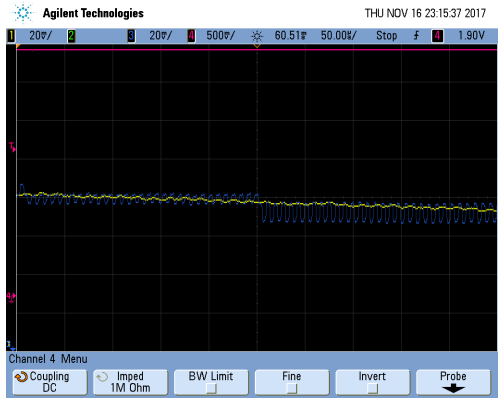


(b) Small amplitude sine.

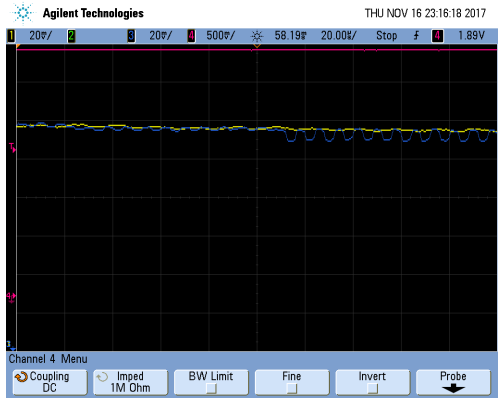
Figure 6.8: Input and output voltage characteristics of the 8 b ADC with sines.



(a) Full range.

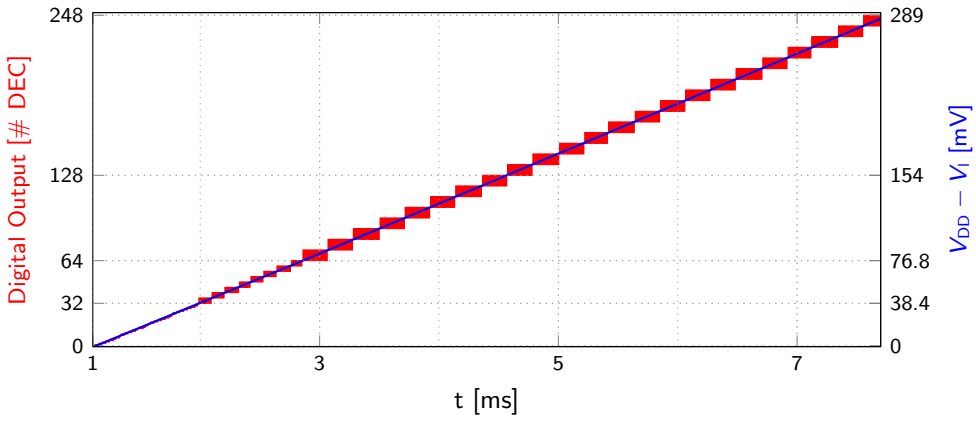


(b) Coarse to fine resolution transition.

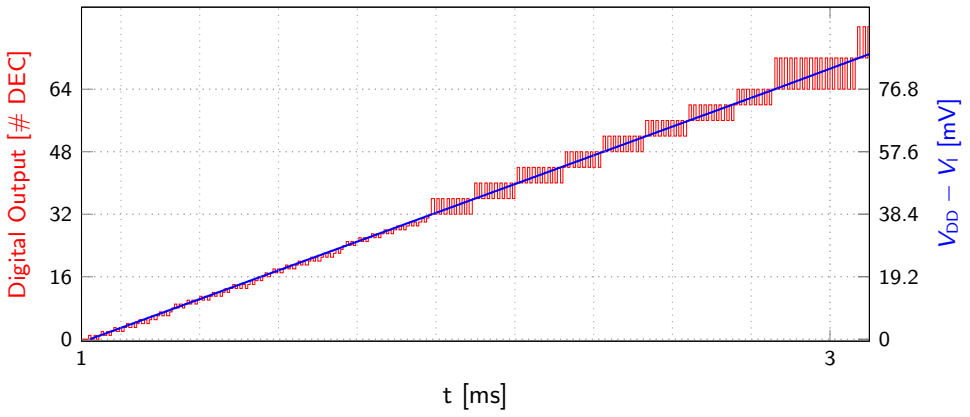


(c) Fine to finest resolution transition.

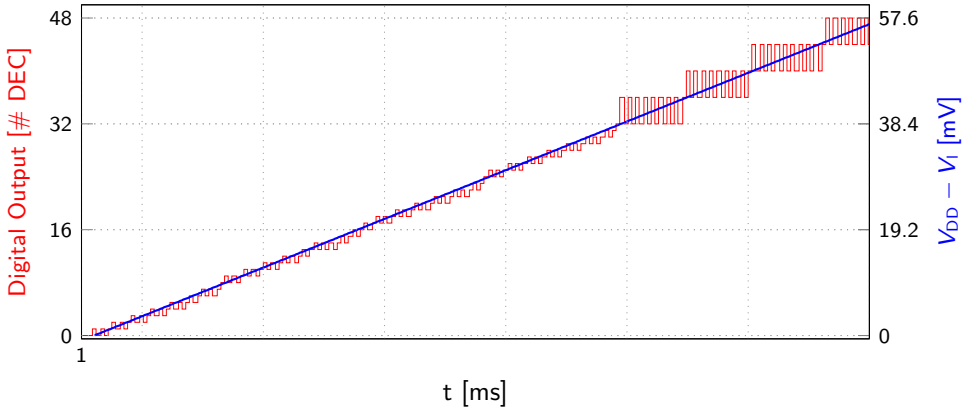
Figure 6.9: Oscilloscope measurements. The yellow line is the voltage input measured at the V_i node, the blue line is the voltage output measured at the V_s node.



(a) I_{load} full input range [0 A − 100 A].



(b) I_{load} zoomed-in range: [0 A − 32 A].



(c) I_{load} range further zoomed-in range: [0 A − 1.2 A].

Figure 6.10: Digital output analysis.

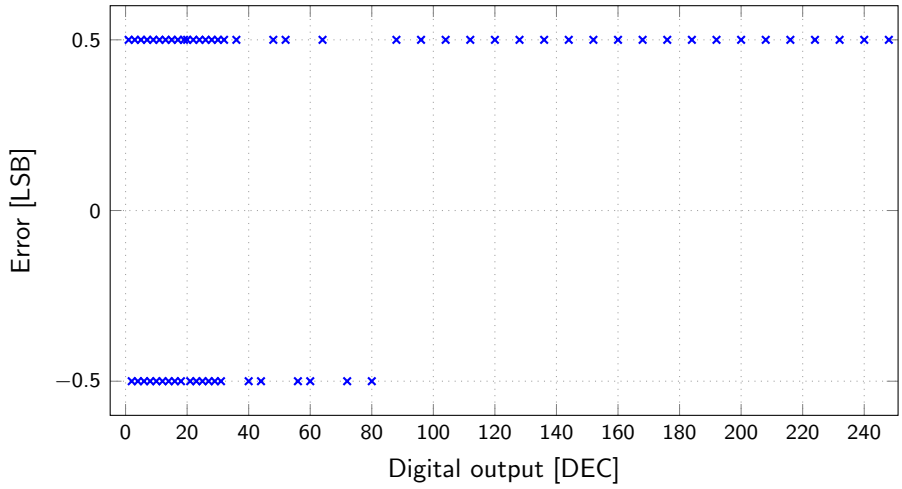


Figure 6.11: Error plot.

Chapter 7

Full system design

7.1 Introduction

This Chapter deals with the implementation of the full system providing the 10 b A-to-D conversion of the input signal and the open-load current detection. Fig. 7.1 shows the scheme of the full system concept designed around the tracking ADC shown in the previous Chapters. The additional blocks implementing the open-load detection are highlighted in red and the temperature estimation block in orange (developed in the next Chapter).

During the normal current measurement operation only the black blocks are used and the switch Sw is in position b. In particular, the 20 K ratio transistors are used to compare V_s and V_s and D1 is used to generate the quantized I_{sense} current. The design of D1 starts from the 8 b ADC already developed and enhances it to provide 10 b resolution.

During the open-load detection operation, the switch Sw is in position a. In this phase I_{load} needs to be compared with one of the two thresholds defined in the requirements by the following Equations:

$$\begin{aligned} I_{load,OL1} = 20\,mA \quad &\mapsto \quad I_{load,th1} = 10\,mA \\ I_{load,OL2} = 60\,mA \quad &\mapsto \quad I_{load,th2} = 50\,mA \end{aligned} \tag{7.1}$$

The proposed solution is to use two auxiliary DACs, namely D2 and D3, both digitally driven and activated only on the open-load detection operation.

D3 is designed to provide the three possible currents used for the two comparisons on the left-hand path of Fig. 3.7, namely the two $I_{OL,th}$ and $I_{load,min}$. Since the possible currents are three and an enable bit is necessary, this DAC needs to be controlled by 2 bit provided by the ADC logics.

D3 is connected on the top-side to an auxiliary scaled-down power transistor with

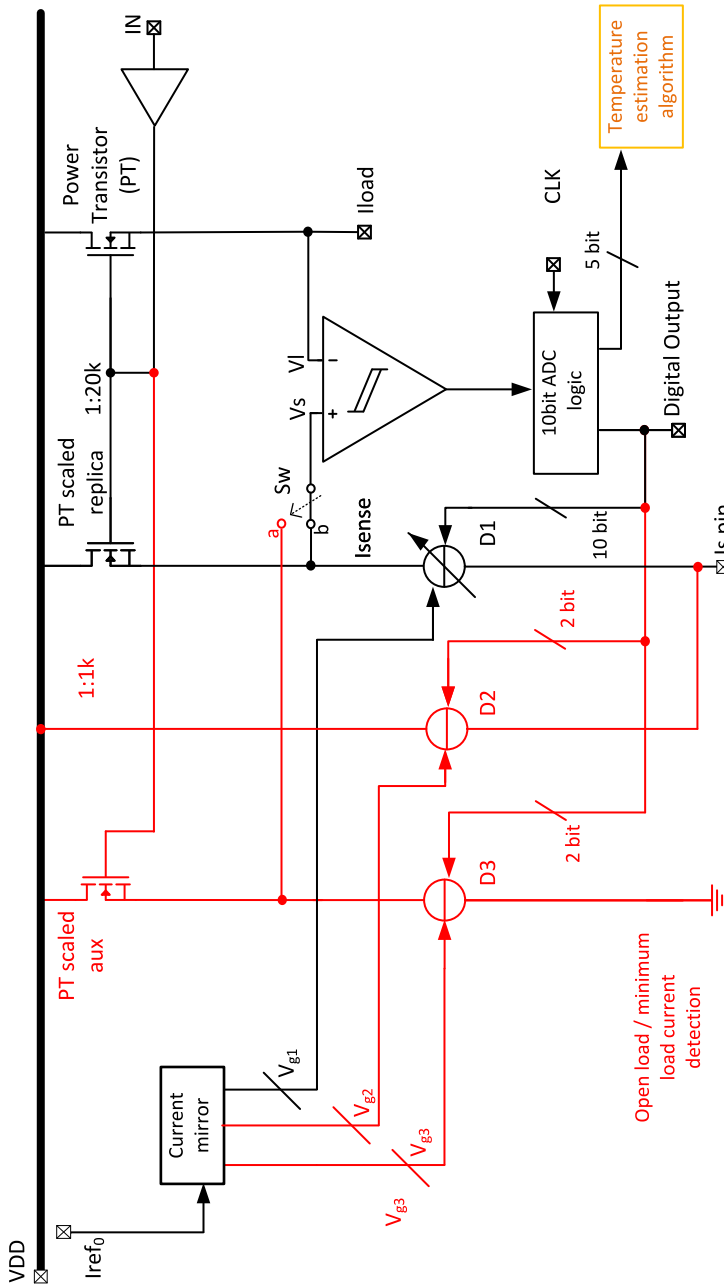


Figure 7.1: Scheme of the full munti-functional system. Based on [28].

a 1 k ratio with respect to the the main PT. This solution allows relaxing the DAC design for the currents comparison as larger currents are generally less sensitive to variations (this is clear if one thinks to two current mirrors with the same sizes: the one with lower current exhibits the smaller overdrive voltage, and therefore it is more sensitive to the transistors threshold-voltage spread). With this solution the current to be provided by D3 are 10 µA, 50 µA and 100 µA instead of 0.5 µA, 2.5 µA and 5 µA.

On the bottom-side D3 is connected to a ground-related pin so to have the current generated by this DAC not flowing into the I_s pin.

The DAC D2 activates only when an open-load current is indeed detected and it provides to the I_s pin a scaled-down by 20 K version of the open-load current flowing on the I_{load} side. Since this DAC is not used to perform any comparison, it is not required to be as accurate as D1 and therefore its design may be relaxed. When enabled, it generates one of the two programmable open-load current down-scaled by 20 K , i.e. either 1 µA or 3 µA. D3 requires 2 b to be driven: one for the current selection and one for the enable.

7.2 10 b ADC design

In this Section the design of the 10 b ADC is presented. The development starts from the 8 b ADC described in Chapter 6 and and the same considerations done in 3 here applies.

7.2.1 Resolution

In the requirements in Section 2.1.2, Point 2iii it is stated that the system shall detect I_{load} values at 100 mA, 200 mA, and 300 mA. This would set the ADC LSB at 100 mA. Considering the full-scale value to be 100 A, this would lead to at least 1000 quantization levels, i.e. a 10 b ADC. However, as already noted in Section 3.1.1, this resolution is not required in the entire input range but limited to the lowest current values $I_{\text{load}} = [0\,\text{mA} - 400\,\text{mA}]$. This observation together with the concept developed for the 8 b presented in Chapter 6 leads to the following resolution specifications (depicted in Fig. 3.1):

- 10 b (finest) resolution for $I_{\text{load}} = [0\,\text{mA} - 400\,\text{mA}]$
- 8 b (fine) resolution for $I_{\text{load}} = [1\,\text{A} - 13\,\text{A}]$
- 5 b (coarse) resolution for $I_{\text{load}} = [13\,\text{A} - 100\,\text{A}]$

Table 7.1 shows for each of the output digital word (expressed both in decimal and binary) the corresponding analog output I_{sense}, which maps to specific I_{load} value and voltage V_{s} values (expressed both absolutely and referred to V_{DD}). The

Table 7.1: 10 b conversion table

# bit [DEC]	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	I_{load} [A]	I_{sense} [µA]	V_s [V]	$V_{DD} - V_s$ [mV]
0	0	0	0	0	0	0	0	0	0	0	0	0	3	0
1	0	0	0	0	0	0	0	0	0	1	0.1	5	2.9997	0.3
2	0	0	0	0	0	0	0	0	1	0	0.2	10	2.9994	0.6
3	0	0	0	0	0	0	0	0	1	1	0.3	15	2.9991	0.9
4	0	0	0	0	0	0	0	1	0	0	0.4	20	2.9988	1.2
8	0	0	0	0	0	0	1	0	0	0	0.8	40	2.9976	2.4
12	0	0	0	0	0	0	1	1	0	0	1.2	60	2.9964	3.6
16	0	0	0	0	0	1	0	0	0	0	1.6	80	2.9952	4.8
20	0	0	0	0	0	1	0	1	0	0	2	100	2.994	6
24	0	0	0	0	0	1	1	0	0	0	2.4	120	2.9928	7.2
28	0	0	0	0	0	1	1	1	0	0	2.8	140	2.9916	8.4
32	0	0	0	0	1	0	0	0	0	0	3.2	160	2.9904	9.6
36	0	0	0	0	1	0	0	1	0	0	3.6	180	2.9892	10.8
40	0	0	0	0	1	0	1	0	0	0	4	200	2.988	12
44	0	0	0	0	1	0	1	1	0	0	4.4	220	2.9868	13.2
48	0	0	0	0	1	1	0	0	0	0	4.8	240	2.9856	14.4
52	0	0	0	0	1	1	0	1	0	0	5.2	260	2.9844	15.6
56	0	0	0	0	1	1	1	0	0	0	5.6	280	2.9832	16.8
60	0	0	0	0	1	1	1	1	0	0	6	300	2.982	18
64	0	0	0	1	0	0	0	0	0	0	6.4	320	2.9808	19.2
68	0	0	0	1	0	0	0	1	0	0	6.8	340	2.9796	20.4
72	0	0	0	1	0	0	1	0	0	0	7.2	360	2.9784	21.6
76	0	0	0	1	0	0	1	1	0	0	7.6	380	2.9772	22.8
80	0	0	0	1	0	1	0	0	0	0	8	400	2.976	24
84	0	0	0	1	0	1	0	1	0	0	8.4	420	2.9748	25.2
88	0	0	0	1	0	1	1	0	0	0	8.8	440	2.9736	26.4
92	0	0	0	1	0	1	1	1	0	0	9.2	460	2.9724	27.6
96	0	0	0	1	1	0	0	0	0	0	9.6	480	2.9712	28.8
100	0	0	0	1	1	0	0	1	0	0	10	500	2.97	30
104	0	0	0	1	1	0	1	0	0	0	10.4	520	2.9688	31.2
108	0	0	0	1	1	0	1	1	0	0	10.8	540	2.9676	32.4
112	0	0	0	1	1	1	0	0	0	0	11.2	560	2.9664	33.6
116	0	0	0	1	1	1	0	1	0	0	11.6	580	2.9652	34.8
120	0	0	0	1	1	1	1	0	0	0	12	600	2.964	36
124	0	0	0	1	1	1	1	1	0	0	12.4	620	2.9628	37.2
128	0	0	1	0	0	0	0	0	0	0	12.8	640	2.9616	38.4
144	0	0	1	0	0	1	0	0	0	0	14.4	720	2.9568	43.2
160	0	0	1	0	1	0	0	0	0	0	16	800	2.952	48
176	0	0	1	0	1	1	0	0	0	0	17.6	880	2.9472	52.8
192	0	0	1	1	0	0	0	0	0	0	19.2	960	2.9424	57.6
208	0	0	1	1	0	1	0	0	0	0	20.8	1040	2.9376	62.4
224	0	0	1	1	1	0	0	0	0	0	22.4	1120	2.9328	67.2
240	0	0	1	1	1	1	0	0	0	0	24	1200	2.928	72
256	0	1	0	0	0	0	0	0	0	0	25.6	1280	2.9232	76.8
288	0	1	0	0	1	0	0	0	0	0	28.8	1440	2.9136	86.4
320	0	1	0	1	0	0	0	0	0	0	32	1600	2.904	96
352	0	1	0	1	1	0	0	0	0	0	35.2	1760	2.8944	105.6
384	0	1	1	0	0	0	0	0	0	0	38.4	1920	2.8848	115.2
416	0	1	1	0	1	0	0	0	0	0	41.6	2080	2.8752	124.8
448	0	1	1	1	0	0	0	0	0	0	44.8	2240	2.8656	134.4
480	0	1	1	1	1	0	0	0	0	0	48	2400	2.856	144
512	1	0	0	0	0	0	0	0	0	0	51.2	2560	2.8464	153.6
544	1	0	0	0	1	0	0	0	0	0	54.4	2720	2.8368	163.2
576	1	0	0	1	0	0	0	0	0	0	57.6	2880	2.8272	172.8
608	1	0	0	1	1	0	0	0	0	0	60.8	3040	2.8176	182.4
640	1	0	1	0	0	0	0	0	0	0	64	3200	2.808	192
672	1	0	1	0	1	0	0	0	0	0	67.2	3360	2.7984	201.6
704	1	0	1	1	0	0	0	0	0	0	70.4	3520	2.7888	211.2
736	1	0	1	1	1	0	0	0	0	0	73.6	3680	2.7792	220.8
768	1	1	0	0	0	0	0	0	0	0	76.8	3840	2.7696	230.4
800	1	1	0	0	1	0	0	0	0	0	80	4000	2.76	240
832	1	1	0	1	0	0	0	0	0	0	83.2	4160	2.7504	249.6
864	1	1	0	1	1	0	0	0	0	0	86.4	4320	2.7408	259.2
896	1	1	1	0	0	0	0	0	0	0	89.6	4480	2.7312	268.8
928	1	1	1	0	1	0	0	0	0	0	92.8	4640	2.7216	278.4
960	1	1	1	1	0	0	0	0	0	0	96	4800	2.712	288
992	1	1	1	1	1	0	0	0	0	0	99.2	4960	2.7024	297.6

middle horizontal lines mark the change of resolution, similarly on what shown in Fig. 3.1 by the colors.

7.2.2 Blocks specifications

Comparator

The comparator input off-set specification depends on the LSB. Considering the $N = 10\,\text{b}$ resolution and the input full-scale FS to be 100 A. The LSB on the I_{load}side is $\text{LSB}_{\text{IL}} = 100\,\text{mA}$ which, according to Equation (3.1), in the voltage domain maps to $\text{LSB}_{\text{V}} = 0.4\,\text{mV}$. The comparator off-set shall therefore be negligible with respect to this value. The Infineon's comparator IP used in the previous scheme provides a 0 V mean input off-set and 27 µV random input off-set at $6\,\sigma$ and therefore can be adopted again.

DAC

The DAC general specifications reported in Section 4.3.2 shall be satisfied, except the resolution, which should be modelled around the concept presented in Section 7.2.1.

Current mirror

The current mirror is designed to provide to the different blocks the required biasing and reference currents by processing an external reference current I_{ref0}. The error introduced by this currents generator shall be small enough to not compromise the overall system accuracy and monotonicity. This blocks provides the reference and the biasing currents for the other blocks present in the system too, therefore its design will be described after them.

7.2.3 Transistor level design

DAC

For the ADC, the main focus is to design a suitable current steering DAC able to provide the required resolution. The core of the block is the DAC implemented for the 8b ADCȦ 2 b DAC can be added to 8 b DAC in order to implement the finest resolution, similarly to what done when designing the 8 b DAC itself. With respect to a full 8 b converter, which needs $2^{10} = 1024$ devices for the DAC, the used solution makes use of $2^5 + 2^3 + 2^2 = 44$ devices, saving potentially more than 90% of the area.

The new 2 b DAC operates only for the I_{load} values listed in the first Section of Table 7.1. Unlike the 3 b DAC added in the previous design, it would never work in parallel with the other converters. This can be noted form the conversion Table, as the 2 LSB's are used only to generate currents within the finest range. This allows relaxing the new DAC design has it does not need to be particularly matched with the 3 b cells.

Fig. 7.2 shows the concept of the 10b current steering DAC concept, which is made of the parallel of the already designed 5b and 3b converters and the new 2b one. The 10b driving the current sources are generated by the ADC logic and two reference currents are required.

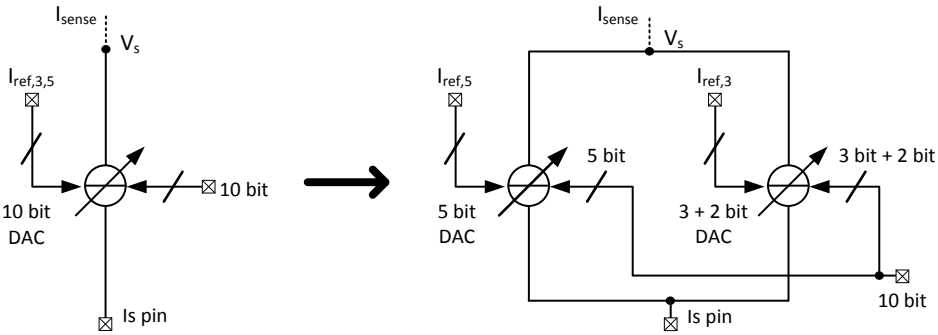


Figure 7.2: 10b current steering DAC concept.

The 5 b is the same as the one designed in Chapter 5. The 3 b presented in Chapter 6 has been slightly modified in order to obtain the additional 2 b binary cells which are not required to be matched to the other cells and therefore their design can be optimized in terms of area.

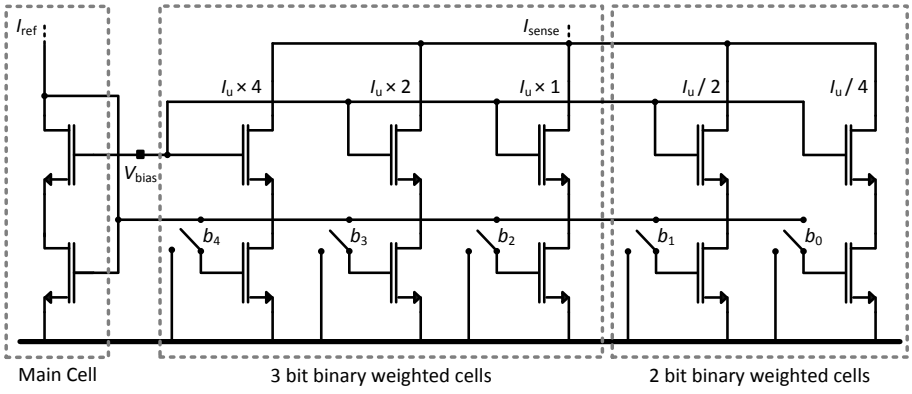


Figure 7.3: Transistor level 3 + 2 b DAC

The unity current to be provided by the 2 b DAC is 5 µA, which is one fourth of

the unity current provided by the 3 b DAC. Consequently the transistors composing these cells are designed four times smaller than the 3 b counterpart, optimizing the area occupation. This leads having:

- Bottom: $W/L = 3\,\mu m/4.8\,\mu m$
- Cascoded: $W/L = 3\,\mu m/1.2\,\mu m$

The resulting overdrive voltages are expected to be similar to the 3 b cells one, as the the transistors sizes and currents scale down proportionally and as a matter of fact the simulated values for the bottom and cascoded devices are respectively $V_{ov,1} = 250\,mV$ and $V_{ov,2} = 130\,mV$.

7.3 Additional DAC's design

The open-load detection functionality requires two additional DAC's, as stated in Section 7.1. Referring to Fig. 7.2, D2 generates a scaled down version of the possibly detected open-load current at the analog output pin Is, whereas D3 provides the currents used for the detection comparisons. The design of these two DAC's is not very demanding in terms of accuracy as the generated currents do not need to match to other currents. This is especially true for D3, which sets an arbitrary threshold between 0 A and the open-load currents and whose value has been already enlarged thanks to the use of a 1 k ratio between the PT and its scaled-down replica.

When activated, D3 shall be able to provide three possible currents used for the open-load detection:

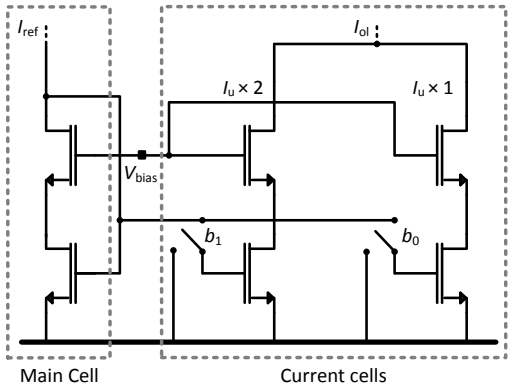
- $I_{ol,th1} = 10\,\mu A$
- $I_{ol,th2} = 50\,\mu A$
- $I_{ol,th3} = 100\,\mu A$

whereas D2 shall be able to provide the two scaled-down versions of the possibly detected open-load currents:

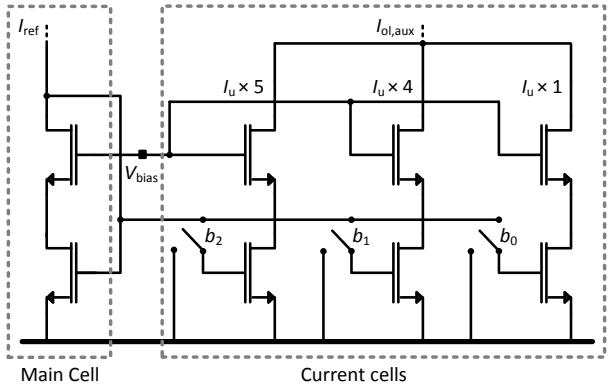
- $I_{ol1} = 1\,\mu A$
- $I_{ol2} = 3\,\mu A$

The implementation of D2 and D3 are shown respectively in Fig. 7.4a and Fig. 7.4b. Both D2 and D3 are implemented similarly to the main DAC D1 i.e. with wide-swing cascode current mirror topology and both reference currents I_{ref} are set to 10 µA. The bit controlling the current cells in D2 and D3 are generated by the the ADC logic block.

D2 unit current I_u is set to 1 µA. When enabled, if the selected open-load current is $I_{load,OL1} = 20\,mA$ then the bit b_0 activates the right-most cell generating $I_{ol} = 1\,\mu A$. If the selected open-load current is $I_{load,OL2} = 60\,mA$ then the bit b_0 and b_1



(a) D2.



(b) D3.

Figure 7.4: Transistor level implementation of the additional DAC's.

activate both cells, generating $I_{\text{ol}} = 3\,\mu\text{A}$.

D2 main cell transistors size are set:

- Bottom: $W/L = 60\,\mu\text{m}/4.8\,\mu\text{m}$
- Cascoded: $W/L = 60\,\mu\text{m}/1.2\,\mu\text{m}$

and the resulting overdrive voltages are respectively $V_{ov,1} = 100\,\text{mV}$ and $V_{ov,2} = 60\,\text{mV}$. The unit cells are ten times smaller, proportionally to the $1\,\mu\text{A}$ current they generate, namely:

- Bottom: $W/L = 6\,\mu\text{m}/4.8\,\mu\text{m}$
- Cascoded: $W/L = 6\,\mu\text{m}/1.2\,\mu\text{m}$

and also in this case the resulting overdrive voltages are respectively $V_{ov,1} = 100\,\text{mV}$ and $V_{ov,2} = 60\,\text{mV}$ as dimensions and current scale down together.

D3 unit current I_{u} is set to $10\,\mu\text{A}$. When enabled, if the selected open-load current threshold is $I_{\text{load,th1}} = 10\,\text{mA}$ then the bit b_0 activates the right-most cell generating $I_{\text{ol,aux}} = 10\,\mu\text{A}$. If the selected open-load current threshold is $I_{\text{load,th2}} = 50\,\text{mA}$

then the bit b_2 activates the left-most cell generating $I_{\text{ol,aux}} = 50\,\mu\text{A}$. If the selected open-load current threshold is $I_{\text{load,th3}} = 100\,\text{mA}$ then the, bit b_0, b_1 and b_2 activate all cells, generating $I_{\text{ol,aux}} = 100\,\mu\text{A}$.

D3 main cell transistors size are set to:

- Bottom: $W/L = 6\,\mu\text{m}/4.8\,\mu\text{m}$
- Cascoded: $W/L = 6\,\mu\text{m}/1.2\,\mu\text{m}$

and the resulting overdrive voltages are respectively $V_{ov,1} = 300\,\text{mV}$ and $V_{ov,2} = 140\,\text{mV}$. The unit cells are equally sized and therefore their overdrive voltages are the same.

7.4 Current mirror design

The current mirror is designed to provide to the different blocks the required bias and reference currents by processing an external reference current $I_{\text{ref,0}}$.

The required output currents are:

- $3 + 2$ b DAC reference current $I_{\text{ref,1}}$ at $20\,\mu\text{A}$
- $3 + 2$ b DAC bias current $I_{\text{bias,4}}$ at $20\,\mu\text{A}$
- 5 b DAC reference current $I_{\text{ref,2}}$ at $160\,\mu\text{A}$
- 5 b DAC bias current $I_{\text{bias,4}}$ at $20\,\mu\text{A}$
- D2 reference current $I_{\text{ref,3}}$ at $10\,\mu\text{A}$
- D2 bias current $I_{\text{bias,1}}$ at $10\,\mu\text{A}$
- D3 reference current $I_{\text{ref,4}}$ at $10\,\mu\text{A}$
- D3 bias current $I_{\text{bias,2}}$ at $10\,\mu\text{A}$
- comparator bias current $I_{\text{bias,3}}$ at $10\,\mu\text{A}$

for a total of four reference currents and five bias currents. The error introduced by this currents generator shall be small enough to not compromise the overall system accuracy and monotonicity.

The implementation of the current mirror block is shown in Fig. 7.5. A p-MOS based structure has been chosen as all of the currents required from the other blocks are positive (i.e. ideally flowing from the voltage supply to the ground). Similarly to the main DAC, the selected topology is a wide-swing cascode topology for increased matching and output resistance.

Two different approach are used for the transistors sizes of the reference and bias currents generator, the former one being optimized in term of accuracy and matching and the latter one being developed to achieve maximum efficiency in area.

The main cell and the unit cell on the reference current side transistors sizes are set to:

- Top: $W/L = 14\,\mu\text{m}/11\,\mu\text{m}$

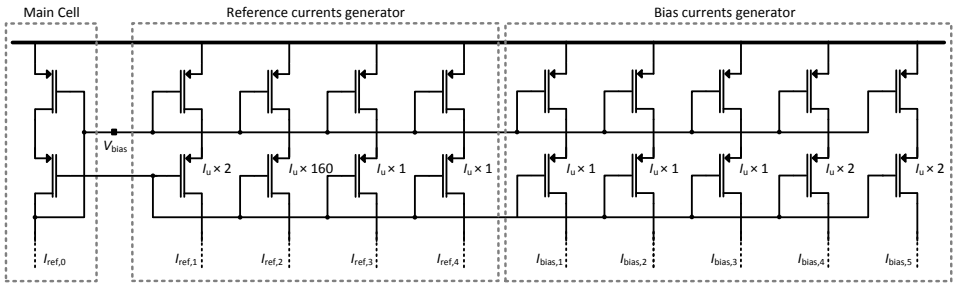


Figure 7.5: Transistor level implementation of the current mirror block.

- Cascoded: $W/L = 14\,\mu m/2.75\,\mu m$

and the resulting overdrive voltages are respectively $V_{ov,1} = 485\,mV$ and $V_{ov,2} = 240\,mV$. The unit cells are equally sized and therefore their overdrive voltages are the same. The W and the L of the bias currents generator unit cell are divided by two as here the accuracy is less important. The resulting overdrive voltages are $\sqrt{2}$ times smaller, i.e. $V_{ov,1} = 340\,mV$ and $V_{ov,2} = 160\,mV$.

7.5 Open-load detection and ADC logic design

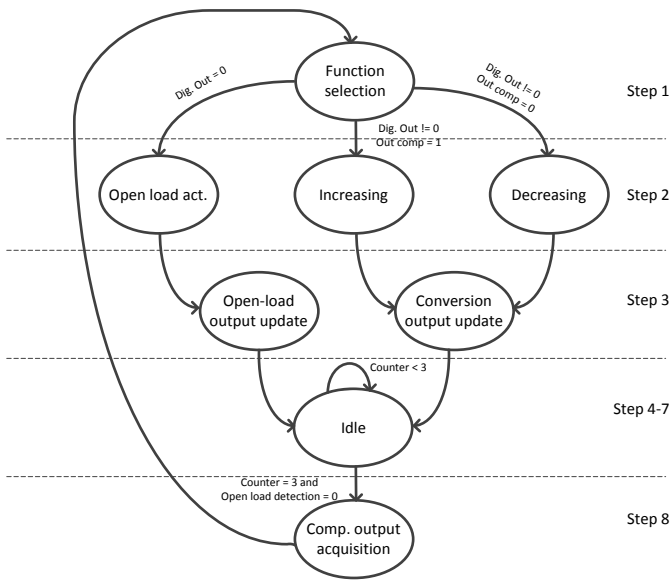


Figure 7.6: Open-load detection and ADC logic design controlling logic implemented with a finite state machine

The ADC logic driving the DAC's, dividing by eight the input clock and possibly enabling the open-load detection mode has been implemented by a Finite-state

machine (FSM) written in VHDL and depicted in Fig. 7.6.

The inputs of the FSM are the comparator output, the external 5 MHz clock, the threshold current selection bit, the reset and the enable. The outputs are the clock at 625 kHz, the 10 b ADC digital output (which drives D1), the digital words driving D2 and D3 (in particular the *open-load mode activation* bit and the *open-load detection* bit).

The FSM implements the functionalities shown in the flow chart in Fig. 3.7 and it is synchronized with the comparator so to read its output and set the current values properly in time. Each step lasts one input clock period and eight cyclic steps are used in order to divide the external clock by simply outputting a logical 1 for the first four steps and a logical 0 for the last four steps.

The first step of the FSM implements the state *Function selection*, which according to the ADC digital output selects the next operation. If the digital output is 0 then the machine enter the *Open-load activation* state, which enables the *Open-load mode activation* bit. Otherwise it proceeds with the normal conversion functionalities by reading the stored comparator output and entering accordingly either the *Increasing* or the *Decreasing* state. This two states take into account the different possible ranges listed in Table 7.1 and add or subtract the corresponding quantities to the digital output. Going down from the *Open-load activation*, in the third step the *open-load output update* function is activated; by processing the current and previous comparator feeds, this state properly sets the digital output driving D2 and D3 and possibly signals the detection of an open-load current. On the other side of Step 3, the *Conversion output update* state updates the digital output of the ADC; the step number of this operation has been timed in order to allows the analog signals (namely I_{sense} and V_{s}) to settle and be ready for the next comparison. Both of the states in Step 3 converge to the *Idle* state, which is iterated for three periods and has been inserted for the synchronization and timing reasons above mentioned. The final Step implements the *Comparator output acquisition* state, which update the comparator output and ready this data for the next FSM cycle. The machine has been programmed to continues its cycles even if an open-load is detected and to go back to the normal conversion functionality if the open-load is not any more present.

7.6 Simulation results

7.6.1 Current mirror and DAC's

The current mirror layout and DAC's have been drawn. The Montecarlo (MC) Post-Layout Simulations (PLS) results at $-40\,°C$ temperature (worst case) are reported in Table 7.2 for the current mirror block only. The first column reports the considered current, the second one the mean values, the third one the standard deviation, the fourth one the ideal value and the last one the six-times standard deviation referred to the ideal value and expressed in percentage. As expected, the error in the mean and in the standard deviation produced in the reference current is less than the bias currents counter parts.

Table 7.2: MC PLSs results of current mirror

Current name	**Mean [A]**	**σ [A]**	**Ideal Value [A]**	**$6 \times \sigma$ [%]**
$I_{\text{ref,1}}$	1.00E-05	5.25E-08	1.00E-05	3.15
$I_{\text{ref,2}}$	2.00E-05	9.00E-08	2.00E-05	2.70
$I_{\text{ref,3-4}}$	1.60E-04	6.08E-07	1.60E-04	2.28
$I_{\text{bias,1-3}}$	1.02E-05	4.95E-07	1.00E-05	4.95
$I_{\text{bias,5-6}}$	2.03E-05	7.52E-07	2.00E-05	3.76

Table 7.3 reports the PLS analysis for the 10 b. In this analysis the reference and bias currents needed by the converter are not ideal but generated by the current mirrors therefore the data shown in Table 7.2 are included in the statistical analysis. The second last column reports the LSB of the considered range used for the last column calculations.

Table 7.3: MC PLSs results of the 10 b DAC

Bit DEC.	**Mean [A]**	**σ [A]**	**Ideal Value [A]**	**LSB [A]**	**$6 \times \sigma$ [# of LSB's]**
1	4.90E-06	1.07E-07	5.00E-06	5.00E-6	0.14
2	9.83E-06	1.58E-07	1.00E-05	5.00E-6	0.20
3	1.47E-05	2.24E-07	1.50E-05	5.00E-6	0.29
4	1.96E-05	2.68E-07	2.00E-05	2.00E-5	0.32
12	6.10E-05	6.19E-07	6.00E-05	2.00E-5	0.20
16	8.14E-05	8.55E-07	8.00E-05	2.00E-5	0.28
28	1.42E-04	1.38E-06	1.40E-04	2.00E-5	0.45
32	1.61E-04	8.84E-07	1.60E-04	2.00E-5	0.29
480	2.41E-03	9.87E-06	2.40E-03	1.60E-4	0.40
512	2.57E-03	1.08E-05	2.56E-03	1.60E-4	0.44

For the 10 b DAC, the most critical points in terms of monotonicity are placed at the different internal DAC's switching, happening between bit number 3 and 4 (when passing from the 2 b to the 3 b DAC) between bit number 28 and 32 (when

passing from the 3 b to the 5 b DAC), and moreover placed at the major carry transitions for each DAC's, i.e. between bit 2 and 3 for the 2 b DAC, between bit 12 and 16 for the 3 b DAC and between bit 480 and 512 for the 5 b DAC. For each of these cases, the $6 \times \sigma$ spread is less than 0.5 referred to considered range LSB, ensuring therefore the DAC monotonicity.

Table 7.4 reports the PLS analysis for the auxiliary DAC's D2 and D3.

Table 7.4: MC PLSs results of auxiliary DAC's

Current name	**Mean [A]**	**σ [A]**	**Ideal Value [A]**	**$6 \times \sigma$ [%]**
$I_{\mathrm{ol},1}$	1.05E-05	1.80E-08	1.00E-06	10.80
$I_{\mathrm{ol},2}$	3.07E-05	6.38E-08	3.00E-06	12.75
$I_{\mathrm{ol,aux},1}$	1.03E-04	1.50E-07	1.00E-05	9.00
$I_{\mathrm{ol,aux},2}$	5.14E-05	6.75E-07	5.00E-05	8.10
$I_{\mathrm{ol,aux},3}$	1.04E-05	1.28E-06	1.00E-04	7.65

As stated above, these results are not required to be very accurate and the error values reported in the last column allows having enough accuracy for both the comparison operation implemented by D3 and the current generation at the IS pin performed by D2.

7.7 Transient analysis

After the analyses shown in the previous Section, the complete system has been implemented by adding to the layout the logic circuit and the auto-zeroing comparator.

A transient analysis has been performed in order to check both the open-load detection and the A-to-D conversion functionalities. The open-load current is set to $I_{\mathrm{load,OL2}} = 60\,\mathrm{mA}$ which is mapped to $I_{\mathrm{ol},2} = 3\,\mu\mathrm{A}$ on the I_{sense} side through D2. The threshold current enabled to detect the open-load is $I_{\mathrm{ol,aux},2} = 50\,\mu\mathrm{A}$, generated by D3.

Fig. 7.7a shows the input current signal applied at the V_{l} node. It is designed to start at the middle value $I_{\mathrm{load}} = 49.6\,\mathrm{A}$ and keep it for 200 µs allowing the tracking ADC output to catch up. Then it slowly goes down to $I_{\mathrm{load}} = 80\,\mathrm{mA}$ at the time $t = 700\,\mu\mathrm{s}$. This current value is supposed trigger the open-load mode and activate the open-load detection bit. Then the input continues to decrease more slowly, reaching 0 A at $t = 750\,\mu\mathrm{s}$; at this point the open-load mode should be still triggered, but the open-load detection bit should be deactivated. Afterwards, the I_{load} starts to rise and reaches the full-scale value at $t = 2\,\mathrm{ms}$. Fig. 7.7b plots the I_{sense} current and it can be observed that the sense current is following the load

counterpart. Fig. 7.7c shows the open-load mode bit and the open-load detection bit, which activate around the time that I_{load} reaches 80 mA.

A clearer picture is given in 7.8 where the zoomed in versions of the previous Figures within the $t = [697\,\mu\text{s} - 693\,\mu\text{s}]$ time range are depicted. Fig. 7.7b plots the sense current coming from the main DAC D1. I_{sense} is tracking I_{load} and it can be noticed that in the beginning the conversion switches from the fine range currents ($I_{\text{sense}} = 400\,\text{mA}$) to the finest range, characterized by the 300 mA, 200 mA and 100 mA levels. Then the sense current goes to zero and the open-load mode is activated. When the load current is around 80 mA, the system detects the open-load and flags it. When the I_{load} is lower than the threshold current $I_{\text{load,OL2}} = 60\,\text{mA}$ than the system recognizes the load current to be null and deactivates the open-load bit. Then the input current starts to rise fast enough to not trigger again the open-load detection. When I_{load} reaches the ADC LSB value, the open-load mode is turned off and the normal conversion operation is resumed.

Fig. 7.9b plots D3 output current. It is enabled by the open-load mode bit and supplies the threshold currents. Even when the open-load is indeed detected it still operates for the system to continuously monitor whether or not the open-load condition is terminated. When the normal conversion resumes, D3 is turned off. Fig. 7.9c plots plots D2 output current. It is controlled by the open-load detection bit and generates the scaled down replica of the open-load current.

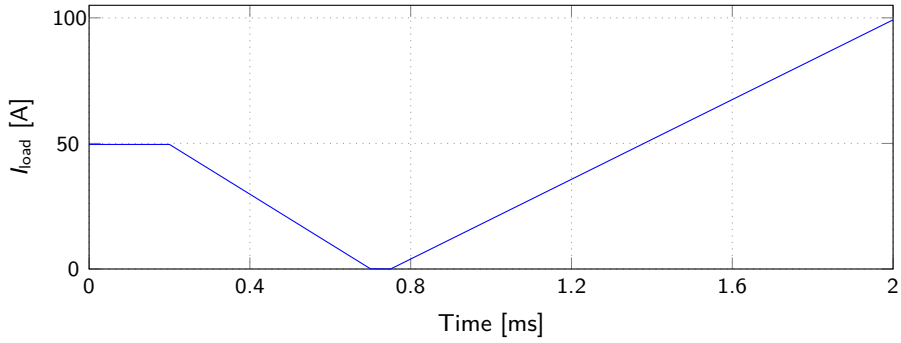
Fig. 7.10a shows the comparator input nodes V_{s} and V_{l} characteristics in time and 7.10b plots the zoomed in time range of interest. It could be noticed that when the open-load mode in enabled, the open-load detection bit activates only when the voltage V_{s} is lower than the V_{l}.

7.8 System accuracy analysis

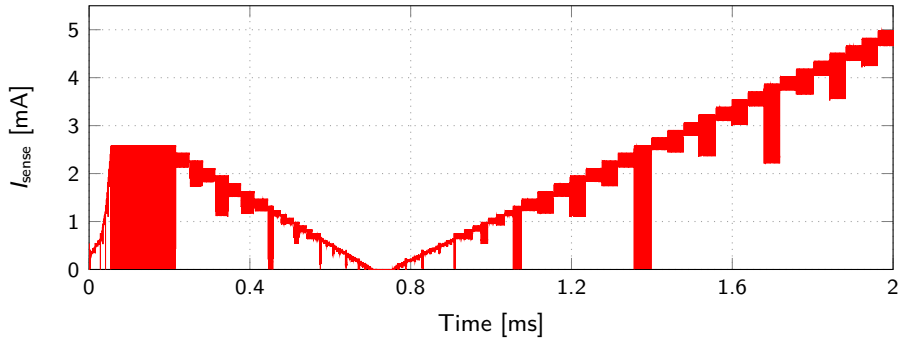
A Matlab model of the system has been developed in order to perform a statistical analysis of the non-idealities present on the system and their effect on the overall conversion accuracy. This mathematical approach is necessary as the system is very complex and a full Monte Carlo simulation at transistor level would require unacceptable CPU time, whereas Matlab offers the tools to effectively speed up this process.

The system model of the ADC has been designed and it takes into account the following non-idealities:

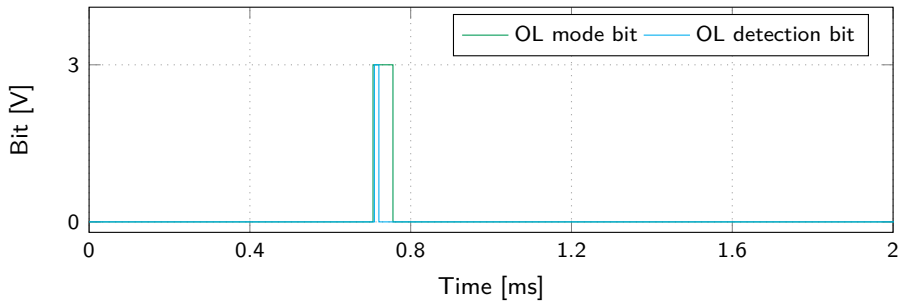
- Power Transistor / Power transistor replica geometrical ratio spread
- Spread of the reference current coming from a trimmed band-gap (a trimmed current with ±5% error



(a) Input current I_{load}.

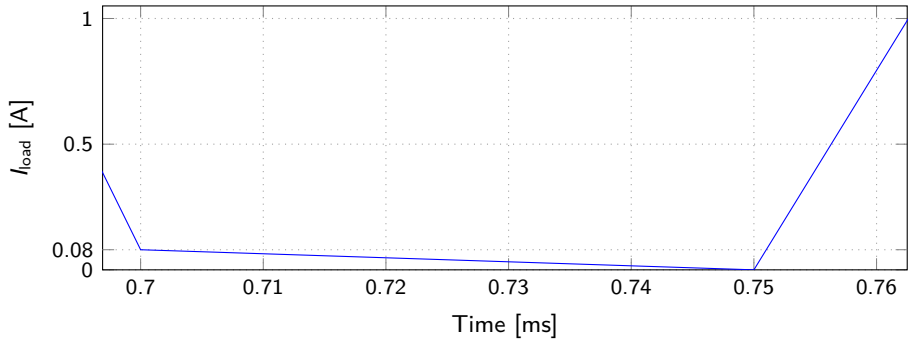


(b) Output current I_{sense}.

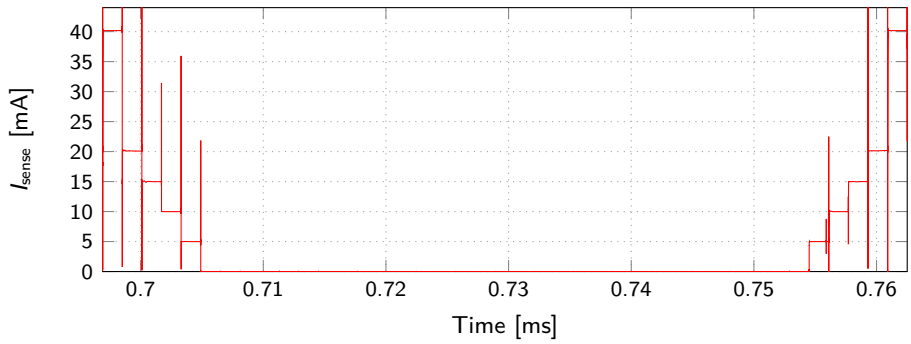


(c) Zoomed in OL mode and detection bit.

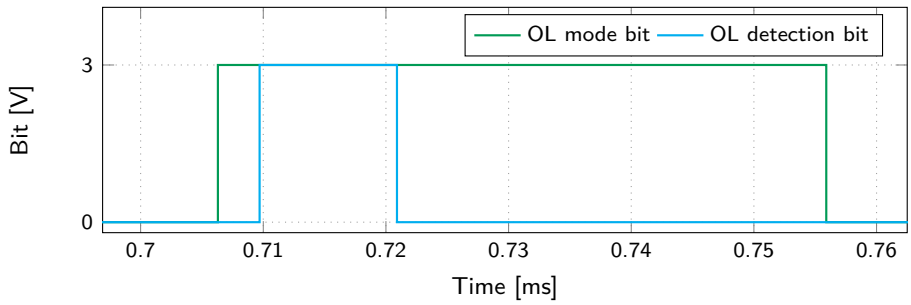
Figure 7.7: Input and output current characteristics of the 10 b ADC with the open-load related bit.



(a) Zoomed in current input I_{load}.

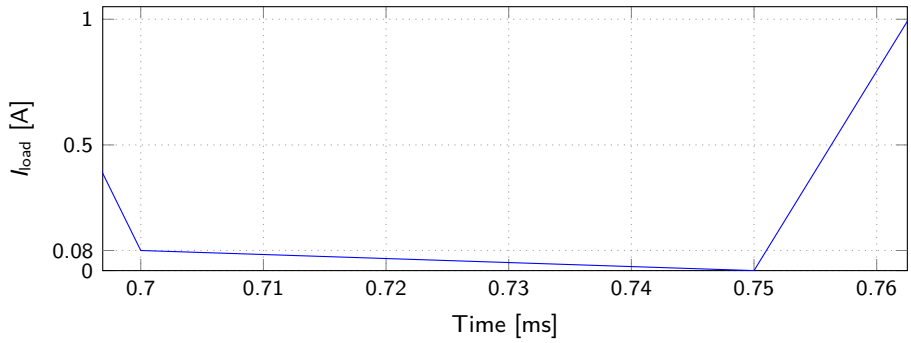


(b) Zoomed in current output I_{sense}.

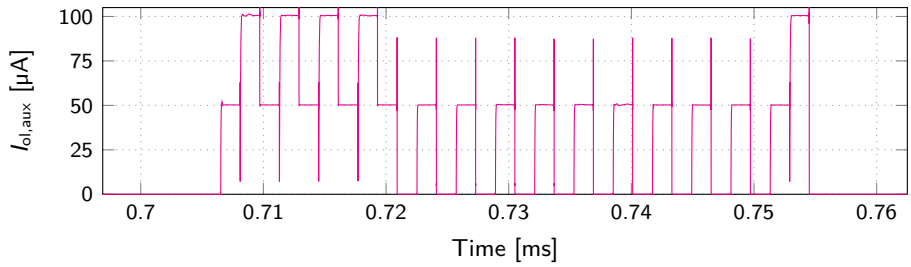


(c) Zoomed in OL mode and detection bit.

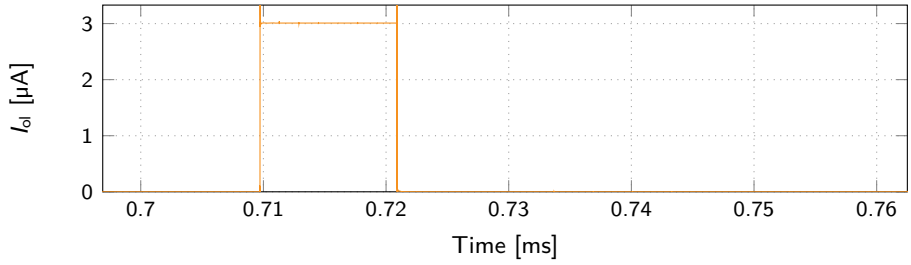
Figure 7.8: Zoomed in input and output current characteristics of the 10 b ADC with the open-load related bit within the $t = [697\,\mu\text{s} - 693\,\mu\text{s}]$ time range



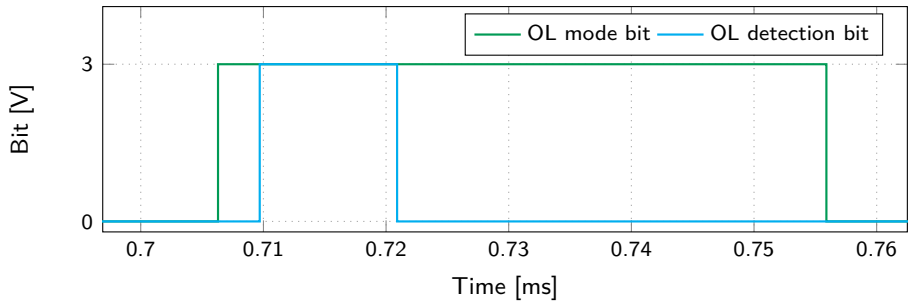
(a) Zoomed in current input I_{load}.



(b) Zoomed in D3 current output.

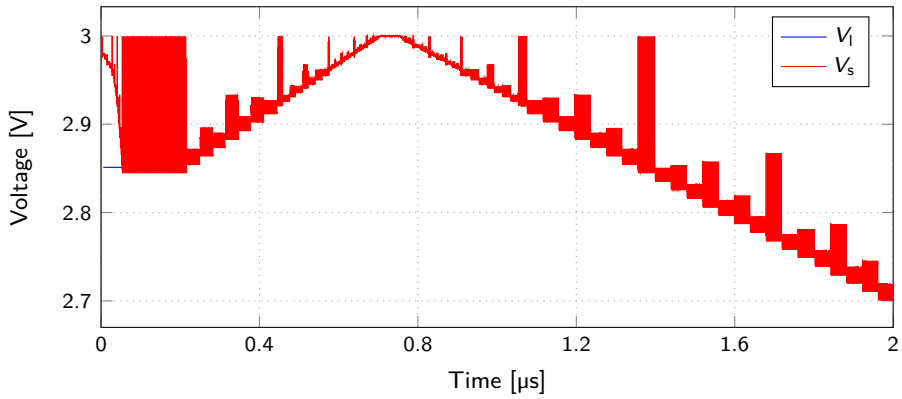


(c) Zoomed in D2 current output.

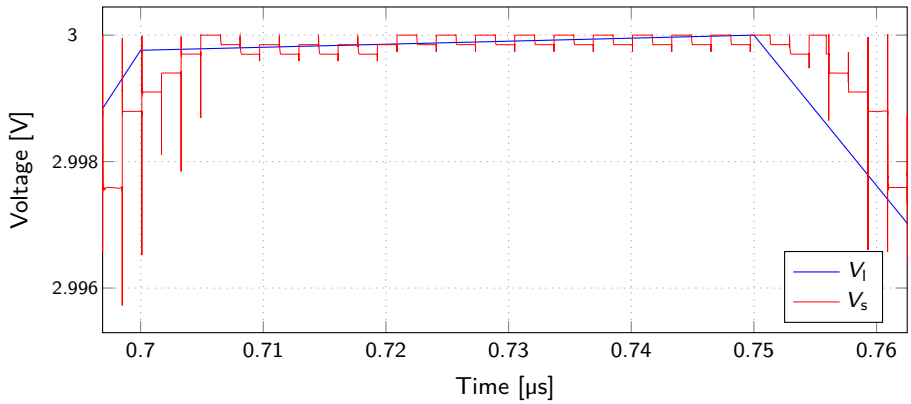


(d) Zoomed in OL mode and detection bit.

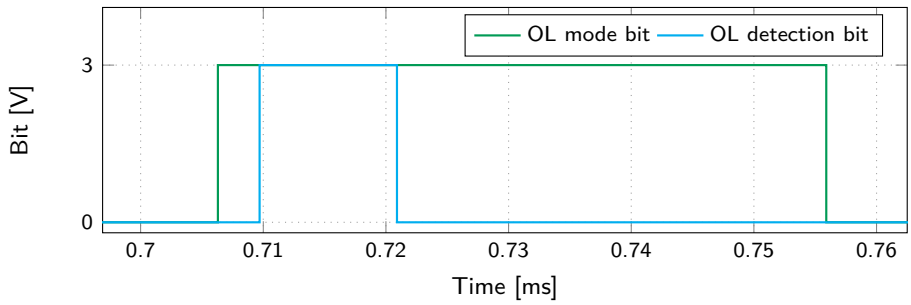
Figure 7.9: Zoomed in input and D2 and D3 current characteristics with the open-load related bit within the $t = [697\,\mu s - 693\,\mu s]$ time range



(a) V_s and V_l.



(b) Zoomed V_s and V_l.



(c) Zoomed in OL mode and detection bit.

Figure 7.10: Input and output voltage characteristics of the 10 b ADC with the open-load related bit.

- Spread due to the reference current mirroring
- Comparator offset
- Quantization error
- DAC's spread

The error affecting the conversion can been defined in two ways:

1) Analog error: Input current I_{load} minus the average of the analog I_{sense} toggling currents (multiplied by the scaling factor)
2) Digital error: Input current I_{load} minus the average of the currents corresponding to the output digital current (according to the conversion Table 7.1).

In the first case a continuous distribution is expected, as the error is calculated on an analog value, whereas in the second case a discrete distribution should present because the error is referred to quantized current errors.

The Matlab model is fed with the blocks accuracy values and then statistically combine them by launching one million of runs. The input value $I_{\text{load}} = 10\,\text{A}$ and required accuracy is $\pm 8\%$.

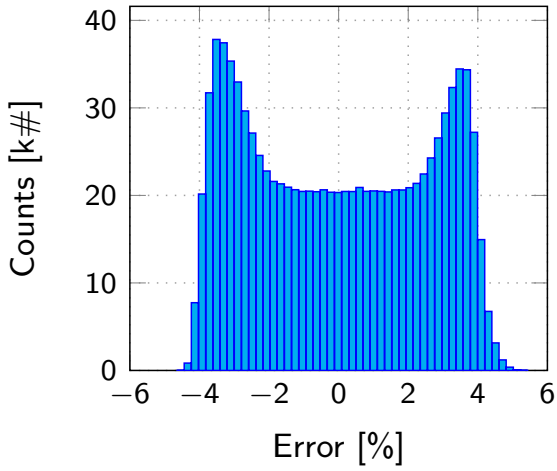
The results are shown in Fig. 7.11. Fig. 7.11a plots the analog error defined in the Point 1 and the maximum and minimum relative error are respectively $+5.53\%$ and -4.75%. Fig. 7.11b plots the digital error defined in the Point 2 and the maximum and minimum relative error are respectively $\pm 6.00\%$.

In both cases the system fulfils the accuracy requirements given for $I_{\text{load}} = 10\,\text{A}$.

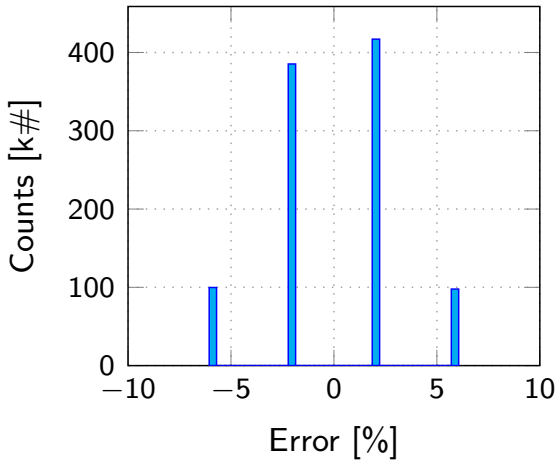
The same analysis has been performed with $I_{\text{load}} = 100\,\text{A}$, which is close to the full scale input value and required accuracy is $\pm 8\%$.

The results are shown in Fig. 7.12. Fig. 7.12a plots the analog and the maximum and minimum relative error are respectively $+7.20\%$ and -3.78%. Fig. 7.11b plots the digital error and the maximum and minimum relative error are respectively $+5.60\%$ and 0.80%. Therefore, also for $I_{\text{load}} = 100\,\text{A}$ the system fulfils the accuracy requirements.

The entire system presented in this Chapter and the temperature estimation and thermo-electrical stress protection block developed in the next one have been integrated and in the next months the chips are going to be available for measurements.

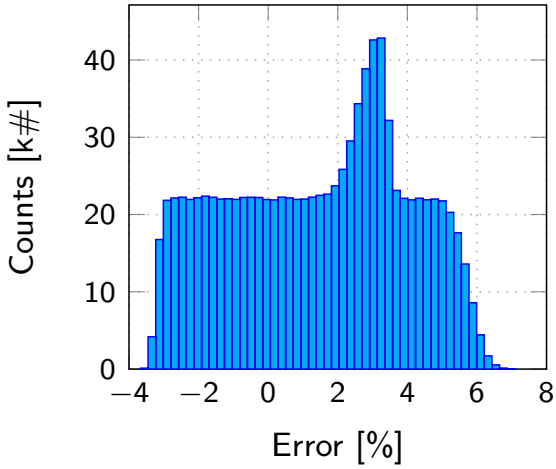


(a) Analog value.

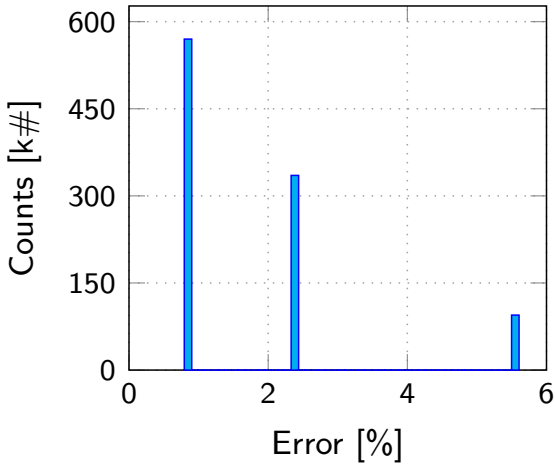


(b) Digital value.

Figure 7.11: Error for $I_{\text{load}} = 10\,\text{A}$.



(a) Analog value.



(b) Digital value.

Figure 7.12: Error for $I_{\text{load}} = 100\,\text{A}$.

Chapter 8

Over temperature protection

This Chapter describes the design of over temperature estimation and thermo-electrical stress protection features, which have been developed digitally. The concept is based on the work presented in these Infineon's patents: [18]–[20].

8.1 Requirements

The systems is required to provide a thermo-electrical stress protection by detecting a critical temperature rise caused by the Joule's effect in the I_{load} wire. In particular the system shall be programmable and able to:

1. select among three critical temperature rises ΔT_c, i.e. 15 K, 25 K and 35 K
2. estimate the temperature behaviour according to five different kind of wires, which differ thermo-geometrically.

Moreover, if the critical temperature is reached, the current measurement system shall shut-down but the digital block is required to continue the temperature estimation considering 0 A input current. This is because the wire temperature would naturally decrease due to the absence of current and therefore the digital block shall keep track of it. In fact the DSP block shall detect when the 10 K cool-down threshold is reached and signal this event to the system which will then resume the normal conversion.

8.2 Wire temperature behavioural model

The wire current-temperature-time relationship is expressed by (8.1) [21].

$$\Delta T(t) = \frac{I_{\text{load}}(t)^2 \cdot \alpha}{A} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \tag{8.1}$$

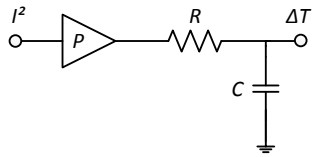


Figure 8.1: Equivalent electric circuit modelling the wire temperature behaviour.

where ΔT [K] is the temperature variation, t $[s]$ is the time, α $\left[\mathrm{K}\cdot\mathrm{m}^2/\mathrm{A}^2\right]$ is a parameter depending on the thermal characteristic of the wire, A $\left[\mathrm{mm}^2\right]$ is the wire section and τ $[s]$ is the thermal time constant. The five wires characteristics are reported in Table 2.1.

The wire temperature behaviour described in Equation (8.1) is similar the step response to a voltage V_s of an RC Low-Pass-Filter (LPF) which is:

$$v(t) = V_s \cdot \left(1 - e^{-\frac{t}{RC}}\right) \tag{8.2}$$

The equivalent electric circuit modelling the wire temperature behaviour is shown in Fig. 8.1 with $RC = \tau$ and $P = \alpha/A$ [19], [20].

The transfer function $H(s)$ in the s-domain of the circuit in Fig. 8.1 is:

$$H(s) = \frac{\Delta T(s)}{I^2(s)} = \frac{P}{1 + s\tau} \tag{8.3}$$

8.3 DSP block design

Fig. 8.2 shows the block diagram of temperature estimation algorithm present in Fig. 7.1. This block shall decide if the system should be shut-off according to the current evolution, which defines the wire temperature. To do so, according to Equation (8.1), the 5 MSB's digital word provided by ADC and representing the current needs to be squared. Then the resulting digital word is processed with a digital block mapping the transfer function defined in (8.3). Finally the processed signal is compared with the programmable temperature threshold to decide if the critical value is reached.

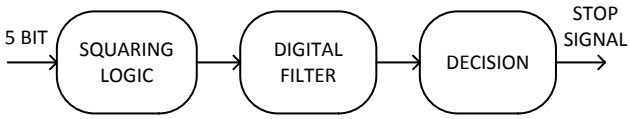


Figure 8.2: Temperature DSP block diagram.

8.3.1 Squaring logic

In digital signal processing applications where the input is corrupted by noise, exact calculations are often less important than achieving high clock rates, low power consumption or low area usage. Depending on the application, a low absolute error or a low relative error may be desired.

For the temperature estimation algorithm, in order to reduce the hardware complexity, an approximate version of the squaring block may be acceptable if it does not degrade performance significantly.

In a paper by *Park and Kim* the state-of-the-art approximate-squaring strategies are compared and the results are shown in Fig. 8.3 [35]. In particular, the most suitable solution for this work is represenented by the blue curve [36], as it presents the smaller approximation error for a 5 b input word.

The solution presented in [36] implements for each input bit an approximated logic function which is compensated heuristically. These Equations are reported in (8.4) where n is the number of bit, $a_{0,1,\ldots,n}$ is the input digital word, $r_{0,1,\ldots,2n}$ is the output word representing the squared result and $k = 2, 3, 4, \ldots n-4$.

$$
\begin{aligned}
r_{2n-1} &= a_{n-1}a_{n-2} \\
r_{2n-2} &= a_{n-1}\overline{a}_{n-2} \cup a_{n-1}a_{n-3} \\
r_{2n-3} &= \overline{a}_{n-1}a_{n-2}a_{n-3} \cup a_{n-1}\overline{a}_{n-2}a_{n-3} \cup a_{n-1}a_{n-2}a_{n-4} \\
r_{2n-4} &= \overline{a}_{n-1}a_{n-2}a_{n-4} \cup a_{n-1}\overline{a}_{n-2}a_{n-4} \cup a_{n-2}\overline{a}_{n-3}\overline{a}_{n-4} \\
r_{2n-5} &= \overline{a}_{n-2}a_{n-3}a_{n-4} \cup a_{n-2}\overline{a}_{n-3}a_{n-4} \cup a_{n-2}a_{n-3}a_{n-5} \cup a_{n-1}a_{n-5} \\
r_{2n-6} &= \overline{a}_{n-2}a_{n-3}a_{n-5} \cup a_{n-2}\overline{a}_{n-3}a_{n-5} \cup a_{n-3}\overline{a}_{n-4}\overline{a}_{n-5} \\
&\vdots \\
r_{2k+1} &= \overline{a}_{k+1}a_k a_{k-1} \cup a_{k+1}\overline{a}_k a_{k-1} \cup a_{k+1}a_k a_{k-2} \cup a_{k+2}a_{k-2} \\
r_{2k} &= \overline{a}_{k+1}a_k a_{k-2} \cup a_{k+1}\overline{a}_k a_{k-2} \cup a_k\overline{a}_{k-1}\overline{a}_{k-2} \cup a_{k+3}a_{k-2} \\
&\vdots \\
r_3 &= \overline{a}_2 a_1 a_0 \cup a_2\overline{a}_1 a_0 \cup a_4 a_1 a_0 \\
r_2 &= a_1\overline{a}_0 \cup a_4 a_1 \\
r_1 &= 0 \\
r_0 &= a_0
\end{aligned}
\tag{8.4}
$$

The Equations (8.4) have been implemented in VHDL. Fig. 8.4 plots the ideal parabola (blue dashed line) and approximated one (red dots) whereas Table 8.1

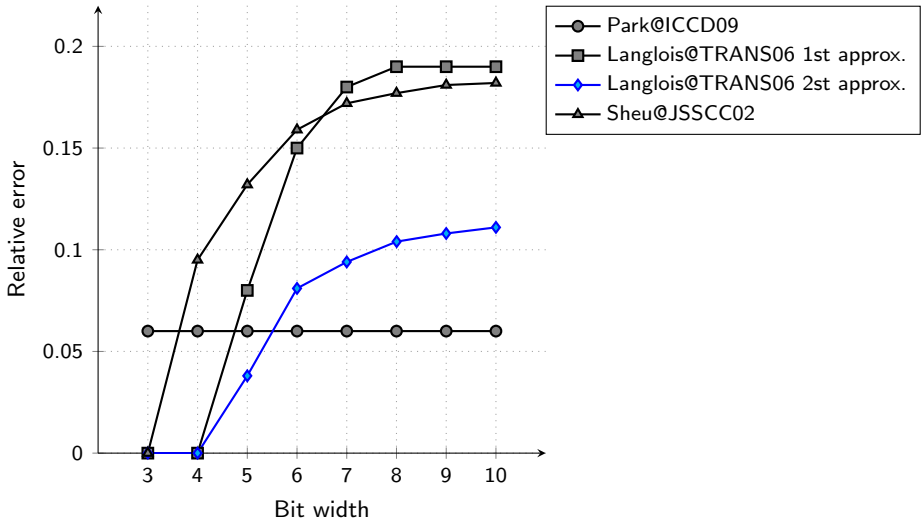


Figure 8.3: State-of-the-art squaring algorithms comparison [35].

reports the numerical value. The input producing errors are highlighted in italic and the maximum relative error is 3.8% which is acceptable for the temperature estimation.

For an area comparison, both the ideal and the approximated squarer have been synthesized with the latter being %55 smaller than the former.

Table 8.1: Digital results of the approximated squaring. The input producing errors are highlighted in italic.

IN	IN^2 ideal	IN^2 approx.	Abs. err.	Rel. err. [%]	IN	IN^2 ideal	IN^2 approx.	Abs. err.	Rel. err. [%]
0	0	0	0	—	16	256	256	0	0
1	1	1	0	0	17	289	289	0	0
2	4	4	0	0	18	324	324	0	0
3	9	9	0	0	*19*	*361*	*365*	*4*	*1.1*
4	16	16	0	0	20	400	400	0	0
5	25	25	0	0	21	441	441	0	0
6	36	36	0	0	22	484	484	0	0
7	49	49	0	0	*23*	*529*	*509*	*20*	*3.8*
8	64	64	0	0	24	576	576	0	0
9	81	81	0	0	25	625	625	0	0
10	100	100	0	0	26	676	676	0	0
11	121	121	0	0	*27*	*729*	*701*	*28*	*3.8*
12	144	144	0	0	28	784	784	0	0
13	169	169	0	0	*29*	*841*	*809*	*32*	*3.8*
14	196	196	0	0	30	900	900	0	0
15	225	225	0	0	*31*	*961*	*941*	*20*	*2.1*

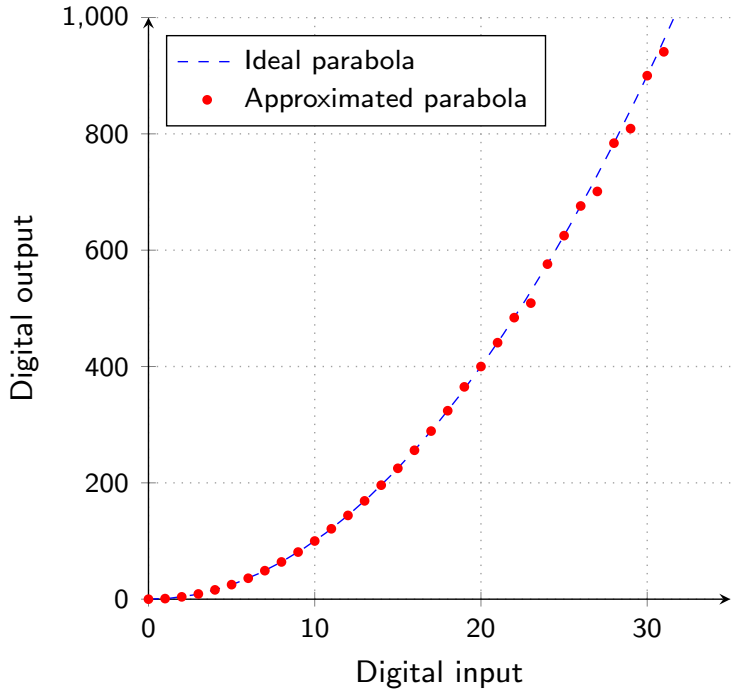


Figure 8.4: Digital results of the approximated squaring.

8.4 Digital Filter

Referring to Fig. 8.2 the output of the squarer is processed by a digital filter, which can be implemented with the classical IIR or FIR design solutions [18]–[20]. However the solution proposed in this work tries a different approach, based on a linear approximation of the filter step response.

8.4.1 Concept

The concept of the linear approximation is shown in Fig. 8.5 where the ideal step response (green curve) is approximated with two lines (black curve): the tangent to the curve in the origin and the horizontal asymptote to the curve for $t \longrightarrow +\infty$. From the implementation point of view, considering for now the tangent gradient to be 1 and the input to be constant, this solution is fairly simple because it would require only an adder summing up and accumulating the input squared values and hold the asymptotic value once it is reached (until the next different input value). However this algorithm is very inaccurate for the temperature estimation, especially around the black line corner, where the calculated temperature value deviates considerably from the real one.

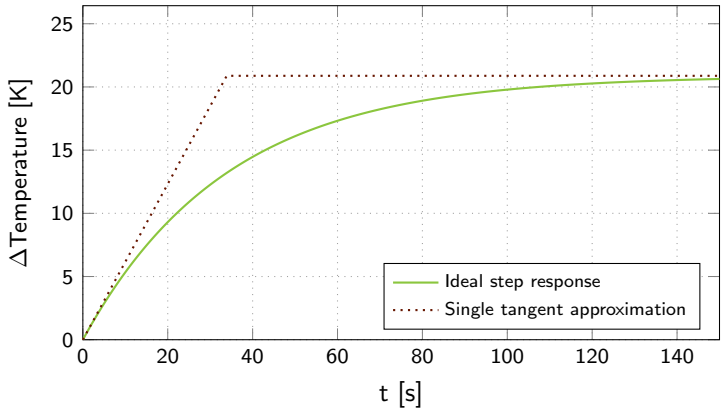


Figure 8.5: Step response first approximation.

A more refined approach is shown in Fig. 8.6 where a set of multiple tangents is used which divides the graph in eight regions (*i* to *viii*). Thanks to the multiple approximating lines the estimation error is considerably reduced at the cost of a greater design efforts.

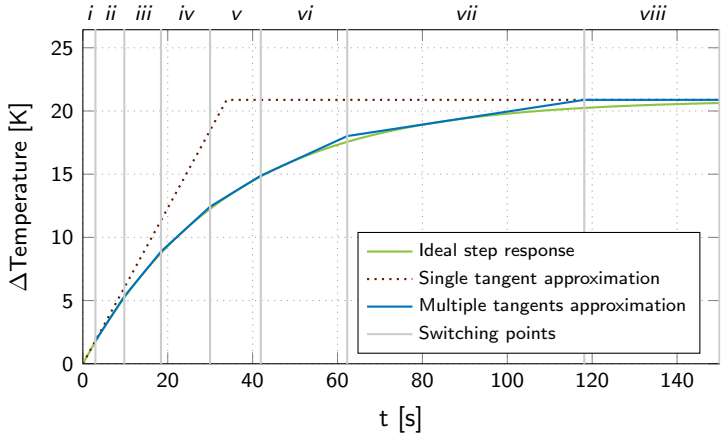


Figure 8.6: Step response first approximation.

The number of tangents is seven (plus the asymptote) and it has been chosen as a trade-off between system complexity and accuracy. From a mathematical point of view, the tangent gradients and the asymptotic depend on the digital input, whereas the tangents switching times (the gray vertical lines in Fig. 8.6) are independent of it. Moreover, it can be easily proven that if the input is not constant, the gradients depend on the difference between the actual and the previous input values and the asymptotic values depend on the actual one only.

8.4.2 System level implementation

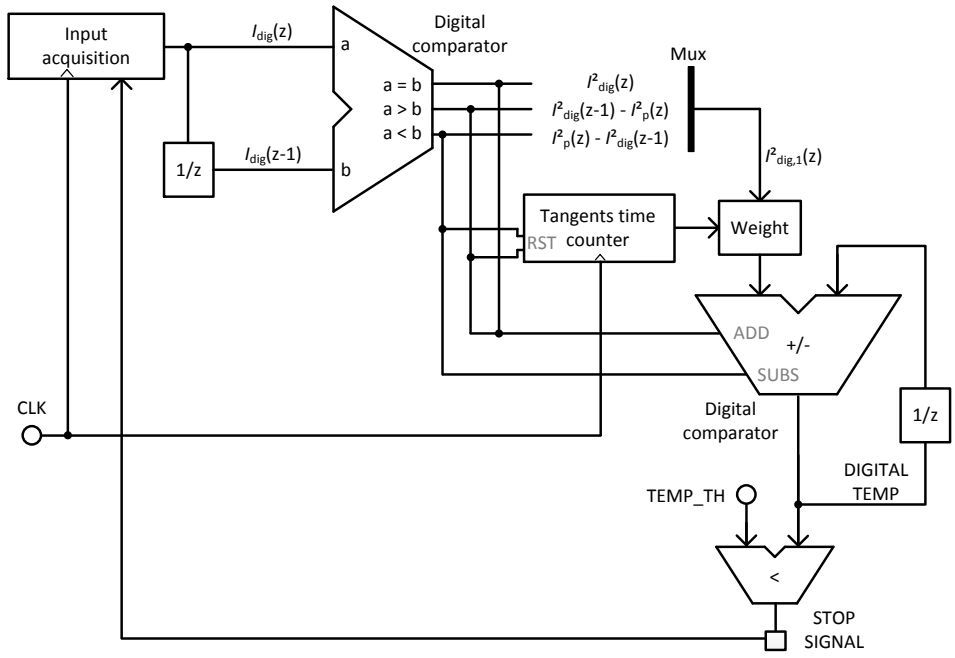


Figure 8.7: Basic block diagram.

The basic block diagram of the algorithm implementing the concept depicted in Fig. 8.6 is shown in Fig. 8.7. The inputs are the external clock and the 5 Most Significant Bit (MSB) of the ADC output. The operations of this scheme are:

- Acquisition of the digital data I_{dig} representing the current to be processed according to the digital comparator outcome:
  - If the current changes, reset the tangents time counter (used to define the gradients switching time), recalculate the asymptotic value and calculate the I_{p}^2 which is used to evaluate the correct quantity to add or subtract to ΔT_{dig} and whose definition is given in Section 8.4.4. Moreover:
    - If the current increases, calculate the difference $I_{\text{dig}}^2(z-1) - I_{\text{p}}^2(z)$, weight the result according to the tangent slope and then add it to the previous digital temperature calculation
    - If the current decreases, calculate the difference $I_{\text{p}}^2(z) - I_{\text{dig}}^2(z-1)$, weight the result according to the tangent slope and then subtract it from the previous digital temperature calculation
  - If the current remains constant, square it (one time), weight the result according to the tangent slope, square it and then then add up to the previous digital temperature calculation

- Compare the digital temperature with the threshold and if it is lower, continue the temperature estimation, else flag the event, force the digital input current at zero and continue with the temperature estimation until the digital ΔT is lower than 10 K. After this, resume the normal temperature estimation process.

8.4.3 Design issues

Temperature mapping

When performing an A-to-D conversion, the ADC reports a *ratiometric* value. For instance, considering a 5 b conversion of the input current I_{load}, the analog full-scale is 100 A, the ADC assumes 100 A is $2^5 - 1 = 31$ and anything less than 100 A will be a weighted ratio between 100 A and 31. Moreover, when calculating quantities deriving from the ADC outputs which involves also the time (like $\Delta T(t)$ in Equation (8.1)), the sampling period needs to be accounted for since in the analog domain the temperature calculation is based on continuous time and the digital domain on a sampled time. With these considerations in mind, the analog to digital temperature conversion ratio R_{ADC} can be defined as:

$$R_{\text{ADC}} = \frac{\tau}{T_s} \frac{1}{G^2 \cdot P} \tag{8.5}$$

where τ is the time constant of the wire, P is a parameter depending on the wire, G is the conversion ratio 100/31 (squared to take the squaring required in the temperature evaluation into account) and T_s is the sampling time.$T_s = 1.6\,\mu\text{s}$

Example: considering the largest wire in Table 2.1 and $T_s = 1.6\,\mu\text{s}$, the ratio R_{ADC} is 3.3E5. The critical temperature threshold $\Delta T_c = 35\,\text{K}$ is transformed to:

$$\Delta T_{\text{dig}} = \Delta T_c \cdot R_{\text{ADC}} \approx 1.2\text{E}7$$

which requires 24 b. Processing this number of bits would be problematic in terms of area with the BCD power-optimized technology, as a large amount of logical blocks like flip-flops is required.

Time counters

Referring to Fig. 8.6, the tangents switching times depend only on the time constants τ, which are around 10 s order of magnitude. In the digital domain, the time is measured with counters applied to the input clock and, when the specific thresholds are reached, then the tangents switches are triggered. Due to the large

τ with respect to the sampling period which for now is equal to clock driving the ADC i.e. $T_s = 1.6\,\mu s$, the counters thresholds may be very large.

Example: considering the largest wire in Table 2.1, the last switching time defining the *viii* region is at 135.6 s, corresponding to 113E6 clock counts. This quantity requires 27 b, which again is difficult to handle with the used technology.

8.4.4 Design solutions

Reducing the number of bit

The main idea in order to reduce the design complexity is to operate only with a certain amount of MSB's for both the time counter and the temperature calculation. In particular

- For the temperature calculation where 24 b are required, 13 MSB's only may be considered
- For the clock counter where 27 b are required, 13 MSB's only may be considered

In both cases 13 b has been found be a fair trade-off between accuracy and logics complexity.

Under-sample period choosing

The sampling clock T_s appears in the definition of the analog to digital temperature conversion ratio $R_{\mathrm{ADC}} = \tau/(T_s \cdot G^2 \cdot P)$. Moreover, this value is used in the Equations defining the digital asymptotic values asy_{dig} and the quantity I_{p}^2:

$$asy_{\mathrm{dig}} = I_{\mathrm{dig}}^2 \cdot \tau/T_s \tag{8.6}$$

$$I_{\mathrm{p}}^2 = \Delta T \cdot \tau/T_s \tag{8.7}$$

T_s can be set arbitrarily and individually for each wire as the clock driving the digital temperature estimator can be separated from the one driving the ADC because no particular synchronization is required between the two blocks. This is of pivotal importance considering time constants involved in Equation 8.1 (which are around 20 s) to be seven orders of magnitude larger then the clock period driving the ADC (1.6 µs), thus T_s can be greatly increased. This value is set according to the following trade-off:

- the largest T_s the less accurate is the temperature estimation, as the current samples time resolution would decrease

- the smaller T_s the the larger is the area due to the larger number of bits involved in the clock counting.

Moreover the sampling time can be selected in a way so that τ/T_s is a multiple of 2 making the multiplications appearing Equations (8.6), (8.7) become the less complex bit-shift operations.

Based on the above considerations, the set T_s values for each wire are summarized in Table 8.2, where U_s is the up-scaling factor applied to the 1.6 µs period clock driving the ADC.

Table 8.2: Clock up-scaling factor and period value for each wire.

Wire	U_s	T_s [µs]	$\log_2(\tau/T_s)$
1	16	25.6	19
2	21	33.6	19
3	13	20.8	20
4	16	25.6	20
5	20	32.0	20

Tangents slopes

Referring to Fig. 8.6, there are eight different regions in which the graph is divided according to the tangent slopes. For each region, the Mux output (Fig. 8.7) is divided (weighted) by a different value: the less steep the slope the larger the divisor. The number of regions has been chosen as a trade-off between system complexity and accuracy.

The divisors related to each tangent are $d_{\text{array}} = [1, 1.2, 1.5, 2, 3, 4]$. In the i region the Mux output is divided by 1, in ii region by 1.2, in iii region by 1.5 and so on.

All of the elements of d_{array} are "submultiples" of 12, i.e. $12/d_{\text{array}} = [12, 10, 8, 6, 4, 3]$. In this way the division can be implemented by mod-12 counters acting similarly to variable decimators, that is they count the number of the Mux output and:

- In region i, 12 out of 12 Mux output results are kept and processed by the next block
- In region ii, 10 out of 12 Mux output results are kept and processed by the next block
- In region iii, 8 out of 12 ...
- ... and so on.

With this implementation the division algorithms are avoided and replaced by simpler counters.

Conclusions

To summarize, the complexity-reducing strategies used in the digital design are hereby enlisted:

- Use a smart squaring algorithm
- Reduce the number of bit to be considered for the digital operations
- Choose a proper under-sample period T_s in order to transform multiplications into bit-shifts
- Avoid division when implementing the tangents and transform them into counting operations.

An area estimation of the digital block has been performed considering a prototype with the complexity-reducing strategies and one without them, with the former being 50% smaller than the latter.

8.5 Simulation Results

The diagram in Fig. 8.7 has been coded into a FSM in VHDL and then synthesized and automatically routed. The inputs of the digital system are the clock, the wire selection word and the temperature thresholds selection word.

In the used test-bench, the digital filter and the ideal temperature model have been placed together. A dynamic analysis has been performed by feeding both of the blocks with the same digital currents and comparing the times in which the two stop signals flag the critical temperature rise. The following plots consider the first wire in Table 2.1 with 25 K temperature threshold. Similar results have been obtained with all of the wires and temperature thresholds.

Fig. 8.8 shows the simulation results considering a constant current input (middle blue line). In the top plot the red line is the wire temperature variation characteristic derived from the ideal block green line is the critical temperature threshold. The bottom plot shows the activation of the digital stop signals calculated by the DSP block, which flags when the it detects the critical temperature rise. The ideal stop time is 28.75 s and digitally calculated time is 28.93 s, with a difference of 0.2 s which is negligible for this application especially considering the involved time constant *tau*.

Fig. 8.9 shows the simulation results with a variable input current shown in the middle graph. The ideal stop time is 66.52 s and digitally calculated time is 65.87 s, again very close.

As mention in Section 8.1, the system shall shut-down whenever the critical threshold is crossed, not allowing any current to flow through the wire and causing the temperature to naturally decrease. The digital block is required to continue to

operate with a 0 digital input in order to keep on tracking the wire temperature. When the cool-down threshold 10 K is crossed, the block shall drive the system to resume its normal operations.

Fig. 8.10 shows an analysis performed to evaluate the digital block behaviour after the critical temperature rise is detected. The variable input (blue line) is set first to force the temperature to rise over the critical threshold and then to change to make it settle below it. When the digital system detects the high threshold crossing, the stop signal is enabled and a null current is forced to be processed, as shown with the golden dashed line representing the actual processed value. Then the wire temperature starts to decrease and as soon as the it reaches the cool-down threshold and the logic detects it than the stop signal is disabled and the system resumes processing the real input current (blue line).

From the graphs in Fig. 8.10 it could be again noticed that the logic timing enabling and disabling the stop signal follows reliably the ideal wire temperature behaviour depicted by the red line.

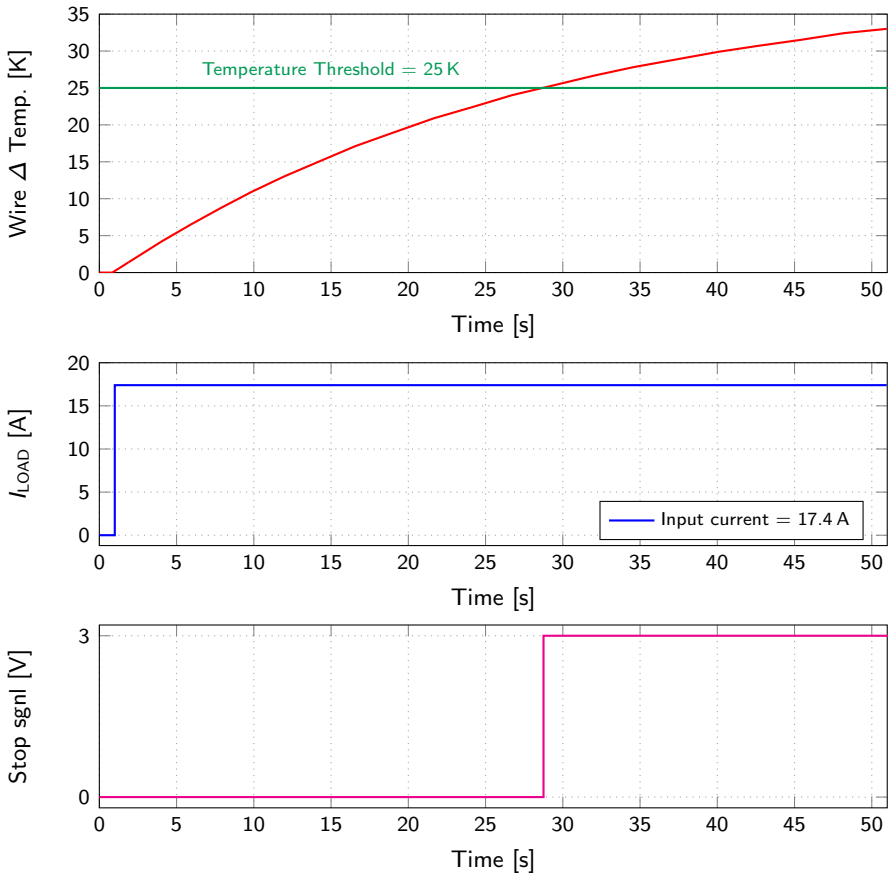


Figure 8.8: Temperature behaviour analysis with constant current.
Ideal stop time: 28.75 s
Digital stop time: 28.93 s

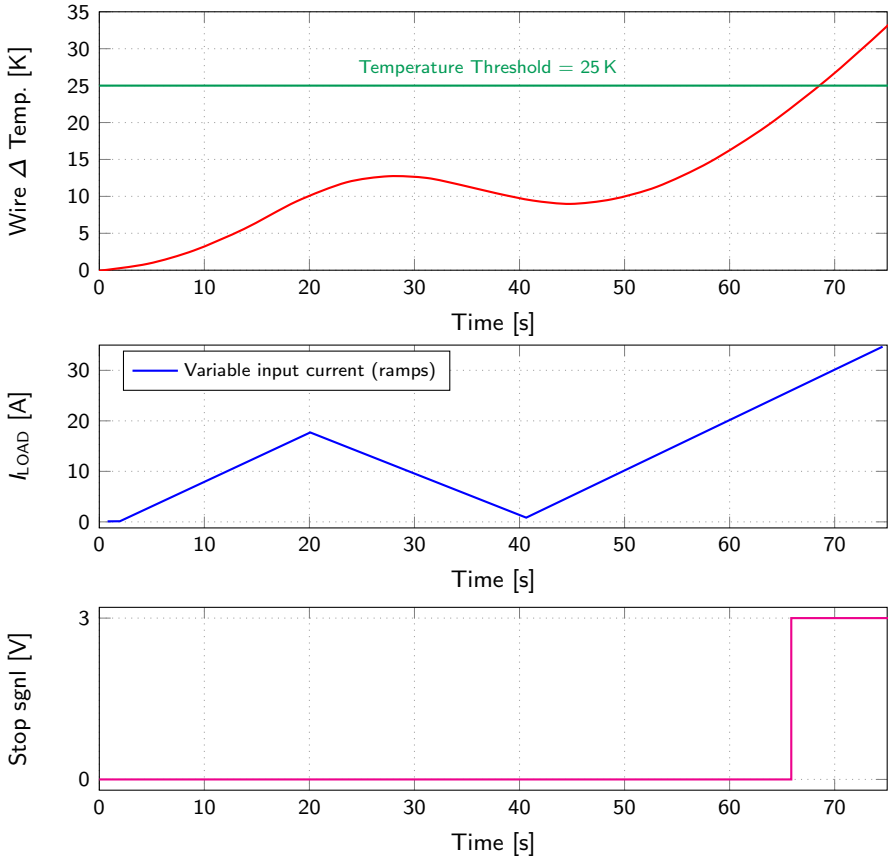


Figure 8.9: Temperature behaviour analysis with constant current.
Ideal stop time: 66.52 s
Digital stop time: 65.87 s

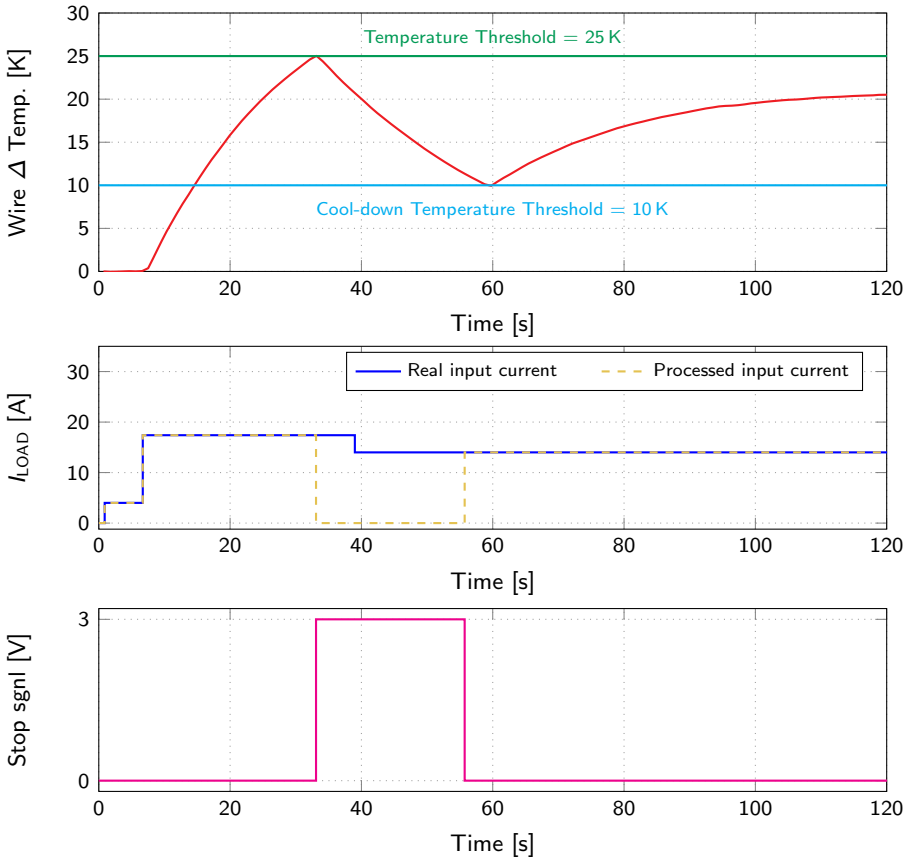


Figure 8.10: Temperature behaviour analysis with variable currents.

Conclusions

A mixed-signal multi-functional system for current measurement, open-load detection and over-temperature protection for automotive applications has been presented. It has been shown an efficient design can be carried out by merging the three functionalities by exploiting the specifications. Moreover it has been shown how the design of the analog and the digital blocks has been carried out in order to effectively use the BCD power-optimized technology in terms of area.

A circuit implementing the starting 5 b ADC has been designed in order to gain familiarity with the technology, which is not tailored for high precision blocks. The simulation results showed the used BCD process to be suitable for targeted applications and the chip prototype has been manufactured, measured and validated with laboratory tests.

After the 5 b ADC design and validation, an 8 b ADC has been implemented for the purpose of increasing the system accuracy and fulfil the accuracy requirements for $I_{\text{load}} = 10\,\text{A}$. It has been shown how the design took advantage of the system specifications in order to relax the performance when possible. Particular attention has been given in to the area usage and to the yield, which are extremely important in any automotive application. The simulations satisfied the system requirements for the accuracy and those results have been confirmed once the relative chip prototype has been measured.

Finally, the full system fulfilling the remaining requirements has been designed. Beside the already implemented features, it provides the additional detectable I_{load} values at 100 mA, 200 mA, and 300 mA, the open-load detection and the thermo-electrical stress protection. The system has been designed and the simulation results satisfied the overall requirements and thus has been taped-out. The prototypes are arriving in the next months in order to be evaluated with measurements.

Appendix: Publications

A paper on the 8 b ADC presented in Chapter 6 has been published in the 2017 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME) held in Taormina (Italy) and it is appended in the next pages.

A mixed-signal multi-functional system for current measurement and stress detection

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***Abstract*—This paper presents the development of a mixed-signal multi-functional system for current measurement and electrical stress detection. The system is composed of a tracking ADC and a double range (a coarse and a fine one) current-steering DAC. The coarse range, designed for the full-scale input values [0A:108A], has a 5b resolution and it is used for the stress detection feature. The fine range is for lower input current values [4A:14A] and it is used for the current measurement, where more accuracy is required. With respect to the full-scale, the resolution of the fine range is 8b.**

I. Introduction

The proportion of electronic components used in motor vehicles has been increasing steeply in recent years. Today, electronics represent around 25% to 30% of a modern car production costs but, more importantly, electronic systems now contribute 90% of car innovations and new features, from emission levels to safety systems (both active and passive) and entertainment/connectivity features [1]. In terms of temperature and vibration, however, the car's environment is very harsh. As a result, electronics design for automotive industry applications presents several challenges.

In this scenario the BCD (BIPOLAR-CMOS-DMOS) is a key technology for power ICs (Fig. 1). This combination of devices aims to bring improved reliability and smaller chip area.

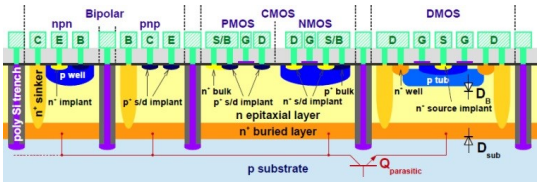

Fig. 1: BCD technology

Regarding the BCD process, several studies[2]–[4] address the need of increasing the technology robustness with respect to the electrical stress. In fact, all integrated power-transistors have to be robust against high energetic pulses. In some applications these devices may be connected directly to the cable harness within cars and so demanding ESD-requirements have to be fulfilled. Moreover, because of the harsh, high-temperature environments, a robust low-voltage CMOS platform is needed. For these reasons it is important not only to ensure the circuits functionalities by technology, but also by design, implementing solutions which allows monitoring, and possibly detecting critical events that could damage devices under severe electrical stress. Besides this aspect, another important trend [2]–[4] in the BCD technology is to decrease the process expenses, and ultimately reduces the prices for end customers.

The primary demand for robustness and the tendency to reduce fabrication-related costs make the BCD a power-optimized technology which is not specifically tailored for high-accuracy signal processing blocks (as ADCs). For instance, some technologies are not featured with elements such as MIM or MOM capacitors therefore all the mixed-signal processing needs to deal, if required to [5], with non-linear elements like MOSFET caps in order to provide the desired performances. For these reasons, designing with a BCD power-optimized technology with the automotive environment presents new challenges for mixed-signals designers which are required to explore new solutions.

This paper deals with the design of a multi-functional system for current measurement and electrical stress detection, whose purpose is increasing the reliability by design. These two features demand two different accuracy specifications. The first one is stricter for the lowest input-scale values whereas the second one is more relaxed on the entire range.

This work presents an area-saving solution based on a double-scale ADC, which allows having more resolution only when required and embedding the two functionalities in the same structure.

In the first part of the paper the system performing the electrical stress detection is described showing the current measurement digitalization with 5b resolution. In the second part the resolution enhancement is shown, which is implemented only within a specific input current range as per system requirement. This input ranges distinction is explained in Section II.

II. System Requirements

As first remark this design shall respect all the following specification within a 4.5σ yield and in a [-40°C:150°C] temperature range, which is typical for any automotive applications. The input current I_{load} ranges from 0A to 108A and the signal bandwidth is 1kHz. The system is required to ensure monotonicity in the A-to-D conversion.

The current measurement functionality, beside the monotonicity, requires ±10% accuracy with a 5% budget for the quantization error for I_{load} = [4A:13A]. For larger values this specification is relaxed and common to the stress detection one. This leads to a 5b ADC design over the [4A:13A] range, which translates in an 8b resolution with respect to the full scale. In this scenario, the Least Significant Bit (LSB) would be $108A/255 \approx 0.4A$, ensuring therefore ±5% quantization error for the lowest current value of interest I_{load} = 4A.

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The protection feature requires for a stressful event to be detected. The stressful event would present as an input signal whose amplitude is around 20 times larger than the nominal input signal (which is around 5A). In this case scenario, since only the event needs to be detected rather than its amplitude, the conversion is not required to be highly accurate. This allows setting for the electrical stress detection functionality a 5b resolution.

III. Multi-functional system concept

Fig. 2 shows the basic multi-function concept. The input current I_{load} flowing in the right side through a Power Transistor (PT) is down-scaled by a factor 1/20k into the I_{sense} current on the left side through the PT scaled replica. The two transistors are kept in linear region by the Gate Driver and the PT scaled replica resistance R_s is 20k times larger than the PT resistance R_l. The currents I_{sense} and I_{load} are indirectly compared by means of the V_s and V_l voltages thanks to a comparator (Comp). Considering $R_l = 3\text{m}\Omega$, and $V_{DD} = 3\text{V}$, the relationship between the currents and the voltages is described by (1-3).

$$V_l = -I_{load} \cdot R_l + V_{DD} \quad (1.a)$$

$$V_s = -I_{sense} \cdot R_s + V_{DD} \quad (1.b)$$

$$I_{load} = [0\text{A} - 108\text{A}] \quad \rightarrow \quad V_l = [3\text{V} - 2.676\text{V}] \quad (2)$$

$$\text{If } V_s = V_l, \text{ then } I_{sense} = I_{load}/20k = [0\text{A} - 5.4\text{mA}] \quad (3)$$

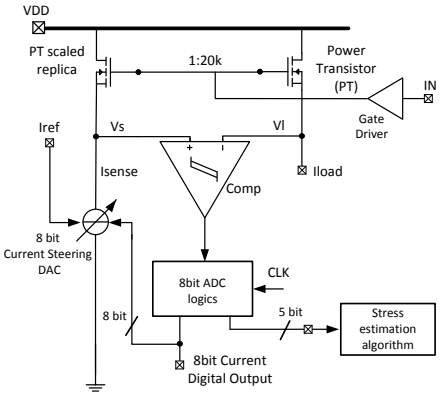

Fig. 2: Multi-function system concept

Referring to Fig. 2, the loop composed of the comparator (Comp), the ADC logics, and the current steering DAC serves the purposes of subtracting an LSB_{Isense} at each clock (CLK) period. In particular, according to (1.a), if $V_s > V_l$ then I_{sense} needs to be increased, and vice-versa. Since the system is following the input analog signal, this loop implements a tracking ADC solution.

The ADC binary output is used in order to get information on the current value and it is also externally digitally-processed for the stress detection feature.

IV. Multi-functional system design

A. ADC design considerations

The system design has been carried out in order to exploit the specifications reported in Section II. Two resolutions requirements are present: 5b for the full range input Iload [0A:108A], which are used for the stress-detection feature, and 8b resolution for Iload = [4A-10A], used for the current measurement.

A first trivial approach is to use a full 8b ADC. However this solution would provide a large accuracy also where not required by the specification at the cost of a large sizes. In fact both of the possible implementations, thermometric and fully-binary weighted, would need large area: the first one in terms of transistors (2^8 = 256 devices) and the second in terms of digital control and matching [6], as for the fully-binary weighted architecture the MOSFETs must be properly sized in order to ensure the monotonicity, i.e. no conversion error in the MSB transition.

Another approach is a logarithmic-scale ADC which would provide higher resolution only on the lowest values. However this implementation would require a non-linear DAC whose cells could only be matched at the cost of an high area consumption [7].

The solution presented in this paper consists of a double-ranged ADC which provides the required resolution only when necessary. The resolution switch from fine (8b) to coarse (5b) conversion is set at I_{load} = 13.7A corresponding to bit 8 for the fine ADC. This is achieved by adding to the full-range 5b ADC an additional 3b ADC for the lowest range input values, for a total 8b resolution.

With respect to a full 8b converter, which needs 2^8 = 256 devices, the proposed solution makes use of 2^5+2^3 = 40 devices. The most critical transition for the monotonicity is moved from bit 127-128 (MSB) switching to bit 15-16 (MSB) switching for the coarse 5b ADC, bit 3-4 (MSB) switching for the 3b ADC, and to bit 7-8 switching for the fine (8b) ADC corresponding to the transition from the 3b ADC to the 5b ADC. The last one is the most critical has the two ADC present MOSFETs with different electrical characteristics as explained in Sec. II.B. Nonetheless, this implementation requires less effort in terms of matching (and therefore less area) with respect to an 8b ADC due to the much fewer devices involved.

Using the double-range ADC a 10% quantization error would affect the system when switching between 5b and 8b resolutions due to the abrupt transition. For this reason an intermediate conversion range has been introduced. The middle steps go from I_{load} = 13.7A to I_{load} = 27.9A with 7b resolution. In this way the quantization errors at both the switching values are reduced to 5.6%. Moreover the transition values have been designed so to use at most 5 out of 8 bits available at each range. In fact, in the first range the five LSBs are used, in the second range from the third to the sixth MSBs, and in the third range the five MSBs. This solution allows reducing the logics complexity as digital operations operate at most on 5 bits.

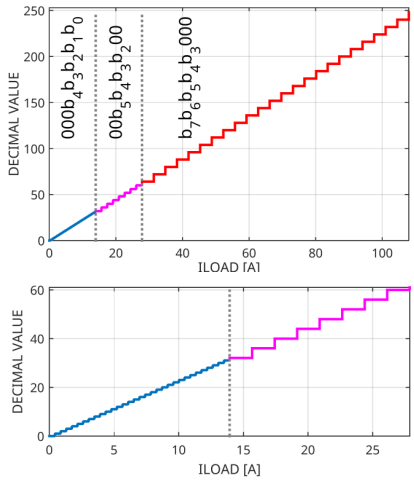

Fig. 3: Multi-ranged ADC concept plot. For each range the used bits are reported. The lowest I_{load} values are zoomed-in in the bottom plot.

B. Block specifications

Referring to Fig. 2, the non-idealities affecting the design are:

- 1:20k ratio whose accuracy is dictated by the technology;
- Reference current accuracy (±3% at 4.5σ);
- DAC accuracy;
- Comparator accuracy.

Based on these considerations the margin to fulfil ±5% requirement for the lowest range is very narrow and the block specs must be carefully set.

In order to set the comparator input offset specification, some considerations on the LSB values need to be done. Referring to Fig.2 the 8b I_{load} LSB_{IL} is 0.4A whereas on the I_{sense} side it is down-scaled by 20k to LSB_{IS} = 21.2µA. According to (1.a) this leads to have in the voltage domain an LSB_V = 1.3mV. The maximum voltage off-set affecting the comparator shall produce an error negligible with respect to the other non-idealities and therefore much less than one LSB_V, setting the maximum off-set value around 30µV at 4.5σ.

The DAC block shall be designed so to ensure monotonicity and to have less than 0.5 LSB current error (according to the considered range) for 4.5σ yield for each ADC outputs.

The comparator IP was already available. The block was designed with an auto-zero scheme, ensuring a 0V mean input offset, and 27µV random input offset at 4.5σ. It is driven with at 622.5kHz clock and the current consumption is 80µA.

C. Transistor level design

In this work a 350nm BCD power-optimized technology has been used, which integrates high-power devices with low-voltage components.

The current steering DAC has been first developed in order to provide the 5b resolution required on the I_{load} full-scale.

A fully binary implementation has been chosen for the DAC so to avoid any decoder required by a (partial) thermometric solution because digital blocks are very area-consuming in this technology. Each of the binary-weighted cell forming the DAC has been carefully designed in terms of size and threshold voltage mismatch, according the well-known Pelgrom's transistors-mismatch model [8].

Regarding the monotonicity, being the DAC fully-binary, the major concern is due to the MSB transition [9], i.e. when passing from the ADC output code (driving the DAC) 15_{DEC} (I_{sense} = 2.613mA) to 16_{DEC} (I_{sense} = 2.787mA) and, the more the binary cells are matched, the less this transition is critical.

Moreover, the DAC cells have been cascoded so to reduce the channel length modulation effect. In the full-scale range, where 5b are considered, the reference current I_{ref} is equal to 1 LSB on the I_{sense} side, i.e. 174.2µA.

The ADC logic circuitry implements a tracking algorithm which increases or decreases the I_{sense} current by one LSB whether V_S is respectively greater or less than V_L.

Table 1: MC PLSs results of the 5b DAC

Bit [DEC]	TEMP [°C]	Mean [A]	Sigma [A]	Ideal Value [A]	4.5*sigma [# of LSBs]
1	-40	1.75E-04	1.17E-06	1.742E-04 (LSB)	0.03
	27	1.75E-04	9.52E-07		0.02
	150	1.74E-04	7.49E-07		0.02
2	-40	3.50E-04	1.98E-06	3.484E-04	0.05
	27	3.49E-04	1.62E-06		0.04
	150	3.49E-04	1.27E-06		0.03
4	-40	6.99E-04	3.51E-06	6.968E-04	0.09
	27	6.98E-04	2.85E-06		0.07
	150	6.97E-04	2.22E-06		0.06
8	-40	1.40E-03	6.67E-06	1.394E-03	0.17
	27	1.39E-03	5.43E-06		0.14
	150	1.39E-03	4.23E-06		0.11
15	-40	2.62E-03	1.22E-05	2.613E-03	0.32
	27	2.62E-03	9.94E-06		0.26
	150	2.61E-03	7.73E-06		0.20
16	-40	2.79E-03	1.32E-05	2.787E-03	0.34
	27	2.78E-03	1.08E-05		0.28
	150	2.78E-03	8.40E-06		0.22
31	-40	5.41E-03	2.51E-05	5.400E-03	0.65
	27	5.40E-03	2.04E-05		0.53
	150	5.40E-03	1.59E-05		0.41

Montecarlo (MC) Post-Layout Simulations (PLS) results are reported in Table 1, with different temperature value (it could be noticed that the worst case is with TEMP = -40°C). The Bit column represents the digital word driving the DAC expressed in decimal. Mean and Sigma columns come from the MC analysis and they may be compared with the ideal values. The last column represents 4.5 times the standard deviation normalized to the I_{sense} LSB = 174µA. Mean values are in all cases very close to the ideal ones. Regarding the monotonicity, it may be observed the 4.5×sigma values corresponding to bit 15 and 16 are both less than 0.5 LSB, ensuring therefore monotonicity.

D. Resolution enhancement implementation

For the required accuracy in the lowest input current range, the ADC has been enhanced with 3b in the [0A:14A] range, (for a total 8b resolution with respect to the full input range) as shown in 3. With this resolution, the I_{load} LSB is 0.42A, and on the I_{sense} side is 21.9µA (notice that 21.9µA = 174.2µA/8, i.e. one eighth of the 5b DAC LSB).

Table 2: MC PLSs results of the double-ranged DAC

Bit [DEC]	Mean [A]	Sigma [A]	Ideal Value [A]	4.5*sigma [# of LSBs]
1	2.22E-05	4.04E-07	2.19E-05 (LSB)	0.08
2	4.43E-05	6.90E-07	4.38E-05	0.14
3	6.64E-05	9.61E-07	6.55E-05	0.20
4	8.84E-05	1.24E-06	8.74E-05	0.26
7	1.55E-04	2.06E-06	1.53E-04	0.42
8	1.75E-04	1.13E-06	1.74E-04	0.23

From the transistor-level implementation point of view this has been done by adding a 3b DAC to the main one instead of designing a full 8b DAC, which would be much area-consuming, and by adjusting the logic circuitry to take into account the different-resolution ranges.

The supplemental 3b DAC has been designed matching the 5b DAC one, i.e. its binary cells are identical to the previous ones. The reference current I_{ref} is equal to its LSB (21.9µA). In this case the major critical point in terms of monotonicity is represented by the DAC transition which happens, considering the 8b resolution, when passing from the ADC output code (driving the two DACs) 7_{DEC} (I_{sense} = 151.1µA) to 8_{DEC} (I_{sense} = 174.2µA). MC analysis results are reported in Table 2 where only TEMP = -40°C (worst case observed in Table 1) is considered. Also in this case the mean values are very close to the ideal one. However sigma results are slightly worse than the 5b DAC because a lower current is flowing in the new binary cells; in fact, since the transistors sizes are the same as before a decreased current brings a reduced overdrive voltage and therefore the cells are more sensitive to threshold voltage spread. Nevertheless, monotonicity is ensured both within the 3b DAC considering the MSB transition from 3_{DEC} (I_{sense} = 65.5µA) to 4_{DEC} (I_{sense} = 87.4µA), and within the DAC switching, as for both of the cases, the 4.5×sigma spread is less than 0.5LSBs.

Spectral analysis has been performed by feeding the system with input current tone at the node V_I (Fig. 2). The amplitude of signal is set from 0A to 108A (the full-scale value) and its frequency to 1kHz (the input bandwidth). Fig. 4 shows the Power Spectral Density (PSD) expressed in dB at the node V_s considering the full-scale input. The Spurious-Free Dynamic Range (SFDR) is 30dB. Fig. 5 shows the PSD at V_s considering the [0A:13.4A] input range and the SFDR is 27dB.

Considering the small-values range these results are expected because for an ideal 5bit ADC the maximum (i.e. taking into account only the quantization noise) SFDR is 28.3dB, which is very close to the SFDR observed in Fig. 5. On the full scale, the used ADC have an effective number of bits larger than 5 because of the highest resolution at lowest values and the SFDR is therefore larger than the ideal 28.3dB.

Conclusion

A mixed-signal multi-functional system for current measurement and electrical stress detection for automotive applications has been presented. It has been shown how the design took advantage of the system specifications in order to relax the performance when possible. Particular attention has been given in order to fulfil the requirements in terms of yield and area, which are extremely important in an industrial environment. Therefore, the design of the mixed-signals circuit has been carried out in order to effectively use the 350nm BCD power-optimized technology.

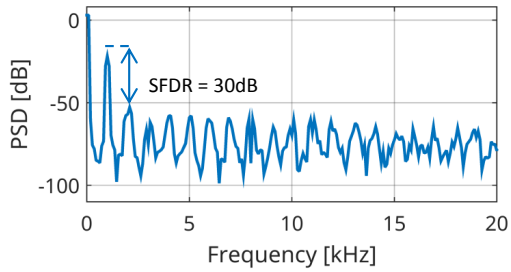

Fig. 4: V_s node PSD with full-scale input tone at 1kHz

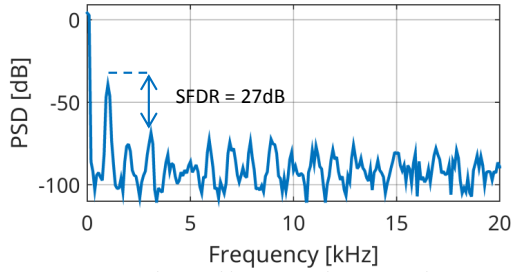

Fig. 5: V_s node PSD with [0A:13.4A] input tone at 1kHz

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