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Cognome / Surname RESTA Nome / Name FEDERICA

Matricola / Registration number 787811

Tutore / Tutor: Massimo GERVASI

Cotutore / Co-tutor:
(se presente / if there is one)

Supervisor: Andrea BASCHIROTTO
(se presente / if there is one)

Coordinatore / Coordinator: Marta CALVI

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UNIVERSITÀ DEGLI STUDI DI MILANO-BICOCCA
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Federica Resta

Tutor: Prof. Massimo Gervasi

Supervisor: Prof. Andrea Baschirotto

Coordinator: Prof.ssa Marta Calvi

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Dedicated to Salvatore

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Introduction

This thesis concerns the electronic circuits used in the physical world. All the discoveries are based on thousands of the data proper processing with potent calculators.

Statistical analysis have been done starting from all events detected and processed through a dedicated electronics. The electronics is inserted between the detectors and the stations of data analysis.

The role of the electronic circuits in the High Energy Physics (HEP) experiments is fundamental. The engineers must collaborate with the scientists to understand the background and create consequently efficient systems. Starting from brief consideration, this thesis includes four chapters organized as follow.

A brief summary of the entire work is inserted in the **Part I** to fix the goals of my activities.

Then, the **Part II** is dedicated on a simplified description of the application field and the goals to achieve with future experiments. In particular, some details on the effects induced by the radiation to integrated electronic component are provided.

Part III and **Part IV** represent the core, including the integrated circuit design done during the three years of PhD. These are dedicated on a read-out front-end for ATLAS experiment and for Pixel detectors, respectively. Their characterization comes from simulations and measurements of the integrated prototypes.

Before concluding, there is the **Part V** with the correlated publications.

Part I

Abstract

Abstract

Physic researches and discoveries depend heavily from efficiency and reliability of the High-Energy Physics (HEP) experiments. The main goal is to study the fundamental constituents of the matter in terms of elementary charge particles, their interactions and their secondary products. Part of these phenomena have already been studied and they have been used for Standard Model definition. The new challenges of CERN project aim to provide other details on the new charged particles as neutrinos and Higgs Bosons.

The Large Hadron Collider (LHC - [1]) at the CERN works every day for this purpose. It is the world's largest and most powerful particle accelerator. It has a superconducting magnetic ring structure able to guide two high-energy particle beams. The beams have opposite directions and they travel to light speed. Charged particles are generated from beam collisions and they are accelerated toward a proper detector. Different detectors are located in different points of the collider. They are organized in shell structures and are designed to detect few topology of particles. Typically, the parameters useful to identify a charged particle are momentum, electrical charge, energy, time of flight and distance.

Detectors design is important but it is enhanced from proper electronic read-out systems. A big experiment requires a hard work of scientists, engineers and technicians. In the last years, electronics parts are more and more efficient and compact. CMOS integrated solution are preferred to discrete one allowing major reliability, cost reduction and performance improvement. The design is not trivial but not impossible. Some characteristics are directly dependent from the electronic designer and his capability to manage the external parasitic effects, as the parasitic capacitance of the connected detector. Unfortunately, other phenomena must be taken in account and they can not be completely eliminated. They include the radiation effects on electronic components behavior. CMOS technology influences strongly the integrated circuit performance and its radiation hardness.

Three read-out front-end circuits for HEP experiments have been designed, integrated and measured. Two of them represent two different prototypes realized in IBM 130nm technology for ATLAS experiment at CERN laboratory. The third one is the first read-out front-end for Pixel detectors in CMOS 28nm technology. The circuits have been designed for two different scenarios in terms of detector parasitic capacitance,

detectable input charges, supply voltage, threshold voltage, power consumption and noise. In overall cases, the integrated systems provide information about amount of detected input charge and arrival time within 25ns. This aspect is very important and allows avoiding mistakes. Successive collisions lead to spurious signals presence and a single detection could have information about two different events. Maintaining the processing time within 25ns, consecutive collisions are detected as different events.

Part II

System Overview

1
Electronic in the physical experiments

1.1 Background and Motivations

The most important discoveries on the matter components has been developed in the CERN laboratory at Geneva exploiting the world's largest and most powerful particle accelerator, known as Large Hadron Collider (LHC). The collider uses few nanoseconds to create high-energy proton-proton collisions at speeds close to light speed. Two opposite beams are accelerated in a ring with superconducting magnets and accelerating structures. The temperature of the system is very low (around −271.3 °C) limiting the loss energy and/or conductivity. For this reason, the accelerator temperature is controlled by distribution system of liquid helium [1].

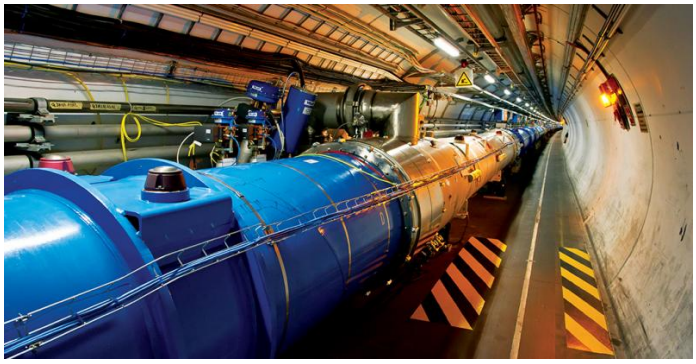

Figure 1.1: Large Hadron Collider (form CERN [1])

Groups of physics and engineering collaborate with the main goal to organize overall experiments, from events generation and detection up to the final data analysis. Different detectors interface with the LHC to analyze the particles produced by the collisions. They are organized in a shell-structure and each of them is able to detect a specific range of charged particles. For each detectors, there is an associated experiment. ATLAS (A Toroidal Lhc ApparatuS) and CMS (Compact Muon Solenoid) are the biggest ones because they investigate the large range of physics possible. The first is thought to have information about energy up to 14 TeV, direction and type of particles. CMS experiment, instead, is very useful for Standard Model studying, including Higgs bosons, muons, photons and electrons.

Physics experiments without electronic control don't exist. In the years, detectors and search methodology of the particles have been developed with the main target to see more and further.

At the same time, the evolution implied a major attention on the electronic parts, on their efficiency and reliability. These requirements led to replace an electronics based on discrete components with integrated circuits. The advantages were remarkable. The costs have been drastically reduced although a different number of prototype must be produced before to have optimal performance.

CMOS technology allows designing mixed-signal circuits, named ASIC, able to work in different worlds, i.e. digital and analog. A high performance analog part is closer to a dense digital logic with considerable benefits of efficiency for unit of area and driving. Integrating a complete mixed-signal circuit in a die, interface and load managing issues are reduced. The ASIC development depends on scaling down technology. Performance, sizing, resolution and number of components integrable in the same area are substantially increased with more work for electronic designers.

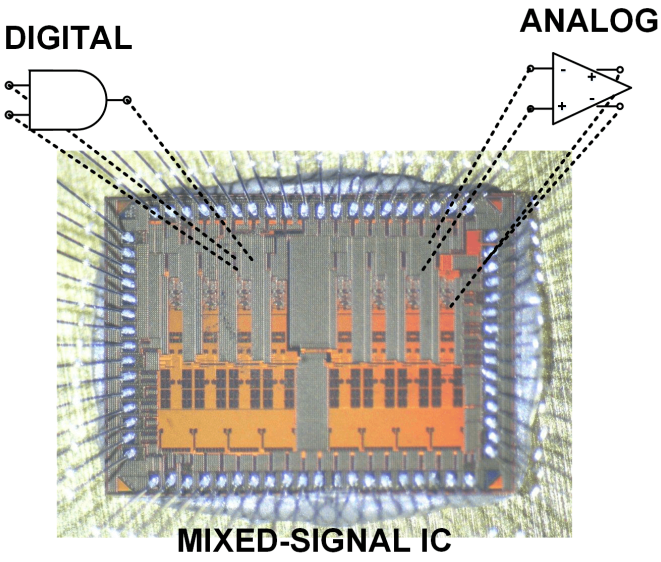

Figure 1.2: Mixed Signal Integrated Circuit

1.2 Radiation Environment

Physics experiments for discovery of new charged particles must deal with the radiation and damage caused. Particle accelerators were developed to produce artificial radiation particles with different intensity and energy. Electronic components and surrounding materials are typically closer to the interaction points and they are exposed to significant environment variations. Each material shows a certain resistance

to these effects depending from its intrinsic characteristics and the incident particles. The type of the material, its mass, its thickness and other parameters could facilitate the radiation absorption. Regarding the damages induced by the incident particles, they depend on kinetic energy, mass, charge, incident direction and velocity. The radiation particles, which move inside a semiconductor structure, can be divided in two groups: charged and neutral particles.

Electromagnetic interactions between the particle and the constituents of the atoms produce charge particles as protons, heavy ions and electrons. Photons, neutrons and neutral pions belong to neutral particles group, instead. Photons result from electromagnetic interactions, the others particles are generated by strong interactions between particles and nuclear components.

1.2.1 Surface and Bulk Damage

A material bombarded with radiation can change slightly or drastically its intrinsic properties [2], deteriorating the performance of the sensors and/or the electronics. In general, the presence of radiation may lead to:

- full inefficiency
- leakage current increment
- crystalline structure modification
- false event detection
- noise increment
- gain decrease
- digital failures.

These effects derive from two classes of damages: Surface and Bulk Damages.

Surface Damage

An ionization energy loss creates an accumulation of positive charges in the oxide (SiO_2) and traps at Si/SiO_2 interface. Radiation particles, i.e. electrons and protons, ionize the Si atoms of crystal and the molecules in the insulating layer, which cover the silicon crystal [3]. Typically, the average ionization energy to produce an electron-hole pairs is 3.6 eV for silicon and 17 TeV for SiO_2. Increasing the ionizing radiation dose, traps and holes densities rise affecting electrical properties and performance of silicon devices.

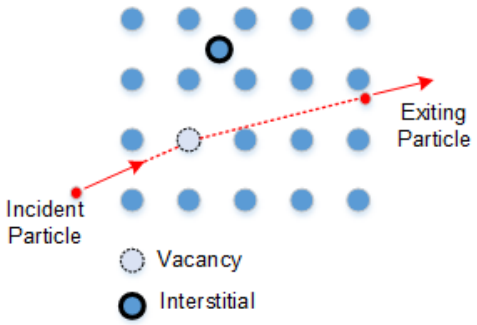

Figure 1.3: Non Ionizing Energy Loss effect

Bulk Damage

Bulk damage is due to the Non-Ionizing Energy Loss (NIEL - [4] - figure 1.3) and affects sensors and detectors. The NIEL is defined as the amount of energy released into the material by an incident particle, which is not loss in ionization. This energy breaks the crystal lattice introducing defects in the material and changing the effective doping concentration or the leakage current. Obviously, the Signal-to-Noise Ratio (SNR) could be drastically reduced [5] [6] [7].

1.3 Radiation and CMOS transistor

A typical CMOS transistor is shown in figure 1.4. It is obtained from a silicon wafer with a sequence of steps (i.e. ion implantation, deposition of oxides, etching, annealing, etc.) widely described in [8]. At the end of the fabrication process, a transistor is a device with four terminals: source, gate, drain e bulk. It becomes conductive device when is proper biased. In particular, applying a positive voltage at the gate (respect to the source), a negative charged inversion layer appears connecting source and drain. This is a conduction channel with resistor feature [9].

A current I_{DS} flows in the channel when at the drain there is a positive voltage respect to the source. The current is due to a flow of electrons from drain to source. The channel conductivity and the number of the electrons that reach the source depends on the speed acquired along the channel, on the gate and bulk voltages, on the C_{ox} and C_D channel capacitances. The I_{DS} current starts flowing as soon as the overdrive voltage becomes positive. It is defined as the difference between V_{GS} and V_{TH} (Threshold Voltage) voltages, as shown in figure 1.5.

The trend of the I_{DS} curve depends on the number of free carriers along the channel, which is directly related to V_{DS} and V_{GS}-V_{TH} voltages. For small V_{DS}, the channel appears homogenous with a resistor behavior ($I_{DS} = \frac{V_{DS}}{R_{DS}}$). Increasing V_{DS}, the current assuming a parabolic trend up to reach a saturation value. Linear region is the

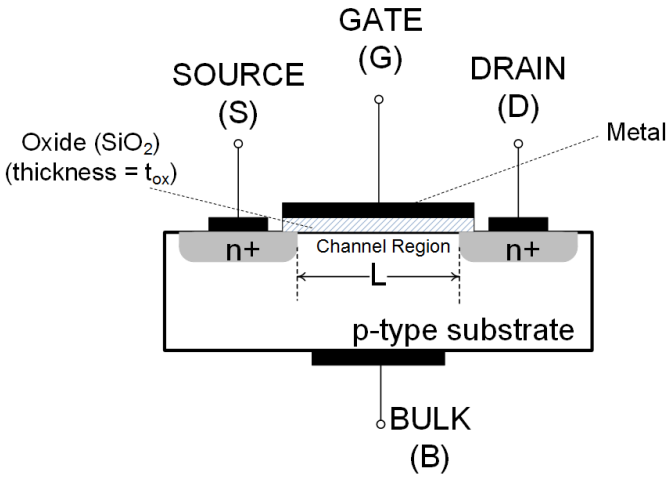

Figure 1.4: Typical CMOS transistor

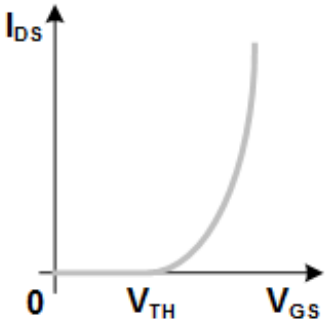

Figure 1.5: I_{DS} vs. V_{GS}

first one; saturation region is the last one. Each region is characterized by a channel resistor R_{DS} given by 1.1.

$$\mathrm{R_{DS}} = \rho \frac{\mathrm{W}}{\mathrm{t_{OX}}} = \frac{1}{\mathrm{n\,q\,\mu_n}} \frac{\mathrm{W}}{\mathrm{t_{OX}}} \tag{1.1}$$

where ρ is the resistivity of the channel, t_{OX} is the MOS oxide thickness, μ_n is the mobility coefficient of the electrons near the silicon surface below the oxide layer, n is the number of the free carriers (electrons) resulting from doped silicon, and free to move along the channel. Considering the small signal model of a transistor, a small signal input voltage (v_{gs}) application produces a transconductance g_m given by 1.2.

$$\mathrm{g_m} = \frac{\partial \mathrm{I_{DS}}}{\partial \mathrm{V_{GS}}} \tag{1.2}$$

All transistor features depend on flow of free carriers in the channel and their number. They could change in radiation environment. The main effect related to this phenomena is a reduction of minority charges lifetime. Ionizing particles generate electron-hole pairs the inside oxides [10] that could disappear in the gate and the substrate for quantum tunneling or remain in the oxides under the influence of the electrical field. The electrons, highly movable charges, are easily swept out from the oxide whereas the holes, being slower, move towards the SiO_2-Si interface. Some of these holes can be trapped in the lattice imperfections, originating this way a fixed positive charge in the oxide. Another effect of the ionizing radiation is the creation of the traps at the SiO_2-Si interface [11] [12]. The probability of having trapped positive charge in the oxide next to the silicon interface depends directly on the number of defects in the oxide. Trapped holes inside oxides and the interface traps generation affect the transistor electrical parameters.

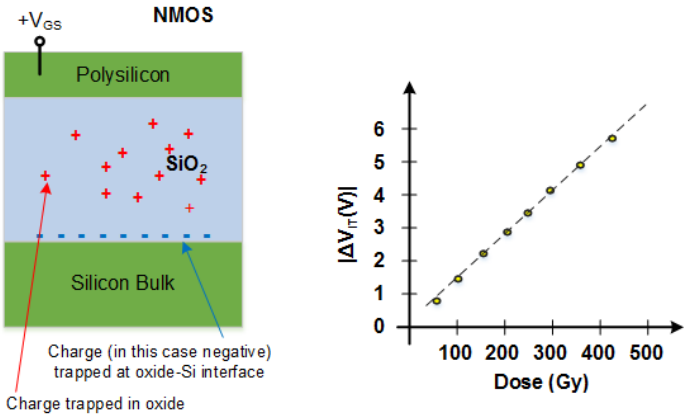

Figure 1.6: Threshold Voltage Shift due to Interface Traps

Threshold Voltage Shift

Positive charged trapped in the oxide (ΔV_{OX}) and interface traps (ΔV_{IT}) appear after irradiation. For this reason, flat-band voltage changes shifting the threshold voltage according to the 1.3 [13].

$$\Delta \mathrm{V_{OX}} = -\frac{1}{\mathrm{C_{OX}}} \int_0^{\mathrm{tox}} \frac{\mathrm{x}}{\mathrm{t_{OX}}} \rho(\mathrm{x})\, \mathrm{dx} \tag{1.3}$$

where t_{OX} is the thickness of the gate oxide, C_{OX} is the capacitance per unit area and ρ(x) is the charge distribution in the oxide per unit volume, as function of the distance from the gate-oxide interface (x). From 1.3 results that the voltage shift is negative when the trapped charges are positive. The presence of interface traps, instead, causes

a positive (ΔV_{IT}) shift according to 1.4 and figure 1.6.

$$\Delta \mathrm{V_{IT}} = -\frac{\Delta \mathrm{Q_{IT}}}{\mathrm{C_{OX}}} \tag{1.4}$$

where ΔQ_{IT} is the charge difference, per unit area, which fills the interface states before and then the irradiation. In NMOS transistor, interface state creation is a slower phenomena that causes an initial threshold voltage reduction followed by a definitively increase. It's worth to be said that, especially in more scaled technologies, the thinner gate oxide makes the radiation-induced charge contribution negligible if compared with the effects of the interface states. For this reasons the NMOS transistor threshold voltage tends to increase in any case.

Leakage Current

Leakage current may be generated or worsened with charges trapped in the oxides. This effect depends on Shallow Trench Isolation (STI) oxide and its thickness. With the scaling down, the thickness of the gate oxide is reduced but STI oxide doesn't change [14]. As consequence, the irradiation creates a large amount of positive charges in the STI oxide. It means that a leakage current path between source and drain arises [15]. Nonertheless, particular layout techniques (i.e. dummy and enclosed transistors) can help to manage this issue.

1.4 Microelectronic Irradiated Circuits

Radiation effects can appear after short or long time of exposure and they are classified in Single Event Effects (SEE) and Total Dose Effects (TDE), respectively. ASIC includes analog and digital parts that may respond to both effects in different ways. A circuit shows a proper radiation hardness mainly dependent on intrinsic properties of the CMOS technology. Quality and quantity of the radiation influence heavely this feature. Ionizing dose (defined in 1.5) is an index of the incident radiation.

$$\mathrm{IONIZING\ DOSE} = \frac{\mathrm{Energy\ Imparted\ by\ Ionizing\ Radiation}}{\mathrm{Mass\ of\ the\ Target}} \tag{1.5}$$

The purpose of this paragraph it to compare SEE and TDE in microelectronic integrated circuits.

1.4.1 Single Event Effect

Single Event Effect (SEE) is induced by a single particle that crosses a sensitive region of the device inducing a macroscopic multifunction on the system. It is not predictable and can occur suddenly. For a given radiation environment, the mechanism of an SEE

and the chance of it occurring depend on the device and the technology. Digital world is more sensible to SEE because an incident particle could cause data corruption, spurious signal or device destruction. For example, if an accumulated charge is collected in a "sensitive" node, inside a memory cell, the information stored can be lost [16].

The probability to have wrong bits depends on the energy of the incident particle and the minimum amount charge, needed to flip state for a storage element. With the scaling down CMOS technology development, the circuits are smaller and the number of the single particle that reach sensible nodes decreases. Nevertheless, the parasitic capacitance on these nodes is smaller and then a less energy is required to cause a bit inversion. Some classes of SEE are:

- *Upset (SEU)*: logic state change (i.e. SRAM memory)
- *Latch Up (SEL)*: creation of low-impedance short circuit that triggers a parasitic PNPN structure blocking proper functioning
- *Single Event Burnout (SEB)*: an ion induced current flow turns on the parasitic npn transistor below the source that leading to device destruction if sufficient short-circuit energy is available
- *Single Event Gate Destruction/Rupture (SEDG/R)*: an ion through the gate (but avoiding the p-regions), generates a plasma filament through the n-epi layer that applies the drain potential to the gate oxide, damaging (increased gate leakage) or rupturing the gate oxide insulation (device destruction).

1.4.2 Total Dose Effect

Total Dose (TD) effect is a consequence of kinetic energy transfer or atoms ionization. It is cumulative and interests many particles. The result is the gradual appearance of surface and bulk damages that may be monitored and predicted. Analog part is more sensible respect to digital one. Indeed, threshold voltage shift and leakage current generation change operating point, current and other parameters. These variations are not critical for digital part because they don't modify the logic ports behaviour.

1.5 CMOS scaling down

CMOS integrated circuits are more and more smaller thanks to sub-nanometer technologies development. This represents a challenge for analog electronic parts that remains essential despite the digital one is becoming more important. Front-end electronics may benefit from scaling in terms of functional density (i.e. pixel application) and digital performance. At the same time, analog design must deal with reduced supply voltage, decreased dynamic range, statistical doping effects, etc.

Smaller devices are obtained by shrinking the gate length. This leads to faster

and more density circuits. To avoid short-channel effects, drain and source depletion regions are made correspondingly smaller by increasing substrate doping concentration and decreasing reverse bias. The supply (V_{DD}) and the threshold (V_{TH}) voltages result thus reduced and increased, respectively.

The gate oxide thickness reduction represents an obstacle to classical scaling down. In fact, in very thin oxides, direct tunneling of carriers leads to a large gate leakage current.

The end of Moore's Law is shifted with new materials and structures discoveries. The increment of the system level integration continues to be important to integrate a wider and more heterogeneous set of components. The new era of device scaling is introduced in [17] [18]. Transistors with high-k and metal gate allow to overcome the gate oxide scaling barrier challenging the leakage current increment. High-k oxide should satisfy the following properties:

- High Dielectric constant and barrier height
- Thermodynamic stability on Si
- Interface quality
- Gate compatibility
- Process compatibility
- Fixed oxide charge.

Part III

MDT-ASD Prototypes

2
Front-End

MDT-ASD is the acronym of Monitored-Drift-Tube Amplifier-Shaper-Discriminator; in other words, it is a read-out front-end designed for muons detection in ATLAS experiments. In the next years, the Phase-II Upgrade of the ATLAS (A Toroidal LHC ApparatuS) Muon Detector is scheduled. Changing the operating conditions, electronics used so far [19] must be replaced with reliable and efficient circuits. The prototype here presented has been realized in collaboration with Max-Plank Institute for Physics (Munich) using the IBM 130 nm CMOS 8 RF−DM technology in place of 0.5 µm n-well triple-metal CMOS one. The ASD [19], presently used for the read-out of Monitored-Drift-Tube (MDT) chambers of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN, is biased at 3.3 V and provided reliable operation and low failure rate. It performs a front-end charge-to-voltage conversion (by a proper Charge-Sensitive-Preamplifier) followed by the analog signal conditioning (amplification and shaping) and A/D conversion. It features a sensitivity (i.e. voltage vs. charge conversion ratio) of 8.9 mV/fC [19], 15 ns nominal Peaking Time Delay (i.e. PTD, the front-end capability to quickly detect charge arrival time) and low-noise enabling 5 fC minimum detected charge at 10 dB (3.2×factor) Signal-to-Noise-Ratio (i.e. SNR).

The new ASD channel it has been designed to satisfy the same requirements like time resolution, gain, sensitivity and noise in presence of challenging environment. The upgraded system will operate at peak luminosities of a factor 5-7.5 beyond the nominal value of 10^{34} cm^{-2} s^{-1}. The high luminosity is a challenge for the readout system of the Monitored Drift Tube chambers (MDT) in the ATLAS Muon Spectrometer in two respects. Higher hit rates, mainly due to increased cavern background, drive data transmission to the rear end electronics at the limit of available bandwidth. In addition, the new operating parameters of the L1 trigger - latency up to 60 µs and trigger rates up to 400 kHz- call for a replacement of the entire readout chain of the MDT chambers.

In this process of renewing the MDT readout, particular attention must be given to the first stage of the readout chain, the Amplifier with Shaping network and Discriminator (ASD), and its improvement including the 60 pF parasitic capacitance of the detector. This stage determines critical quantities, like signal rise-time, signal-to-noise performance and threshold uniformity among the 8 channels of the chip, which are decisive for system parameters like spatial resolution of the track coordinates (represented by the drift time in the MDT tubes) and tracking efficiency.

Before analyzing in detail the structure and the new read-out performance, the next section will deal with a brief introduction on ATLAS experiment and the muon detection system.

2.1 ATLAS Detector at the LHC

High-Energy-Physics (HEP) experiments developed in the last decades [20]-[21]-[22]-[23] seek to describe the high energy particle interactions.

The main target of High-Luminosity Large-Hadron-Collider (LH-LHC) ATLAS experiments is to search the elementary particle of the Standard Model (named Higgs Boson) studying a broad spectrum of physics processes. For this purpose, it is required a complex detection system as that shown in figure 2.1.

According to [26] [27], muons measurement uses two completely independent systems called Inner Tracker and Muon Spectrometer [28]. The Inner Tracker is surrounded by a superconducting coil which generates a magnetic field parallel to the beam axis where there are three different sensor systems. It performs the measurements of direction, momentum and charge of electrically charged particles produced in each proton-proton (p-p) collision. The muons emerging from the primary collision, being the most penetrating charge particle component, are able to transverse the Calorimeters and to reach the Muon spectrometer, the outermost shell of the ATLAS detector. The Muon Spectrometer (MS) surrounds the calorimeters and consists of three large air-core superconducting magnets providing a toroidal field (each with eight coils); a system of precision tracking chambers and fast detectors. A proper electronics is designed for each part and the here presented read-out front-end is dedicated to the Monitored Drift Tube (MDT) chambers.

The MDT chambers are the main components of the precision tracking system [25]. The tubes have 29.970 mm of diameter and they are organized in six layers arranged as shown in [28]. They are connected to electronics containing the 8×ASD channels as represented in figure 2.4. An impedance matching network avoids reflections and losses of charge detected. About that, each wire operates with Ar/CO_2 gas (93/7) at 3 bar and it is terminated with the equivalent transmission line impedance of the tube (383 Ω). In addition, all contacts between the chamber and the hedgehog board are gold plated to ensure a long-term connectivity. A section of the MDT tube is reported in figure 2.3. Electrons generated by muons in the gas-filled pressurized MDT tubes are drifted to the central wire of the tube, where their time-of-arrival is used to determine the distance of the track from the wire (R_{MIN} in figure 2.3). As the muon usually passes through a large number of drift tubes, the position of the muon track can be reconstructed from a combination of measurements in the tubes along the muon trajectory. Other specific details (not important for the purposes of this discussion) on ATLAS experiment and setup can be found in [29] and they are not reported here to focus more attention on the channel description.

Considering a simplified MDT readout scheme (see figure 2.4), the small charge signals, coming from the wires, are sent to the 'mezzanine board' where the 8×ASD channel is placed. Each 'mezzanine board' contains 24 channels organized in 3 Octal ASDs and it is connected to a single 24 channel Time-to-Digital Converter (TDC) and to a proper control circuitry [19]. Instead, the generic block scheme of the single-channel is reported in figure 2.5 and will be discussed in section 2.3.

The monolithic 8×ASD chip senses, shapes and converts the signal coming from

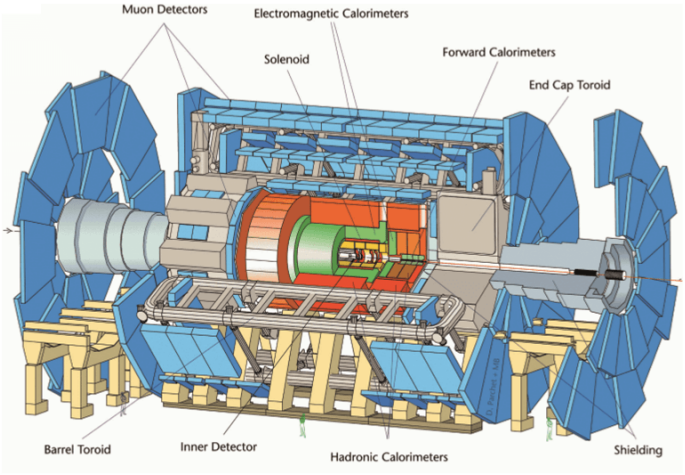

Figure 2.1: Scheme of complex ATLAS Detector (from [24])

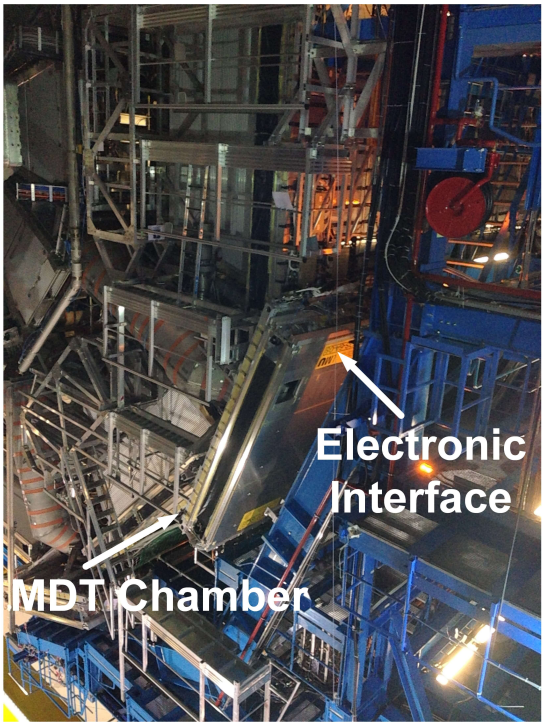

Figure 2.2: Photo of ATLAS Detection System

the tubes, providing time-domain voltage pulses, whose duty cycle is proportional to the amount of charge at the 8×ASD input. The output signal of the discriminator, triggered when the voltage pulse crosses a predefined and adjustable threshold, is

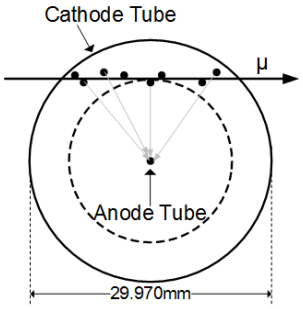

Figure 2.3: Section of MDT tube

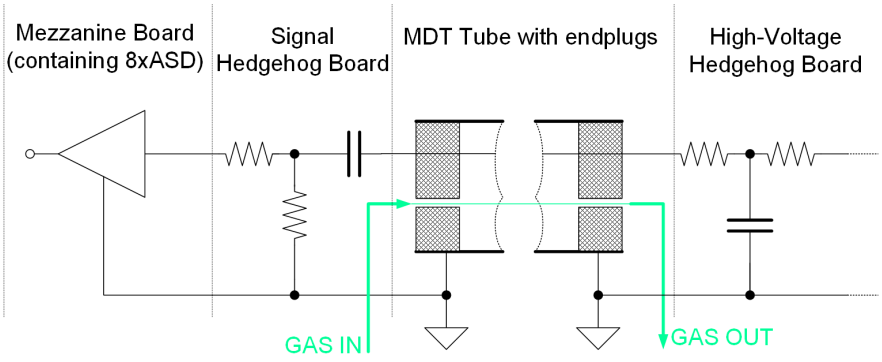

Figure 2.4: Simplified Scheme of Muons Detection system ([25])

subsequently sent to an off-chip TDC, which forwards the signal arrival times down the data acquisition chain for recording and track reconstruction.

Before moving on to analyze the most important requirements for MDT-ASD read-out channel, it is worth to point out that the choice of the ionizing gas has been done for its favorable aging properties in the LHC environment [19]. Unfortunately, it is a non-linear drift gas and from this situation results difficult track reconstruction solving with a programmable dead-time up to the total drift time.

2.2 MDT-ASD Requirements

The new MDT-ASD prototype is developed in IBM 130 nm CMOS 8 RF-DM and it is designed starting from the requirements widely described in [30] - [19] and brief summarized in this section.

First of all, the input impedance of the Charge-Sensitive-Preamplifier (CSPreamp) must be minimized in order to maximize the collected charge. Typically it must be maintained under 120 Ω.

The front-end noise level must be low to not-compromise the position resolution. At the same time, a peaking time delay within 15 ns is required to avoid loss of resolution to the advantage of stability and vice versa [31].

Bipolar shaping scheme is mandatory to avoid multiple threshold crossings coming from non-linearity and long drift time (up to 800 ns) of Ar/CO_2 gas (93/7 at 3 bar).

A fully differential structure is strongly recommended with the main target to improve the power supply rejection.

Finally, the minimum sensitivity required at discriminator input is 8.9 mV/fC.

2.3 Octal MDT-ASD V4 Chip

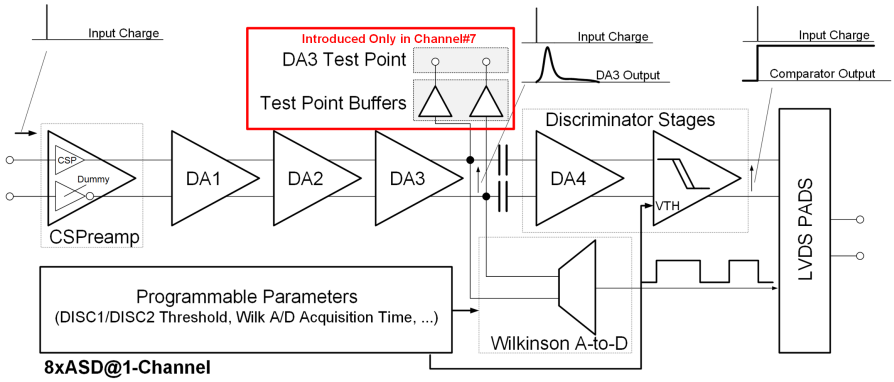

Figure 2.5: 8×ASD Front-End Generic Block Scheme

MDT-ASD V4 Chip includes eight identical channels and it has been realized in IBM 130 nm CMOS 8 RF-DM technology in order to cope the requirements (like signal rise-time, sensitivity, signal-to-noise performance, channel uniformity, etc.) introduced at the begin of this part.

The chip can be operated in two output modes, the ADC mode and the Time-over-Threshold (ToT).

- ***ADC Mode*** *implemented by a Wilkinson ADC*
  The Wilkinson A/D is in on-state and the output pulse provides edge time (event detection) and charge measure. The time elapsed between leading and trailing edge is proportional to the charge inside a predefined integration window of about 15 ns, which is an approximate measure of the amplitude of the initial signal, triggering the discriminator. More specifically, charge information (encoded in the pulse time width) is then used for edge time correction, since different amounts of charge produce different edge time (this effect is called time-slew [25] and it will be corrected in the off-chip digital signal processing by properly exploiting the total amount of input charge measurement).

- ***ToT Mode*** *implemented by a Discriminator Stage*
  The Wilkinson A/D is disabled and the output signal gives the information in terms of rising and falling edge timing.

The main motivation of this work is to replace the ASIC presented in [19] with a new

design, where improvements are expected in terms of technological scaling-down (from 0.5 µm to 0.13 µm minimum channel length CMOS technology), increased sensitivity to higher luminosity, higher SNR and better radiation hardness. Nonetheless, a simple porting cannot be a reliable solution for several reasons, among them:

- MOS transistor threshold voltage (MOST VTH) is lower in HV 0.13 µm than 0.5 µm CMOS process of the old design (0.45 V vs. 0.75 V, respectively for NMOS MOST). This difference obviously affects the biasing point of all analog stages in the chain (Charge Sensitive Preamplifier and Shaping Amplifiers) since at constant MOST drain-source current (i.e. I_{DS}) overdrive voltages will increase and this leads to lower transconductance (i.e. g_m) and lower MOST efficiency (i.e. g_m/I_{DS} ratio that, as well explained in [9], is maximized at lower overdrive voltages)

- this g_m/I_{DS} efficiency reduction is crucial for several pure analog performance of the front-end, like sensitivity, noise, and Peaking-Time-Delay (i.e. CSPreamp output voltage rising-time) which are strongly linked to the MOST g_m

- transistor intrinsic gain slightly reduces in HV 0.13 µm devices comparing with the 0.5 µm CMOS process and this implies changes in the CSPreamp, where dc open-loop gain is crucial for maximizing sensitivity in terms of charge-to-voltage conversion.

The architecture of a single-channel 8×ASD (named Analog Front-End (AFE) also) is shown in figure 2.5. Each channel includes an analog part (described in 2.3.1) and a digital (described in 2.3.2) one. In particular, the input signal is a current pulse signal coming from the muon detector. It is converted into a voltage signal by the Charge-Sensitive-Preamplifier (CSPreamp). The CSPreamp output voltage is then properly shaped by the cascade of three Differential-Amplification stages (DA_1, DA_2, DA_3) to increase the signal power, and to perform out-of-band noise rejection and anti-aliasing filtering for the following ADC. The DA_4 output signal feeds a Comparator (Discriminator Stage in figure 2.5), which allows detecting the charge arrival time.

Furthermore, the DA_3 output signal is connected to Wilkinson ADC input which generates a time representation of the input signal, performing a voltage-to-time conversion. A Programmable Parameters stage has been also embedded to set the Discriminator threshold (the minimum charge to be detected) and the signal needed for Wilkinson ADC operation. Moreover, LVDS drivers have been designed to interface the 8×ASD chip with the subsequent TDC chip. Test point for the DA_3 output voltage is an analog buffer, able to drive the probe for testing purposes (with -2 dB (0.8× factor) drop and a few ns as additional delay).

2.3.1 Analog Chain

The chain of a Charge-Sensitive-Preamplifier and three Differential Amplifiers composes the 8×ASD. These are the more critical blocks for the channel performance and

they are essential to define bipolar shaping used in ADC or ToT channel operating mode.

Charge Sensitive Preamplifier

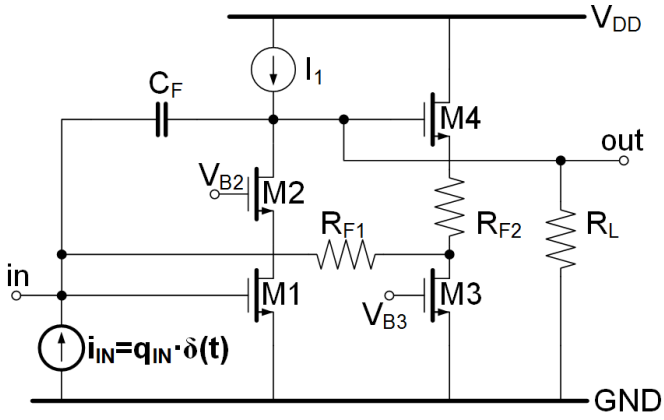

Figure 2.6: 8×ASD Charge-Sensitive-Preamplifier Schematic

The overall system behavior is strongly dependent on the CSPreamp performance, which converts the input muon current signal in differential voltage one. For this reason, it is composed by two identical symmetrical paths. A dummy preamp has been used for differential signal processing, and as a consequence the input charge is read from one single path. The transistor level scheme of each path is reported in 2.6 and it is the same of the previous design [19].

The first aspect to taken in account is the presence of a very large parasitic capacitance ($C_D \approx 60\,\mathrm{pF}$) connected between the CSPreamp input node and ground. It is mainly due to the PCB parasitics and the long wires of connection between the ASD and the tubes (see the Muon Detection block scheme in figure 2.4). Obviously it strongly affects CSPreamp performance in terms of closed-loop-gain bandwidth reduction (i.e. voltage response rise-time reduction) and sensitivity (i.e. the voltage gain per fC, whereas the ideal sensitivity is $S_{CSP_{IDEAL}} = 1/C_F$). These aspects are further stressed by the more scaled technology node, that reduces MOST efficiency comparing with the 0.5 µm process. For these reasons, the CSPreamp has been completely re-designed to improve the performance in terms of input impedance (now <120 Ω), noise and speed of response.

The CSPreamp input MOST transconductance ($g_{m_{M1}} = 25\,\mathrm{mA/V}$) is here much larger than in previous design, as trade-off between noise, speed, and power. In this direction, transistor M_1 operates in moderate inversion region ($V_{OV} \approx 75\,\mathrm{mV}$): it has large size ($W = 900\,\mu\mathrm{m}$ and $L = 500\,\mathrm{nm}$) and sinks a nominal current of 1.6 mA. The larger bias current however does not increase total power consumption w.r.t. the state-of-the-art design [19], thanks to a better redistribution of the total power among the different stages. The larger power allocated to the CSPreamp input stage

is compensated by saving power elsewhere (mainly in the DA_X chain, and in the bias circuit), where it was not necessary. On the other side the large input device sizes results in approximately 1.2 pF gate-source parasitic capacitance, which is however negligible w.r.t. the detector parasitic capacitance C_D. Small-signal feedback network has been slightly changed, since the equivalent feedback resistor has been here split in $R_{F1} + R_{F2}$. This way, the $M_3 - R_{F2} - M_4$ source-follower optimizes the output node common-mode voltage, for better operation of the following DA_1 stage, which has NMOS input transistors (and for thermal noise minimization).

Considering the scheme represented in figure 2.6, the CSPreamp transfer function depends on the feedback capacitor (C_F), the transconductance of M_1 input MOS ($g_{m_{M1}}$), the equivalent feedback resistor ($R_F = R_{F1} + R_{F2}$), the load resistor (R_L) and the detector capacitance (C_D). It can be approximated by 2.1. This equation can be further approximated by 2.2, assuming $R_L = R_F$ and the zero at much higher frequency than the pole (since $g_{m_{M1}} \gg 1/R_F$, i.e. $\approx 5\,\mathrm{GHz}$).

$$T(s) \cong -R_F \frac{1 + s\frac{C_F}{g_{m_{M1}}}}{\left(1 + sC_F R_F \left(1 + \frac{C_D}{C_F}\left(1 + \frac{R_L}{R_F}\right)\frac{1}{1+g_{m_{M1}}R_L}\right)\right)\left(1 + s\frac{C_D}{g_{m_{M1}}}\right)} \tag{2.1}$$

$$T(s) \cong -R_F \frac{1}{\left(1 + sC_F R_F \left(1 + 2\frac{C_D}{C_F}\frac{1}{g_{m_{M1}}R_L}\right)\right)\left(1 + s\frac{C_D}{g_{m_{M1}}}\right)} \tag{2.2}$$

In this design $C_D/C_F \approx 88$ and $g_{m_{M1}} R_L \approx 400$, hence the dominant pole time constant is approximately the $30\,\%$ higher than the ideal $C_F R_F$. This leads to an effective sensitivity of the CSPreamp (i.e. S_{CSP}) given by 2.3.

$$S_{CSP} \cong S_{CSP_{IDEAL}} \left(\frac{1}{1 + 2\frac{C_D}{C_F}\frac{1}{g_{m_{M1}}R_L}}\right) = 0.68\, S_{CSP_{IDEAL}} \tag{2.3}$$

As a result the CSPreamp achieves a 1.04 mV/fC sensitivity, even in presence of very large C_D capacitor. Moreover, non-dominant pole is at $g_{m_{M1}}/C_D$, and, then, the large $g_{m_{M1}}$ value allows also to push non-dominant pole at higher frequencies and to reduce its time-delay effect. Hence, the main concept of this design is to mitigate the effects of the large C_D capacitance.

The CSPreamp sensitivity is confirmed by time-response simulations reported in figure 2.7. In this picture, there is a comparison between the simulated transient noise CSPreamp output voltage and other simplified cases. In particular, there are plotted the following curves:

- IDEAL case: C_D and no-ideality of the gain stage are neglected and the CSPreamp output depends on ideal time constant approximated by $C_F R_F$
- Case 1: where C_D of 60 pF and the finite dc loop-gain $A_0 = g_{m_{M1}} R_L$ have been considered. In this case, there is still one dominant pole, which is affected by introduced no-ideality and the associated time constant is given by 2.4

- Case 2 (overlapped to transient noise simulation): where C_D of 60 pF, finite dc loop-gain and finite bandwidth have been considered. This is practically the effective case and the system has two poles. The dominant one is associated to 2.4 time constant. The second depends on $C_D/g_{m_{M1}}$ time constant.

$$C_F\, R_F \left(1 + 2\,\frac{\frac{C_D}{C_F}}{g_{m_{M1}} R_L}\right) \tag{2.4}$$

The large CSPreamp open-loop gain (i.e. A_0) strongly mitigates the sensitivity

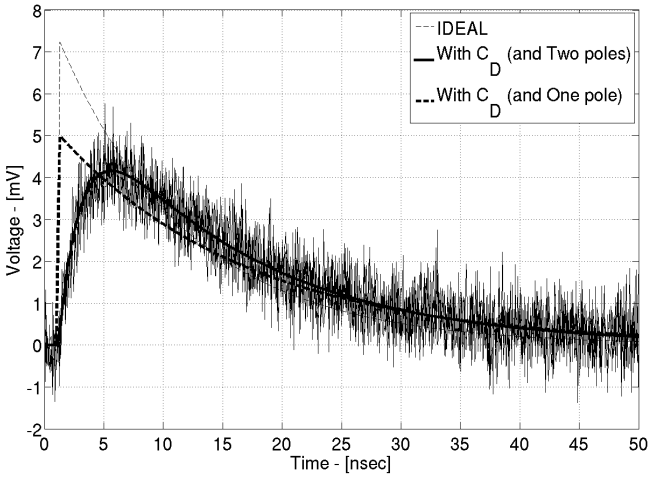

Figure 2.7: Simulated Transient Noise CSPreamp Output Voltage

reduction induced by C_D/C_F ratio (4.5 $\text{mV}_{\text{0-PEAK}}$ instead of 7 $\text{mV}_{\text{0-PEAK}}$ for minimum $Q_{IN} = 5\,\text{fC}$). In addition, the second pole (whose time-constant is $C_D/g_{m_{M1}}$) leads to lower time response speed (Peaking Time Delay (PTD) is 7 ns instead of 4 ns), w.r.t. the single-pole ideal case. This effect is also mitigated by the larger g_m, and it is a reasonable trade-off, since they allow to satisfy the MDT chambers requirement of PTD<15 ns. This validates the choice of pushing M_1 transistor in moderate inversion region (maximizing this way its $g_{m_{M1}}$), which avoids sensitivity degradation due to the large parasitic C_D, mitigates the second pole time-delay effect, and improves noise performance.

For sake of completeness, figures 2.8 and 2.9 are also reported. The first is dedicated to magnitude and phase of the CSPreamp loop gain frequency response considering C_D effect. The v_{OUT}/q_{IN} and Z_{IN} frequency responses are instead plotted in figure 2.9, with and without the C_D effects.

The input impedance is maintained almost constant for all in-band frequencies, since at low frequency, it is fixed by $R_L = 16k\Omega$ and $R_F = 16\,\text{k}\Omega$, while, at higher frequency, it is regulated by the Feedback Capacitance ($C_F = 680\,\text{fF}$) and by the detector capacitance ($C_D = 60\,\text{pF}$). Finally, transient noise simulations have been ran

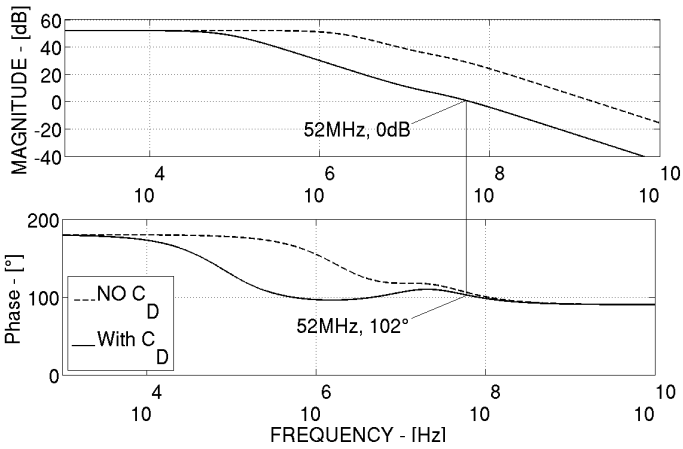

Figure 2.8: CSPreamp Loop-Gain Frequency Response

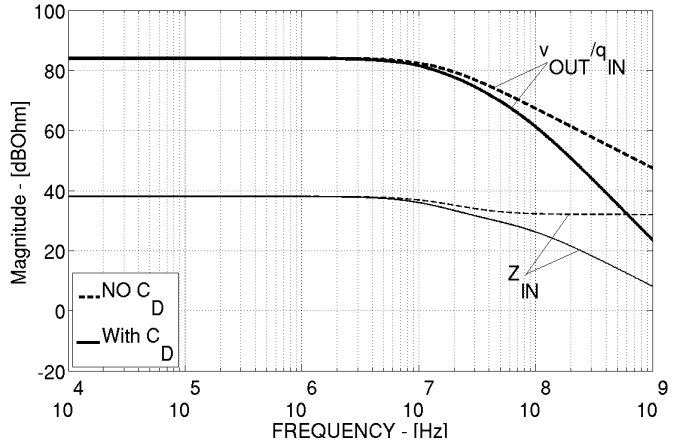

Figure 2.9: CSPreamp v_{OUT}/q_{IN} and Z_{IN} Frequency Response

(see figure 2.7), to highlight the thermal noise contribution, resulting in 0.55 mV_{RMS}-in-band output noise power (to be further reduced by the following shaping filtering stages, i.e. DA_1-DA_2-DA_3). The SNR at the CSPreamp output is 19 dB in case of minimum input charge of 5 fC, and it rises up to 45 dB at 100 fC. The most important CSPreamp design parameters vs. process variations are then listed in Table 2.1.

Differential Amplifiers

The CSPreamp output signal is amplified and filtered by the cascade of three stages (DA_1-DA_2-DA_3), which shape the signal in order to convert the waveform of figure 2.7 into a bipolar shaping and to define the fall-down time. In this DA_1-DA_2-DA_3 chain, the scaled 0.13 µm devices have been exploited in the reduction of the parasitic capacitance, and, then in increasing the speed while reducing power consumption w.r.t. the state-of-the-art design in [19].

Parameter	*Min*	*Nominal*	*Max*
Current Consumption	1.8 mA	2.1 mA	2.6 mA
Supply Voltage	3.3 V	3.3 V	3.3 V
Peaking Time Delay (PTD)	8 ns	7 ns	6.2 ns
Output Noise	0.63 mV_{RMS}	0.55 mV_{RMS}	0.47 mV_{RMS}
In-Band IRN PSD	5.8 $nV/\sqrt{Hz}$	5 $nV/\sqrt{Hz}$	4 $nV/\sqrt{Hz}$

Table 2.1: CSPreamp Main Design Parameters

Stage	Z_1	Z_2
DA_1	1.35 kΩ	6.26 kΩ
DA_2	2.45 kΩ ‖ (2.45 kΩ + $1/(s\,47\,\mathrm{pF})$)	6.26 kΩ
DA_3	2.45 kΩ + $1/(s\,47\,\mathrm{pF})$	9.77 kΩ

Table 2.2: DA_1-DA_2-DA_3 Impedances

The main schematic of all DA_1-DA_2-DA_3 stages is shown in figure 2.10. DA_1-DA_2-DA_3 have different Z_2-Z_1 impedance values, performing this way different shaping, whose frequency response per-stage are shown in figure 2.11. The design values of Z_1-Z_2 are reported in Table 2.2, organized as a function of the specific DA_1-DA_2-DA_3 stage.

The frequency responses at the CSPreamp output and at the full channel output are plotted in figure 2.11. The full chain exhibits a pass-band characteristic with a 5 MHz center frequency. The high-pass part, mainly imposed by DA_3, shows a 30 kHz high-pass frequency and a slope of +6 dB/octave (1st-order high-pass filter). The low-pass part is the superposition of all four amplifier low-pass characteristics, which have a bandwidth between a few tens and hundreds MHz.

2.3.2 Digital Chain

The DA_3 output signal feeds to the $DISC_1$ stages and the Wilkinson ADC (W-ADC), to provide information regarding the arrival time and the total amount of input charge at the CSPreamp input node. The $DISC_1$ is a comparator, which detects the presence of a specific minimum charge at the CSPreamp input nodes and provides the charge arrival time and the Start-of-Conversion signal for the W-ADC. The W-ADC, instead, performs a Voltage-to-Time conversion. The schematic of the W-ADC is shown in figure 2.12.

The sample capacitor (C_H) is charged for a given time range TGW (programmable by the external between 8 ns and 32 ns). Such capacitance is then discharged down to the zero-crossing instant. Charge and discharge phases depend on Θ_1 and Θ_2 signals, such as on ON-OFF switches phases. Θ_1 and Θ_2 signals control complementary MOS switches. The equivalent time-width needed to discharge the C_H will be proportional to the analog input voltage and, as a consequence, to the equivalent amount of charge

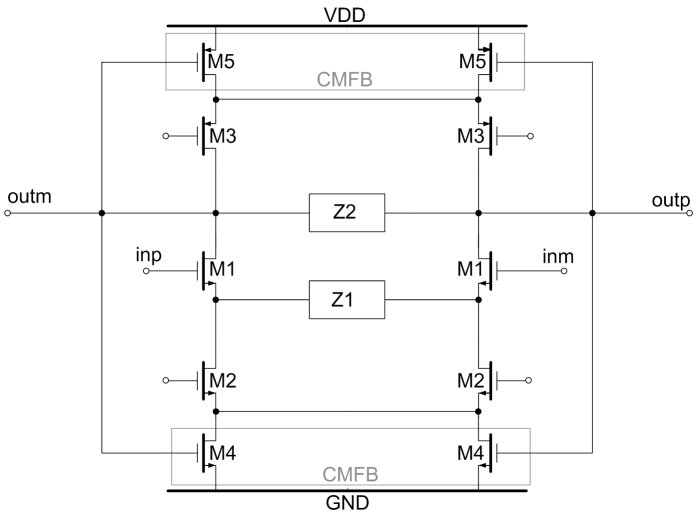

Figure 2.10: DA_1 - DA_2 - DA_3 Stages Main Scheme

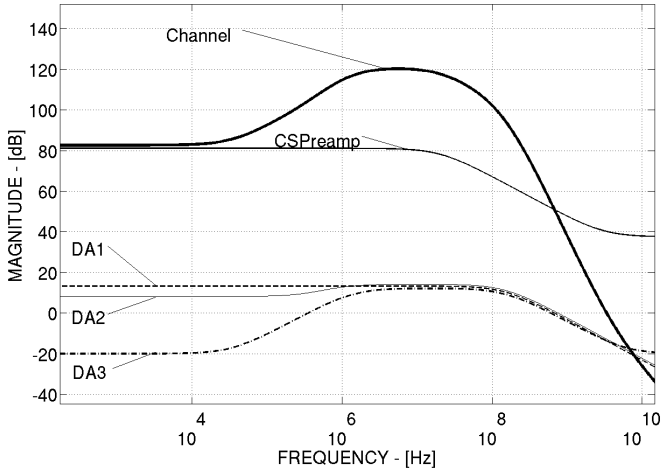

Figure 2.11: Channel AC Frequency Responses

at the CSPreamp input nodes.

As in figure 2.12, with the same integration time TGW, the higher is the analog voltage peak value (i.e. the Q_{IN} input charge), the higher is the time needed to cross down the horizontal axis. The transconductor stages design had to face the lower output impedance of the 0.35 µm devices w.r.t. the 0.5 µm devices. Specific arrangements have then been adopted to guarantee the same impedance level. On the other hand, the power here is unchanged since it is fixed by CH value (3 pF), to make negligible any parasitic effects. The transconductor stages are based on the scheme shown in figure 2.10, where Z_1 and Z_2 are replaced by poly-silicon resistors.

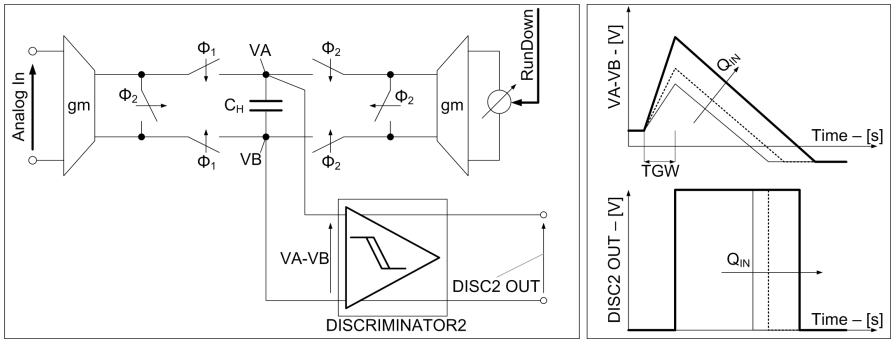

Figure 2.12: Wilkinson ADC Operating Principle

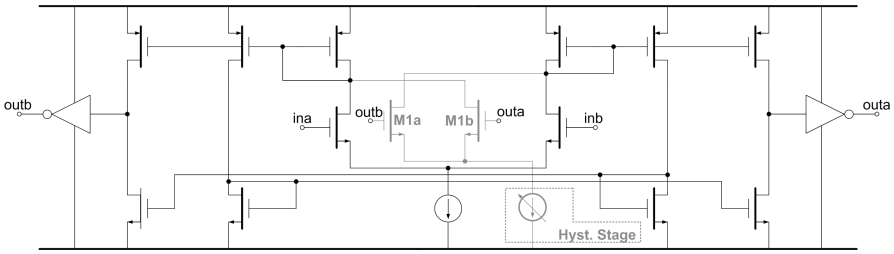

Figure 2.13: $DISC_1$ and $DISC_2$ Block Scheme

The complete schematic of both $DISC_1$ and $DISC_2$ is shown in figure 2.13. A mirrored input stage has been used, performing very high dc-gain, with approximately 300 µA static current consumption. Output digital buffers are then used to square the output signal. Hysteresis is here implemented by using an additional input pair M_{1a} and M_{1b}, whose main aim is to unbalance the dc current by using a digital programmable current source (Hyst. Stage in figure 2.13). The required hysteresis value is set by a proper JTAG digital interface (Programmable Parameters stage in figure 2.5).

2.3.3 Programmable Parameters

Programmable Parameters stage in figure 2.5 manages voltage and current references of the 8×ASD channels through a digital signal of 55 bits. For this purpose, a serial I/O data interface has been introduced and connected to proper Digital-to-Analog Converters (DACs). In this way, the digital data is converted in analog one avoiding countless external references. The 55 bits are transmitted to ASDs serial interface through a JTAG like protocol. They are generated by control logic placed into TDC chip, which coordinates control signals and shift register clock, also.

For compatibility reason with the previous ASD versions, the total number of bits is unchanged and they are used to generate the programmable parameters summarized in Table 2.3 (see [19] for major parameter details).

Two complementary 8-bit dual resistor divider voltages-DACs produce the dif-

ferential $DISC_1$ threshold voltage applied to DA_4 inputs. In analog way, two complementary 3-bit resistor divider voltages-DACs provide to $DISC_2$ its differential threshold in the range 32 mV - 256 mV.

A binary-weighted switched resistor chain is used for Wilkinson Discharge (Rundown) Current, Wilkinson Integration Gate and Dead-Time parameters generation. To reduce the channels mismatch, the resistor of the last two parameters are placed in each channel implementing a local generation. $DISC_1$ Hysteresis depends instead on binary-weighted switched current mirrors.

One of 55 bits is shared by the eight channels allowing to selection ADC and ToT operating Chip Mode. Finally, other two bits for each channel are reserved to choice Channel Mode operation. Typically, it is set on ON state with default working setting. Otherwise, there are HI or LO states, which force the LVDS output to High ('1') or Low ('0') Logic Level regardless of what happens in the analog part of this channel.

Parameter	*Range*	*LSB*	*Units*	*Resolution (bits)*
$DISC_1$ Threshold	-255 to +255	2	mV	8
$DISC_1$ Hysteresis	0 - 320	20	µA	4
Wilkinson Integration Gate	8 - 47	2.5	ns	4
$DISC_2$	32 - 256	32	mV	3
Wilkinson Discharge Current	4 - 13	1.1	µA	3
Dead-Time	17.85 - 657.7	111	ns	3
Channel Mode	ON, HI, LO	-	-	-
Chip Mode	ADC, ToT	-	-	-

Table 2.3: Summary of Used Programmable Parameters

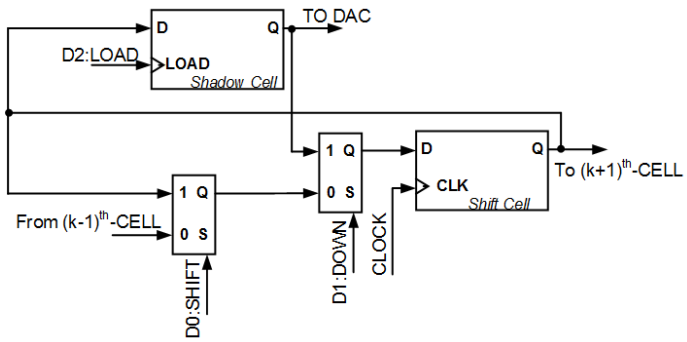

Figure 2.14: Generic Block of the k^{th} Jtag Interface Unit Cell

2.3.4 JTAG Serial Interface

The ASDs serial interface [19] has been implemented by a chain of 56 unit cells (see figure 2.14) composed as follows:

- ***A Shadow Cell:***
  static transparent latch that interfaces with the following DACs reserved to Programmable Parameters generation

- ***A Shift-Register Cell:***
  static master-slave D flip-flop to propagate the bit in the chain and to shadow cell

- ***2 two-in-one multiplexers***
  to manage Shadow and Shift Cells working.

There is a single unit cell for each data bit (55) plus one to complete the all control bits loading. According the protocol, $DATA_{IN}$ and $DATA_{OUT}$ represent the input and the output of the unit cell, respectively. In addition, there are a clock input signal (named CLK) and other three control lines (D_0, D_1, D_2). They are used to control the data flow and to select the interface operation mode between

- ***SHIFT Mode:*** right shifting at CLK rising edge

- ***HOLD Mode:*** each bit is kept in a register

- ***DOWN Mode:*** the bit kept in the shadow register is copied to shift cell at CLK rising edge

- ***LOAD Mode:*** the bit kept in the shift register is loaded to shadow cell any time.

In this design differently from [19], the clock signal is the same for the all shift registers, also for the last one.

3
Octal MDT-ASD V4 Layout

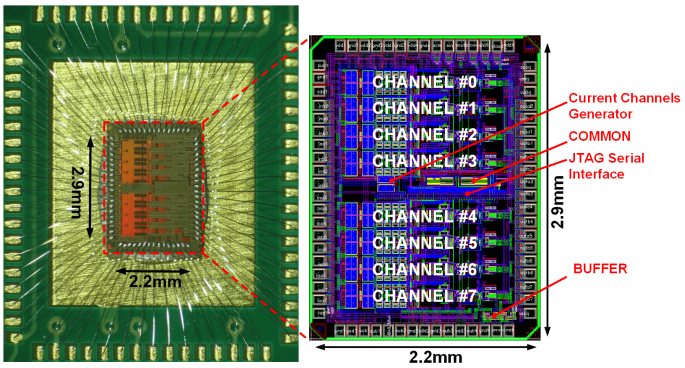

Figure 3.1: Octal MDT-ASD V4 Chip before (on the rigth) and then (on the left) Fabrication

This section is dedicated on the Octal MDT-ASD V4 layout. The layout is the last design step before chip fabrication and consists of a circuit layer representation. Schematic designed is translated in a drawing used from foundry to realize the chip. A photo of the chip before and then the fabrication is reported in figure 3.1. The full chip occupies an area of 6.73 mm^2 and includes the following blocks:

- a ***Padring*** (with 70 pads, which an area approximately given by $70 \times 0.029\,mm^2$)
- ***8 MDT-ASD V4 Channels*** (with single channel area of about $0.4\,mm^2$)
- a ***Common Block*** (with an area occupancy of $0.1\,mm^2$)
- a ***JTAG Serial Interface*** (with an area occupancy of $0.087\,mm^2$)
- a ***Current Channels Generator*** (with an area occupancy of $0.035\,mm^2$)
- a ***Buffer*** (with an area occupancy of $0.04\,mm^2$).

3.1 Padring Layout

The Padring is formed by 70 I/O pads, one for each input or output. It allows chip interface with the off-chip world. Typically, the pad circuits are defined by the foundry including a bondpad contact and protection diodes. The idea is to limit the on-chip circuit damage following to external electrical discharges, welds of discrete external components, etc.

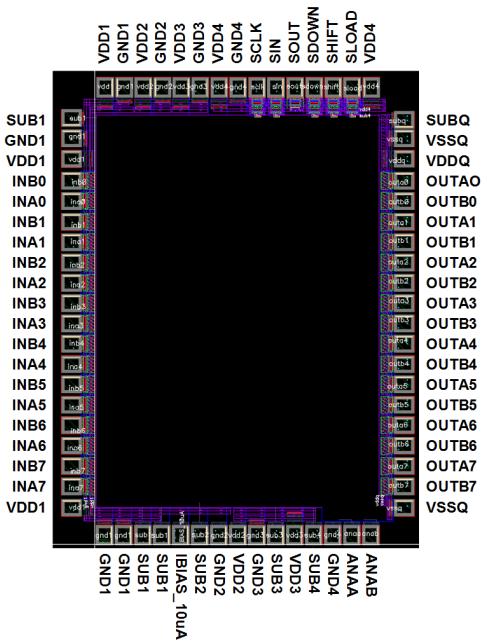

Figure 3.2: Octal MDT-ASD V4 Pin Diagram

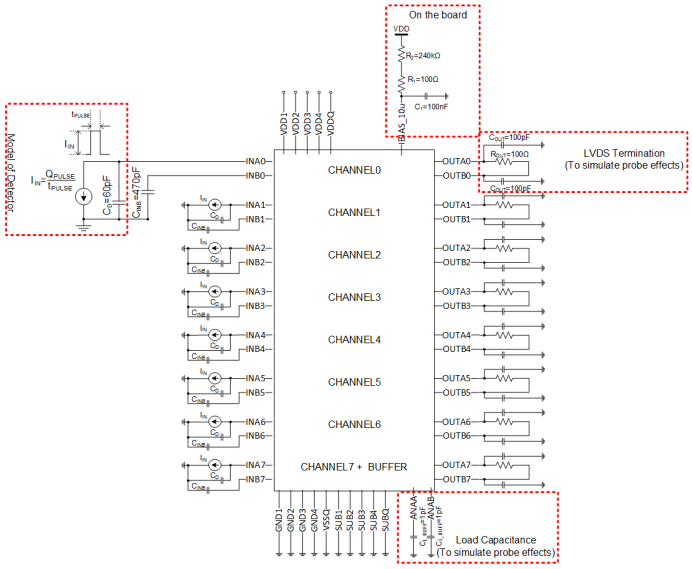

Figure 3.3: Octal MDT-ASD V4 Simplified Simulated Scheme

The pads are placed to form a ring around the Octal MDT-ASD V4 chip. In particular, the position occupied from each pad has been highlighted in the Pin Diagram (see figure 3.2). For sake of completeness, the generic simulated block

BLOCK	PIN NAME	DESCRIPTION	TYPE	#	I/O INTERFACE
JTAG Serial Interface 6 PADs	SCLK	Clock Line	Digital In	1	Vpulse Generator
	SIN	Load Control Line	Digital In	1	Vbit Generator
	SDOWN	Down Control Line	Digital In	1	Vpulse Generator
	SHIFT	Shift Control Line	Digital In	1	Vpulse Generator
	SLOAD	Data Line	Digital In	1	Vpulse Generator
	SOUT	Data Line	Digital Out	1	noConn Istance
MDT-ASD V4 Channel 32 PADs	<ina0:ina7>	Positive Channel Input	Analog In	8	1 nF Cap or Current Generator in parallel with 60 pF Cap
	<inb0:inb7>	Negative Channel Input	Analog In	8	470 pF Cap
	<outa0:outa7>	Positive Channel Output	Analog Out	8	Input 'A' LVDS Termination
	<outb0:outb7>	Negative Channel Output	Analog Out	8	Input 'B' LVDS Termination
Channel#7 Buffer 2 PADs	anaa	DA_{3oa} of Channel#7	Analog Out	1	1 pF Cap
	anab	DA_{3ob} of Channel#7	Analog Out	1	1 pF Cap
Current Channels Generator 1 PAD	IBIAS_10 µA	Current Generator	Analog In	1	Current Generator of 10 µA± 5 %
Supplies 29 PADs	<vdd1:vddq>	Supply Voltage	Analog In	10	DC-Voltage Generator of 3.3 V± 5 %
	<sub1:subq>	Ground Voltage	Analog In	7	DC-Voltage Generator of 0 V
	<gnd1:gndq>	Ground Voltage	Analog In	12	DC-Voltage Generator of 0 V

Table 3.1: Octal MDT-ASD V4 Pin List

scheme of the Octal MDT-ASD V4 has been shown in figure 3.3. In the Table 3.1 is instead reported the whole list and description of the pin diagram components, specifying in detail membership block, name, description, type, number and what was connected during the simulations.

The input charge signal is provided through an input pulse current generator to <ina0:ina7> pins. To emulate detector parasitic capacitance, the simulations have been done inserting 60 pF of capacitance between these points and ground. Otherwise, the channels disconnected from detector have only 1 nF of Cap between ina_x and ground. Finally, as regards supplies/grounds, they are divided to separate analog and digital worlds. In particular, there are:

- VDD1 and GND1 for charge sensitive preamplifier and the current generator used to provide 10 µA of current to each channel

- VDD2 and GND2 for several analog blocks (DAx, Hysteresis, Channel Current

Mirrors, Wilkinson ADC)

- VDD3 and GND3 for Discriminators and Wilkinson Phase Generator

- VDD4 and GND4 for Common, JTAG Serial Interface and MUX Blocks (Common is dedicated to Programmable Parameters managements. Instead, the MUX come before the LVDS block allowing the chip and the channel operation modes.)

- VDDQ and VSSQ for the last blocks: LVDS and Channel#7 Buffer.

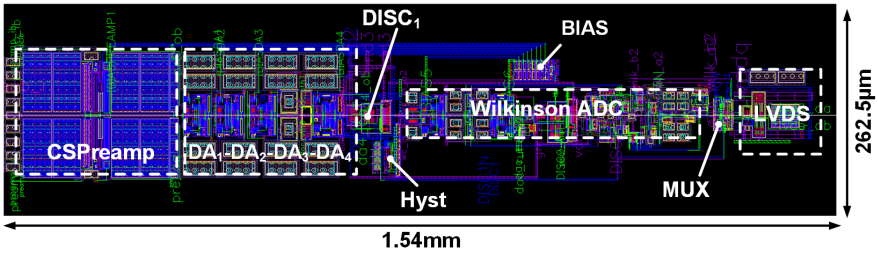

Figure 3.4: Layout of MDT-ASD V4 Channel

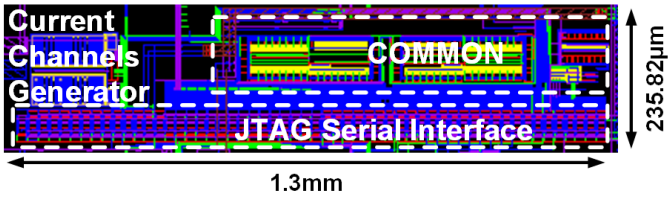

Figure 3.5: Layout of the "COMMON", "JTAG Serial Interface" and "Current Channels Generator" Blocks

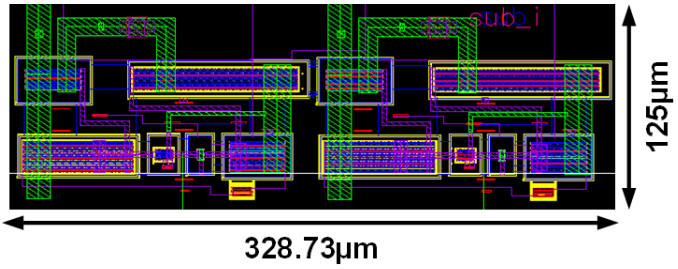

Figure 3.6: Layout of the "BUFFER" Block

3.2 Core Layout

The Core layout includes the entire Octal MDT-ASD V4 chip except the Padring shown in 3.1.

In figure 3.4 is reported the most important block described in 2.3: the MDT-ASD V4 single channel. It is formed by the analog part (CSPreamp and DA_x), the digital part (Discriminator and Wilkinson ADC), the Hysteresis Block Generator (Hyst), the Current Bias generator (BIAS), the MUltipleXer (used to chip and channel operation mode selection) and the LVDS block. For sake of completeness, the "Current Bias Generator" generates the bias currents for CSPreamp and DA_x starting a single current of 10 µA coming from the "Current Channels Generator". The symmetrical structure (shown in figure 3.4) is fundamental in fully differential architecture.

In figure 3.5, instead, "COMMON", "JTAG Serial Interface" and "Current Channels Generator" layouts have been reported. They are located in the middle chip in order to uniformly distribute the Programmable Parameters and 10 µA currents between the channels.

Finally, there is the "BUFFER" (see figure 3.6). It is near the Channel#7 because it is connected to its DA_3 output as test-point for analog channel part.

4
Measurements

Octal MDT-ASD V4 (8×ASD V4) chip has been designed and realized with the final target to replace Octal MDT-ASD V1 [19] currently used in ATLAS experiments for Muons detection. The replacement is necessary with the HL-LHC Phase II Upgrade but it will be done only when the proper tests will confirm desired performance. For this purpose, a complete electrical characterization has been carried-out by mounting the 8×ASD V4 on the 'mezzanine board', working in the same boundary conditions of the MDT tubes environments.

4.1 Octal MDT-ASD V4 Channel Measurements

All the presented time-measurements have been performed using different equivalent input charge (Q_{IN}) in the full input range 5 fC - 100 fC. The analog characterization is provided only for Channel#7 through a proper *BUFFER* block (see section 3.2) connected to DA_3 voltage output signal analysis. Test point presence for the last channel is the unique different between the eight channels, whose generic block scheme is shown and described in figure 2.5 and in section 2.3, respectively. The $LVDS$ output signals of each channel have been measured allowing a time-domain characterization of the $DISC_1$ and Wilkinson ADC stages, also.

4.1.1 Analog Section Characterization

The analog section of the 8×ASD V4 is composed by the cascade of the CSPreamp and the DA_1-DA_2-DA_3 stages. In order to testing its performance, the ASD has been stimulated with different equivalent input charges and the DA_3 buffer output has been measured (see figure 2.5). Figure 4.1 shows the DA_3 output signal vs. time.

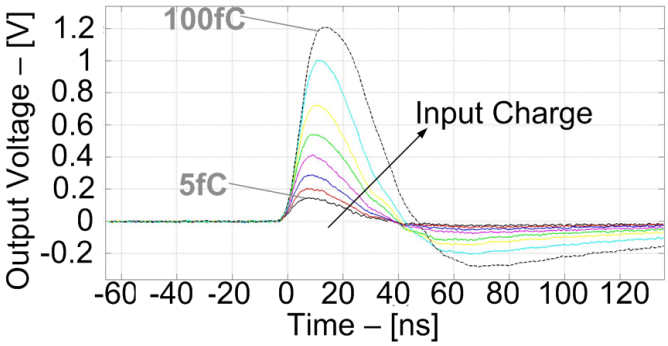

Figure 4.1: DA_3 Output Signal vs. Input Charge 5 fC-100 fC

Some voltage peak drop and a small additional delay (i.e. about 3 dB and 2 ns additional time delay) are observed w.r.t. the effective on-chip DA_3 output signal (really managed by the Wilkinson A/D), mainly due to the on-chip test-point buffers (see figure 2.5) that feature limited frequency/time response performance.

Considering these effects, sensitivity, peak voltage and peaking time delay char-

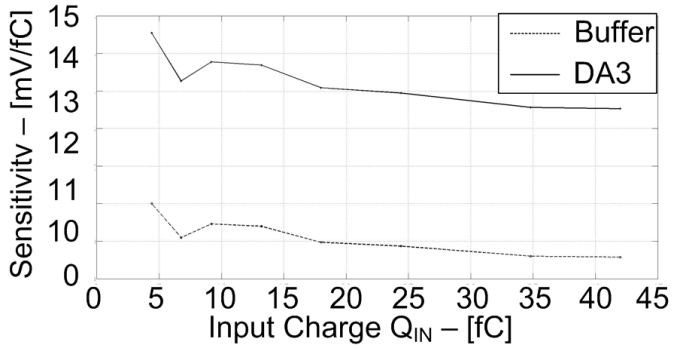

Figure 4.2: Sensitivity at DA_3 and *BUFFER* Output vs. Input Charge

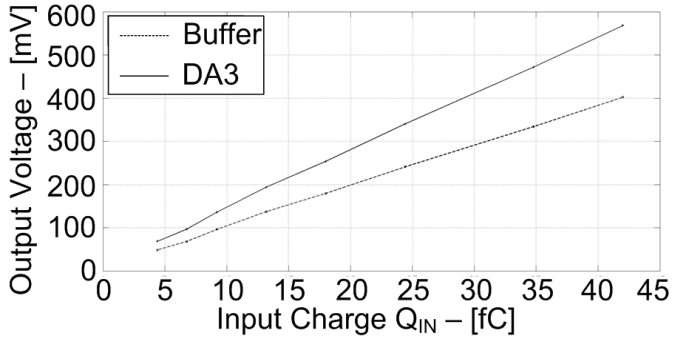

Figure 4.3: Peak Voltage at DA_3 and *BUFFER* Output vs. Input Charge

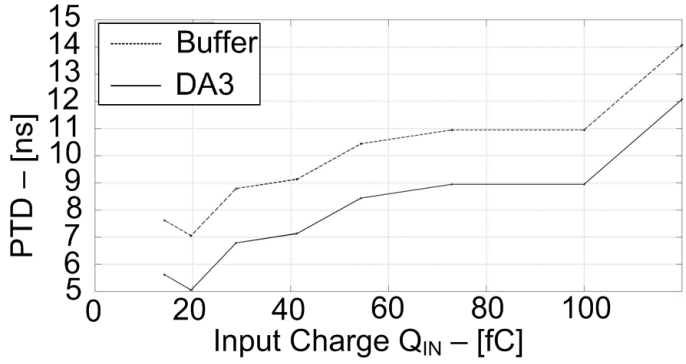

Figure 4.4: Peaking Time Delay at DA_3 and *BUFFER* Output vs. Input Charge

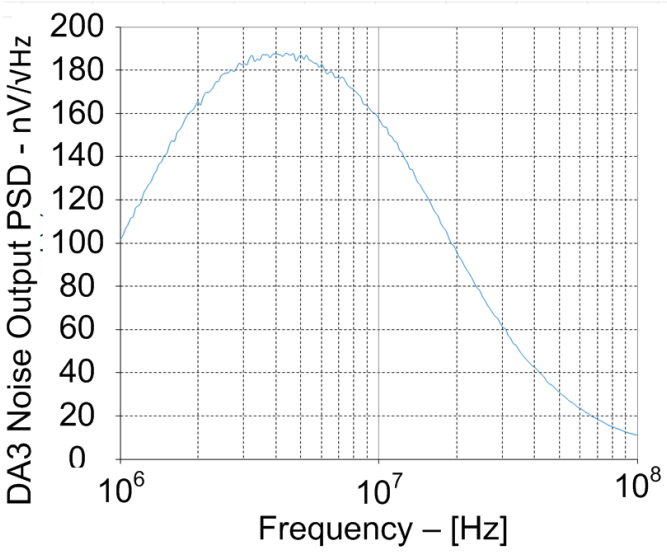

Figure 4.5: DA_3 Output Noise Power Spectral Density

acteristics at DA_3 output has been extrapolated from the measured buffer output signals. For sake of completeness, in the following figures a comparison has been considered. In particular, the DA_3 output voltage ranges from 90 $mV_{0\text{-}PEAK}$ up to 1.2 $V_{0\text{-}PEAK}$. Figure 4.2 shows the sensitivity (i.e. the peak-voltage of the curves in figure 4.3 vs. the input charge) that is 14.2 mV/fC for minimum Q_{IN}. Such sensitivity is quite constant over the input charge range, so no significant voltage swing saturation is presented over the 5 fC - 100 fC range, resulting in a very linear behavior. Peaking-Time-Delay is plotted in figure 4.4. It is lower than 9 ns for minimum Q_{IN} (5 fC) and raises up to 12 ns at 100 fC. This is because for very high input charge the target slope at the output of the CSPreamp increases and as a consequence the analog stages exhibit a small slew-rate saturation (larger input charges imply larger signal swing). So the PTD is lower in small-signal domain (i.e. at input charge <40 fC) and tends to increase when the voltage output swing at the DA_3 passes to hundreds of mV range.

The entire analog section of the channel (including CSPreamp-DA_1-DA_2-DA_3 cascade) has been also evaluated in terms of noise Power Spectral Density (PSD) at the output of the DA_3 buffers. For this noise measurement the input pad (where the input charge pulse has been provided) has been left open and the equivalent C_D capacitor is always connected to ground. Noise PSD curve is shown in figure 4.5, resulting in about 190 $nV/\sqrt{Hz}$ output in-band noise.

4.1.2 Digital Section Characterization

The digital part of MDT-ASD V4 channel includes Wilkinson ADC (W-ADC) and Discriminator stages (see figure 2.5).

Regarding the Wilkinson ADC, it is characterized measuring its output for four different input charge (in the 20 fC - 100 fC range). From this results the linear pulse

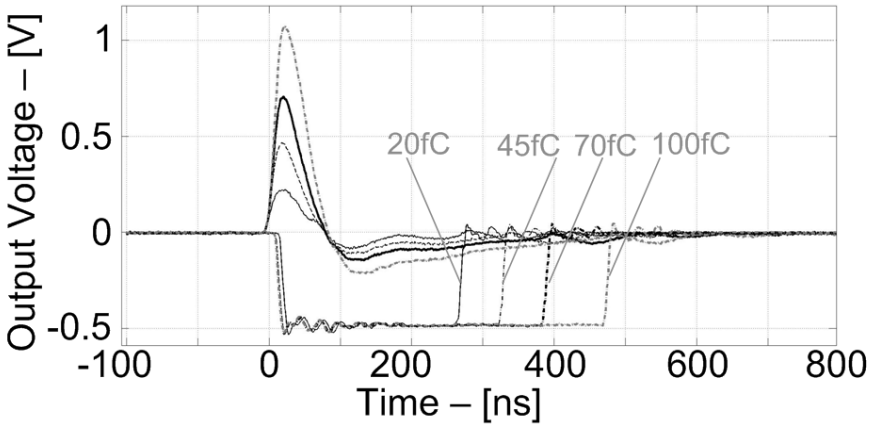

Figure 4.6: W-ADC, DA_3 Output Signal vs. Input Charge

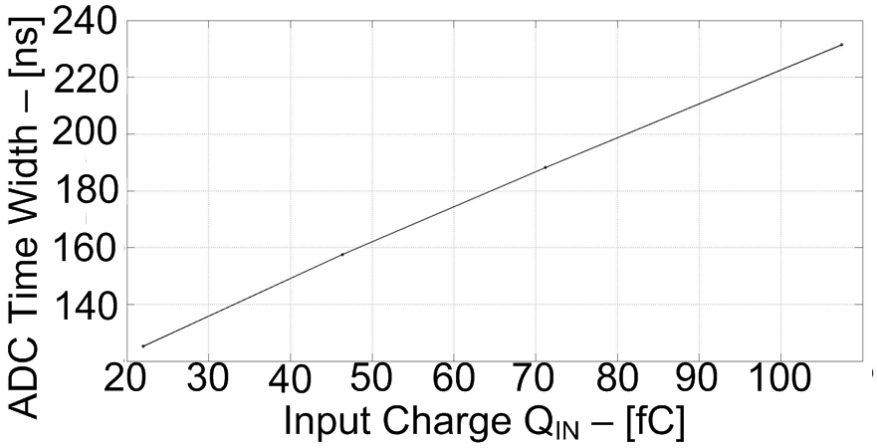

Figure 4.7: W-ADC Output Pulse Time Width vs. Input Charge

width trend reported in figure 4.7 and extrapolated from the W-ADC time domain measured signals (see figure 4.6). The channel provides information about the amount input charges through the pulse width that varies proportionally with the input.

Finally, the discriminator stage has been used to have information about the channels mismatch. In this topology of multi-channels structure, this is important in order to guarantee uniformity, reliability and reproducibility of the acquired data. For this reason, the hit-rate data at the output of the $DISC_1$ vs. channel (see figures 4.8 and 4.9) has been evaluated. The hit-rate is defined as the number of 0→1 switching of the $DISC_1$ in absence of any charge at the input of the channel, whereas the ideal behavior should have 0 hit-rate, i.e. no switching. Such parameter plays a key role in this kind of physics experiments, because it is directly linked with the minimum input charge that can be detected. The hit-rate performances are shown in figures 4.8 and

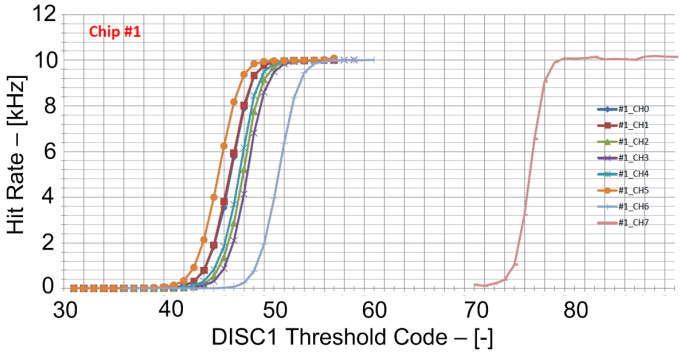

Figure 4.8: Chip#1 Hit-Rate vs. Channel

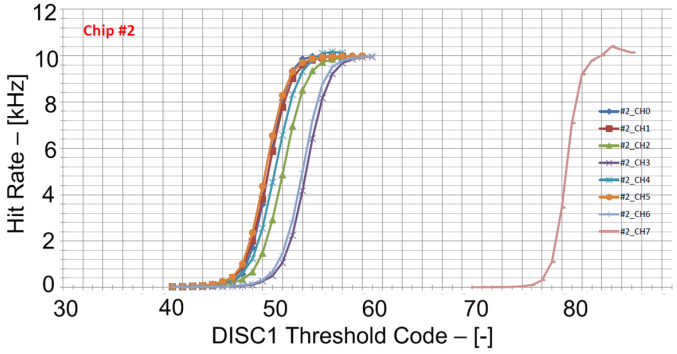

Figure 4.9: Chip#2 Hit-Rate vs. Channel

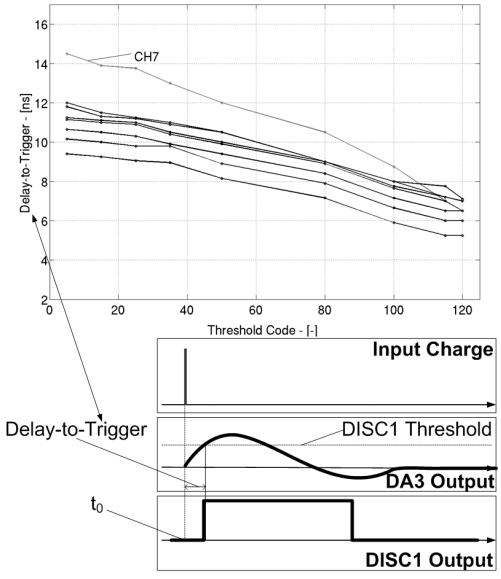

Figure 4.10: Delay-to-Trigger vs. Threshold Code for CH0-CH7

4.9. The 0/6 channels (i.e. CH0 - CH6) look like very similar differently from CH7, where the presence of the DA_3 test point buffer is introducing some additional delay and voltage drop. However such test-points are here only used for testing purposes and they will be disabled in the final application. Basically for each channel, and for a given $DISC_1$ hysteresis value, the $DISC_1$ input threshold voltages are swept, and the DISC1 output signal is evaluated. Hence, there is a certain threshold code range (40/50 digital threshold code, corresponding to approximately 175 mV/155 mV differential threshold), where a certain number of switching events are observed at the output of $DISC_1$ in absence of any input signal. These are noisy events, since no signal has been applied at the CSPreamp input node. As a result, the 175 mV/155 mV threshold voltage corresponds to approximately <5 fC input charge, fixing this way the minimum detectable event at about 5 fC.

Figure 4.10 shows the delay-to-trigger for each channel, sweeping the threshold code of the $DISC_1$ for 0 to 120. The delay-to-trigger is defined as the delta time between the charge arrival time and the DISC1 switching (as highlighted in figure 4.10). Notice that with reference to the horizontal axis in figure 4.10, when the differential threshold is in the few mV range (higher digital codes), the $DISC_1$ speed response obviously increases. On the other hand, at lower digital codes (when the differential voltage threshold is higher) the delay-to-trigger tends to be higher. The most relevant result of such time performance is that a few ns variation is observed in delay-to-trigger curves for each channel (CH0 - CH6) and that each curve fits with the maximum allowed delay-to-trigger (i.e. <15 ns).

Parameter	***Octal MDT-ASD V4***	***[19]***
CMOS Tech.	130 nm	500 nm
Total Die Area	6.38 mm^2	11.9 mm^2
Supply Voltage	3.3 V	3.3 V
Channel Current Consumption	10 mA	11 mA
Detector Parasitic Cap.	60 pF	60 pF
Shaping Function	Bipolar	Bipolar
Input Charge Range	5 fC - 100 fC	5 fC - 100 fC
Front-End Delay at 100 fC-Q_{IN}	12 ns	∼15 ns
Front-End Sensitivity	14 mV/fC	8.9 mV/fC
ENC	0.6 fC	1 fC
SNR at minimum input charge	15 dB	10.9 dB

Table 4.1: MDT-ASD V4 State-of-the-Art Comparison

4.1.3 Octal MDT-ASD V4 Performance

The most important performance have been compared (see Table 4.1) with the previous implementation [19]. Thanks to 130 nm technology, area (2×factor) and noise are reduced maintaining the same power budget. Notice that in this design the CSPreamp input transistor has been pushed into moderate inversion region maximizing this

way MOST efficiency, or in other words higher g_m at slightly lower I_{DS} current has been achieved. This allows to reduce of about 9 % the current consumption (10 mA instead of 11 mA, respectively). This power reduction has been obtained without degrading sensitivity (charge-to-voltage conversion gain) and noise performance. More specifically, higher sensitivity at the Comparator input has been measured (14 mV/fC vs. 8.9 mV/fC) and ENC in 0.6 fC instead of 1 fC. As a consequence also SNR is 4.1 dB higher than in previous design. This improves the sensing capability of the front-end, reduces the bit error probability and finally enhances signal quality. The peaking time delay is 12 ns, i.e. 3 ns lower than the state-of-the-art, resulting in faster response and reduced probability to muons data loss.

4.2 From Octal MDT-ASD V4 to Octal MDT-ASD V5

Although in the section 4.1 promising results have been reported, Octal MDT-ASD V4 chip testing shown some issues, also. Generally, the system is able to perform all functions but an optimization is required before the final fabrication. In particular, optimized details in Octal MDT-ASD V5 chip are discussed in the remaining part of this section.

4.2.1 Channel#7 Mismatch

As highlighted in figures 4.8 and 4.9, Octal MDT-ASD V4 chip presents a mismatch from the others channels linked to *BUFFER* presence as shown with Calibre PEX simulations. According to measurements, the Channel#7 begins to trigger events through $DISC_1$ around -95 mV (code 80) and not in the range -157 mV to -133 mV (code range 49 - 61). These numbers are justified with a DA_3 output signal smaller, slower and less noisy of a factor in the range 1.4 - 1.65. Post-layout simulations demonstrated that the connection between the DA_3 and the *BUFFER* is inappropriate. It has a width and a length of 25 µm and >1 mm, respectively, influencing DA_3 performance with a parasitic capacitance of ∼1.5 pF. In fact, adding this parasitic capacitance at Channel#7, AC and noise simulations demonstrate bandwidth and PSD reduced by a 1.35 factor. The same results have been obtained with Post-Layout simulation connecting or disconnecting the *BUFFER*. In time domain, this condition is instead translated in:

- Amplitude reduction from 161.7 mV to 95.5 mV (see figure 4.13)
- Peaking Time Delay increment from 12.8 ns to 16.8 ns (see figure 4.13).

To avoid these effects, layout must be improved moving the *BUFFER* in proximity of the Channel#7 DA_3 and using shorter and less width wires to connect them. This approach has been adopted in Octal MDT-ASD V5 chip providing the possibility to disconnect the *BUFFER* through some switches, also. The new prototype has been realized and the preliminary measurements shown that the issue has been fixed. In particular, the new Hit Rate is represented in figure 4.14 highlighting that the Channel#7, when the *BUFFER* is disconnected, is in line with the others and the internal offset of channels is extremely low -4 mV. Enabling analog output, the

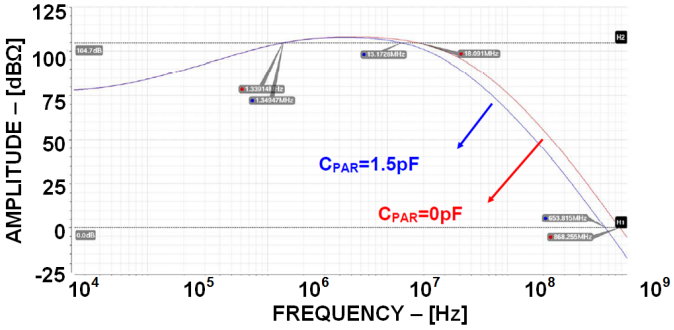

Figure 4.11: Frequency Response DA_3 Output with (1.5pF) and without (0pF) BUFFER

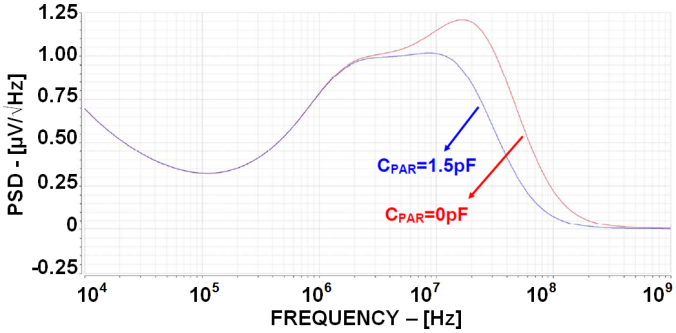

Figure 4.12: Noise DA_3 Output with (1.5pF) and without (0pF) BUFFER

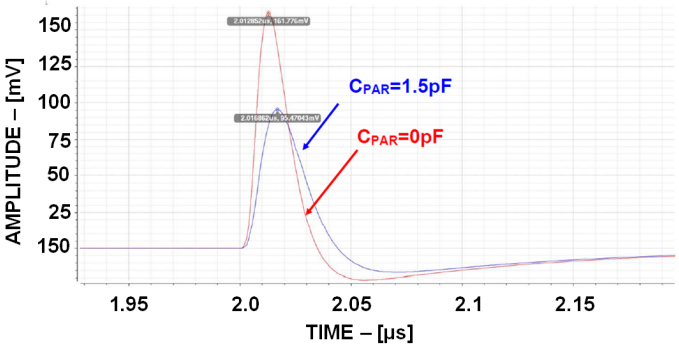

Figure 4.13: DA_3 Output Voltage with (1.5pF) and without (0pF) BUFFER

situation is very similar and there is an effective shifting threshold of 5 mV (see figure 4.15).

4.2.2 Feedback Ringing

Another important phenomena observed in Octal MDT-ASD V4 measurements is shown in figure 4.16. A tiny pulse ($\sim$ 35 mV differential) is induced into the analog

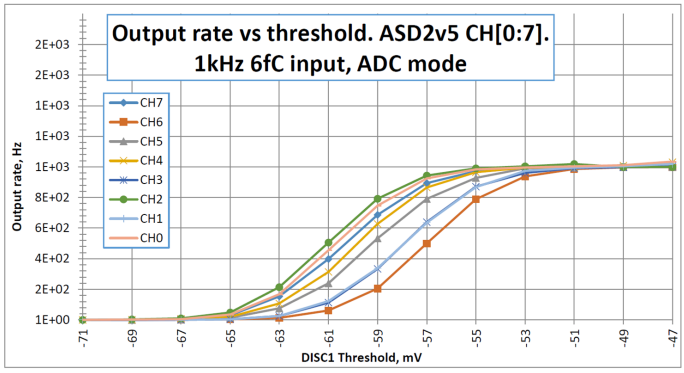

Figure 4.14: Hit-Rate vs. Channel disabling the *BUFFER*

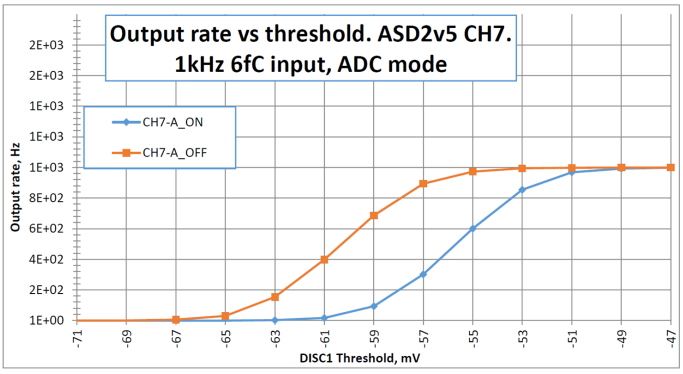

Figure 4.15: Channel#7 Hit-Rate enabling and disabling the *BUFFER*

chain by the trailing edge of the output signal. This may cause re-trigger of the discriminator when operating at low threshold (see bottom of the figure 4.16). Instead, the interval between leading and trailing edge results correct varying with pulse height.

The bump presence is translated in $DISC_1$ oscillation represented in figure 4.18. Here the signal seems to oscillate for low threshold1 level near to the channel noise. In this case, there is not a proper oscillation but a discriminator sensible to the channel noise. For this purpose, an analysis of the all possible noise contributions has been done to search because the noise is greater than that expected. Considering the simplified scheme reported in figure 4.18, at DA_3 output the overall noise derives from quadratically sum of the following components:

- noise due to electronic components
- supply noise amplified by the analog chain
- ground noise amplified by the analog chain.

In the ideal situation, supply and ground noises must be negligible. Unfortunately this does not happen because the structure implemented is pseudo-differential and

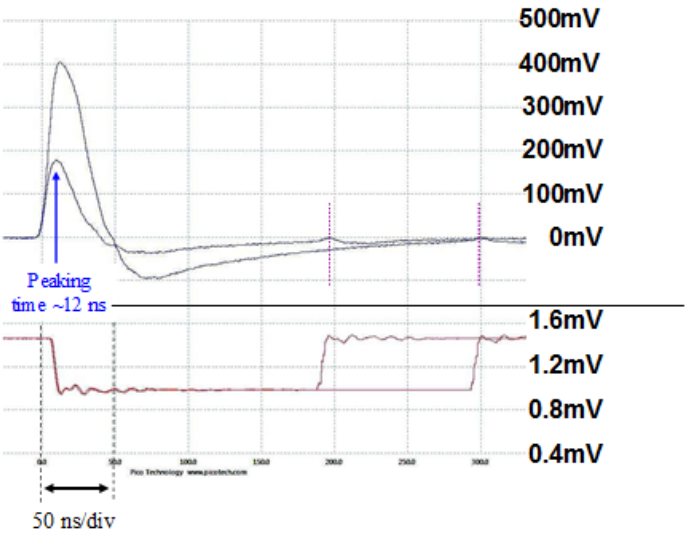

Figure 4.16: DA_3 (top) and LVDS (bottom) Outputs of Channel#7

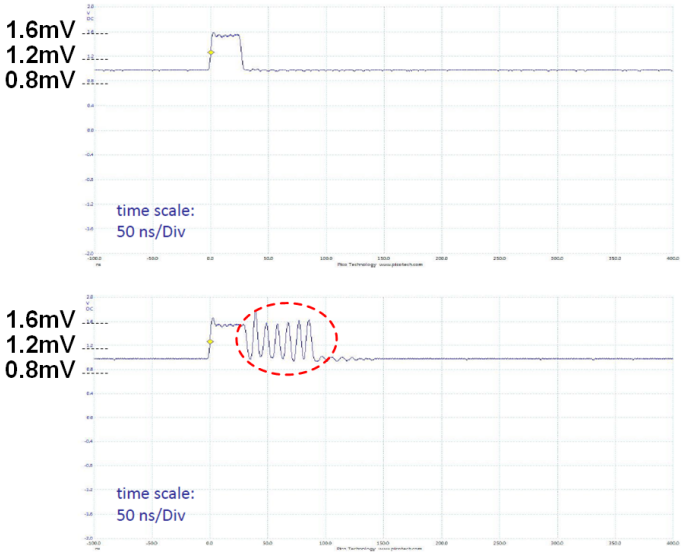

Figure 4.17: $DISC_1$ Output for threshold code 105 (top) and 107 (bottom)

not fully differential. Supplies interferes result amplified of 6.2 dB around 26 MHz at CSPreamp (first MDT-ASD V4 stage) output (see figure 4.19). A more robust architecture is required and an optimization of CSPreamp represented in figure 2.6 is more difficult. The problem of this circuit topology is that the ground (and so the noise) is directly connected to M_1 input transistor. A CSPreamp based on single ended cascoded opamp helps to de-coupling output from the noise generator benefiting

of node A virtual ground. The CSPreamp implemented in MDT-ASD V5 channel is shown in figure 4.20. It is a single ended opamp in closed loop with a resistor (R_F + R_S) and a capacitance C_F. The result is an improvement of the noise propagation confirmed by figure 4.21. The factor of 6.2 dB amplification is reduced up to -9 dB without degrading the CSPreamp performance as shown in 4.22.

The noise propagation in MDT-ASD V5 channel is limited improving supplies and groundes connections, also. For this reason, in Octal MDT-ASD V5 chip, BFMOAT layer has been used in order to increase the substrate isolation and improve the supplies division. Considering layout influence on noise propagation, routing of the more critical block has been reviewed inducing changes in terms of area, number and position of the pins. The area has been increased from 6.73 mm^2 to 7.64 mm^2 and 74 pins (organized as shown in figure 4.23 and 4.22) are used.

4.2.3 Rundown Issue

Measurements demonstrated no output signals appear (unexpected results) for rundown code above 4 (see 4.25). In Octal MDT-ASD V5 chip this issue is automatically resolved improving robustness to noise and substrate isolation.

4.2.4 Dead Time Issue

The last issue taken in account regards the Dead-Time (DT) range. The DT parameter is used to disable the Wilkinson ADC for a DT time. In measurements, it is smaller than expected: the maximum measured dead-time is around 480 ns instead of 700 ns. For this purpose, the generator of DT has been re-designed changing the size of the binary weighted switched resistor string. Finally, a local DT generation in each channel has been introduced to limit mismatch between the channels. Simulating the channel in this condition, V5 DT range varies from 23.92 ns to 738.67 ns.

Octal MDT-ASD V5 chip is in testing phase and measurements on these details are not performed, yet.

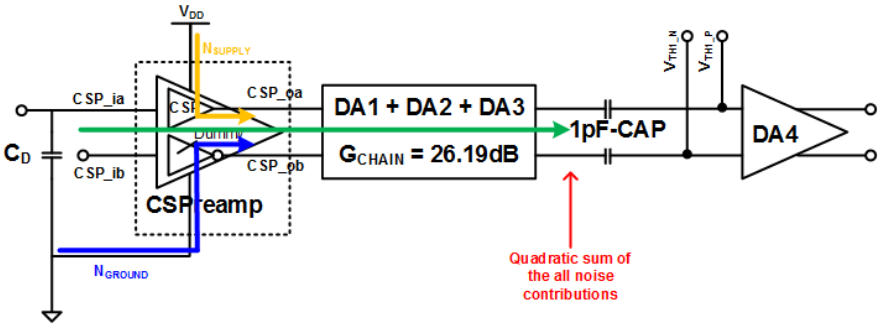

Figure 4.18: Simplified Scheme of Analog Noise contributions

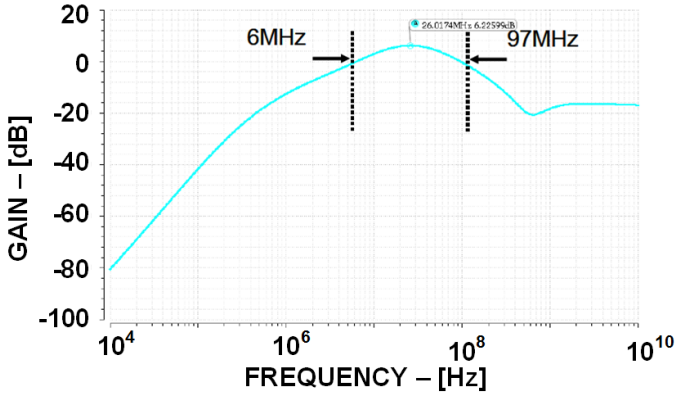

Figure 4.19: Frequency Response of N_{SUPPLY} and N_{GROUND} contributions

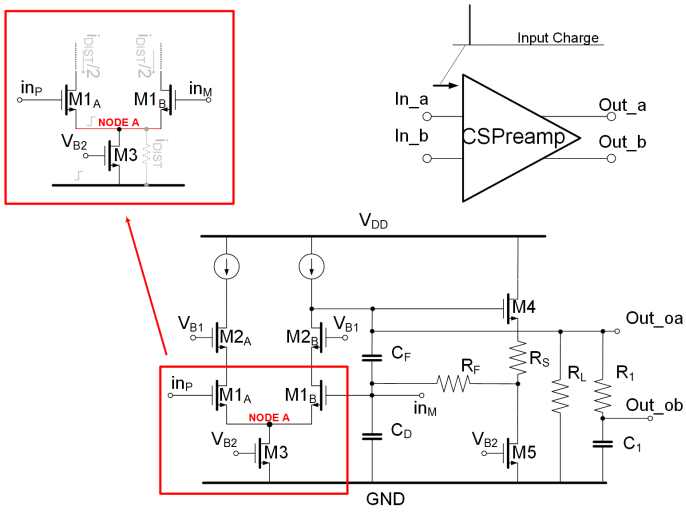

Figure 4.20: Block scheme of the CSPreamp implemented in MDT-ASD V5 channel

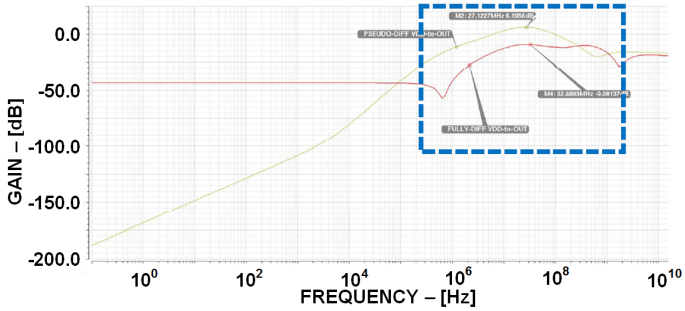

Figure 4.21: Frequency Response of N_{GROUND} contributions for CSPreamp V4 (Yellow Curve) and CSPreamp V5 (Red Curve)

Parameters	Units	OLD CSPreamp			NEW CSPreamp		
		Nominal	PVT		Nominal	PVT	
			min	max		min	max
Peak Voltage Preamp	mV	3.933	3.644	4.278	3.528	3.338	3.66
Peaking Time Preamp	ns	8.446	6.89	9.597	8.174	7.436	9.531
Peak Voltage DA1	mV	9.93	8.425	11.17	8.997	7.58	10.35
Peaking Time DA1	ns	9.746	7.22	11.13	8.615	7.815	9.892
NOISE_Preamp	μV_{RMS}	554.5	506.9	593.1	565.2	506.8	634.4
SNR_Preamp	dB	14.01	13.16	14.92	12.9	13.4	12.2
CSPreamp Current Consumption	mA	3.91	3.807	3.99	4.381	4.202	4.43

Figure 4.22: V4 (Old) and V5 (New) CSPreamp Performance

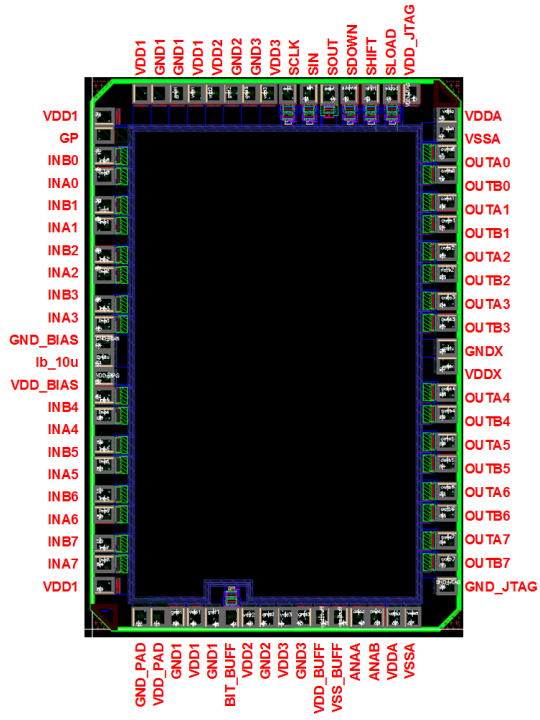

Figure 4.23: Octal MDT-ASD V5 Pin Diagram

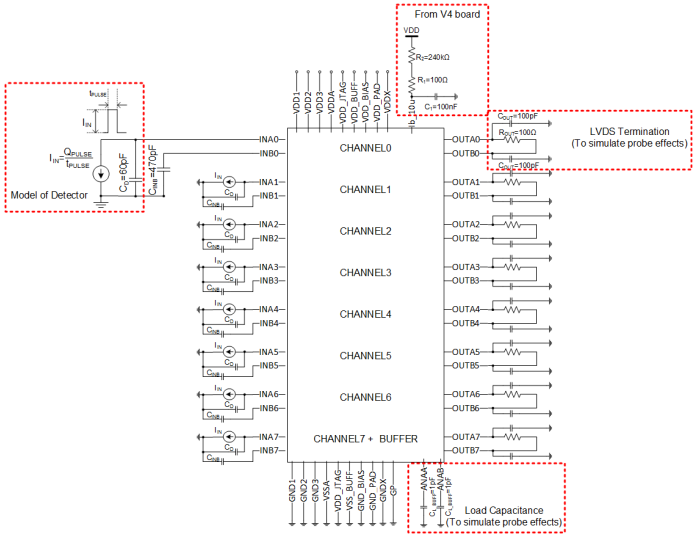

Figure 4.24: Octal MDT-ASD V5 Simplified Simulated Scheme

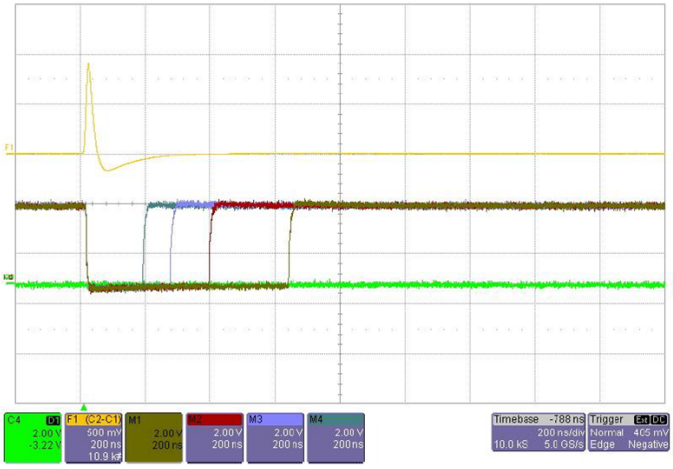

Figure 4.25: Measure of Wilkinson ADC Output for different Rundown Code

BLOCK	PIN NAME	DESCRIPTION	TYPE	#	I/O INTERFACE
JTAG Serial Interface 8 PADs	SCLK	Clock Line	Digital In	1	Vpulse Generator
	SIN	Load Control Line	Digital In	1	Vbit Generator
	SDOWN	Down Control Line	Digital In	1	Vpulse Generator
	SHIFT	Shift Control Line	Digital In	1	Vpulse Generator
	SLOAD	Data Line	Digital In	1	Vpulse Generator
	SOUT	Data Line	Digital Out	1	noConn Istance
	VDD_JTAG	JTAG Supply Voltage	Analog In	1	DC-Voltage Generator of 3.3 V±5 %
	GND_JTAG	JTAG Ground Voltage	Analog In	1	DC-Voltage Generator of 0 V
MDT-ASD V4 Channel 55 PADs	<ina0:ina7>	Positive Channel Input	Analog In	8	1 nF Cap or Current Generator in parallel with 60 pF Cap
	<inb0:inb7>	Negative Channel Input	Analog In	8	470 pF Cap
	<outa0:outa7>	Positive Channel Output	Analog Out	8	Input 'A' LVDS Termination
	<outb0:outb7>	Negative Channel Output	Analog Out	8	Input 'B' LVDS Termination
	VDD_1	CSPreamp Supply Voltage	Analog In	5	DC-Voltage Generator of 3.3 V±5 %
	GND_1	CSPreamp Ground Voltage	Analog In	4	DC-Voltage Generator of 0 V
	VDD_2	Analog Section Supply Voltage	Analog In	2	DC-Voltage Generator of 3.3 V±5 %
	GND_2	Analog Section Ground Voltage	Analog In	2	DC-Voltage Generator of 0 V
	VDD_3	Digital Supply Voltage	Analog In	2	DC-Voltage Generator of 3.3 V±5 %
	GND_3	Digital Ground Voltage	Analog In	2	DC-Voltage Generator of 0 V
	VDD_A	MUX-LVDS Supply Voltage	Analog In	2	DC-Voltage Generator of 3.3 V±5 %
	VSS_A	MUX-LVDS Ground Voltage	Analog In	2	DC-Voltage Generator of 0 V
	VDD_X	Common Block Supply Voltage	Analog In	1	DC-Voltage Generator of 3.3 V±5 %
	GND_X	Common Block Ground Voltage	Analog In	1	DC-Voltage Generator of 0 V
Channel#7 Buffer 2 PADs	anaa	DA_{3oa} of Channel#7	Analog Out	1	1 pF Cap
	anab	DA_{3ob} of Channel#7	Analog Out	1	1 pF Cap
	VDD_BUFF	Buffer Supply Voltage	Analog In	1	DC-Voltage Generator of 3.3 V±5 %
	VDD_BUFF	Buffer Ground Voltage	Analog In	1	DC-Voltage Generator of 0 V
	BIT_BUFF	Buffer Power ON bit	Digital In	1	Vpulse Generator
External Bias 3 PADs	Ib_10 u	Current Generator	Analog In	1	Current Generator of 10 µA± 5 %
	VDD_BIAS	External Bias Supply Voltage	Analog In	1	DC-Voltage Generator of 3.3 V± 5 %
	GND_BIAS	External Bias Ground Voltage	Analog In	1	DC-Voltage Generator of 0 V
Supplies 3 PADs	VDD_PAD	Padring Supply Voltage	Analog In	1	DC-Voltage Generator of 3.3 V± 5 %
	GND_PAD	Padring Ground Voltage	Analog In	1	DC-Voltage Generator of 0 V
	GP	Padring Ground Plane	Analog In	1	DC-Voltage Generator of 0 V

Table 4.2: Octal MDT-ASD V5 Pin List

Part IV

IC-PIX28 Prototype

5
Front-End

A dedicated integrated circuit for pixel detector has been integrated in 28nm Bulk-CMOS Technology. It is named "ICPIX28", acronym of Integrated Circuit for PIXel in 28nm. In this chapter, the most relevant features of this chip will be analyzed, from design to experimental test measurements. In figure 5.1, the generic block scheme of a single pixel read-out channel has been represented. It includes three main blocks:

- *Pixel Detector*: particle detection and electrical signal generation;
- *Charge Sensitive Preamplifier*: for charge to voltage conversion and amplification;
- *Comparator*: for voltage to time conversion.

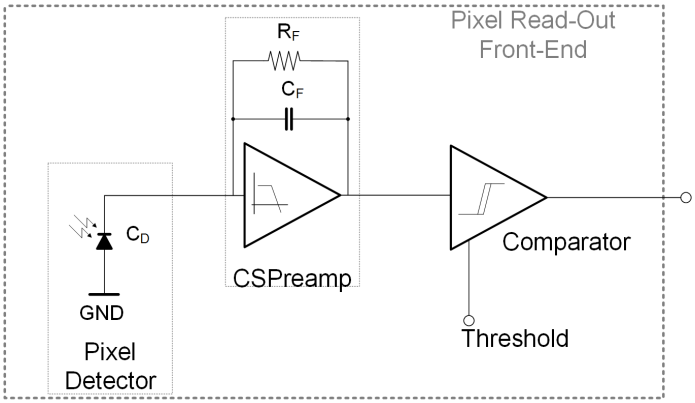

Figure 5.1: Pixel Read-Out Front-End Block Scheme

5.1 Pixel Detector

Pixel detectors were born for particle physics but they are widely used in many other fields where the incident photons may be detected to rebuild an image. The imaging is important in the photography world as well as in medicine, biology and astrophysics ones. Each applications is unique and it is thought for a specific purpose. In every cases, the efficiency depends on the capability to detect and convert a very small charge in a very short time. Increasing the number of the detectors, it is possible to recover a lot of information about the same system increasing the resolution. It is fundamental because if we consider the particle physics, one of the main target is to study the short-lived particles with high speed, good time resolution, good sensitivity

and stability without being affected by the noise and the surrounding radiation. It is not trivial.

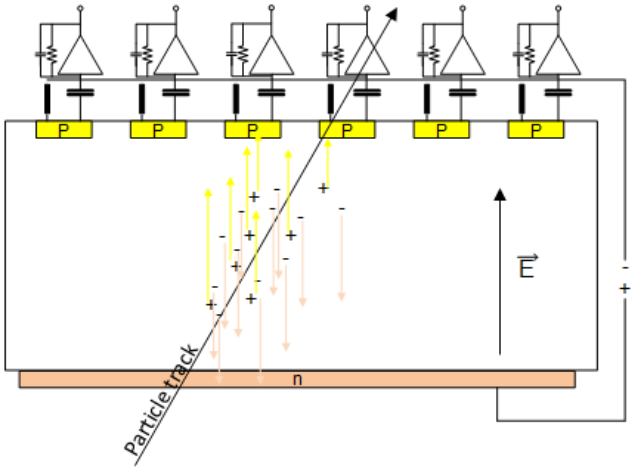

Figure 5.2: Simplified Scheme of a APSs matrix

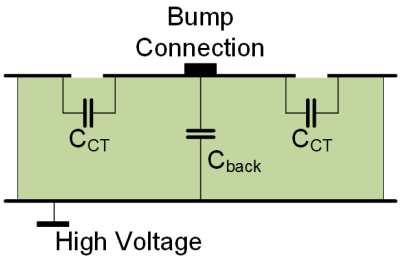

Figure 5.3: Capacitances of a pixel sensor

Typically, a pixel detector works with high-energy accelerators that generate elementary particle collisions at a rate of 10 – 100 MHz. The number of the particles emerging from every collision is restricted to maximum a hundred and its lifetime is in the order of few picoseconds.

To increase performance and efficiency of the system, matrices of pixel detectors are necessary and they may cover large area. In this scenario, area optimization of the single pixel system is fundamental. A pixel system is a CMOS Active Pixel Sensor (APS [32] [33]) and includes the detection and the electronic processing sections. In the same die, there are sensor and electronics with more benefits in terms of compatibility, information loss and reliability. A simplified scheme of a APSs matrix is reported in figure 5.2 including single-sided positive sensitive strip detector [34]. Electrodes of single-sided microstrip detectors are thin parallel strips of low resistivity p-doped silicon. These thin layers are able to convert the energy deposited by a particle to an electrical signal. The pn-junction is realized between n-well and p-type epitaxy and the charge collection happens through drift and diffusion of the carriers.

In a fully-depleted semiconductor sensor, electron-hole pairs are swept to electrodes by an electrical field, inducing an electrical current.

The ionizing of the particle in the silicon is proportional to the energy loss. This is the input charge (in term of electrical current) of the preamplifier. In the physics application, one hit pattern reveals one event presence. Proper read-out architectures are capable to extract information from some patterns selecting only events with the same features. Other applications (like X-ray radiography) require instead that one image is made of many events because the information is uniformly distributed on all events [35].

The electronics chip must be very close ($10-20\,\mu m$) to the sensor occupying a small area. Considering scaled technology development, the area for each channel is in order of few thousand μm^2 allowing an increment of pixel density in a complex system. The sensing element of the pixel detectors has a small area respect the other physics detectors and its paracitic capacitance is very low (smaller than 0.5 pF). This is an advantage for this topology of the circuit since it allows fast signal shaping with very low noise. The total capacitance of each pixel is originated from the capacitance to the backside (C_{back}), to neighbor pixels (Cross Talk Capacitance - C_{CT}) and to the ground plane (see figure 5.3). The former contribution (C_{back}) is determined by the pixel area A, the sensor thickness d and the dielectric costant of the sensor material ϵ (5.1).

$$C_{back} = \epsilon_0 \, \epsilon_{Si} \, \frac{A}{d} \tag{5.1}$$

The collected charge on the detector depends on the detector characteristics (i.e. active thickness or crystalline structure of the material) and the irradiation flux in the surrounding environment.

The evolution of the accelerators (scheduled for 2024 with High-Luminosity Large Hadron Collider project at the CERN) forces detector and electronics updating with the main target to show reliability in presence of:

- charged particles with higher energies and intensities;
- a Total Ionizing Dose (TID) of 1 Grad in 10 years.

This is possible thanks the development of new scaled technology as the 28nm CMOS one. The first test on the single devices showed encouraging results up to 1 Grad TID [36] and it has been done in parallel with this work. The collaboration has allowed to validate and justify the changes of IC-PIX28 behaviour between before and after radiation that will be shown in the Chapter 7.2. The entire study was carried out within the ScalTech28 project of INFN Milano Bicocca with the main target to improve the radiation hardness of HEP electronics.

5.2 28nm Bulk-CMOS Technology

The choice of a certain type of technology is important and heavily dependent on the application. 28nm Bulk CMOS Technology is one of the new Scaled Technology

(ScalTech). Its development is fundamental for high-speed and/or low-power digital circuits and critical for analog circuits. The joint reduction of supply voltage (V_{DD}) and capacitance *C* (quadratically with the device size) trivially leads to a power decrement according to 5.2. On the other hand, scaling down doesn't imply low power and high performance for analog part.

$$P = f\, C\, V_{DD}^2 \tag{5.2}$$

In fact achievable analog performance are strongly dependent on schematic and layout design. Typical technology scaling effects are:

- lower device output impedance (r_o) and consequent lower transistor intrinsic dc-gain ($g_m\, r_o$ < 10 dB);
- lower supply voltage (V_{DD} of 0.9 V), due to the thinner oxide;
- higher threshold voltage (V_{TH}) and consequent lower ($V_{DD} - V_{TH}$=0.4 V);
- large Process-Voltage-Temperature (*PVT*) variability that requires wider and asymmetrical compensation range arrangements;
- higher gate leakage current due to quantum tunneling effect.

Considering these not negligible changes, schematic design and its optimization are not trivial. Unfortunately, this situation is worsen by layout and its parasitic components introduction. Some of them are due to limited freedom in MOS sizing (not all combination of width and length are possible) and to metal sheet resistance very high (up to 0.45 Ω/sq). Furthermore Well Proximity Effect (WPE) and Shallow Trench Isolation (STI) stress produce mobility/V_{TH} variation and mismatch affecting bandwidths, currents, gains, etc... This scenario becomes even more critical with extremely high Total Ionizind Dose (TID) as that expected for the future High-Luminosity Large Hadron Collider (HL-LHC). To guarantee the target performance even in presence of these effects the solution is to combine improved and/or novel analog techniques and Digital Assisted (DA) approach. This consist in exploiting the high efficiency *ScalTech* digital section to recover performance loss due to analog device poorer behavior.

IC-PIX28 is a Pure Analog circuit where the DA approach is not applicable. In principle, DA approach cannot be efficiently applied in several analog circuits like non-repetitive chains and fully-continuous-time chains. In these cases, it is fundamental to have a deep knowledge of the *ScalTech* devices behavior and of the system to be developed in order to search suitable solutions to achieve target performance (i.e. linearity, gain accuracy, bandwidth, speed-of-response, noise, ...).

5.3 IC-PIX28 Channel

A pixel detector is designed with suited read-out electronics composed by a matrix of several thousand channels, as highlighted in the previous section (see figure 5.2). The

area of each pixel must be maintained as small as possible to guarantee a good spatial resolution of the system.

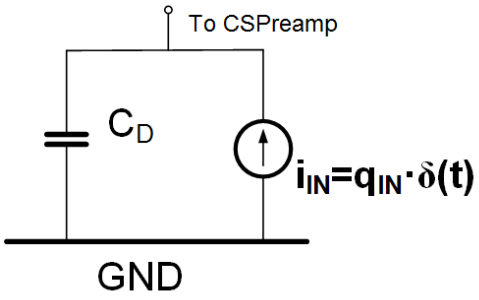

Figure 5.4: Simplified equivalent circuit of a pixel sensor (neglecting the leakage current)

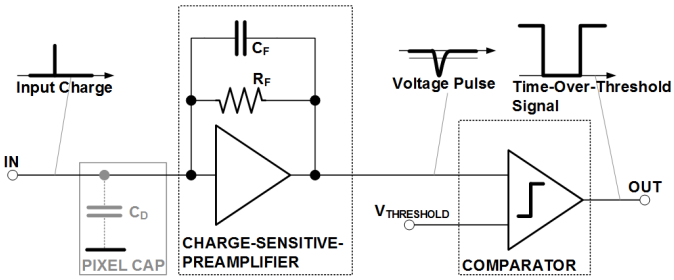

Figure 5.5: IC-PIX28 generic block scheme

A single channel can be modeled as the chain shown in figure 5.1: a preamplifier in cascade with a voltage to time converter. It is a simplified version neglecting the interface between the overall system. The input chain signal is a current signal coming from the pixel sensing element. Channel design must be done considering that the input current signal is affected by the sensor detector. Its simplified equivalent circuit as reported in figure 5.4 includes a current generator and a parasitic capacitance (C_D) to emulate C_{back} and C_{CT} capacitances. Typical Pixels have capacitance in the order of 100 fF and leakage current of the order of 10 pA before irradiation [35].

IC-PIX28 architecture is shown in figure 5.5 and it has been designed to feature the performance summarized in 5.1. The proposed read-out front-end channel design manages the issues mentioned in 5.2 with dedicated and efficient low-power techniques. In particular, sub-threshold devices have been exploited to minimize Charge-Sensitive-Preamplifier (CSPreamp) power consumption and the static power of the comparator is reduced to zero implementing a switched-cap scheme.

5.3.1 Charge Sensitive Preamplifier

The Charge Sensitive Preamplifier (CSPreamp) is the first and the main critical block of a read-out front-end for physics particle. A typical CSPreamp converts an input

Parameter	*Value*
Power Supply	0.9 V
Power Consumption	< 5 µW
Rise Time	< 25 ns
Noise Level	∼ 200 e⁻
Detector Capacitance	∼ 100 fF
Equivalent Noise Charge	< 0.1 fC

Table 5.1: Summary of Specification

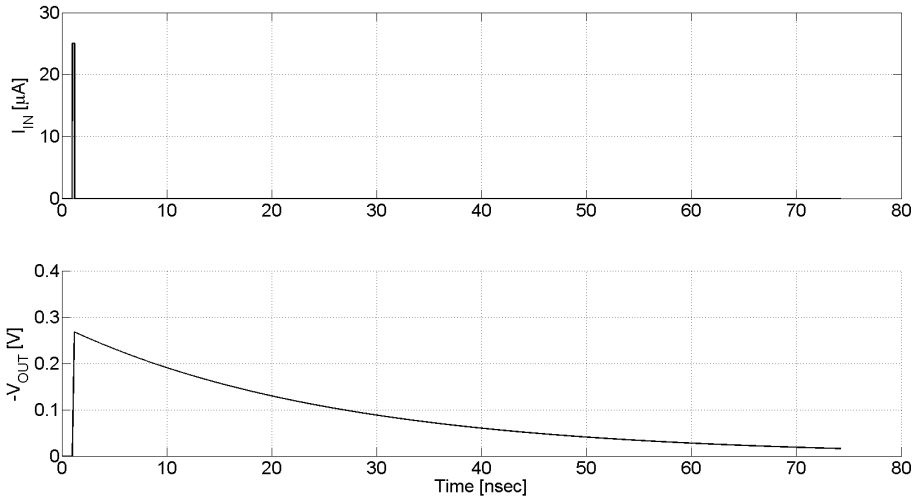

Figure 5.6: Input Current and Inverted Output Voltage

charge Q_{in} to a voltage through an inverting amplifier with a capacitor C_F and a resistor R_F in feedback. R_F is required in order to define the DC-operating point of the CSPreamp and to remove signal charges from the input nodes (or from C_F after the dynamic response of the amplifier) so that the preamplifier output voltage returns to its initial value [35]. As shown in figure 5.6, when the system detects an input charge, an infinitesimal impulse of current (I_{IN}) appears at CSPreamp input. I_{IN} amplitude depends on the ratio between the input charge Q_{IN} and the impulse life (Q_{TIME}). In presence of an I_{IN}, the CSPreamp instantly returns an output voltage signal (V_{OUT}) with a temporal trend given by the expression 5.3.

$$V_{OUTid}(t) \cong \frac{Q_{in}}{C_F}\, e^{\frac{t}{\tau_{p1}}} \tag{5.3}$$

The τ_{p1} is the time constant of the system and it is determined by $C_F\, R_F$ product. Baseline recovery is entrusted only to CSPreamp when its output voltage is directly connected to hit discriminator. In this case, the discharge must be finished before that

the next signal arrives because it could affect the maximum peak reached.

In an ideal world, the gain amplifier is infinite, the input is a node of perfect virtual ground, the frequency response is given by 5.4 and the output voltage signal reaches a maximum V_{PEAKid} depending on input charge Q_{in} and C_F capacitance (5.5).

$$\frac{v_{OUTid}}{i_D}(s) = -\frac{R_F}{1 + s\,C_F\,R_F} \tag{5.4}$$

$$V_{PEAKid} = -\frac{Q_{in}}{C_F} \tag{5.5}$$

In the real world, the CSPreamp gain is finite (A_0) and a small voltage signal at the input node appears. This input voltage is inversely proportional to A_0 and the input capacitance C_{in} according to 5.6 [35].

$$\Delta V_{in} = \frac{Q_{in}}{C_{in} + (1 + A_0)\,C_F} \tag{5.6}$$

C_{in} is the sum of the detector capacitance C_D, the preamplifier input capacitance C_{amp} and parasitic capacitance C_{par}. In the next equations, C_{in} is supposed equal to C_D. This approximation is true in the cases if it is in the pF-order. For pixel application, all C_{in} components are in the same fF-order and there is not a predominant one. Hence, the approximation is not valid but the equations may still be used including in C_D the other components. Considering these no-ideality, 5.3, 5.4 and 5.5 become 5.7, 5.8 and 5.9, respectively.

$$V_{OUT}(t) \cong \frac{Q_{in}}{C_F}\,\frac{1}{1 + \frac{1}{A_0} + \frac{C_D}{A_0\,C_F}}\,e^{\frac{-t}{\tau_{p2}}} \tag{5.7}$$

$$\frac{v_{OUT}}{i_D}(s) = -\frac{A_0\,R_F}{1 + A_0 + s(C_D\,R_F + C_F\,R_F + A_0\,C_F\,R_F)} \tag{5.8}$$

$$V_{PEAK} = -\frac{Q_{in}}{C_F}\,\frac{1}{1 + \frac{1}{A_0} + \frac{C_D}{A_0\,C_F}} \tag{5.9}$$

$$\tau_{p2} = C_F\,R_F\,(1 + \frac{C_D}{A_0\,C_F}) \tag{5.10}$$

The time constant τ_{p2} (5.10) depends on $R_F\,C_F$ product, A_0 gain and the ratio between C_D and C_F. Therefore they could be properly sized in order to maximize the charge collection efficiency. The A_0 maximum value depends on CMOS technology and it is linked to the circuit complexity. A key parameter of the CSPreamp is also the sensitivity (S), defined as the ratio between the peaking voltage at the CSPreamp output and the corresponding input charge. In this particular case, S is given by 5.11, where S_{id} is the ideal sensitivity, i.e. neglecting A_0 and C_D effects. Unfortunately, A_0 and C_D effects are not negligible and they have been reported in figure 5.7 and 5.8.

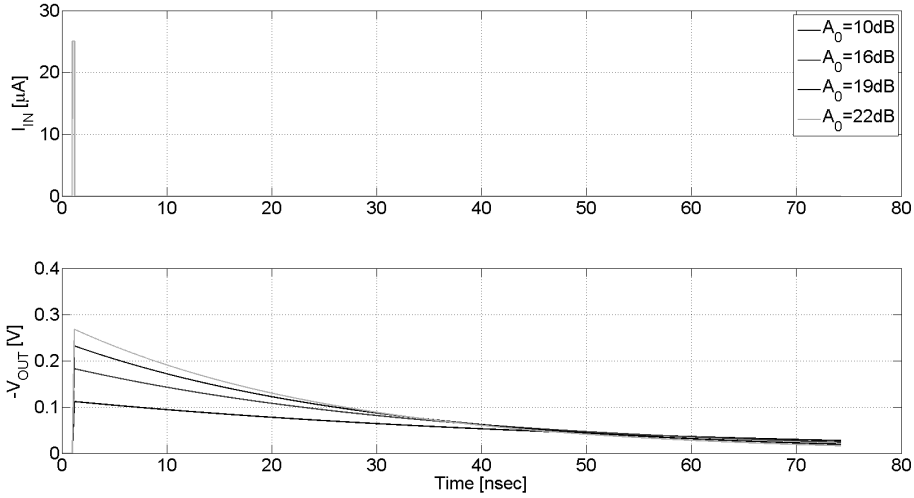

Figure 5.7: Input Current and Inverted Output Voltage vs. Amplifier Gain

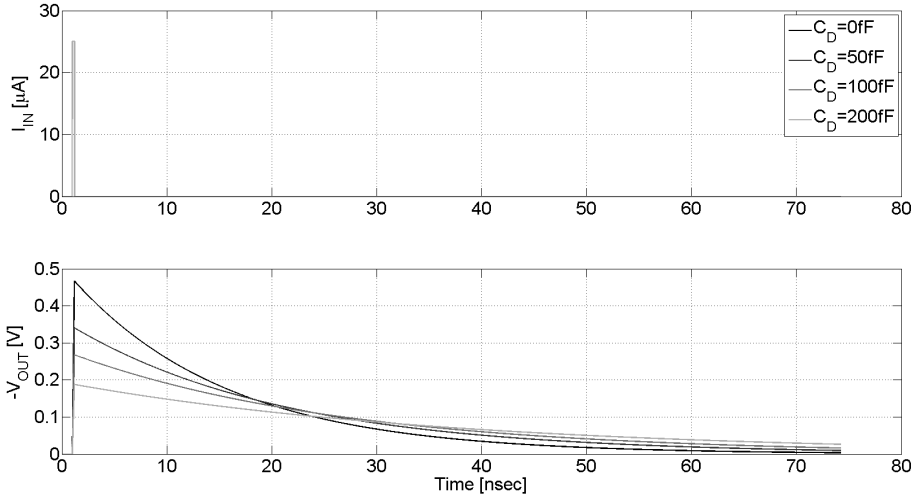

Figure 5.8: Input Current and Inverted Output Voltage vs. Detector Capacitance

$$S = \frac{1}{C_F \left(1 + \frac{C_D}{A_0 C_F}\right)} = S_{id} \frac{1}{\left(1 + \frac{C_D}{A_0 C_F}\right)} \tag{5.11}$$

In first approximation, if $A_0 \gg \frac{C_D}{C_F}$, S is the almost equal to S_{id}. It is reasonable to assume that $\frac{C_D}{C_F}$ is the minimum value of A_0 allowed in order to have the minimum

acceptable value of sensitivity (S_M) as shown in 5.12.

$$S_M = \frac{1}{2\,C_F} = \frac{S_{id}}{2} \tag{5.12}$$

As seen here, CSPreamp performance are strongly dependent on amplifier performance. Another parameter that must be taken in account is the Peaking Time Delay (PTD). It indicates the front-end capability to detect charge arrival time within 25 ns of rise time. In an ideal world, this parameter is equal to zero. Finite gain (A_0) and bandwidth (f_{UGB}) of the amplifier lead to have a no zero PTD. Considering a gain stage with a transfer function $T(s)$ as 5.13, closed loop CSPreamp frequency response is more complex and it is characterized by two complex poles as shown in 5.14

$$T(s) = \frac{A_0}{1 + s\frac{A_0}{2\,\pi\,f_{UGB}}} \tag{5.13}$$

$$\frac{v_{OUT}}{i_D}(s) = -\frac{A_0}{1 + A_0}\,\frac{1}{\alpha_1\,s^2 + \alpha_2\,s + 1} \tag{5.14}$$

with

$$\alpha_1 = \tau_A\,C_F\,R_F\,\left(\frac{1 + \frac{C_D}{C_F}}{1 + A_0}\right) \tag{5.15}$$

$$\alpha_2 = C_F\,R_F\,\left(1 + \frac{\frac{\tau_A}{C_F\,R_F} + \frac{C_D}{C_F}}{1 + A_0}\right) \tag{5.16}$$

$$\tau_A = \frac{A_0}{2\,\pi\,f_{UGB}} \tag{5.17}$$

Choosing $\tau_A = C_F\,R_F$, these equations are simplified and the two complex poles become two real poles arising from τ_1 (5.18) and τ_2 (5.19) time constants.

$$\tau_1 = C_F\,R_F \tag{5.18}$$

$$\tau_2 = C_F\,R_F\,\frac{1 + \frac{C_D}{C_F}}{1 + A_0} \tag{5.19}$$

Notice that this choice allows maintaining a constant impedance at the amplifier input. In this way, the PTD depends only on the poles position. For a data set of parameters ($A_0, f_{UGB}, R_F, ..$), CSPreamp output signal reaches the maximum amplitude in a longer time increasing the detector capacitance (see figure 5.9) or decreasing the feedback one (see figure 5.10).

The CSPreamp is the first block of the chain and plays a main role for the noise and leakage compensation performance, also. The Equivalent Noise Charge (ENC)

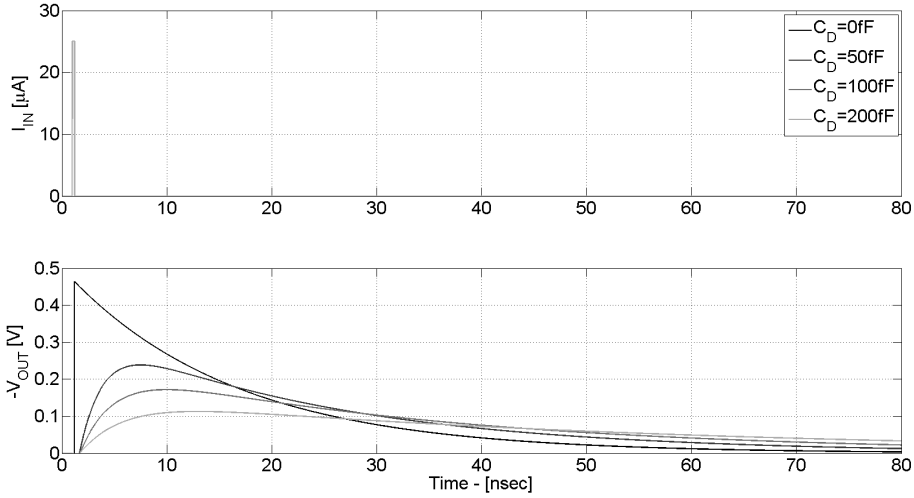

Figure 5.9: Input Current and Inverted Output Voltage vs. Detector Capacitance

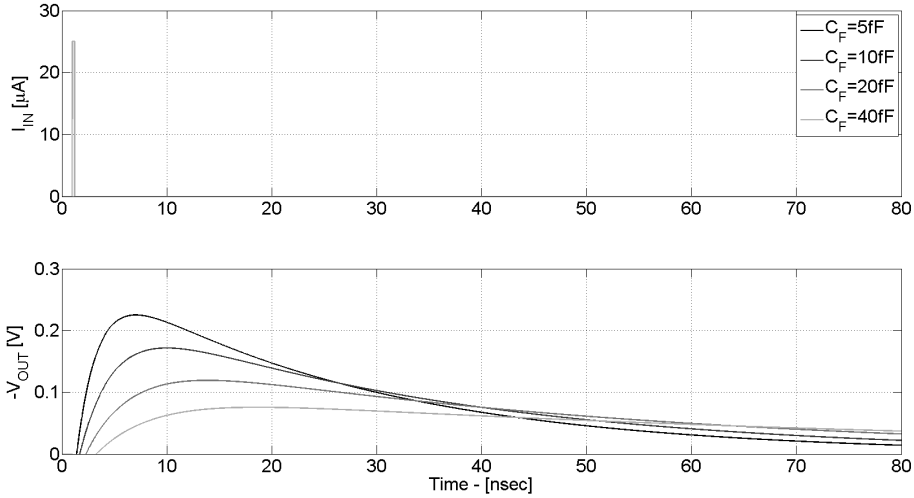

Figure 5.10: Input Current and Inverted Output Voltage vs. Feedback Capacitance

is the channel noise parameter. It is give by the ratio between the root mean square noise output voltage and the sensitivity (output voltage for an input charge).

The input transistor and the total input capacitance are usually the dominant noise contribution.They are taken in account in order to be carefully chosen and sized. The noise depends on the transfer function of the channel and could be reduced in the chain with a filter/shaping after the CSPreamp. In IC-PIX28, the chain includes

only the CSPreamp and its output noise must be such as to ensure minimum input charge detection. The ENC is linked with the CSPreamp noise (i.e. $v_{nA,RMS}$) by the equation 5.20.

$$ENC \cong C_F \left(1 + \frac{C_D}{A_0\, C_F}\right) v_{nA,RMS} \tag{5.20}$$

For an optimal design, the minimum transconductance (g_m) of the amplification stage must be fixed as a starting point, since it implies the maximum value of the allowed thermal noise. At the same time, it determines the minimum power consumption. The choice of C_F value is related to the sensitivity specification and it fixes the minimum A_0.

CSPreamp CMOS implementation

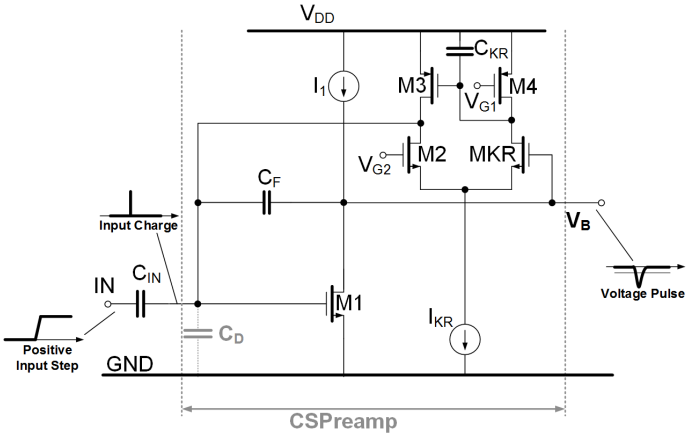

Figure 5.11: Transistor Level Scheme of CSPreamp

Figure 5.11 shows the transistor level scheme of the IC-PIX28 CSPreamp. In pixel read-out system, the sensor is connected to CSPreamp through a coupling capacitance (C_{IN}). The amplifier is not external biasing and it may be influenced by the leakage current that get to several 10 nA after irradiation. Without any compensation technique, leakage current flows through the feedback circuit worsing CSPreamp performance. Possible solutions are based on the capability to sink all or a significant fraction of the leakage current [35] [37] [38].

CSPreamp of the IC-PIX28 channel uses KRummenacher (KR) circuit [37] to implement the resistor feedback as shown in figure 5.11. The choice implies a major number of the transistor and a dedicated current consumption (around 60 nA in IC-PIX28). Transistor M_1 in common source configuration is the gain stage connected to KR circuit. Instead, the $M_2 - M_3 - M_4 - M_{KR}$ transistors are the core of the resistor feedback.

The incoming positive charge forces a negative output pulse voltage ($V_B(t)$ signal). The amplitude of $V_B(t)$ signal is proportional to the input charge and the system

could have a large negative output step. For this reason, output DC-point (V_B) is biased around 550 mV. On the other hand, the input bias voltage is fixed by the V_{GS} (around 300 mV) of M_1, which operates in strong subtreshold to maximize g_m and then minimize thermal noise. The W/L of M_1 is $12\,\mu\mathrm{m}/100\,\mathrm{nm}$, and its bias current and g_m are 1.7 µA and 51 µA/V, respectively.

Krummenacher transimpedance amplifier [37] [39] [40] compares the DC-value of the CSPreamp output to a reference voltage (V_{G2}) with the differential pair M_2 - M_{KR}, performing a feedback resistor given by 5.21. The presence of two gain loops could lead to instability problems. Choosing properly C_{KR} and $g_{m_{M3}}$ in order to satisfy 5.22, CSPreamp stability is guaranteed [39] [40].

$$R_F \simeq \frac{2}{g_{m_{KR}}} \tag{5.21}$$

$$\frac{C_{KR}}{g_{m_{M3}}} \gg 2\,\frac{C_F}{g_{m_{KR}}} \tag{5.22}$$

Size of transistor and the most important parameters are reported in the tables 5.2 and 5.3, respectively.

Transistor	***W***	***L***
M_1	12 µm	100 nm
M_2	1.5 µm	100 nm
M_3	300 nm	50 nm
M_4	6 µm	100 nm
M_{KR}	6 µm	100 nm

Table 5.2: List of Transistor Dimensions

Parameters	***Values***
C_{IN}	50 fF
C_D	100 fF
C_F	10 fF
$g_{m_{M1}}$	51 $\mu A/V$
I_1	1.7 µA
$g_{m_{KR}}$	0.8 $\mu A/V$
I_{KR}	60 nA
C_{KR}	20 pF

Table 5.3: List of Most Important Parameters

5.3.2 Comparator Stage

A comparator stage is connected to CSPreamp output through a decoupling capacitance (C_C) of 1pF, which allows biasing at different DC-voltages both CSPreamp output and comparator input. The scheme of the overall channel is shown in figure 5.12.

The comparator is a discriminator stage able to detect CSPreamp output voltage

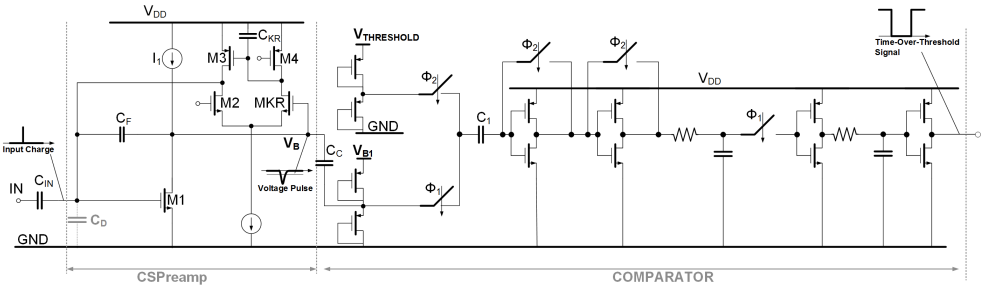

Figure 5.12: Transistor Level Scheme of IC-PIX28 channel

signal above a given threshold. It generates a digital hit signal named Time-over-Threshold (ToT). ToT signal carries out information about input charge arrival time and amount of detected charge. The threshold is set as low as possible in order to maximize the detection efficiency but not too low, on the other hand, to keep the rate of the noise hits at an acceptable level. The response time of the comparator is crucial as the rise time. The required specification is to 25 ns. It is the maximum acceptable value to perform a detection with high resolution.

High speed with low power consumption would be the optimal targets. Bulk CMOS 28nm technology helps to perform high-speed response even in presence of low-voltage operation.

In the literature, there are different circuits used to implement a comparator. Typically, it is based on differential amplifier for its simplicity and current operation [35] [41]. Instead, in IC-PIX28, this circuit has been realized with a chain of inverters with Switched-Capacitor (SC) scheme [42] for threshold setting (see figure 5.12). In addition a distributed noise-shaping function is implemented to improve SNR mainly at low-input signal amplitude.

Switched-Capacitor Logic-Inverter ($SC-LI$) comparators are very interesting because they implement an offset cancellation with AutoZero (AZ) technique. As shown in figure 5.12, the input operating point and the $V_{THRESHOLD}$ of comparison are fixed by a proper reference voltage generator circuit and they are independent of each other. The CSPreamp output and the threshold are connected to comparator input switches. Instead, two very-deep sub-threshold diodes (drawing 80 pA and featuring 1.5 $M\Omega$) bias comparator inputs.

The basic idea is to sample the offset during one clock phase and subtract it from the signal in the other no-overlapped clock phase. The first stage scheme of $SC-LI$ comparator is based on Output Offset Storage (OOS) [43] and it is reported in figure

5.13. C_1 is a sampling capacitance of 250 fF. During the sampling phase, the amplifier

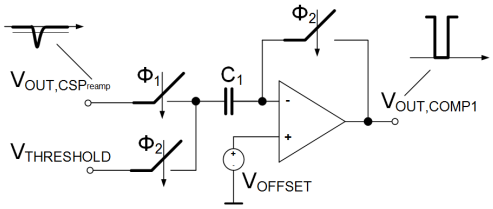

Figure 5.13: First Stage of $SC - LI$ comparator

is in unity-gain closed-loop configuration, the offset (V_{OFF}) is canceled on C_1 and the threshold is set. During the comparison phase, the gain stage is in open-loop configuration and zero-crossing detection is performed (according to 5.23).

$$V_+ - V_- = -(V_{OUT,CSP_{reamp}} - V_{THRESHOLD}) + V_{OFF,RES} \tag{5.23}$$

$V_{OFF,RES}$ is the input-referred residual offset. It depends on switch charge injection and it is equal to V_{OFFSET} reduced by the gain factor. Adding other similar stages, this contribution is further attenuated and becomes negligible. A simple gain stage can be implemented with a CMOS inverter implementing a comparator with a cascade of inverters (see figure 5.14). Timing phase signals are shown in figure 5.15. The phases ϕ_1 and ϕ_2 impose a preliminary idle timing (AZ phase) at the system in order to charge the C_1 capacitor and to set $V_{THRESHOLD}$. During the idle timing, M_5-M_6-M_7-M_8 transistors are diode connected and the current consumption is not controlled. A summary of the transistors and passive components sizes is reported in table 5.4.

The critical reset switch (connected to M_5 and M_6) is implemented with a natural

Transistor	***W***	***L***
M_5	600 nm	300 nm
M_6	300 nm	300 nm
M_7	600 nm	300 nm
M_8	300 nm	300 nm
M_9	100 nm	200 nm
M_{10}	100 nm	200 nm
M_{11}	600 nm	300 nm
M_{12}	300 nm	300 nm

Component	***Value***
C_1	250 fF
C_2	10 fF
C_3	10 fF
R_2	32 $k\Omega$
R_3	32 $k\Omega$

Table 5.4: List of Comparator Components

device, which offers very low V_{TH}. Such device has not be adopted elsewhere due to its larger minimum size, which forces larger area and then larger capacitance. The resulting large charge injection is mitigated by using large C_1. The structure is based on the cascade of four inverters that amplify the difference between the CSPreamp

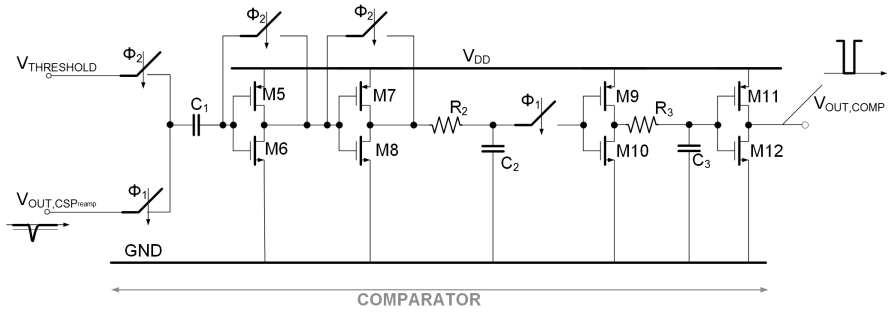

Figure 5.14: Transistor Level Scheme of $SC - LI$ Comparator

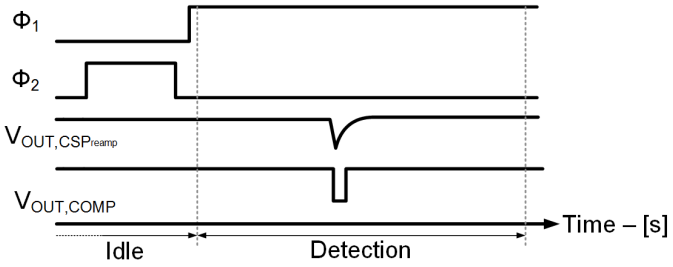

Figure 5.15: Logic-Inverters-Based Switched-Cap Phases

output signal and the threshold. The last inverter has a rail-to-rail output voltage. A key aspect of this design is the first amplification inverter (M_5 and M_6), which must perform sufficient gain and speed at very low V_{DD}/V_{TH} ratio. The last inverters are used to definitively square the signal, so less current is allocated (few hundred of nA). In addition, after the 2nd one and the 3rd one, two RC ($R_2\,C_2$ and $R_3\,C_3$) passive networks are inserted. This, together with the AC-coupling, implements a distributed bipolar shaping with several advantages. It is only passive, then with larger linearity without any power consumption. Moreover, it performs an amplitude-dependent shaping. In fact the analog filters operate only for small input signal when the inverters are linear amplifiers. The large signal inverters are clamped and RC-nets are not fully effective. This means that small signal noise is rejected, while it is not for large amplitude. In this way, the target SNR is guarantee for any signal amplitude.

6
IC-PIX28 Layout

Layout activity follows design and simulation ones. It consists in the real circuit generation. Typically, the foundry provides three different views (schematic, layout and symbol) for each components. The designers use them to implement complex integrated chips first to schematic and then to layout level. In the latter part, a drawing of the each connections and the all components have been done. On the one hand, this activity is only a conversion of the schematic. On the other side, it is not automatic because it could drastically worsen the performance. Each connection may be more or less long and width. In addition, there are a given number of metals (i.e. seven for bulk-CMOS 28 nm), one of them must be selected for each wire to limit parasitic effects introduction. Each metal and each via feature a sheet resistance depending on dimension. For example, 28 nm metal sheet resistance is in the order of $0.45\,\Omega/\mathrm{sq}$ generating parasitic poles in the bandwidth of interest.

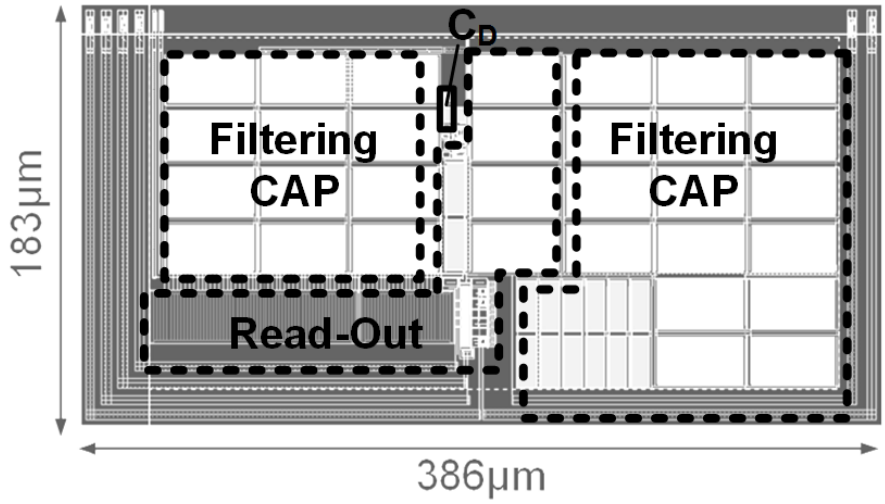

Figure 6.1: Photo of IC-PIX28 Layout

The minimum and the maximum allowed dimensions depend on the technology. At the same time, there are restrictions on metal wire distance, minimum number of via required to connect two different metals, etc. Cadence® tools are able to verify geometry conformity and schematic matching. They are based on DRC (Design Rule Check) and LVS (Layout Versus Schematic) controls, respectively.

Layout photo of IC-PIX28 circuit is shown in figure 6.1. It occupies a total area of

0.07 mm^2. Different metals are distinguished for the colors but figure 6.1 is reported in gray-scale in order to separate the IC-PIX28 sub-blocks. IC-PIX28 area is divided as follows:

- 0.02 mm^2 for actual read-out channel;
- 0.04 mm^2 for filtering capacitance connected to bias current mirrors;
- 0.000 52 mm^2 for on-chip detector capacitance (C_D), which emulates the HEP pixel detector;
- the last for external routing.

Layout of the most important blocks will be briefly shown in 6.1 and 6.2 sections.

6.1 IC-PIX28 CSPreamp

In section 5.3.1, there was transistor level scheme of the CSPreamp. A single mos M_1 (shown in figure 6.2) is used as amplifier in closed loop with R_F and C_F. It has a total width (W_{TOT}) of 12 µm and a length (W) of 100 nm. W_{TOT} results from a multifinger structure. Four fingers with W_{FINGER} of 3 µm are connected to implement a transistor with $W_{TOT} = 4\,W_{FINGER}$. In 28 nm, the maximum finger width is 3 µm and to implement larger mos, multifinger structure is required. Drains, sources and gates of all fingers have been connected together by designer to drawn the transistor M_1 previously simulated. In addition, the transistor is within a ground ring in order to uniformly bias the substrate.

Layout of the other CSPreamp components have been highlighted in figure 6.3. The total area is $336\,\mu\text{m} \times 160\,\mu\text{m}$; in particular M_1 and analog channel part occupy an area of only $6\,\mu\text{m} \times 3\,\mu\text{m}$ and $20\,\mu\text{m} \times 95\,\mu\text{m}$, respectively. The analog channel part is composed by: CSPreamp amplifier (M_1), input capacitance (C_{IN}), detector capacitance (C_D), decoupling capacitance (C_C), feedback capacitance (C_F), KR feedback circuit, voltage reference generators and current mirrors. The remaining area is reserved for filtering capacitances connected to current mirrors.

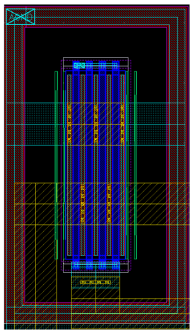

Figure 6.2: Zoom of M_1 Layout

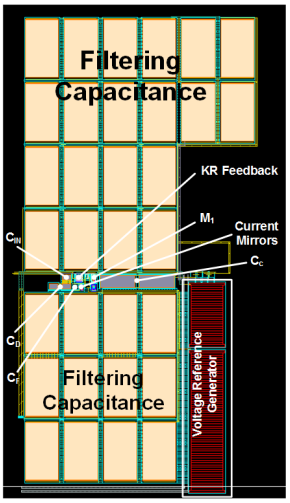

Figure 6.3: Layout Photo of IC-PIX28 Charge Sensitive Preamplifier

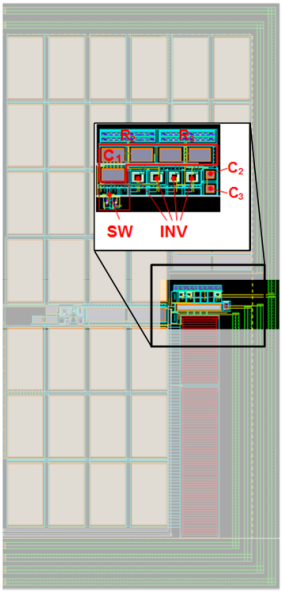

Figure 6.4: Layout Photo of IC-PIX28 Comparator

6.2 IC-PIX28 Comparator

Scheme of IC-PIX28 comparator was analyzed in section 5.3.2. As highlighted in figure 6.4, it is very small (about 830 μm^2) and it is very near the CSPremp avoiding long connection. This is important to prevent delay introduction and channel performance worsening. In addition, in figure 6.4, there are the main comparator components: four inverters (INV), SW switches, C_1 sampling capacitance and RC nets ($R_2\,C_2$ and $R_3\,C_3$).

7
IC-PIX28 Experimental Results

Cadence® Spectre® Simulations have been run in order to characterize IC-PIX28 channel in time and frequency domains. In the years, Cadence® Spectre® tools have been developed and optimized. The results change with the CMOS technology. Obviously, the mature technologies provide an high reliability of the results. The new and sub-nm technologies (as bulk-CMOS 28 nm) are not well known and the models are continuously updating. Nevertheless, pre and post layout simulations allow to investigate on critical points of the circuits with the main target to limit their variations. An integrated circuit changes its behavior with the surrounding. To emulate different environments, the simulator provides settings for critical conditions (i.e. temperature variations from -40 °C to 120 °C, voltage variations in order of 10 % and process variations (Slow-Slow, N-Slow P-Fast, N-Fast P-Slow, Fast-Fast, Typical-Typical)).

At the begin of this part, a brief description of the simulations made for the IC-PIX28 channel is presented. They have been run in nominal conditions and varying the input charge in the range of 0.1 fC - 6 fC.

Following, an overview of the first measurements in presence and in absence of radiation has been presented. For this topology of circuits, the radiation hardness is an important factor that it must be carefully studied. IC-PIX28 is the first prototype in bulk-CMOS 28 nm and the measurements are more important then simulations. The simulations are a starting point, but the measurements are fundamental to optimize Cadence® simulator models and circuit performance. For this reason, only one channel has been integrated. The small number of the components helps to quickly debug malfunctions.

7.1 IC-PIX28 Channel Simulations

Some results of nominal Cadence® simulations are reported in the next pages.

They demonstrate as IC-PIX28 channel works even in presence of the noise. As shown in figure 7.1, read-out front-end system is able to detect input charges of 0.15 fC supposing to have a pixel detector with 100 fF of parasitic capacitance (C_D). At the top of 7.1 there is the input current signal applied to CSPreamp input. This is then converted in voltage signal (see CSPreamp Output signal in the middle figure 7.1), which is compared with a threshold of −3 mV. The output of the comparator stage is the Comp Output signal (in the bottom of the figure 7.1). These signals are shown in presence (black line) and in absence of the noise (colored line) verifying that the maximum variation of the comparator output pulse width is about 33 % respect the nominal value of 71.24 ns.

IC-PIX28 channel detects input charges in the range 0.1 fC - 6 fC. In particular, an

input impulse current (up to 0.2 µA, Input Current signal (see figure 7.2)) is converted before in voltage signal at CSPreamp Output (see figure 7.3) and then in timing signal at comparator output (see figure 7.4). The current pulse is very short (30 ps) as highlighted in the box of figure 7.2. For input charge between 0.1 fC and 6 fC, the maximum peak voltage varies from 4.4 mV to 250 mV and the characteristic has been reported in figure 7.5.

Other important information obtained from 7.3 are the Sensitivity (named S), the Peaking Time Delay (named PTD) and the Equivalent Noise Charge (named ENC) characteristics. They are shown in figure 7.6, 7.7 and 7.8. In particular, results an almost constant sensitivity around 44 mV/fC, a peaking time delay under 25 ns and equivalent noise around 0.03 fC.

To complete IC-PIX28 characterization, in figure 7.9 has been represented the variation of the ToT width. Increasing the input current charge, the comparator output width raises from 55 ns to 297 ns.

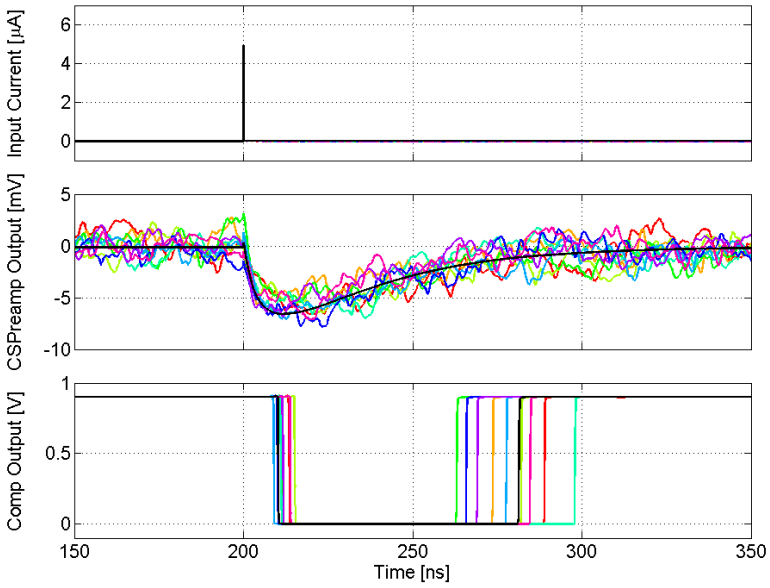

Figure 7.1: Input Current, CSPreamp and Comparator Outputs with and without noise

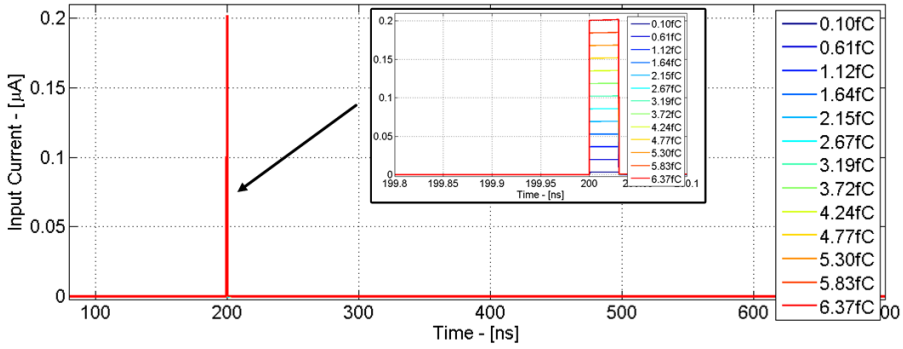

Figure 7.2: CSPreamp Input Current signal vs. Input Charge

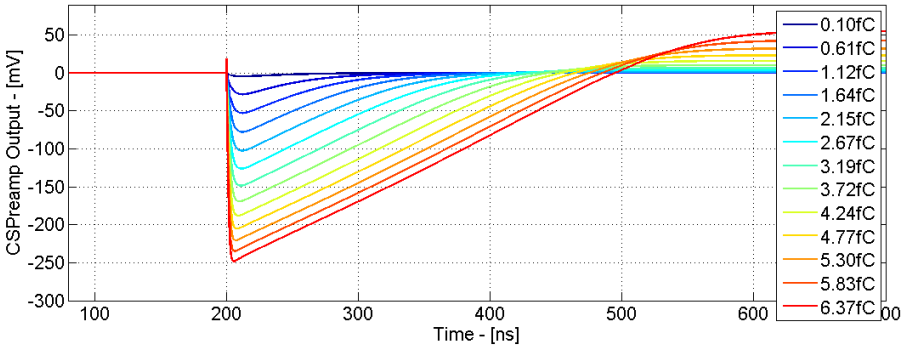

Figure 7.3: CSPreamp Output Voltage signal vs. Input Charge

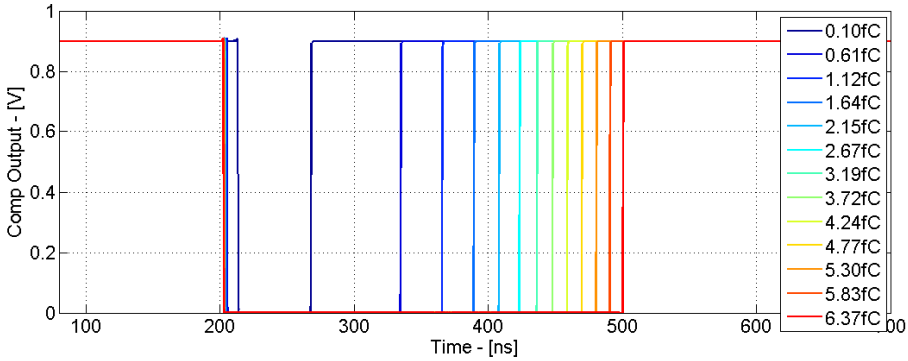

Figure 7.4: Comparator Output vs. Input Charge

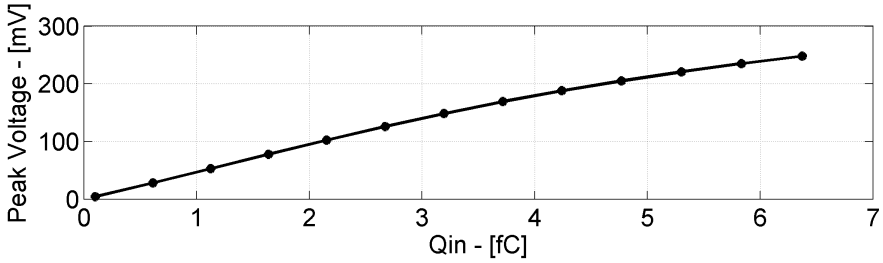

Figure 7.5: CSPreamp Input Current signal vs. Input Charge

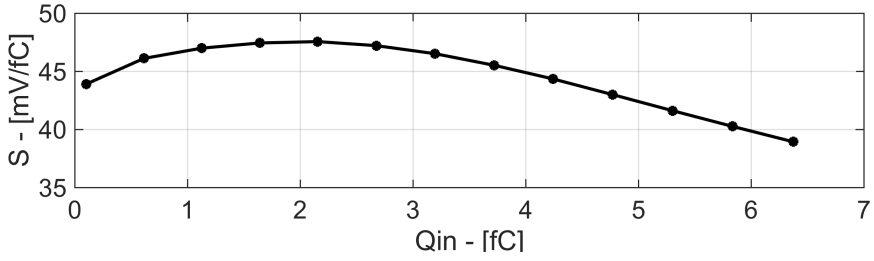

Figure 7.6: CSPreamp Output Voltage signal vs. Input Charge

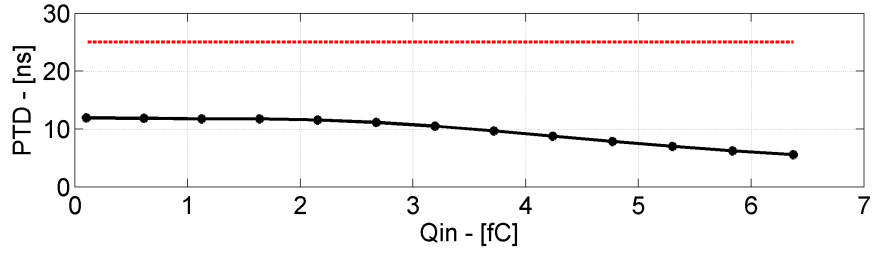

Figure 7.7: Comparator Output vs. Input Charge

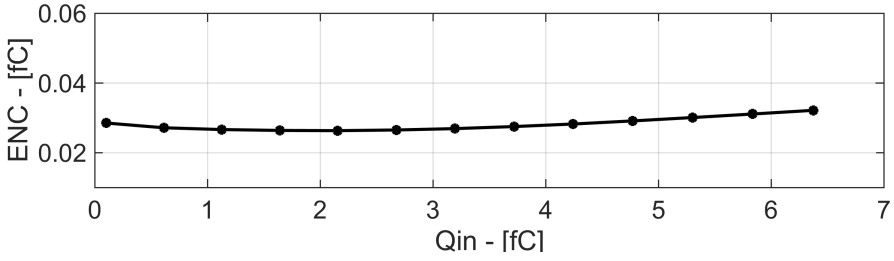

Figure 7.8: Comparator Output vs. Input Charge

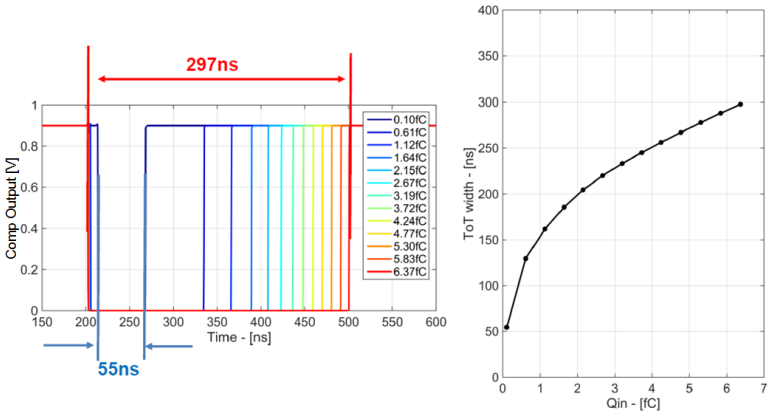

Figure 7.9: Time-over-Threshold (comparator output) signal for different input charges

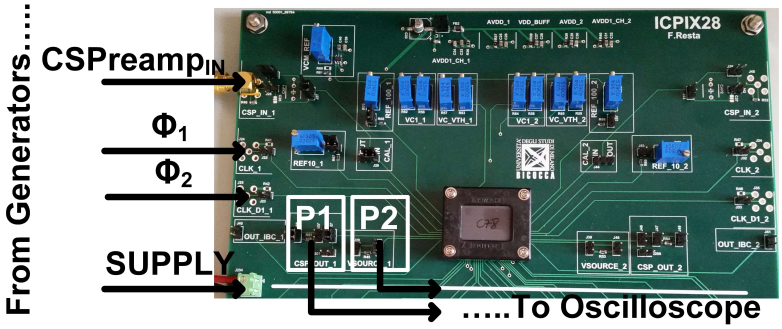

Figure 7.10: Photo of Printed Circuit Board for IC-PIX28 channel

7.2 IC-PIX28 Channel Measurements

IC-PIX28 read-out channel has been integrated in bulk-CMOS 28nm technology. In order to test its functionality, a proper Printed Circuit Board (PCB) has been realized. A photo of the PCB is shown in figure 7.10. At the center, there is the socket with encapsulated chip. It is connected to external components (resistors, connectors, voltage and current references) that have not been integrated. This provides different degrees of freedom to designers, which use them to debug the integrated circuit. Externally, there are two current generators to separately manage the Krummenacher and M_1 currents. Starting from a single supply voltage of 0.9 mV, comparator threshold ($V_{TRHESHOLD}$) and baseline voltage (V_B) are generated on board and provided to the chip. They are changed through proper voltage trimmers.

Although board supply is unique, IC-PIX28 channel has two different supplies; one is reserved for analog part and an another for digital part. The separation

guarantees a good hardness to the disturbs coming from the supplies and/or grounds connections. To preserve this condition, it is important to have potent filtering system near voltage generator and to avoid disturb propagation.

Measurement setup is formed by a DC-generator to supply the board (and then IC-PIX28 chip), an arbitrary pulse generator with two channels (to provide CSPreamp input signal synchronized with the two comparator phases) and two test points (P_1 and P_2) connected to an oscilloscope (for time domain characterization) or to an spectrum analyzer (for frequency domain characterization).

IC-PIX28 has been measured in presence (see 7.2.1 section) and in absence (see 7.2.2 section) of X-ray radiation. All measurements have been done with the same setup, the same board, the same chip and the same instrument configuration.

7.2.1 Standard Measurements

The preliminary measurements have been done at room temperature and before radiation exposure. In nominal condition (i.e. standard supply of 0.9 V and room temperature), the IC-PIX28 chip consumes 4.3 μW. The CSPreamp is AC coupled with the input pad by a $C_{IN} = 50fF$ capacitance, hence input voltage steps with variable amplitudes from 80 mV to 200 mV (see figure 7.11) are used to model variable input charges. The voltage steps have a rising time (corresponding to charge duration) of 20 ns and they are used to generate an input charge range of 4 fC-20 fC. Although, in pixel applications, the charges are impulsive (few hundreds of ps of duration) and their minimum value is typically in the order of fraction of fC, IC-PIX28 measurements setup is unable to generate so small and short charges. For this purpose, experimental results (before and then radiation exposure) will be shown only in the range between 4 fC and 20 fC.

Figure 7.11 shows the oscilloscope time evolution of the input signal, while figure 7.12 and 7.13 show the output voltage of the CSPreamp and the Comparator stages, respectively. The system senses an input variation and consequently, it modifies its outputs. Increasing the detected charge, the maximum amplitude observed at CSPreamp output increments with an almost linear trend. At the same way, the comparator perceives these changes and then it produces an output as that shown in figure 7.13. The comparator output switches to 0-level as soon as it begins a detection and it stays in this level until the CSPreamp output comes back to baseline. In other word, the signal is 0 when the threshold is exceeded. The 0 time is named Time-over-Threshold (ToT) and it is proportional to the amount of detected charge.

All these information are extrapolated from timing output signal of the CSPreamp and the Comparator stages; in particular, they are peak voltage (see figure 7.14), sensitivity (see figure 7.15) and peaking time delay (see figure 7.16) characteristics.

Notice that the CSPreamp features a very linear behavior for charges up 10 fC and tends to compress for higher charges. The resulting sensitivity (defined as the ratio between the voltage peak and the input charge) is then plotted in figure 7.15 and it is almost constant around 30 mV/fC. The CSPreamp output reaches an amplitude of 122.9 mV for minimum input charge (4 fC) and it increases up to 482.9 mV for maximum one (20 fC). A good pixel read-out front-end detects an input charge

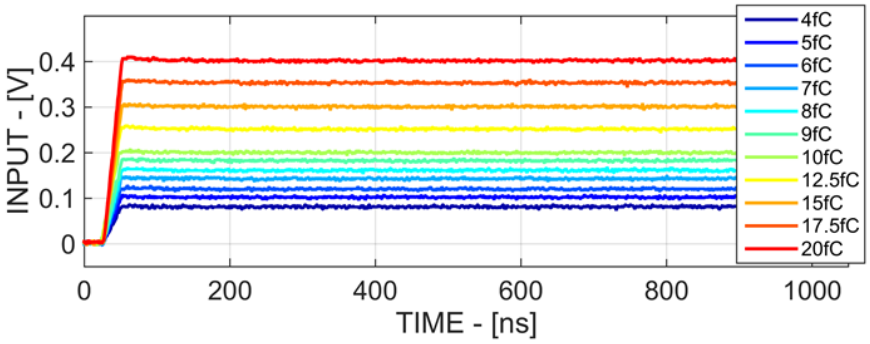

Figure 7.11: Pre-Radiation CSPreamp Input Voltage Steps

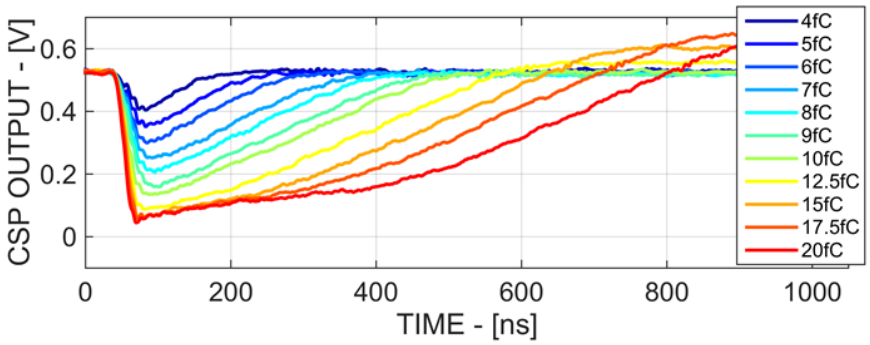

Figure 7.12: Pre-Radiation CSPreamp Output Voltage signals for different input charges

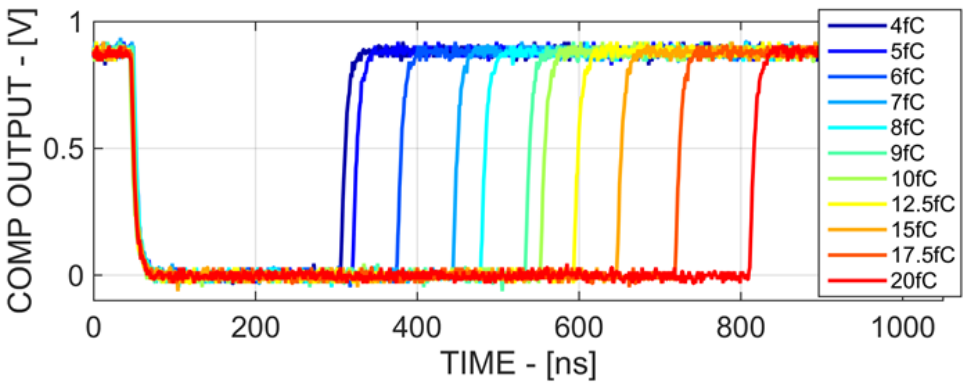

Figure 7.13: Pre-Radiation Comparator Output Voltage signals for different input charges

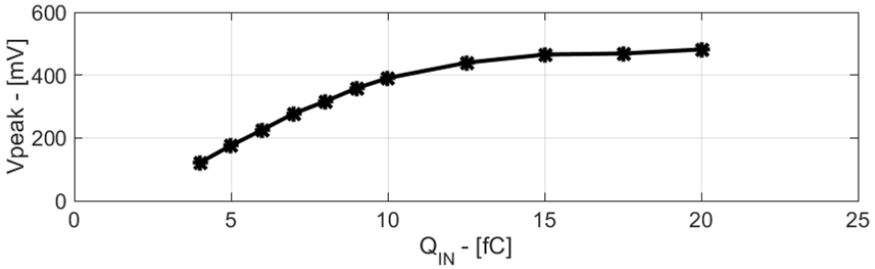

Figure 7.14: Peak Voltage of CSPreamp Output

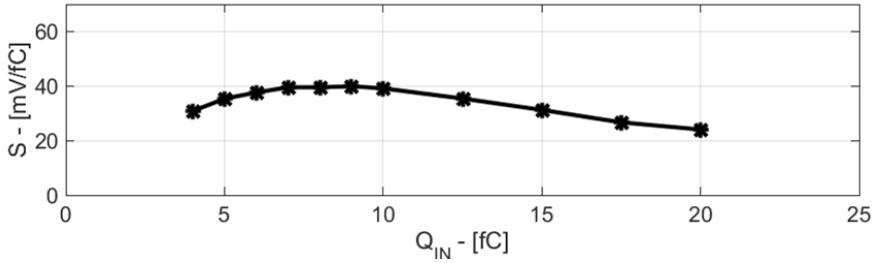

Figure 7.15: Sensitivity at CSPreamp Output

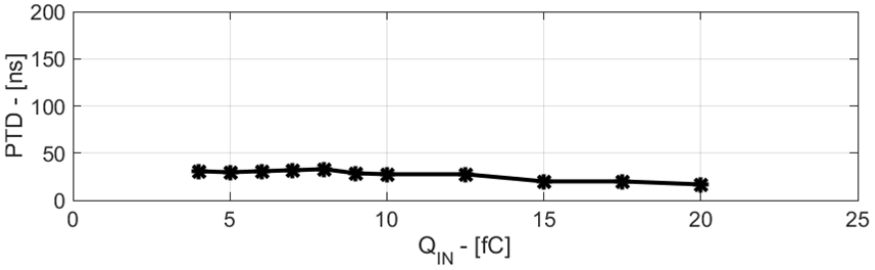

Figure 7.16: Peaking Time Delay at CSPreamp Output

within 25 ns. This specification is partially performed. According to figure 7.16, the CSPreamp reaches the maximum amplitude within 31 ns not satisfying the request. At the same the comparator is able to detect an input within 10 ns. The time response of the comparator is depicted from extrapolated DELAY curve (see figure 7.17) carrying out information about input charge arrival time.

Concluding the time characterization, Time-over-Threshold (ToT) is the last extrapolated parameter. It is an index of the input charge amount. Fixing the comparator threshold to 10 mV, the ToT varies linearly from 258 ns to 763 ns. In this situation, the ToT time range (named $C_{OMP_{RANGE}}$) is around 500 ns that will be quantized with a resolution depending on the used Time-to-Digital Converters ($TDCs$). If we suppose to have an advanced TDC as that described in [44], the time-to-bit conversion has

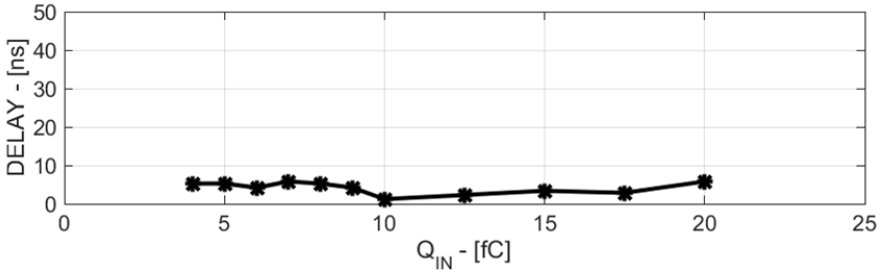

Figure 7.17: Comparator Delay Characterization

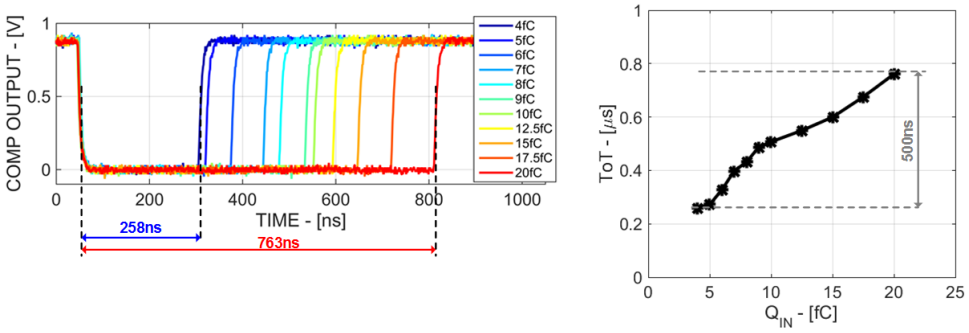

Figure 7.18: Time-over-Threshold Characterization

been achieved in 50 ps of T_{CONV} and the minimum time resolution (N_{BIT}) results equal to 13 bit (according to 7.1).

$$N_{BIT} = \log_2\left(\frac{C_{OMP_{RANGE}}}{T_{CONV}}\right) = \log_2\left(\frac{500\,\text{ns}}{50\,\text{ps}}\right) = 13\,\text{bit} \tag{7.1}$$

At the end of the timing measurements, the oscilloscope and the arbitrary pulse generator have been disconnected in order to use the spectrum analyzer for frequency analysis. Frequency response of the proposed CSPreamp is reported in figure 7.19. It results in line with post-layout simulation. The AC signal is provided by C_{IN} of 50 fF, so the CSPreamp output is AC coupled with the Spectrum Analyzer. Pass-band gain is 5.2 dB, while −3 dB high-pass and low-pass frequencies are 2.8 MHz and 17.8 MHz, respectively. A dedicated output buffer has been used for testing purposes, which however introduces some pass-band gain drop and frequency variation, w.r.t. the effective frequency shaping at the output of the CSPreamp. During measurements, gain loss is taken into account and in figure 7.19 the effect has been removed reporting the measure to before buffer (and so to the real CSPreamp output).

In the last, connecting to ground the input, the measured power spectral density at CSPreamp output ("PreRad" curve) is represented in figure 7.20 for a frequency range of 500 kHz - 30 MHz. The integrated noise is given by the area under "PreRad" curve.

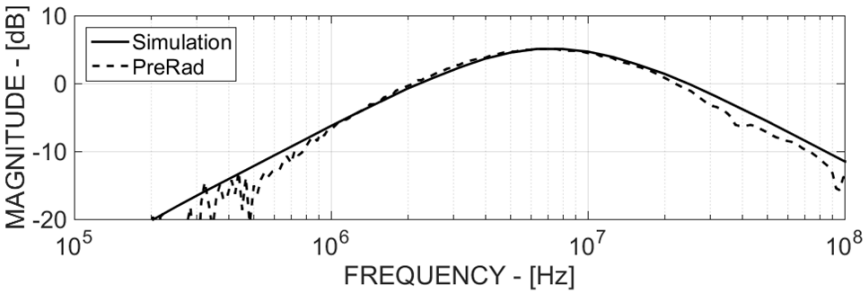

Figure 7.19: Frequency Response at CSPreamp Output

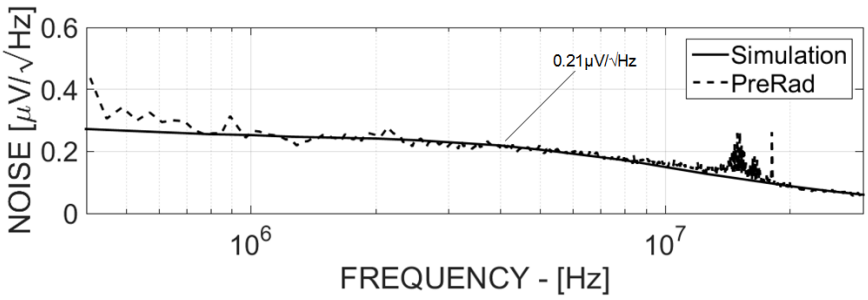

Figure 7.20: Power Spectral Density at CSPreamp Output

Considering the central value of 0.21 $\mu V/\sqrt{Hz}$, the integrated noise in 29.5 MHz of bandwidth is approximatively equal to 806 μV_{RMS}. It is given by 7.2 and it can be used to calculate the Signal Noise Ratio (SNR) for minimum (7.3) and maximum (7.4) input charges and the Equivalent Noise Charge (ENC) (7.5). The minimum measured SNR is 40 dB with 0.0269 fC (equivalent to 165 e^-) of ENC and 100 fF of C_D.

$$0.21\,\frac{\mu V}{\sqrt{Hz}} \times \sqrt{29.5\,\mathrm{MHz}} = 806\,\mu V_{\mathrm{RMS}} \tag{7.2}$$

$$\begin{aligned} SNR_{Q_{IN}=4fC} &= 20\,\log_{10}\frac{V_{PEAK_{Q_{IN}=4fC}}}{\sqrt{2}\,\times\,V_{NOISE}} \\ &= 20\,\log_{10}\frac{122.9\,\mathrm{mV}}{\sqrt{2}\,\times\,806\,\mu V_{\mathrm{RMS}}} = 40\,\mathrm{dB} \end{aligned} \tag{7.3}$$

$$\begin{aligned} SNR_{Q_{IN}=20fC} &= 20\,\log_{10}\frac{V_{PEAK_{Q_{IN}=20fC}}}{\sqrt{2}\,\times\,V_{NOISE}} \\ &= 20\,\log_{10}\frac{482.9\,\mathrm{mV}}{\sqrt{2}\,\times\,806\,\mu V_{\mathrm{RMS}}} = 52.5\,\mathrm{dB} \end{aligned} \tag{7.4}$$

$$ENC = \frac{V_{NOISE}}{S} = \frac{806\,\mu V_{\mathrm{RMS}}}{30\,\mathrm{mV/fC}} = 0.0269\,\mathrm{fC} \tag{7.5}$$

7.2.2 Radiation Measurements

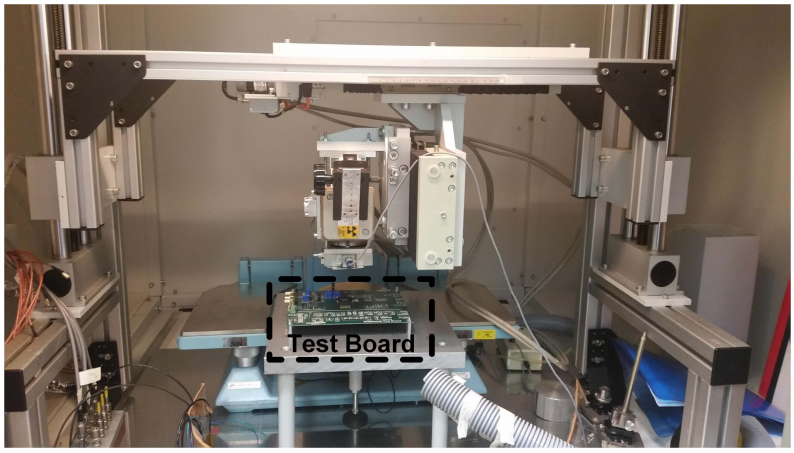

Figure 7.21: Photo of X-ray machine with inside IC-PIX28 board and chip

In order to evaluate radiation effects, the circuit has been supplied and irradiated with X-ray total ionizing dose up to 1 Grad. The system absorbed a dose of 6.64 Mrad/h at room temperature reaching 1 Grad in 1560 hours. A photo of irradiation environment is reported in figure 7.21; it is composed by X-ray machine with inside IC-PIX28 board. Then IC-PIX28 channel has been connected to the arbitrary pulse generator, to the oscilloscope and to spectrum analyzer in order to stimulate the chip with the same signals used in the previous measurements. In particular, input voltage steps with variable amplitudes from 80 mV to 200 mV (see figure 7.22) are used to model variable input charges. In presence of these input signals, the CSPreamp and the Comparator stages modify their performance. In figures 7.23 and 7.24 are reported the timing evolution of the outputs after 1 Grad of TID.

The system continues to sense the presence of a variable input charge but it is slower and it has a smaller gain. For this purpose, a comparison of the CSPreamp and Comparator outputs are shown in figure 7.25. X-ray radiations cause a reduction of the intrinsic transistor gain ($g_m\, r_0$), a decrement of V_{TH} and an increment of the leakage current worsening the CSPreamp performance in terms of sensitivity, peaking time delay, noise [36]. The radiations produce trapped charges in the oxide (N_{ot}) and at Si-oxide interface (N_{it}) inducing DC transistor parameters (i.e. IC-PIX28 performance) variation. In particular, trapped charges in the oxide change the effectively I_{DS} current translatable in a V_{TH} reduction. Instead, the sub-threshold slope increments for N_{it} effects. Up to 65 nm, Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) effects have been limited by enclosed structure implementation. In 28 nm, the DRC rules are more stringent prohibiting transistor gates rotation (i.e. enclosed transistor) and since, the radiations represent a not negligible operating condition in HEP experiments, circuit topologies must be optimized to increase the rad-hardness. The main idea is to study all data and to search rad-hard

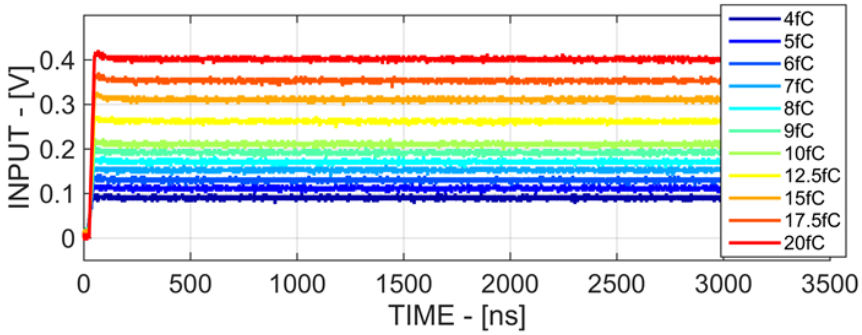

Figure 7.22: 1 Grad CSPreamp Input Voltage Steps

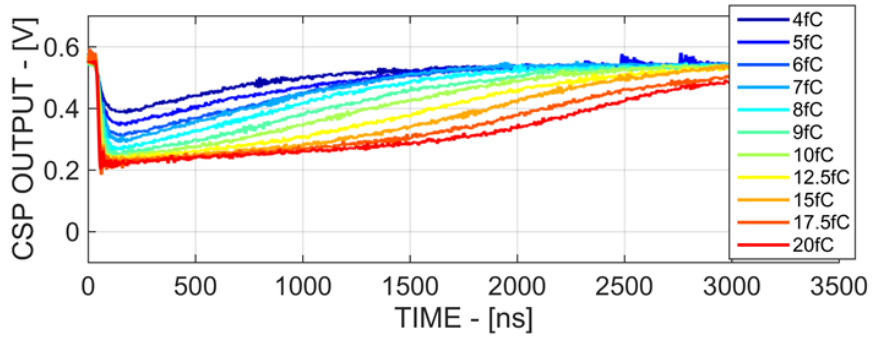

Figure 7.23: 1 Grad CSPreamp Output Voltage signals for different input charges

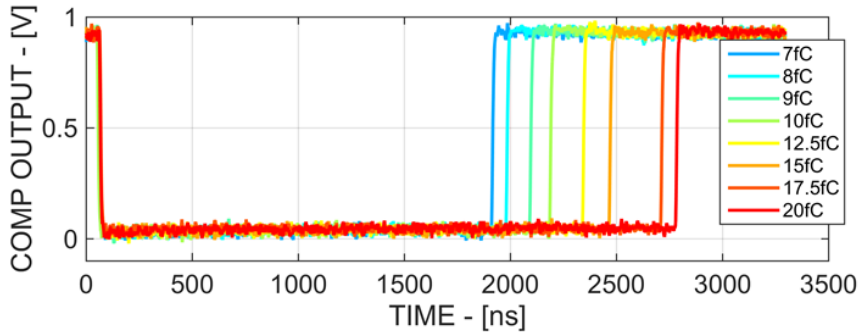

Figure 7.24: 1 Grad Comparator Output Voltage signals for different input charges

circuital solutions.

1 Grad of Total Ionizing Dose has been reached step by step. For simplicity, the timing output signals are reported only for maximum dose. Instead, the main important characteristics are extrapolated in all measured conditions: 480 Mrad, 750 Mrad, 909 Mrad and 1 Grad. At the begin, there are the peak voltage (figure 7.26), the sensitivity (figure 7.27) and the peaking time delay (figure 7.28) curves. Considering the

pre-radiation measure as reference, the peak voltage (as also the sensitivity) suffers a reasonable decrement (around −15 %) for small charges but it reaches −30 % of gain loss for higher inputs. The medium value of sensitivity under 1 Grad-TID is about 24 mV. In figure 7.28, the situation is opposite, the radiations produce a PTD up to three times larger.

Increasing the rising and recovery baseline times, the comparator detects the input charges with longer signals resulting a measured ToT four times longer (see figure 7.29). Fixing the threshold to 10 mV, the minimum charge detectable from the comparator is 7 fC. This is an issue for pixel application that will be taken in account in the IC-PIX28 channel optimization. 1 Grad-ToT range varies from 1.85 µs at 7 fC to 2.7 µs at 20 fC. Furthermore, the comparator time delay drastically increments (see figure 7.30) in the overall input charge range, the amount charge information is maintained and the arrival time one is distorted.

Concluding frequency response and noise measurement are reported in figure 7.31 and 7.32, respectively. Pass-band gain of frequency response is 4 dB, while −3 dB high-pass and low-pass frequencies are 3 MHz and 8.6 MHz, respectively. As expected, the noise increases after 1 Grad of X-ray exposure. The power spectral density is reported in figure 7.32 for a frequency range of 500 kHz - 30 MHz. As done for pre-radiation measurements, the integrated noise is given by the area under "PostRad - 1 Grad" curve. Considering the central value of 0.25 $\mu V/\sqrt{Hz}$, the integrated noise in 29.5 MHz of bandwidth is approximately equal to 960 μV_{RMS}. It is given by 7.6 and it can be used to calculate the Signal Noise Ratio (SNR) for minimum (7.7) and maximum (7.8) input charges and the Equivalent Noise Charge (ENC) (7.9). The minimum measured SNR is 45 dB with 0.04 fC (equivalent to 247 e^-) of ENC and 100 fF of C_D.

$$0.25\,\frac{\mu V}{\sqrt{Hz}} \times \sqrt{29.5\,MHz} = 960\,\mu V_{RMS} \tag{7.6}$$

$$\begin{aligned} SNR_{Q_{IN}=7fC,1Grad} &= 20\,\log_{10}\frac{V_{PEAK_{Q_{IN}=7fC,1Grad}}}{\sqrt{2}\,\times\,V_{NOISE}} \\ &= 20\,\log_{10}\frac{258.3\,mV}{\sqrt{2}\,\times\,960\,\mu V_{RMS}} = 45\,dB \end{aligned} \tag{7.7}$$

$$\begin{aligned} SNR_{Q_{IN}=20fC,1Grad} &= 20\,\log_{10}\frac{V_{PEAK_{Q_{IN}=20fC,1Grad}}}{\sqrt{2}\,\times\,V_{NOISE}} \\ &= 20\,\log_{10}\frac{334.6\,mV}{\sqrt{2}\,\times\,960\,\mu V_{RMS}} = 47.8\,dB \end{aligned} \tag{7.8}$$

$$ENC_{1Grad} = \frac{V_{NOISE_{1Grad}}}{S_{1Grad}} = \frac{960\,\mu V_{RMS}}{24\,mV/fC} = 0.04\,fC \tag{7.9}$$

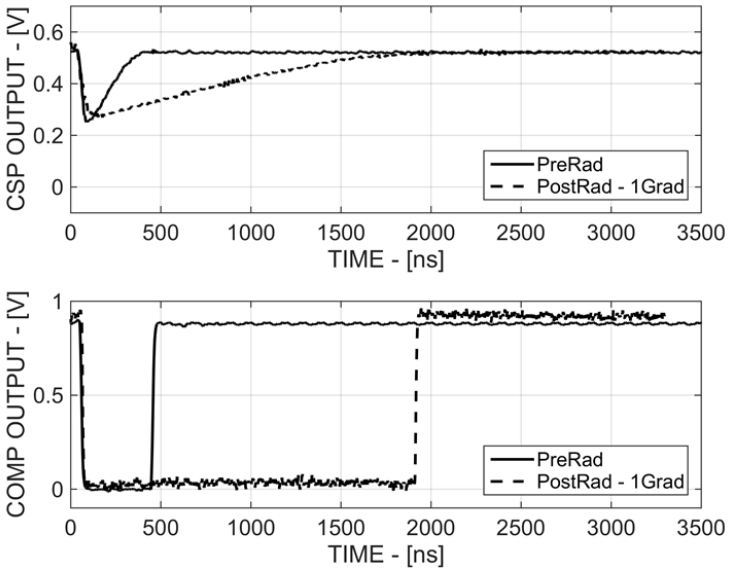

Figure 7.25: Pre and Post Radiation Outputs

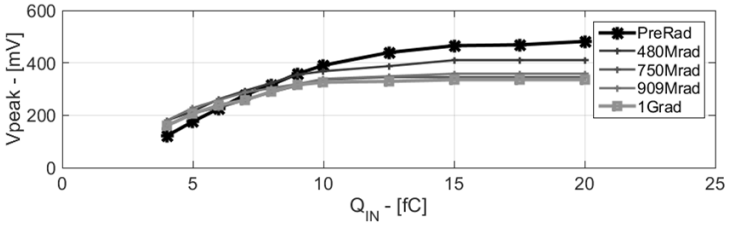

Figure 7.26: Peak Voltage of CSPreamp Output

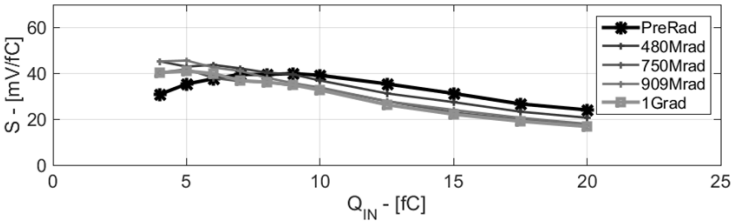

Figure 7.27: Sensitivity at CSPreamp Output

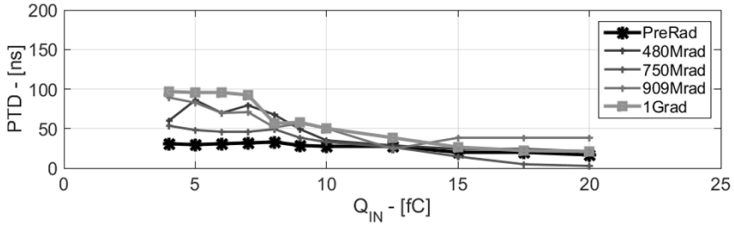

Figure 7.28: Peaking Time Delay at CSPreamp Output

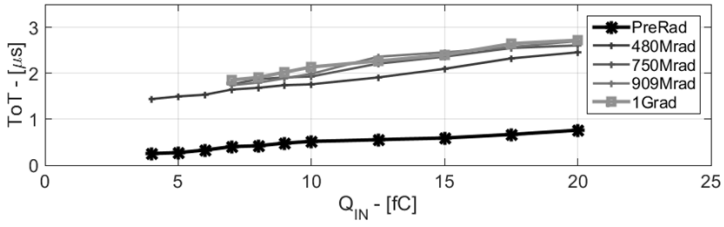

Figure 7.29: Time-over-Threshold Characterization

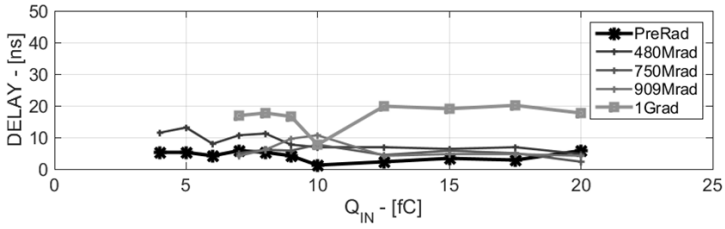

Figure 7.30: Comparator Delay Characterization

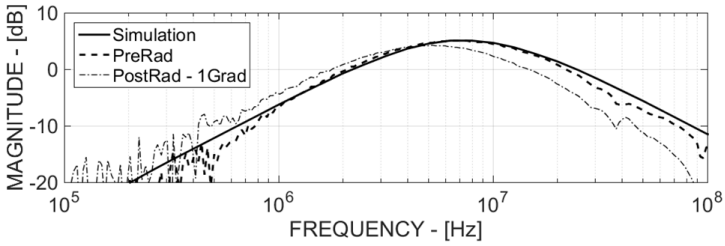

Figure 7.31: Frequency Response at CSPreamp Output

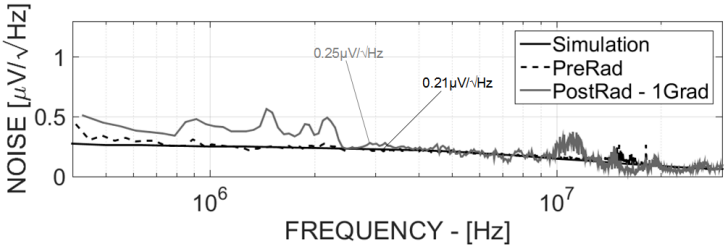

Figure 7.32: Power Spectral Density at CSPreamp Output

Part V

Papers

8
MDT-ASD Related Papers

The papers dedicated to MDT-ASD are listed in the next pages.

The first has been presented at IEEE SENSORS 2015 Conference in Busan, South Korea. It deals with a schematic description of the most important blocks highlighting the fundamental design choices.

The second, "Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC" has been published then an oral presentation to 2015 Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC).

The third, presented at TWEPP Conference in Lisbon, Portugal and published in JINST 2015 Journal, goes in a deeper detail about the overall MDT-ASD chain implementation. The publications follow the poster presentations.

Anyway, all papers here reported are completed and validated with experimental results and data extrapolated from prototype measurements.

8.1 IEEE SENSORS 2015

An 8-Channels 0.13µm-CMOS Front-End for ATLAS MDT-Detectors

M. De Matteis[1], F. Resta[1], R. Richter[2], H. Kroha[2], M. Fras[2], Y. Zhao[2], V. Danielyan[2], S. Abovyan[2], A. Baschirotto[1]
[1]Dept. of Physics "G. Occhialini" - University of Milano-Bicocca, Italy, [2]Max-Planck-Institute for Physics, Munich, Germany
marcello.dematteis@unimib.it

***Abstract*—An 8-channels read-out front-end for LHC ATLAS Muon-Drift-Tubes detectors is presented (8xAFE). The system is composed by the cascade of the analog signal processing Front-End and of the Wilkinson A/D (to perform voltage-to-time conversion for time-over-threshold detection). The sensitivity at the output of the analog signal processing chain is 13.8mV/fC, while the Equivalent-Noise-Charge (ENC) is 0.6fC (~3.38ke), performing <12ns preamplifier rise-time. These performances have been achieved, managing very high detector parasitic capacitance at the front-end input (~60pF). Each channel consumes 11mA from a single 3.3V supply voltage. In 0.13µm CMOS, the total area occupancy is 6.3mm^2.**

***Keywords*—ATLAS,Muon-Drift-Tubes, Detector, CMOS Front-End.**

I. Introduction

In the last years Integrated Circuit (IC) solutions have been widely used in high-energy physics experiments (HEP), with the main aim to replace the common service electronics (based on previous CMOS processes and/or discrete components [1][2]), with more efficient scaled-down ICs, able to improve sensitivity/noise/power performance while reducing area and consequently increasing pixels read-out resolution. This automatically leads to have better imaging and understanding of the particles collision phenomena.

The Analog Front-End (AFE) [1], actually used for the Monitored-Drift-Tube (MDT) chambers of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN, is a 0.5µm CMOS design, biased at 3.3V. It performs a front-end charge-to-voltage conversion (by a proper Charge-Sensitive-Preamplifier) followed by the analog signal conditioning (amplification and shaping) and the A/D conversion. It features a sensitivity (i.e. voltage vs. charge conversion ratio) of 8.9mV/fC[1], 15ns nominal Peaking Time Delay (i.e. PTD, the front-end capability to quickly detect charge arrival time) and relatively low-noise enabling 5fC minimum detected charge at 10dB Signal-to-Noise-Ratio (i.e. SNR).

As it is well known, LHC is under an aggressive improving process (defined Phase 2 [2]) to enable higher energy events, and better measurement set-up, while maintaining the present structure that exhibits good robustness. In this scenario, concerning the above MDT system, also the AFE has to be improved in terms of performance, while maintain the same architecture (including the 60pF detector capacitance) that is well established in the full system. This paper present the 8-channels MDT-AFE (8xAFE) resulting from the design improvement in terms of:

- lower PTD (to achieve the required resolution in the drift time and distance measurement of the MDT drift tubes);
- larger sensitivity and higher SNR at 5fC minimum charge.

The large swing required to adopt a single 3.3V supply voltage that can be sustained only by the 0.35µm High-Voltage (HV) devices. Concerning the other requested signal processing improvements, they have been achieved with a fully improved 8xAFE design. In this way, the 8xAFE performs 11ns-PTD (w.r.t. the original 15ns), 13.8mV/fC-sensitivity (w.r.t. the original 8.9mV/fC) and 15dB-SNR (w.r.t. the original 10dB). These improved results have been obtained without increasing the power consumption that is strongly fixed by the input noise specifications. This means that the technology scaling has been here exploited for rad-hard, performance robustness improvement, and area reduction (about a factor 2x with 6mm^2 die size w.r.t. the original 11.9mm^2). This paper is organized as follows. Section II introduces the ATLAS experiment key points for electronics development. Section III presents the CMOS 8xAFE circuital/design choices and Section IV is focused on the experimental results, in terms of operating point and time performance (rise time, noise, etc).

II. The ATLAS Experiment

The ATLAS experiment at the CERN LHC collider is designed to record collisions from protons on protons (p-p collisions) at center-of-mass energies of up to 14 TeV. In order to determine energy and direction of the secondary particles, emerging from the p-p collisions, a sequence of specialized detectors is used for the detection of charged and neutral particles through a shell-like structure. Fig. 1 shows the MDT read-out simplified scheme. The muons emerge from the primary collision and so they are considered the most penetrating component among the charge particles.

The outer ATLAS shell is reserved for muons detection. Electrons generated by muons in the gas-filled pressurized MDT tubes are drifting to the central wire of the tube. The time-of-arrival of this ionization at the wire is used to measure the distance of the track from the wire. As the muon usually passes through a large number of drift tubes, the position of the muon track can be reconstructed from a combination of measurements in the tubes along the muon trajectory.

Interesting details about the ATLAS MDT readout electronics are given in [4]. The small charge signals coming from the wires are sent to the 'mezzanine' board where the 8xAFE is placed (see Fig. 2 for the single-channel system generic block scheme).

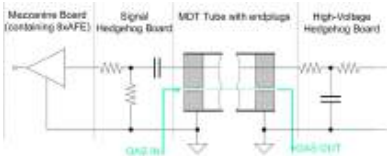

Fig. 1 – Muons Detection Scheme [2].

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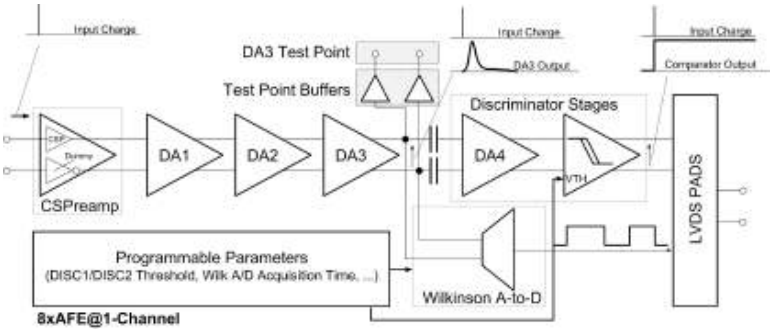

Fig. 2 – 8xAFE Front-End Generic Block Scheme.

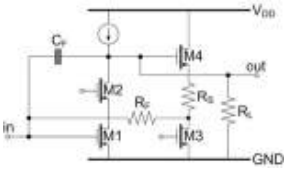

Fig. 3 – 8xAFE Charge-Sensitive-Preamplifier Schematic.

This monolithic 8xAFE senses, shapes and converts the signal coming from the tubes, providing time-domain voltage pulses, whose duty cycle is proportional to the amount of charge at the 8xAFEinput. Then the time signal is sent to an off-chip Time-to-Digital Converter (TDC), which forwards the signal arrival times down the data acquisition chain for recording and track reconstruction and further analysis.

III. MDT-ASD Circuital Implementation

The architecture of a single-channel 8xAFE is shown in Fig. 3[3]. The overall system consists of 8 identical channels.

The device has been realized in IBM 0.13µm CMOS technology, selected since it has been characterized for radiation hardness. Each channel input signal is an (almost ideal) current pulse signal coming from the detector. It is converted into a voltage signal by the Charge-Sensitive-Preamplifier (*CSPreamp*). The *CSPreamp* output voltage is then properly shaped by the cascade of three Differential-Amplification stages (DA_1, DA_2, DA_3) to increase the signal power, and, also, to perform out-of-band noise rejection and anti-aliasing filtering for the following ADC.

The DA_4 output signal feeds a Comparator (Discriminator Stage in Fig. 2) that by switching-on allows detecting the charge arrival time. Hence the DA_3 output signal is the analog input signal for the Wilkinson ADC. The ADC provides a time representation of the input signal, performing a voltage-to-time conversion. A proper Programmable Parameters stage has been also embedded, to set the Discriminator threshold (the minimum charge to be detected) and the phases signal needed for Wilkinson ADC operation. Moreover, LVDS drivers have also been designed to interface the 8xAFEchip with the external components of the "mezzanine" board and the following TDC chip. Test point for DA_3 output voltage consists on an analog buffer able to drive the probe for testing purposes (with –2dB drop and a few ns as additional delay).

A. Charge-Sensitive Preamplifier

The overall system behavior is strongly dependent on the performance of the *CSPreamp* that must manage a very large detector parasitic capacitance (C_D≈60pF).

The *CSPreamp* is composed by two identical symmetrical paths. A dummy preamp has been used for differential signal processing, and as a consequence the input charge is read from one single path (CSP in Fig. 2). The transistor-level scheme of the *CSPreamp* is shown in Fig. 3.

While the *CSPreamp* structure is maintained as in the previous design for overall system operation, the circuit parameters have been completely re-designed to improve the performance in terms of the input impedance (<120Ω), noise, and speed of response.

Regarding the input impedance, the *CSPreamp* is based on a cascode common source amplifier, which guarantees large loop-gain for closed-loop operation, and as consequence a better virtual ground at the input node (required by the large C_D). The input impedance is maintained almost constant for all in-band frequencies, since at low frequency, it is fixed by R_L(=16kΩ) and R_F(=16kΩ), while, at higher frequency, it is regulated by the Feedback Capacitance (C_F=680fF) and by the detector capacitance (C_D=60pF).

The output signal is read at the M_2 drain. The M_3-R_S-M_4 source-follower is used to increase and optimize the output node common-mode voltage, for the following DA_1 stage, which has NMOS input transistors (for noise minimization).

Moreover *CSPreamp* noise and speed of response are optimized by suitable input device transconductance (g_{m1}). In this direction, transistor M_1 operates in moderate inversion (V_{ov}≈100mV) with a nominal current of 1.6mA in order to have large g_{m1}=25mA/V, much larger than in previous design. This improves both noise and speed for the same power, thanks to a better redistribution of the power among the different stages. Larger power is allocated to the *CSPreamp* input stage, saving power elsewhere (mainly in the DA_X chain, and in the bias circuit), where it was not necessary. Such large g_{m1} value improves the speed-of-response as follows. The CSPreamp transfer function is, in first approximation, given by:

$$(1)\quad T(s) \cong -R_F \cdot \frac{1-s\cdot\frac{C_F}{g_{m1}}}{\left(1+s\cdot C_F\cdot R_F\left(1+\frac{C_D}{C_F}\cdot\frac{1}{1+g_{m1}\cdot R_L}\right)\right)}$$

Since g_{m1}=25mA/V and $C_F \ll C_D$, the zero is at much higher frequency and can be neglected. Assuming infinite g_{m1}, the dominant pole is given by C_F·R_F, and the output pulse voltage peak value should be approximately given by Q_{IN}/C_F≈7mV$_{0\text{-}PEAK}$. In this design g_{m1} has been fixed at 25mA/V, as trade-off between noise and power, resulting in a *CSPreamp* sensitivity of 1.4mV/fC. These considerations are validated by Fig. 4, where the simulated *CSPreamp* time

response is shown (NO-NOISE curve) and compared with the single-pole ideal system (No-Noise, No-C_D curve).

The main effects of the C_D capacitance are: lower sensitivity ($4mV_{0\text{-}PEAK}$ instead of $6mV_{0\text{-}PEAK}$for minimum Q_{IN}=5fC) and slightly slower time response (7ns instead of 4ns), w.r.t. the ideal case. The large design g_{m1} not only avoids significant sensitivity degradation due to the large parasitic C_D, but also mitigates the second pole effect, pushing it up to very much higher frequency, hence improving the time performance of the *CSPreamp*, as shown in eq. (2):

$$(2)\quad T(s) \cong -R_F \cdot \frac{1-s\cdot\frac{C_F}{g_{m1}}}{\left(1+s\cdot C_F\cdot R_F\left(1+\frac{C_D}{C_F}\frac{1}{1+g_{m1}\cdot R_L}\right)\right)\cdot\left(1+s\cdot\frac{C_D}{g_{m1}}\right)}$$

Such large g_{m1} enforces virtual ground and, then, lowers *CSPreamp* equivalent input impedance down to ≈60Ω, (nominal, in order to be <120Ω over PVT) acceptable for PTD, and noise. Two transient noise iterations have been run, to highlight the thermal noise contribution, resulting in $0.55mV_{RMS}$-in-band output noise power. The SNR at the *CSPreamp* output is 19dB in case of minimum input charge of 5fC, and it rises up to 45dB at 100fC.

B. DA_1-DA_2-DA_3

The *CSPreamp* output signal is amplified&filtered by the DA_1-DA_2-DA_3 stages, which shape the signal to convert the pulse into a bipolar shaping and to define the fall-down time. In this DA_1-DA_2-DA_3 chain, the scaled 0.35µm devices have been exploited in the reduction of the parasitic capacitance, and, then in increasing the speed while reducing power consumption. The frequency response at the output of each stage is plotted in Fig. 5. The full chain exhibits a pass-band characteristic with a 5MHz center frequency. The high-pass part, mainly imposed by DA_3, shows a 30kHz corner frequency and a slope of +6dB/octave (1st-order high-pass filter). The low-pass part is the superposition of all 4 amplifier low-pass characteristics that have a bandwidth between a few tens and hundreds MHz.

C. Wilkinson-ADC

The DA_3 output signal feeds to the Discriminator and the Wilkinson-ADC (W-ADC) stage, to provide information regarding the arrival time and the total amount of input charge at the *CSPreamp* input node. The Discriminator is a comparator, which detects the presence of a specific minimum charge at the *CSPreamp* input nodes and provides the charge arrival time, and the Start-of-Conversion signal for the W-ADC. The W-ADC, instead, performs a Voltage-to-Time conversion, as shown in Fig. 6. The sample capacitor (C_H) is charged for a given time range T_{GW} (programmable by the external between 8ns and 32ns). Such capacitance is then discharged down to the zero-crossing instant. Charge and discharge phases depend on Φ_1 and Φ_2, such as on ON-OFF switches phases. Φ_1 and $\Phi_2$signals are complementary MOS switches. The equivalent time-width needed to discharge the C_H will be proportional to the analog input voltage and, as a consequence, to the equivalent amount of charge at the *CSPreamp* input nodes. As in Fig. 6 with the same integration time T_{GW}, the higher is the analog voltage peak value (i.e. the Q_{IN} input charge), the higher is the time needed to cross down the horizontal axis. The transconductor stages design had to face the lower output impedance of the 0.35µm devices w.r.t. the 0.5µm devices. Specific arrangements have then been adopted to guarantee the same impedance level. On the other hand, the power here is unchanged since it fixed by C_H value, maintained equal to 3pF to make negligible any parasitic effects.

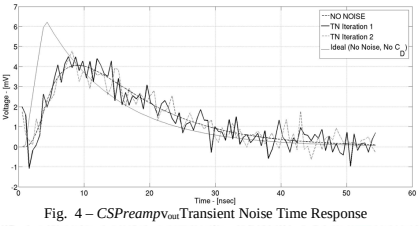

Fig. 4 – *CSPreamp*v_{out}Transient Noise Time Response

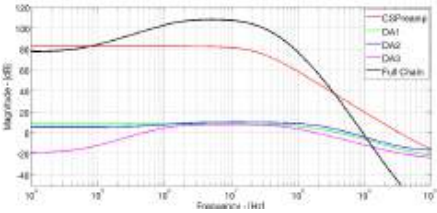

Fig. 5 – *CSPreamp*-DA_1-DA_2-DA_3 chainAC Frequency Responses

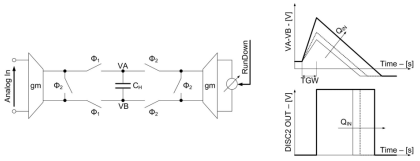

Fig. 6 – Wilkinson-ADC Operating Principle.

IV. Experimental Results

The presented 8xAFEchip has been integrated in 0.13µm CMOS technology (Fig. 7 shows the chip photo). A complete electrical characterization has been carried-out mounting the 8xAFEon the mezzanine board, working in the same boundary conditions w.r.t. the ATLAS experiment environments. The 8 channels are placed&routed in order to guarantee symmetrical paths w.r.t. the bias and setting circuits (located in the center region of the layout top-view, and used to program/regulate the discriminators thresholds, gain, etc). Each channel occupies $0.4mm^2$. The total area (including additional pads, JTAG, etc..) is about $6.38mm^2$. All the presented time measurements have been performed using different equivalent input charge (Q_{IN}) in the full input range 5fC÷100fC.

A. Analog Section Electrical Characterization.

The analog section of the 8xAFE composed by the cascade of the *CSPreamp* and the DA_1-DA_2-DA_3 stages is here presented. Fig. 8 shows the output signal vs. time at DA_3 output buffers test pins (see Fig. 2), hence some voltage peak drop (i.e. about 3dB and 2ns additional time delay) and an additional PTD is expected w.r.t. the effective on-chip DA_3 signal (really managed by the ADC). The DA_3 output voltage ranges from $90mV_{0\text{-}PEAK}$ up to $1.2V_{0\text{-}PEAK.}$ Fig. 9 and Fig. 10 shows the $V_{OUT,DA3}/Q_{IN}$ trans-characteristic and the sensitivity that is 14-2mV/fC for minimum Q_{IN}. Moreover, the sensitivity is quite constant over the input charge range, so no voltage swing saturation is presented over the 5fC÷100fC range, resulting in a very linear behavior. Finally Fig. 11 shows PTD vs Q_{in}. The PTD is lower than 9ns for minimum Q_{IN} (5fC),and raises up to 12nsat 100fC. For sake of completeness, the Fig. 9-Fig. 12 are shown with and without the amplitude/time effects of the test points output buffers.

B. Analog Section Electrical Characterization.

The Wilkinson ADC has bee also tested for 4 different equivalent input charge values (in the 20fC÷100fC range).

The output pulse width is proportional to the equivalent amount of charge at the 8xAFE input, resulting in the very linear characteristic in Fig. 13.

TABLE I. STATE-OF-THE-ART COMPARISON

Parameter	**This Work**	**[3]**
CMOS Tech.	**0.13µm**	0.5 µm
Total Die Area	**6.38mm²**	11.9mm²
Supply Voltage	**3.3V**	3.3V
Channel Current Consumption	**10mA**	11mA
Detector Parasitic Cap.	**60pF**	60pF
Input Charge	**5fC÷100fC**	5fC÷100fC
Front-End Delay at 100fC@Q_{IN}	**12ns**	~ 15ns
Front-End Sensitivity	**14mV/fC**	8.9mV/fC
ENC	**0.6fC**	1fC
SNR	**15dB**	10.9dB

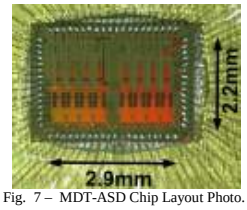

Fig. 7 – MDT-ASD Chip Layout Photo.

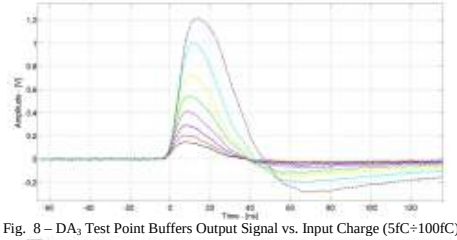

Fig. 8 – DA_3 Test Point Buffers Output Signal vs. Input Charge (5fC÷100fC)

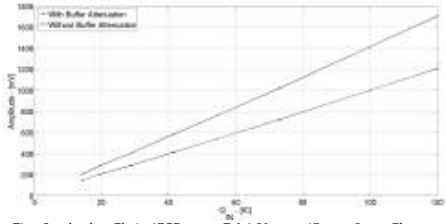

Fig. 9 – Analog Chain (CSPreamp-DA_3) $V_{OUT,DA3}/Q_{IN}$ vs. Input Charge

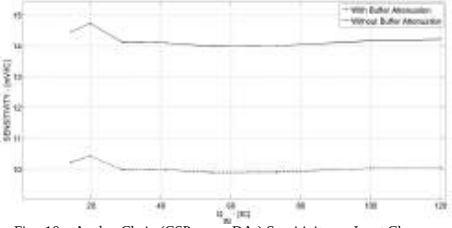

Fig. 10 – Analog Chain (CSPreamp-DA_3) Sensitivity vs. Input Charge

V. CONCLUSIONS

An 8-channels read-out front-end for MDT ATLAS detectors at CERN LHC has been presented. The design has been carried-out in IBM 0.13µm CMOS technology, targeting area and noise reduction at the same power budget of the state-of-the-art for ATLAS MDT detectors. Table I summarizes the most important performance of the presented 8xAFE for the MDT-ATLAS-read-out, compared with the previous implementation. The device exhibits a factor 2 area reduction (lower than the CMOS scaling-down factor due to 0.35µm High-Voltage devices). For the same detector capacitance, the single channel power consumption is approximately the same than in [3], whereas input charge signal quality improves (higher SNR, given by better *CSPreamp* ENC noise performance). The peaking time delay is 12ns, i.e. 3ns lower than the state-of-the-art, resulting in faster response and reduced probability to muons data loss. The outstanding achieved results will be used in ATLAS experiments in Phase 2.

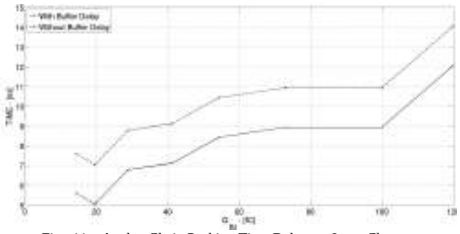

Fig. 11 – Analog Chain Peaking Time Delay vs. Input Charge

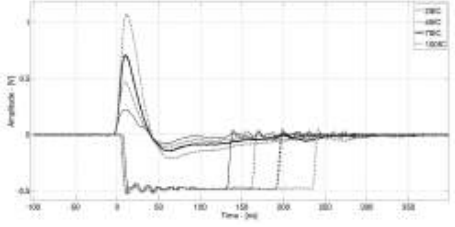

Fig. 12 – Wilkinson ADC Output Pulse/DA3 output Signal vs. Input Charge

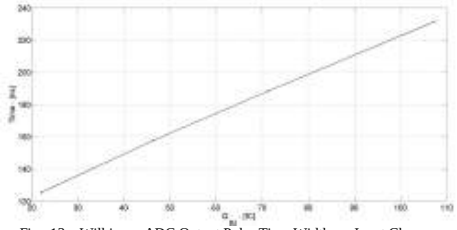

Fig. 13 – Wilkinson ADC Output Pulse Time Width vs. Input Charge

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Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT Chambers at the HL-LHC

H. Kroha*[1], S. Abovyan[1], A. Baschirotto[2], V. Danielyan[1], M. Fras[1], F. Müller[1], S. Nowak[1], F. Resta[2], M. De Matteis[2], R. Richter[1], K. Schmidt-Sommerfeld[1], Y. Zhao[1]
[1]*Max-Planck-Institut für Physik, Munich*
[2]*Univ. of Milano-Bicocca, Physics Department, Milano, Italy*

***Abstract*—The Phase-II Upgrade of the ATLAS Muon Detector requires new electronics for the readout of the MDT drift tubes. The first processing stage, the Amplifier-Shaper-Discriminator (ASD), determines the performance of the readout for crucial parameters like time resolution, gain uniformity, efficiency and noise rejection. An 8-channel ASD chip, using the IBM 130 nm CMOS 8RF-DM technology, has been designed, produced and tested. The area of the chip is 2.2 x 2.9 square mm size. We present results of detailed measurements as well as a comparision with simulation results of the chip behaviour at three different levels of detail.**

The HL-LHC at CERN will operate at peak luminosities of a factor 5–7.5 beyond the nominal value of 10^{34} cm^{-2}s^{-1}. The high luminosity is a challenge for the readout system of the Monitored Drift Tube chambers (MDT) in the ATLAS Muon Spectrometer in two respects. Higher hit rates, mainly due to increased cavern background, drive data transmission to the rear end electronics to the limit of available bandwidth. In addition, the new operating parameters of the L1 trigger - latency up to 60 μs and trigger rates up to 400 kHz - call for a replacement of the entire readout chain of the MDT chambers.

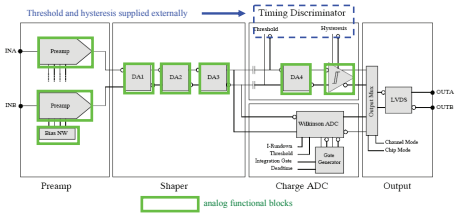

Fig. 1: The functional block diagram of the ASD.

In this process of renewing the MDT readout, particular attention must be given to the first stage of the readout chain, the Amplifier with Shaping network and Discriminator (ASD). This stage determines critical quantities, like signal risetime, signal-to-noise performance and threshold uniformity among the 8 channels of the chip, which are decisive for system parameters like spatial resolution of the track coordinates (represented by the drift time in the MDT tubes) and tracking efficiency.

To cope with these requirements, a chip was developed in the IBM 130 nm CMOS 8RF-DM technology. The design contains a preamplifier, three shaping stages and a discriminator (see Fig. 1). The chip can be operated in two output modes, the time-over-threshold (ToT) and the ADC mode. In the ADC mode, implemented as a Wilkinson ADC, the time elapsed between leading and trailing edge is proportional to the charge inside a predefined integration window of about 15 ns, which is an approximate measure of the amplitude of the initial signal, triggering the discriminator. The ADC information allows to apply a slewing correction to the time of threshold crossing (measurement of the drift time) and is useful for monitoring stability of the gas gain and other operational parameters over extended periods.

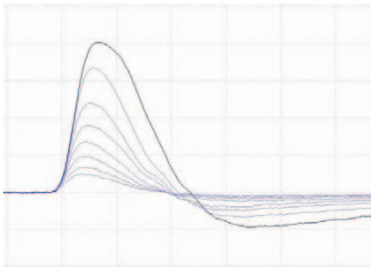

Fig. 2: Delta pulse response of the ASD with a peaktime of 12.5 ns. Horiz/vert.scale: 20 ns/100 mV.

The most important performance parameters of the chip in our application are signal rise time, signal-to-noise and the uniformity of signal gain among the 8 channels. The measured pulse shape behind the third shaping stage (D3 in Fig. 1) is shown in Fig. 2. The Fig. 3 shows the same signal at two amplitudes together with the output response in the ADC mode. The linearity of the analog part w.r.t. the incoming signal is shown in Fig. 4.

Fig. 5 shows the small gain variations among the channels of the ASD. The variation of 8 mV at a pulseheight of ... mV (as used in this example), corresponds to a 3% gain variation

*Corresponding author: kroha@mpp.mpg.de

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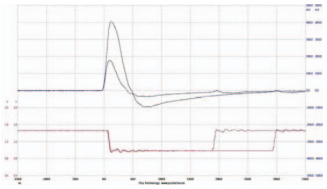

Fig. 3: Shaped signal at two different amplitudes and the corresponding output in ADC mode. The length of the output is a measure of the charge of the pulse amplitude. Horiz./vert. scale: 50 ns/ blue: 100 mV,red: 400 mV.

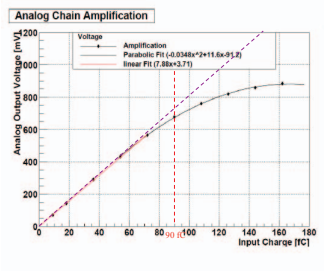

Fig. 4: Linearity of the delta pulse response of the ASD.

among the channels.

Fig. 6 shows the simulated pulse shape (top) and the resulting output in ADC mode (bottom). The middle track shows the voltage on the internal storage capacitor, where the charge in the integration window is stored at the beginning of the cycle.

Fig. 7 shows the layout of the 8-channel chip The size of this 8-channel chip is 2.2 x 2,9 mm^2.

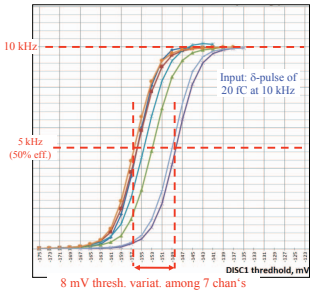

Fig. 5: Threshold scan shows small gain variation among the channels of the ASD.

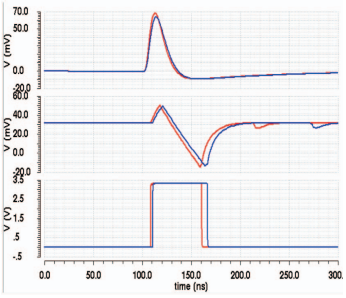

Fig. 6: Sequence of pulses in the ADC, in schematic (red) and post layout simulation (blue).

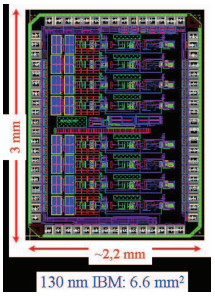

Fig. 7: Layout of the chip.

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Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC

M. De Matteis,[a,1] **F. Resta,**[a] **R. Richter,**[b] **H. Kroha,**[b] **M. Fras,**[b] **Y. Zhao,**[b] **V. Danielyan,**[b] **S. Abovyan**[b] **and A. Baschirotto**[a]

[a] *Physics Department,*
Piazza della Scienza 3, Milano, Italy
[b] *Max-Planck-Institute for Physics,*
Munich, Germany

E-mail: marcello.dematteis@unimib.it

Abstract: The Phase-II Upgrade of the ATLAS Muon Detector requires new electronics for the readout of the MDT drift tubes. The first processing stage, the Amplifier-Shaper-Discriminator (ASD), determines the performance of the readout for crucial parameters like time resolution, gain uniformity, efficiency and noise rejection. An 8-channel ASD chip, using the IBM 130 nm CMOS 8RF-DM technology, has been designed, produced and tested. The area of the chip is $2.2 \times 2.9\ mm^2$ size. We present results of detailed measurements as well as a comparison with simulation results of the chip behavior at three different levels of detail.

Keywords: Front-end electronics for detector readout; Analogue electronic circuits; Radiation-hard electronics

[1]Corresponding author.

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1 Introduction

In the last years, integrated circuits (ICs) solutions have been widely used in high-energy physics experiments (HEP), with the main aim to replace the common service electronics (based on very old CMOS processes and/or off-the-shelf components [1, 2]), with more efficient scaled-down ICs, able to improve sensitivity, noise and power performance.

The analog front-end, named ASD, includes Amplifier, Shaping and Discriminator stages. The ASD [1], presently used for the read-out of Monitored-Drift-Tube (MDT) chambers of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN, is a 0.5 µm CMOS design. It is biased at 3.3 V and provided reliable operation and low failure rate. It performs a front-end charge-to-voltage conversion (by a proper Charge-Sensitive-Preamplifier) followed by the analog signal conditioning (amplification and shaping) and A/D conversion. It features a sensitivity (i.e. voltage vs. charge conversion ratio) of 8.9 mV/fC [1], 15 ns nominal Peaking Time Delay (i.e. PTD, the front-end capability to quickly detect charge arrival time) and low-noise enabling 5 fC minimum detected charge at 10 dB (3.2× factor) Signal-to-Noise-Ratio (i.e. SNR).

The LHC collider at CERN is presently in an upgrade process ([2]) to be implemented after the year 2025, called Phase-II, to enable higher luminosities of a factor $5-7.5$ beyond the nominal value of $10^{34}\,cm^{-2}s^{-1}$. This high luminosity is challenging for the MDT read-out system for two aspects. Higher hit rates, mainly due to increased cavern background, drive data transmission to the rear end electronics to the limit of available bandwidth. In addition, the new L1 trigger operating parameters — latency up to 60 µs and trigger rates up to 400 kHz — call for a replacement of the entire readout chain.

In this scenario, the ASD performance of the MDT system has to be improved, while maintaining the present, well established system architecture (including the parasitic capacitance of the detector of about 60 pF).

This paper presents the 8-channels MDT-ASD (8xASD) in CMOS 0.13 µm technological node, where improvements are performed in terms of:

- lower peaking time delay (PTD) to achieve the required time resolution;
- larger sensitivity and higher SNR at 5 fC minimum charge.

The large swing required to adopt a single 3.3 V supply voltage that can be sustained only by the 0.35 µm High-Voltage (HV) devices. The 8xASD performs 11 ns PTD (w.r.t. the original 15 ns), 13.8 mV/fC sensitivity (w.r.t. the original 8.9 mV/fC) and 15 dB (5.6× factor) SNR (w.r.t. the original 10 dB). These improved results have been obtained without increasing the power consumption that is strongly fixed by the input noise specifications. This means that the technology scaling has been exploited for performance improvement and area reduction (about a factor 2× with 6 mm^2 die size w.r.t. the original 11.9 mm^2).

This paper is organized as follows. Section 2 introduces the ATLAS experiment key points for electronics development. Section 3 presents the CMOS 8xASD circuital/design choices, while section 4 is focused on the preliminary experimental results. At the end conclusions will be drawn.

2 The ATLAS experiment

The ATLAS experiment at the CERN LHC collider is designed to record collisions from protons on protons (p-p collisions) at center-of-mass energies of up to 14 TeV. In order to determine energy and direction of the secondary particles, emerging from the p-p collisions, a sequence of specialized detectors is used for the detection of charged and neutral particles through a shell-like structure.

The muons emerging from the primary collision, being the most penetrating charge particle component, are able to transverse the Calorimeters and to reach the Muon spectrometer, the outermost shell of the ATLAS detector. Electrons generated by muons in the gas-filled pressurized MDT tubes are drifting to the central wire of the tube, where their time-of-arrival is used to determine the distance of the track from the wire. As the muon usually passes through a large number of drift tubes, the position of the muon track can be reconstructed from a combination of measurements in the tubes along the muon trajectory. Details about the MDT ATLAS readout electronics are given in [4]. Figure 1 shows a simplified MDT readout simplified scheme. The small charge signals coming from the wires are sent to the 'mezzanine' board where the 8xASD is placed (see figure 2 for the single-channel system generic block scheme).

This monolithic 8xASD senses, shapes and converts the signal coming from the tubes, providing time-domain voltage pulses, whose duty cycle is proportional to the amount of charge at the 8xASD input. The output signal of the discriminator, triggered when the voltage pulse crosses a predefined, adjustable threshold is subsequently sent to an off-chip Time-to-Digital Converter (TDC), which forwards the signal arrival times down the data acquisition chain for recording and track reconstruction.

3 MDT-ASD circuital implementation

The device includes eight identical channels and it has been realized in IBM 0.13 µm CMOS technology. The architecture of a single-channel 8xASD is shown in figure 2 [3]. Each channel input signal is a current pulse signal coming from the detector. It is converted into a voltage signal

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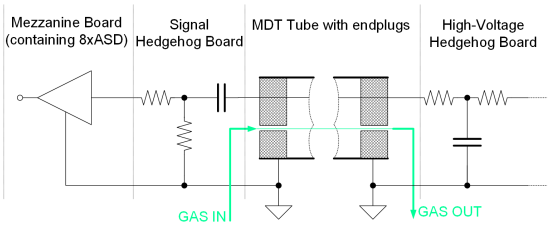

Figure 1. Muons Detection Scheme [2].

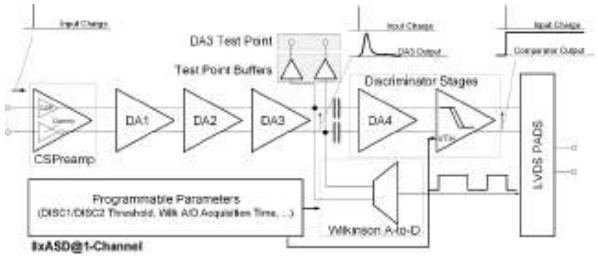

Figure 2. 8xASD Front-End Generic Block Scheme.

by the Charge-Sensitive-Preamplifier (*CSPreamp*). The *CSPreamp* output voltage is then properly shaped by the cascade of three Differential-Amplification stages (DA_1, DA_2, DA_3) to increase the signal power, and to perform out-of-band noise rejection and anti-aliasing filtering for the following ADC. The DA_4 output signal feeds a Comparator (Discriminator Stage in figure 2), which allows detecting the charge arrival time.

The DA_3 output signal also provides the input signal for the Wilkinson ADC which generates a time representation of the input signal, performing a voltage-to-time conversion. A Programmable Parameters stage has been embedded to set the Discriminator threshold (the minimum charge to be detected) and the phases signal needed for Wilkinson ADC operation. Moreover, LVDS drivers have been designed to interface the 8xASD chip with the subsequent TDC chip. Test point for the DA_3 output voltage is an analog buffer, able to drive the probe for testing purposes (with -2 dB (0.8× factor) drop and a few ns as additional delay).

3.1 Charge-Sensitive-Preamplifier

The system behavior is strongly dependent on the performance of the *CSPreamp* that must manage the large detector capacitance of about 60 pF.

The *CSPreamp* is composed by two identical symmetrical paths. A dummy preamp has been used for differential signal processing, and as a consequence the input charge is read from one single path (CSP in figure 2). The transistor-level scheme of the *CSPreamp* is shown in figure 3.

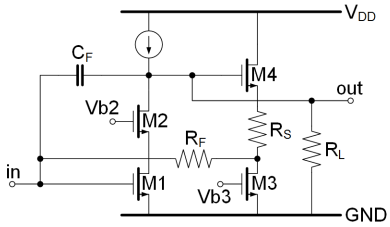

Figure 3. 8xASD Charge-Sensitive-Preamplifier Schematic.

The *CSPreamp* structure is the same of the previous design. However the design strategy and parameters have been completely re-designed to improve the performance in terms of the input impedance (< 120Ω), noise, and speed of response. Regarding the input impedance, the *CSPreamp* is based on a cascode common source amplifier, which guarantees large loop-gain for closed-loop operation, and as consequence a better virtual ground at the input node (required by the large C_D). The input impedance is maintained almost constant for all in-band frequencies, since at low frequency, it is fixed by R_L (= 16 kΩ) and R_F (= 16 kΩ), while, at higher frequency, it is regulated by the Feedback Capacitance (C_F = 680 fF) and by the detector capacitance (C_D = 60 pF). The output signal is read at the M_2 drain. The $M_3 - R_S - M_4$ source-follower is used to increase and optimize the output node common-mode voltage, for the following DA_1 stage, which has NMOS input transistors (for noise minimization). Vb2 and Vb3 nodes are connected to diode transistors of cascode mirrors.

Regarding *CSPreamp* noise and time-response, both are optimized by suitable input device transconductance (g_{m1}). In this direction, transistor M_1 operates in moderate inversion region ($V_{ov} \approx 100$ mV) with a nominal current of 1.6 mA in order to have large g_{m1} (25 mA/V), much larger than in previous design. This improves both noise and speed. Nonetheless, thanks to a better redistribution of the power among the different stages, the overall power consumption is not increased. In fact, larger power is allocated to the CSPreamp input stage, saving power where it was not necessary (mainly in the *DAx* chain, and in the bias circuit). Such large g_{m1} value improves the speed-of-response as follows. The CSPreamp transfer function is approximately given by:

$$T(s) \cong -R_F \cdot \frac{1 - s \cdot \frac{C_F}{g_{m1}}}{\left(1 + s \cdot C_F \cdot R_F \left(1 + \frac{C_D}{C_F} \cdot \frac{1}{1+g_{m1} \cdot R_L}\right)\right) \cdot \left(1 + s \cdot \frac{C_D}{g_{m1}}\right)} . \tag{3.1}$$

Since g_{m1} = 25 mA/V and $C_F \ll C_D$, the zero is at much higher frequency and can be neglected. Assuming infinite g_{m1}, the dominant pole is given by ($C_F \cdot R_F$), and the output pulse voltage peak value should be approximately given by (Q_{IN}/C_F) ≈ 7 mV_{0-PEAK}. In this design g_{m1} has been fixed at 25 mA/V, as trade-off between noise and power, resulting in a CSPreamp sensitivity of 1.4 mV/fC. These considerations are validated by figure 4, where the simulated CSPreamp time response is shown (NO-NOISE curve) and compared with the single-pole ideal system (No-Noise, No-C_D curve). The main effects of the C_D capacitance increase are lower sensitivity (4 mV_{0-PEAK} vs. 6 mV_{0-PEAK} for minimum Q_{IN} = 5 fC), and slightly slower time response (7 ns vs. 4 ns).

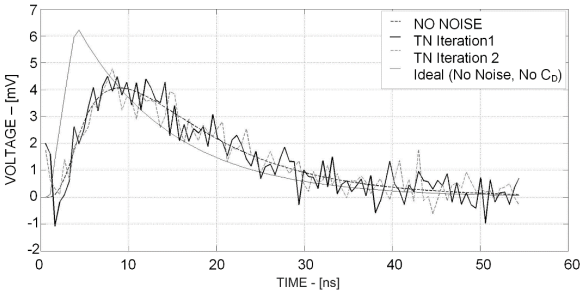

Figure 4. CSPreamp. v_{out} Transient Noise Time Response.

The large g_{m1} value avoids significant sensitivity degradation due to the large parasitic detector capacitance and mitigates the second pole effect, pushing it up to much higher frequency. This improves the CSPreamp transient performance (the second pole time constant is inversely proportional to g_{m1}, as stated in eq. (3.1)). Moreover, such large g_{m1} value enforces virtual ground and lowers *CSPreamp* equivalent input impedance down to $\approx 60\Omega$, (nominal, in order to be $< 120\Omega$ in nominal condition and in presence of CMOS process, supply voltage and temperature variations) acceptable for the peaking time delay, and noise. Two transient-noise iterations have been run, to highlight the thermal noise contribution, resulting in 0.55 mV_{RMS}-in-band output noise power. The SNR at the *CSPreamp* output is 19 dB (8.9× factor) in case of minimum input charge of 5 fC, and it rises up to 45 dB (178× factor) at 100 fC.

3.2 DA_1-DA_2-DA_3

The *CSPreamp* output signal is amplified&filtered by the DA_1-DA_2-DA_3 stages, which convert the signal into a bipolar pulse and define the fall-down time. In this DA_1-DA_2-DA_3 chain, the scaled 0.35 µm devices have been exploited in the reduction of the parasitic capacitance, and in increasing the speed while reducing power consumption. The frequency response at the output of each stage is plotted in figure 5. The full chain exhibits a pass-band characteristic with a 5 MHz center frequency. The high-pass part, mainly imposed by DA_3, shows a 30 kHz corner frequency and a slope of +6 dB/octave (1^{st}-order high-pass filter). The band-pass section is the superposition of all four amplifier low-pass characteristics.

3.3 Wilkinson A/D

The DA_3 output signal feeds to the Discriminator and the Wilkinson ADC (W-ADC) stage, to provide information regarding the arrival time and the total amount of input charge at the *CSPreamp* input node. The Discriminator is a comparator, which detects the presence of a specific minimum charge at the *CSPreamp* input nodes and provides the charge arrival time, and the Start-of-Conversion signal for the W-ADC. The W-ADC, instead, performs a Voltage-to-Time conversion, as shown in figure 6. The sampling capacitor (C_H) is charged for a given time range T_{GW} (programmable between 8 ns and 32 ns) and the capacitance C_H is then discharged down to the time of zero-crossing.

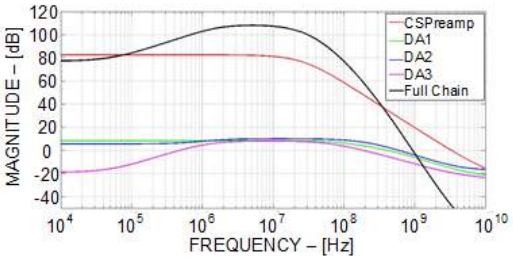

Figure 5. CSPreamp-DA_1-DA_2-DA_3 chain. AC Frequency Responses.

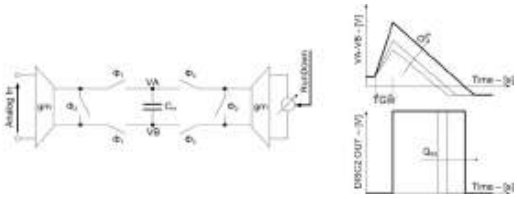

Figure 6. Wilkinson-ADC Operating Principle.

Charge and discharge phases depend on Φ_1 and Φ_2, such as on ON-OFF switches phases. Φ_1 and Φ_2 signals are complementary MOS switches. The time to discharge C_H will be proportional to the analog input voltage and, as a consequence, to the equivalent amount of charge at the *CSPreamp* input nodes. For a given integration time T_{GW}, the analog voltage peak value (i.e. the input charge Q_{IN}) is proportional to the time to cross the horizontal axis (figure 6). The transconductor stages design had to face the lower output impedance of the 0.35 µm devices w.r.t. the 0.5 µm devices. Specific arrangements have then been adopted to guarantee the same impedance level. On the other hand, the power here is unchanged since it is fixed by the value of C_H, maintained to be equal to 3 pF, to make parasitic effects negligible.

4 Preliminary measurements result

The presented 8xASD chip has been integrated in CMOS 0.13 µm (figure 7 shows the chip photo). The electrical characterization has been carried-out mounting the 8xASD on the mezzanine board, working in the same boundary conditions w.r.t. the ATLAS experiment environments. The 8 channels are placed and routed in order to guarantee symmetrical paths w.r.t. the bias and setting circuits (located in the center region of the layout top-view, and used to program and regulate the discriminators thresholds, gain, etc). Each channel occupies 0.4 mm^2. The total area (including additional pads, JTAG, etc.) is about 6.38 mm^2. All measurements have been performed using input charge (Q_{IN}) in the range 5 fC – 100 fC.

4.1 8xASD electrical characterization

The analog section of the 8xASD composed by the cascade of the *CSPreamp* and the DA_1-DA_2-DA_3 stages is here presented. Figure 8 shows the output signal vs. time at DA_3 output buffers test pins (see figure 2), hence some voltage peak drop (i.e. about 3 dB (1.4× factor) and 2 ns additional time delay) and an additional peaking time delay is expected w.r.t. the effective on-chip DA_3 signal. The DA_3 output voltage ranges from 90 mV_{0-PEAK} up to 1.2 V_{0-PEAK}. Figure 9 shows the $V_{OUT,DA3}/Q_{IN}$ trans-characteristic, justifying the 14.2 mV/fC of sensitivity for minimum Q_{IN}. Moreover, the sensitivity is quite constant over the input charge range, so no voltage swing saturation is presented over the 5 fC – 100 fC range, resulting in a sufficiently linear behaviour. Finally, figure 10 shows Peaking Time Delay that is lower than 9 ns for minimum Q_{IN} (5 fC), and raises up to 12 ns at 100 fC. For sake of completeness, the figures 9–11 are shown with and without the amplitude and time effects of the test points output buffers.[1] The Wilkinson ADC has bee also tested for four different equivalent input charge values (in the 20 fC – 100 fC range). The output pulse width is proportional to the equivalent amount of charge at the 8xASD input, resulting in the sufficiently linear characteristic in figure 12.

5 Conclusions

An 8-channels read-out front-end for the MDT ATLAS detectors at CERN LHC has been presented. The design has been carried out in IBM 0.13 µm technology, targeting area and noise reduction at the same power budget of the state-of-the-art for ATLAS MDT detectors. Table 1 summarizes the most important performance of the presented 8xASD for the MDT-ATLAS-read-out, compared with the previous implementation.

The device exhibits a factor 2 area reduction (lower than the CMOS scaling-down factor due to 0.35 µm High-Voltage devices). For the same detector capacitance, the single channel power consumption is approximately the same than in [3], whereas input charge signal quality improves (higher SNR, given by better *CSPreamp* ENC noise performance). The peaking time delay is 12 ns, i.e. 3 ns lower than the state-of-the-art, resulting in faster response and reduced probability to muons data loss.

[1] Note that there are not measurements without buffer. The curves, indicated as 'without buffer', have been extrapolated from simulations.

Table 1. State-of-the-art comparison.

Parameter	This Work	[3]
CMOS Technology	0.13 µm@3.3 V	0.5 µm@3.3 V
Total Die Area	6.38 mm^2	11.9 mm^2
Channel Current Consumption	10 mA	11 mA
Detector Parasitic Cap.	60 pF	60 pF
Input Charge	5 fC – 100 fC	5 fC – 100 fC
Front-End Delay at 100 fC@Q_{IN}	12 ns	~ 15 ns
Front-End Sensitivity	14 mV/fC	8.9 mV/fC
ENC	0.6 fC	1 fC
SNR	15 dB	10.9 dB

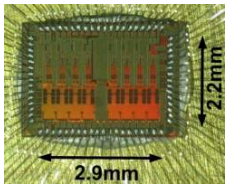

Figure 7. Chip Layout Photo.

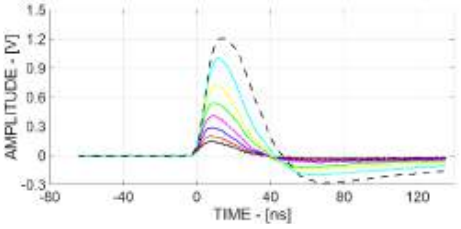

Figure 8. DA_3 Test Point Buffers Output Signal vs. Input Charge (5 fC-100 fC).

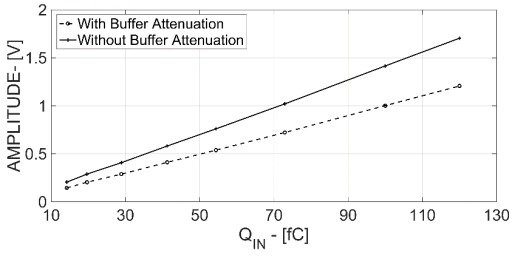

Figure 9. Analog Chain (CSPreamp-DA_3) $V_{OUT,DA3}/Q_{IN}$ vs. Input Charge.

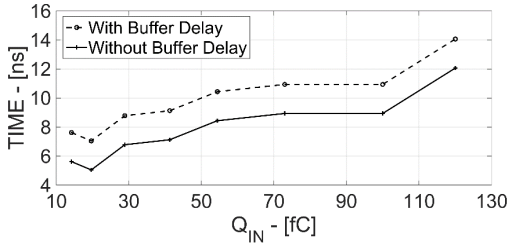

Figure 10. Analog Chain Peaking Time Delay vs. Input Charge.

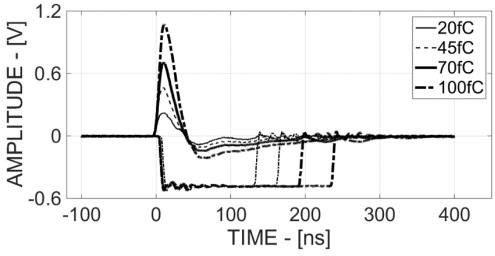

Figure 11. Wilkinson ADC Output Pulse/DA3 output Signal vs. Input Charge.

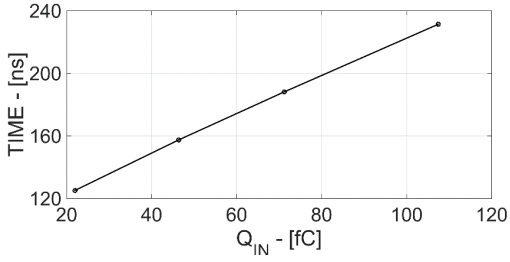

Figure 12. Wilkinson ADC Output Pulse Time Width vs. Input Charge.

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9
IC-PIX28 Related Papers

The papers dedicated to IC-PIX28 are listed in the next pages.

The first has been presented at IEEE ICECS 2015 Conference in Cairo, Egypt. It deals with a general overview of the integrated circuits and the simulation results. It is selected within the 10 best papers.

The second, presented at IEEE SENSORS 2016 Conference in Orlando, Florida, is dedicated to measured performance of the entire Charge Sensitive Preamplifier and Comparator chain.

9.1 IEEE ICECS 2015

IC-PIX28: a 28nm read-out channel for pixel detector

F. Resta, M. De Matteis, G. Rota, A. Pezzotta, A. Pipino, A. Baschirotto
Physics Department University of Milano-Bicocca, Italy - f.resta@campus.unimib.it

***Abstract*—An Integrated Chip prototype for PIXel read-out, named IC-PIX28 and designed in 28nm CMOS technology, is here presented. The chip features a single channel including a cascade of a Charge-Sensitive-Amplifier (CSA) and a comparator, performing a Time-over-Threshold (ToT) operation. The IC-PIX28 comparator can operate with thresholds ≥3mV, generated on-chip starting from an off-chip reference voltage. A few number of transistors allows processing an input charge within 0.1fC÷5fC range. With the minimum input charge, the CSA output peak voltage is 4.6mV reached in 11ns. In this condition, 44mV/fC sensitivity and 0.029fC (180e⁻) Equivalent-Noise-Charge (ENC) are achieved with 4.67μA current consumption and 0.07mm² area occupancy.**

Keywords—CMOS 28nm, Pixel Detection, Integrated Front-End, Physics Experiment.

I. Introduction

Most of the high-energy physics experiments (HEP) inside the Large Hadron Collider (LHC) at CERN exploit Silicon Pixel Detectors (SPDs) to analyze charged particles produced by collisions in the accelerator. ATLAS [1] and CMS [2] experiments are two well-known examples. SPDs development plays a main role where the efficiency, precision and resolution are fundamental requirements. In the HEP community, it is important to achieve them despite the radiation damage and the challenging high data acquisition rate. Integrated solutions allow realizing the detectors and the front-end electronics in the same wafer increasing their reliability.

The Active Pixel Sensors (APS) world is an endearing field for the physics researchers and the industrial business of image sensors. APS development has been facilitated by the aggressive CMOS scaling technology [3] and the guaranteed compatibility with on-chip read-out electronics. Integrated mixed-signal solutions are intrinsically more complex but reliable. With sub-μm CMOS technologies, there was an increase in the number of integrated devices in the same area as well as of the signal-processing rate. At the same time, the transistor intrinsic gain ($g_m \cdot r_{ds}$) and the ratio between the supply voltage and the threshold voltage decrease. Therefore, a careful design of interface analog blocks between APSs and digital processing is required.

The choice of designing mixed-signal read-out systems for pixel detector in ultra-scaled technologies has the advantages to develop devices with smaller area occupancy, higher radiation hardness [4] and higher robustness to mismatch and/or aging variations. In this scenario, IC-PIX28 is the first prototype designed in 28nm technology within the ScalTech28 collaboration and here presented.

This paper is organized as follows. Section II presents a brief overview on 28nm CMOS technology, his issues and the reasons why it could be largely used in pixel applications. Section III and IV are dedicated to the Charge Sensitive Amplifier (CSA) characterization and the main circuital choices for IC-PIX28 channel design. Before concluding, Section V provides an overview of the most important simulation results.

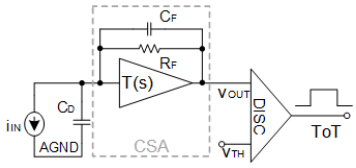

Fig. 1 - Generic block scheme of a Charge-Sensitive-Amplifier.

II. 28nm Technology for Pixel Detection

28nm bulk CMOS technological node represents an interesting innovation for integrated circuits used in detecting/sensing application. In HEP field, high energetic particles flux generates free electron-hole pairs in the oxide volume causing MOS intrinsic parameters variations. These effects, named as Total Ionizing Dose (TID) effects, can not be neglected because shifted threshold voltages create unexpected behavior and not usable circuits. A proper layout activity could help to reduce the leakage for the N-channel devices. A typical approach is designing enclosed geometry and implementing P+ guardrings wherever necessary [5]. Unfortunately, 28nm technology DRC (Design Rule Check) rules prohibit enclosed structure implementations but according to [6], the TID tolerance increases with scaling down technological nodes. Therefore, 28nm technology would perform better than 65nm. The expectations predict the overcoming of 1Grad TID that 65nm fails to tolerate [7]. Considering also SOI (Silicon On Insulator) technologies, including a buried oxide layer, this one (bulk) is expected to be more radiation hard. In fact, most of radiation interactions occur inside oxides [8]. Moreover, it exploits new processing techniques to ensure dielectric robustness to electrical stress and high permittivity gate dielectric stacks [4].

Reducing the minimum feature size, an increase of the integration and the signal processing rate can be achieved. In high-energy physics experiments, it is mandatory to acquire the time-of-flight and the amount of charge information from an incident particle. 28nm technology operates with a reduced supply voltage (0.9V) and a low output signal swing, due to the reduced V_{DD}/V_{TH} ratio. This is not necessarily an issue in sensor systems for pixel read-out because very small signals are processed (e.g. few hundred of mV).

As regards parasitics, this 28nm technology has a high-k dielectric in place of the silicon dioxide reducing the gate leakage currents and parasitic capacitance (few fF). Hence, higher sensitivity accuracy of the CSA block can be achieved.

The prototype here presented aims to demonstrate the advantages arising from the technology choice, in terms of better power/noise trade-off, reduction in silicon area occupation and radiation hardness.

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III. CSA Characterization

In Fig. 1 the architecture of the IC-PIX28 channel prototype is shown. It composes of a Charge-Sensitive-Amplifier (CSA) and a Time-over-Threshold (ToT) block, connected in cascade. In a future implementation, the pixel read-out chip will include a matrix of those and it will be important to guarantee matching between channels.

The read-out system behavior is heavily dependent on the CSA performance. For this reason, a Matlab script aims to simplify the design workflow and it is useful to find an optimal solution starting from system level specifications. Detector Capacitance (CD), Sensitivity (S), Peaking Time Delay (PKT) and noise represent the key parameters.

A typical CSA scheme is represented by a gain stage in closed loop with a Feedback RC net (R_F and C_F). Considering an ideal amplifier with finite gain (A_0) and infinite bandwidth, the CSA frequency response is given by Eq. 1. Here R_F is used also to fix the input-output operating point. τ (Eq. 2) is the time constant associated to the dominant pole.

$$\frac{v_{OUT}}{i_{IN}}(s) = -\frac{A_0 R_F}{(1+A_0)(1+s\tau)} \quad \text{Eq. 1}$$

$$\tau = C_F R_F \left(1 + \frac{C_D/C_F}{1+A_0}\right) \quad \text{Eq. 2}$$

The time constant τ and the output voltage peak are strictly dependent on C_D/C_F ratio and A_0. Therefore they could be properly sized in order to maximize the charge collection efficiency. The A_0 maximum value depends on CMOS technology and it is linked to the circuit complexity.

A key parameter of the CSA is also the sensitivity, defined as the ratio between the peaking voltage at the CSA output and the input charge. In this particular case, the sensitivity (S) is given by Eq. 3, where S_{ID} is the ideal sensitivity, i.e. neglecting A_0 and C_D effects.

$$S = \frac{1}{C_F\left(1 + \frac{C_D/C_F}{1+A_0}\right)} = S_{ID}\frac{1}{\left(1 + \frac{C_D/C_F}{1+A_0}\right)} \quad \text{Eq. 3}$$

In a first approximation, if $A_0 \gg C_D/C_F$, S_{ID} could be considered equal to S. It is reasonable to assume that C_D/C_F is the minimum value of A_0 allowed in order to have the minimum acceptable value of S, named S_M (Eq. 4). Similarly, the output peaking voltage is given by Eq. 5.

$$S_M = \frac{1}{2C_F} = \frac{S_{ID}}{2} \quad \text{Eq. 4}$$

$$V_{PEAK} = V_{PEAK,ID}\left(1 + \frac{C_D/C_F}{1+A_0}\right)^{-1};\ V_{PEAK,ID} = \frac{Q_{IN}}{C_F} \quad \text{Eq. 5}$$

Regarding the CSA performance, noise and output rise time must be considered. In a first approximation, the Equivalent Noise Charge (ENC) depends on the amplifier noise according to Eq. 6, where $\overline{v_{A,IN}}$ is the input referred noise of the amplifier.

$$ENC = C_F\left(1 + \frac{C_D/C_F}{1+A_0}\right)\sqrt{\overline{v_{A,IN}}^2} \quad \text{Eq. 6}$$

In the developed Matlab script, the Peaking Time Delay (PKT) has been set to zero considering an amplifier with finite gain A_0 and infinite bandwidth. In reality, the amplifier has a generic transfer function as in Eq. 7, where f_{UGB} is the unity gain frequency.

$$T(s) = \frac{A_0}{1+s\tau_A}; \qquad \tau_A = \frac{A_0}{2\pi f_{UGB}} \quad \text{Eq. 7}$$

In this context, the CSA frequency response modifies as shown in Eq. 8.

$$\frac{v_{OUT}}{i_{IN}}(s) = -\frac{A_0 R_F}{(1+A_0)}\frac{1}{(\alpha_1 s^2 + \alpha_2 s + 1)} \quad \text{Eq. 8}$$

$$\alpha_1 = \tau_A C_F R_F\left(\frac{1 + C_D/C_F}{1+A_0}\right) \quad \text{Eq. 9}$$

$$\alpha_2 = C_F R_F\left(1 + \frac{\tau_A/(C_F R_F) + C_D/C_F}{1+A_0}\right) \quad \text{Eq. 10}$$

Choosing $\tau_A = C_F R_F$, the closed loop poles can be identified as two real poles. Eq. *11* gives their time constants (τ_1 and τ_2).

$$\tau_1 = C_F R_F; \qquad \tau_2 = C_F R_F\left(\frac{1 + C_D/C_F}{1+A_0}\right) \quad \text{Eq. 11}$$

Notice that this choice allows maintaining a constant impedance at the amplifier input. In this way, the PKT depends only on the poles position. For an optimal design, the minimum transconductance (g_m) of the amplification stage must be fixed as a starting point, since it implies the maximum value of the allowed thermal noise. At the same time, it determines the minimum power consumption. The choice of C_F value is related to the sensitivity specification and it fixes the minimum A_0.

IV. Channel Implementation

IC-PIX28 is a channel prototype realized in CMOS 28nm technology, operating with 0.9V supply voltage. Fig. 2 shows the overall architecture composed by the cascade of the CSA, the C_1-R_{EQ} net and the discriminator (DISC). The channel receives as input a current signal (I_{IN}) coming from the pixel detector. In this particular systems, the detector is integrated close to the read-out front-end. Every detector has a characteristic parasitic capacitance (C_D) that affects the time and the frequency responses. In pixel read-out, typical C_D values are hundreds of fF. The pixel detector silicon integration allows a local data processing such as amplification, shaping and discrimination. The full system integration helps to avoid the chip I/O pad capacitance, managing pixel capacitance only. It implies to limit current consumption in order to comply with the specifications.

A summary of the channel main specifications are reported in the TABLE I. The system has been optimized to operate with C_D of 100fF. The CSA architecture is composed by a common source stage with a capacitor (C_F=10fF) and a resistor ($R_F \approx 1.25M\Omega$) in feedback. Transistor M_{IN} of Fig. 2 represents the amplification stage characterized by a transfer function as described in Eq. 7. The choice to implement the amplification stage with a single transistor (M_{IN}) reduces the number of noise contributions and the overall current consumption. The stage is characterized by 23dB of DC gain and 300MHz of bandwidth. This system performs a sensitivity of 44mV/fC, an integrated noise at the CSA output of 1.25mV$_{RMS}$, a peaking time delay of 11ns. The W/L of M_{IN} transistor is 12µm/100nm operating in subthreshold region with a nominal current of 1.7µA and a g_{mIN}

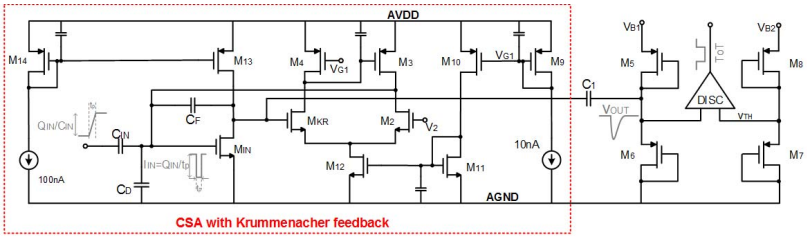

Fig. 2 - Block scheme of IC-PIX28 channel prototype.

TABLE I. SUMMARY OF SPECIFICATIONS

Parameter	Value
Power Consumption	<5μW
Input Charge Range	Up to 30ke⁻
Minimum Detectable Charge	1ke⁻
Rise Time	<25ns
Noise Level	<200e⁻
Detector Capacitance	100fF

(transconductance) of 51μA/V. Considering the 0.9V supply voltage and 0.55V transistor threshold, the chosen g_{mIN} value allows to find a reasonable trade-off between all the specifications. In this condition, A_0 value is 14, that is greater than C_D/C_F=10. The result is a sensitivity of 44mV/fC.

As shown in Fig. 2, the feedback resistor (R_F) has been replaced by an equivalent resistor realized with the transistors (M_2-M_3-M_4-M_{KR}), implementing the Krummenacher feedback broadly described in [9]. At the cost of a very small increase of the current consumption (30nA for each branch), the circuital solution implements a 1.25MΩ R_F through a transconductance (gm_{KR}) of 800nA/V. This choice fixes the CSA input-output operating point helping to automatically compensate the detector leakage current. The CSA is followed by a C_1-R_{EQ} net in order to decouple the CSA output from discriminator. R_{EQ} is given by the impedance at the V_{OUT} node, that is $r_{DS5}//r_{DS6}$. Regarding the discriminator, the input operating point and the threshold V_{TH} are fixed by off-chip V_{B1} and V_{B2} voltages through diode connected transistors. The choice of replacing R_1 with a diode transistor has been made after post-layout simulations in order to increase the accuracy, to improve the matching and to decrease the parasitic effects introduced by the large value of the resistor.

After a first conversion of the input current signal in voltage one, the Time-of-Threshold (ToT) is performed in digital way. ToT provides information about the amount of the input charge in terms of pulse width. The discriminator is a comparator stage based on switched-capacitor architecture as that shown in Fig. 3.

The phases Φ1 and Φ2 impose a preliminary idle timing at the system in order to charge the Cc capacitor and to set V_{TH} threshold. During the idle timing, the input charge cannot be detected. The structure is based on the cascade of inverters that gradually amplify the input difference in order to have a rail-to-rail output. The critical part is the first amplification because its behavior depends on the operating point and works with very small signals. Consequently, most of discriminator power consumption derives from it. The last inverters are used only to amplify the signal with very low current (few hundred of nA).

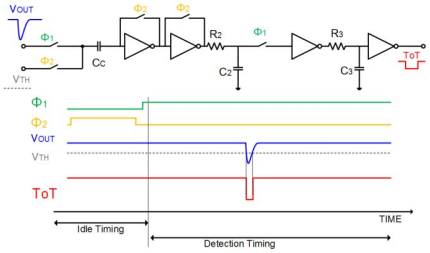

Fig. 3 - Block scheme of Discriminator stage and signal timing.

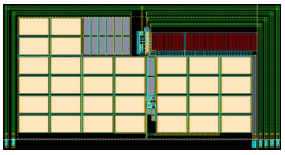

Fig. 4 - Photo of IC-PIX28 Layout.

However also noise continues to increase along the chain. A possible solution to reduce noise is to filter it through RC nets inserted before each of the two last inverters.

V. SIMULATION RESULTS

The presented IC-PIX28 prototype has been integrated in CMOS 28nm technology and its layout view is reported in Fig. 4. The area is about 0.07mm² but the most of it is occupied by the filtering capacitance inserted between the gates of the current mirrors and supply/ground. A complete characterization of the prototype has been done in time and frequency domains varying the input charge in the range of 0.1fC ÷ 6fC and including layout parasitic components. Transient and transient noise simulations demonstrate the correct conversion also with minimum input charge (0.15fC) and 100fF of C_D.

In Fig. 5 there is a description of the system in terms of input current, CSA output and DISC output signals with (colored line) and without noise (black line). Noise is below the -3mV comparator threshold and the maximum variation of the ToT pulse width at the DISC output is about 33% respect the 71.24ns of the nominal value.

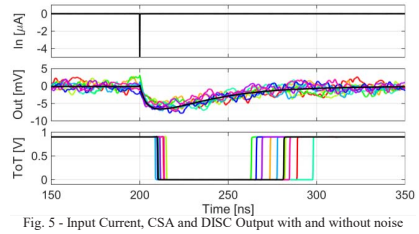

Fig. 5 - Input Current, CSA and DISC Output with and without noise

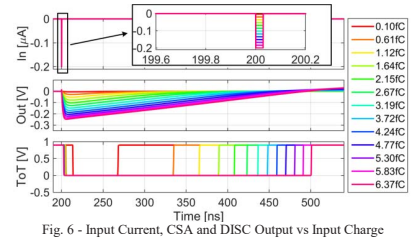

Fig. 6 - Input Current, CSA and DISC Output vs Input Charge

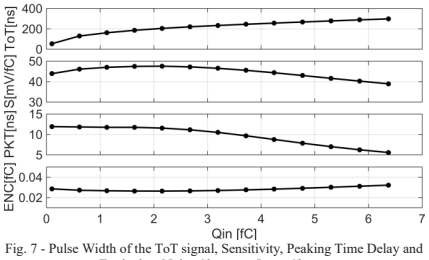

Fig. 7 - Pulse Width of the ToT signal, Sensitivity, Peaking Time Delay and Equivalent Noise Charge vs Input Charge

In Fig. 6 there is the same type of signals obtained for different input charge. The current pulse is very short (30ps) as highlighted in the box. For input charge between 0.1fC and 6fC, the maximum peak voltage varies from 4.4mV to 250mV with a variation of the ToT pulse width from to 55ns to 297ns. The linear trend of ToT signal variation versus the input charge is shown in Fig. 7.

Other relevant parameters for this circuit topology are the sensitivity, the peaking time delay and the equivalent noise charge (Fig. 7). The sensitivity, given by the maximum peaking voltage and input charge ratio, has an almost constant trend around 44mV/fC.

The resulting performance of the IC-PIX28 and a comparison with other CMOS pixel front-ends are reported in TABLE II. . Significant benefits respect to the other read-out systems are shown, above all in terms of power consumption, equivalent noise charge and peaking time delay.

VI. Conclusions

IC-PIX28 is the channel prototype implemented in CMOS 28nm technology. As Apsel65 [4], it is designed in nanometer technology, with the possibility of increasing the number of integrated channels per unit area and improving the radiation hardness. With a detector capacitance of 100fF, IC-PIX28 performs 44mV/fC of sensitivity, 11ns of peaking time and 0.029fC (180e$^-$) of ENC. CSA and DISC show 2.4μA and 2.2μA of current consumption respectively. With 0.9V of supply voltage, the power consumption of the overall chain is 4.2μW. The work here presented is very competitive with state-of-arts pixel read-out systems, although the 28nm technology issues.

A single channel has been integrated and the future measurements will give a complete characterization of it, useful to optimize the matrix of channels.

Acknowledgment

This research has been funded by the INFN project ScalTech28.

TABLE II. State of the Art Comparison

Parameter	[10]	[4]	IC-PIX28
Technology	130nm	65nm	28nm
Supply Voltage	1.2V	1.2V	0.9V
Power Consumption	200μW	6μW	4.2μW
Equivalent Noise Charge	250e$^-$	200e$^-$	180e$^-$
Charge Sensitivity	80mV/fC	40mV/fC	44mV/fC
Peaking Time	25ns	25ns	11ns
Detector Capacitance	200fF	100fF	100fF

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9.2 IEEE SENSORS 2016

A 4.3µW 28nm-CMOS Pixel Front-End with Switched Inverter-Based Comparator

F. Resta[1], A.Pipino[1], A.Pezzotta[1], M. De Matteis[1], M. Croce[2], A. Baschirotto[1]

[1] Physics Department and INFN Milano Bicocca – University of Milano Bicocca – Italy
[2] Dept. of Electrical, Computer and Biomedical Engineering – University of Pavia - Pavia, Italy
f.resta, a.pipino1@campus.unimib.it, alessandro.pezzotta, marcello.dematteis, andrea.baschirotto@unimib.it

***Abstract*—The complete design and electrical characterization of a readout frontend for high luminosity pixel detectors is hereby presented. The design has been carried out in 28nm bulk-CMOS technology. The selected technology process shows significant advantages in terms of radiation hardness, faster/low-power digital signal processing and whole chip area reduction. Nonetheless, it is challenging in terms of operating point (0.9V supply voltage at 0.5V threshold voltage for standard process transistors), dynamic range, and large sensitivity to Process-Voltage-Temperature variations. The proposed integrated circuit includes the cascade of a low-noise preamplifier stage and a switched-capacitor inverter-based comparator. The overall system detects input charges up to 14fC and provides information about the amount of the charge with a Time-over-Threshold (ToT) technique. It features 4.3µW power consumption, 54dB Signal Noise Ratio and 0.02mm² area occupancy. A ToT range of 180ns in 28nm bulk-CMOS represents a challenge for the future Time-to-Digital Converters (TDC) used in High-Energy-Physics readout systems. Analog front-end and TDC development anticipate a higher charge quantization resolution in the next physics experiments.**

Keywords—Technological Scaling, 28nm CMOS technology, analog front-end, physics experiments.

I. INTRODUCTION

Advanced electronic front-end for High Energy Physics (HEP) experiments is fundamental for the research of the new matter components. Efficient integrated circuits are essential to discover new charged particles. Starting from 2024, the main goal of an important CERN project, known as High-Luminosity Large Collider Hadron Collider (HL-LHC) project, is to increase 10 times the luminosity coming from proton-proton collisions. It represents an important step that may be helped by advanced scaled-down electronics.The demand of Silicon Pixel Detectors (SPDs) to analyze this world is undergoing an evolution in conjunction with a significant technological development. Designing reliable electronics for ATLAS and CMS [1]-[4] experiments is not trivial. The most important requirements include:

- to guarantee high performance in extreme conditions, as in presence of a Total Ionizing Dose up 1Grad
- to increase the number of devices for unit of area in order to increase the resolution and the detected event number
- to make front-end able to process an input charge within 25ns
- to guarantee reliable with low power consumption and very low Equivalent Noise Charge (ENC) or in other words high Signal-to-Noise-Ratio (SNR).

In this scenario, the scaling down and the choice to work in 28nm bulk technology allows a major tolerance to the radiation[5], smaller channels, lower consumption at the cost of an increment of Process-Voltage-Temperature variations, a lower supply voltage (0.9V), a lower V_{DD}/V_{TH} ratio, layout parasitic effects not negligible and not predictable during the design.

The topic of this paper is the development of a read-out front-end for pixels detectors (with 100fF of equivalent capacitance) in advanced 28nm bulk-CMOS technology. The device performs 54dB-SNR and consumes 4.3µW from a single 0.9V supply. This paper is organized as follows. Section II is dedicated to analog front-end description. Section III shows the experimental results and it is followed by conclusions.

TABLE I– SPECIFICATIONS SUMMARY

PARAMETERS	VALUES
Maximum Power Consumption	5µW
Minimum Detectable Input Charge	~1ke⁻ (0.16fC)
Maximum Comparator Delay	25ns
Noise Level	~200e⁻
Pixel Capacitance (C_D)	~100fF
Equivalent Noise Charge - ENC	<0.1fC

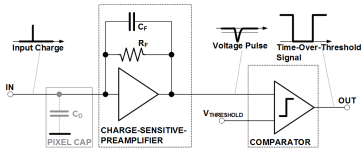

Fig. 1 – Simplified pixel front-end block scheme

II. FRONT-END DESCRIPTION

Fig. 1 shows the generic single channel block scheme of the front-end composed by the cascade of a Charge-Sensitive-Preamplifier (for charge-to-voltage conversion) and the Comparator (for Time-over-Threshold operation [6]) in 28nm bulk CMOS technology.

The pixel equivalent capacitance has been also integrated (Pixel Cap in Fig. 1 of 100fF) with the main aim to emulate the effective parasitic capacitance due to the pixel connected to the front-end (typically off-chip). This way the full electrical characterization of the silicon prototype will include the effective final application boundary conditions

Noise, time-response and sensitivity performances of the overall front-end derive from CSPreamp and from its ability to manage the C_D. A summary of the typical specifications for pixel readout systems are listed in the TABLE I.

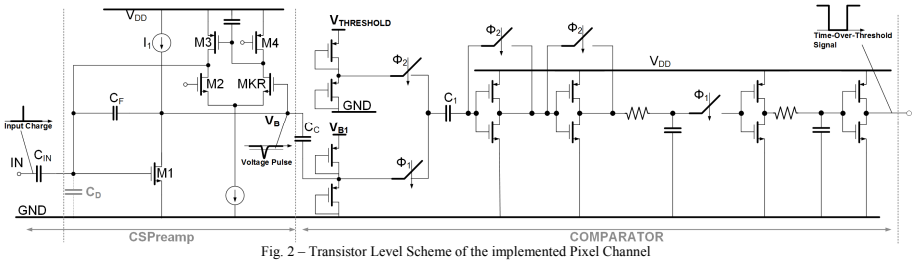

Fig. 2 – Transistor Level Scheme of the implemented Pixel Channel

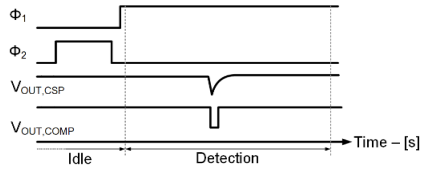

Fig. 3 – Timing of Switched Inverter-based Comparator

A. CSPreamp: Input Charge to Voltage Conversion

The transistor level scheme of the implemented pixel readout architecture is reported in Fig. 2. The CSPreamp main role is to convert into voltage domain the amount of charge at the input, and to provide such pulse-shaped analog signal to the Comparator for event and ToT detection. In order to prevent multiple events detection, the maximum allowable rising time for the CSPreamp output voltage is 20ns.

The CSPreamp includes a transistor (M_1) with a capacitance (C_F=10fF) and a Krummenacher [7] resistor (R_F=1/gm_{KR}=1.25MΩ) in feedback. The 28nm CMOS process (selected for rad-hard performance) forces to use sub-threshold region transistors. Hence, M_1 has a W/L of 12µm/100nm and 0.3V of V_{GS_M1}. Its g_m is 51µA/V with a current of 1.7µA.

The node V_B voltage operating point is fixed at 0.5V through Krummenacher feedback allowing a large negative step voltage at CSPreamp output.

The M_2-M_3-M_4-M_{KR} transistors synthesize the Krummenacher net with g_{m_KR}=0.8µA/V at 60nA current consumption. This way V_{GS_M1} and V_B are biased at 300mV and 550mV, respectively. This choice help to manage the 28nm drawbacks, i.e. gate leakage current increment and intrinsic changes due to radiation damage [5] and/or Process-Voltage-Temperature (PVT) variations.

B. Comparator: Voltage to Time Conversion

Switched Capacitor Inverter-based Comparator performs the voltage to time conversion and it is represented in Fig. 2. In this way, the output provides arrival time and amount of the input charge information. The comparator is connected to the previous CSPreamp through 1pF coupling capacitance (C_C). The input operating point and the comparison threshold are externally fixed through the voltage V_{B1} and $V_{THRESHOLD}$, respectively. The topology choice includes the cascade of four inverters with very low static power consumption (i.e. 2.2µA). As shown in Fig. 2, there are two switches (controlled by Φ_1 and Φ_2 phases, in series to C_1) used to fix the comparator threshold through a pre-charge of C_1 (250fF) capacitor (during Idle Timing, Fig. 3) and then to make the comparison with the threshold (during the Detection Timing, Fig. 3). RC passive nets are inserted at the output of the second and third inverters helping to reject the noise in presence of small signals and to guarantee a proper Signal-to-Noise-Ratio for any signal amplitude.

III. EXPERIMENTAL RESULTS

The layout of the 28nm bulk CMOS Pixel Front-End with Switched Inverter Comparator is shown in Fig. 4. Unfortunately, dummy insertion compromises the possibility to make an acceptable chip photo. An area of 0.07mm^2 is shared between the real front-end (0.02mm^2), the filtering capacitance of the current mirrors (0.04mm^2), the Pixel Cap of 100fF (0.00052mm^2) and the routing.

Time domain measurements have been done to have a completely characterization of the integrated circuit in different operating conditions. Two different test points, one after the ac-coupled C_C and one at the comparator output, allow monitoring the CSPreamp output and the Time-over-Threshold (ToT) signal. The test points are represented by analog integrated buffers, which introduce additional delays and voltage drop.

Using the ac-coupled C_{IN} (as shown in Fig. 2), input charge range of 5fC – 14fC depends on the voltage step amplitude directly connected to the input pad IN (highlighted in Fig. 2). The measured signals at CSPreamp and Comparator output are reported in Fig. 5 and Fig. 6.

Experimental results exhibit an almost constant trend of the sensitivity around 20mV/fC (Fig. 7) and a comparator delay within 25ns (maximum value is 18ns, see Fig. 6). Other important extrapolated information, in terms of CSPreamp peak voltage, sensitivity, comparator delay and ToT width, are represented in Fig. 7 and Fig. 8.

The delay ranges from 13ns up to 18ns, while ToT final range is 180ns. Assuming that the state-of-the-art 28nm Time-to-Digital Converters (i.e. TDCs in [8]) allow about 50ps time resolution (instead of 500ps, typical value for TDCs actually mounted at the CERN), 12bits (instead of 8.5bits) could be performed cascading this pixel front-end with the TDC.

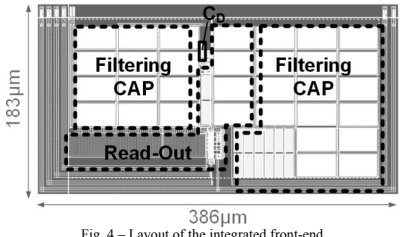

Fig. 4 – Layout of the integrated front-end

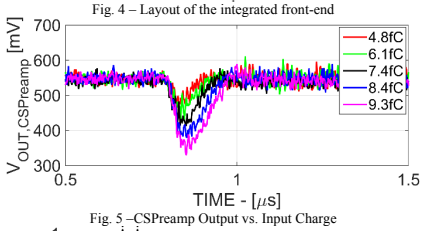

Fig. 5 –CSPreamp Output vs. Input Charge

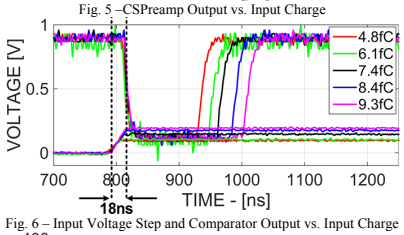

Fig. 6 – Input Voltage Step and Comparator Output vs. Input Charge

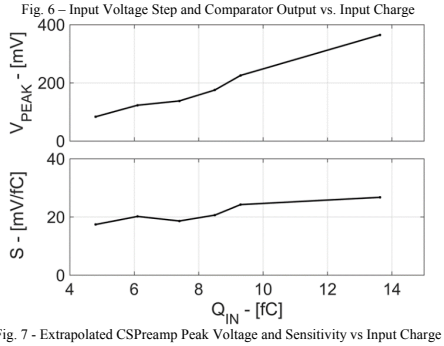

Fig. 7 - Extrapolated CSPreamp Peak Voltage and Sensitivity vs Input Charge

IV. Conclusions

A read-out front-end for next-generation high luminosity pixel detectors has been hereby presented. The design is in 28nm bulk CMOS technology. It operates with 0.9V of supply voltage and 0.5V transistor voltage threshold. The total power consumption is 4.3µW and it is shared between the charge sensitive preamplifier (around 2.4µA) and the switched-capacitor inverter-based comparator (around 2.2µA). The system includes an integrated Pixel Cap of 100fF.

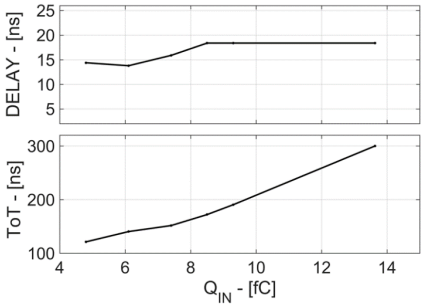

Fig. 8 – Extrapolated Comparator Delay and ToT

In these conditions, the sensitivity is 20mV/fC with maximum comparator delay of 18ns and a Time-over-Threshold range of 180ns. Experimental results confirm the possibility to use 28nm technology to design analog front-end for pixel detectors. In addition, 28nm devices show a good radiation tolerance (Total Ionizing Dose up to 1Grad is allowed [5]), typical environment of the High Energy Physics (HEP) experiments. A summary of most important characteristics of the analog front-end is reported in TABLE II.

Acnowledgment

The authors thank INFN of University Milano Bifocal for its support in ScalTech28 project research.

TABLE II – Measurements Summary

Parameter	IC-PIX28
Technology	28nm
Supply Voltage	0.9V
Die size	0.02mm^2
Power Consumption	4.3µW
Maximum Peak Voltage	365mV
Delay Range	13.8ns – 18.4ns
Time-over-Threshold Range	121ns – 300ns
Detector Capacitance	100fF
SNR at Minimum Input Charge	41dB
SNR at Maximum Input Charge	54dB

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10
Poster

Before concluding, posters correlated to MDT-ASD and IC-PIX28 integrated circuits have been reported in this section.

10.1 IEEE SENSORS 2015

An 8-Channels 0.13μm-CMOS Front-End for ATLAS MDT-Detectors

M. De Matteis[1], F. Resta[1], R. Richter[2], H. Kroha[2], M. Fras[2], Y. Zhao[2], V. Danielyan[2], S. Abovyan[2] and A. Baschirotto[1]

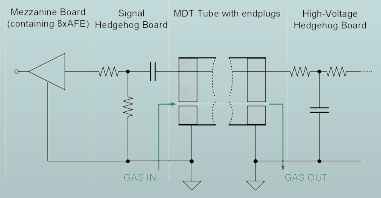
[1]*Physics Department University of Milano-Bicocca, Italy;* [2]*Max-Planck-Institute for Physics, Munich, Germany*

Abstract

An 8-channels read-out front-end for LHC ATLAS Muon-Drift-Tubes (MDT) detectors is presented (8 xAFE). The system is composed by the cascade of the analog signal processing Front-End and the Wilkinson A/D (to perform voltage-to-time conversion for time-over-threshold detection) and satisfies the critical specifications (i.e. time resolution, gain, efficiency, noise rejection) required by the Phase-2 Upgrade of the LHC. In this scenario, the overall system performances have been improved with respect to previous similar realizations in order to detect with the 8 xAFE higher energy events. The analog signal processing chain output-sensitivity is 13.8 mV/fC, while the Equivalent-Noise-Charge (ENC) is 0.6 fC (3.38 ke⁻), performing <12 ns preamplifier rise-time. These performances have been achieved, managing very high detector parasitic capacitance at the front-end input (60 pF). Each channel consumes 11mA from a single 3.3 V supply. In 0.13μm CMOS, 8 xAFE total area occupancy is 6.3 mm^2.

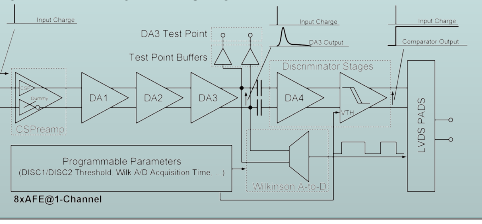
ATLAS Experiment and Muon Detection Scheme

- Recording p-p collisions at center-of-mass energies of up to 14eV
- Secondary particles detection through a shell-like structure
- Outer ATLAS shell is reserved to muons detection
- 'Mezzanine' Board contains the 8xAFE



8xAFE Channel Block Scheme

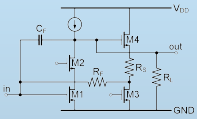
- CSPreamp and Differential Amplifiers in chain for analog input charge processing
- Discrimination Stage for arrival time input charge information
- Wilkinson ADC Stage for arrival time/total amount input charge information
- Several Programmable Parameters determine channel behavior
- Programmable Parameters are generated on-chip through a JTAG block



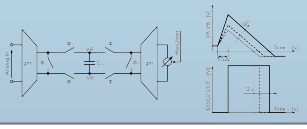
CSPreamp and Wilkinson ADC

- 60 pF Detector Capacitance Managing
- Current-to-Voltage conversion through Charge-Sensitive Premplifier (CSPreamp)
- Two identical symmetrical paths for differential signal processing
- CSPreamp circuit based on a cascode common source amplifier
- Large power is allocated to the CSPreamp input stage to improve noise and speed performance
- Voltage-to-Time conversion through Wilkinson ADC

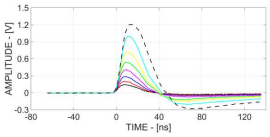
Charge-Sensitive Preamplifier Scheme



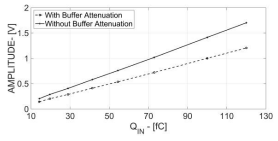
Wilkinson-ADC Operating Principle



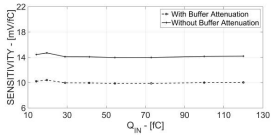
DA3 Test Point Buffers Output Signal vs. Input Charge



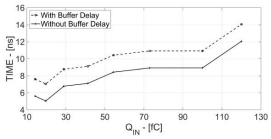
Analog Chain (CSPreamp-DA3) Voltage vs. Input Charge



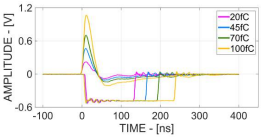
Analog Chain (CSPreamp-DA3) Sensitivity vs. Input Charge



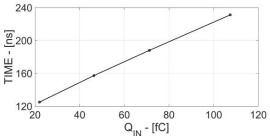
Analog Chain Peaking Time Delay vs. Input Charge



Wilkinson ADC Output Pulse/DA3 output Signal vs. Input Charge



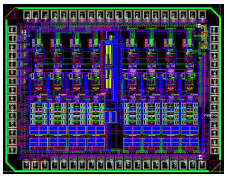
Wilkinson ADC Output Pulse Width vs. Input Charge



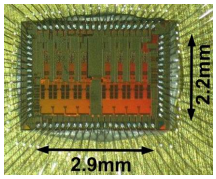
Conclusions

- Measurements phase is not completed, yet
- First measurements show good agreement with the simulations
- Other tests for different thresholds and operating conditions
- Final chip version is expected for new MDT read-out electronics of the Muon Drift Tubes in Phase-II of the HL-LHC

Layout View



Chip Photo



Performance Resume

Parameter	Value
CMOS Technology	130 nm
Total Die Area	6.38 mm^2
Supply Voltage	3.3 V
Channel Number	8
Channel Current Consumption	10 mA
Detector Parasitic Capacitance	60 pF
Input Charge Range	from 5fC to 100fC
Front-End Delay	12 ns
Front-End Sensitivity	14 mV/fC
ENC	0.6fC
SNR	15dB

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Email: *federica.resta@mib.infn.it* – Phone: +39 0264482346 – Web: *https://fisica.mib.infn.it/media/homepages/applicata/microlab/index.html*

10.2 IEEE TWEPP 2015

A New Amplifier Shaper Discriminator for the Readout of the MDT Drift tubes in the ATLAS Muon Spectrometer in IBM 130 nm Technology

Robert Richter on behalf of the ATLAS Muon collaboration

History: The ASD in Agilent 500 nm technology *)

1997 -2003 development of the chip (8-channels)
2004 production of 50k packaged chips
→ test of threshold spread among the 8 channels/ASD leads to 3 categories of quality (< 12, <16, <20 mV)
2005 → rad-tol tests up to 1 Mrad: no failures
→ the lvds-driver allows for undefined logic levels → hangups in the TDC !

2007-15 → reliable operation in „edge mode“
→ very low failure rate of ASDs

*) MDT-ASD *User's Manual* ATL-MUON-2002-003, rev. 2.1
Y. Arai et al., *ATLAS Muon Drift Tube electr.*, 2008 *JINST* **3** P09001

Functional diagram of the ASD

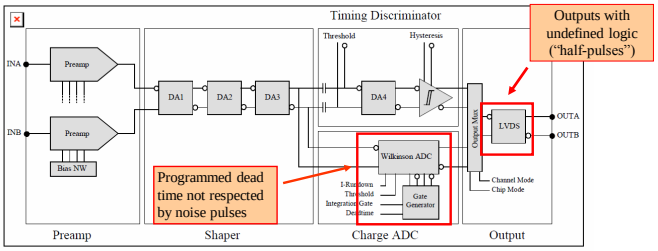


Figure 2. MDT-ASD channel block diagram

50k New ASDs needed for the Phase-II Upgrade of the Muon Spectrometer

- The Agilent technology is no more available. Go to new design in IBM 130 nm, supported by CERN
- Design aims:
  → match the "good" properties of the Agilent chip
  → fix the lvds driver problem to be able to use "pair mode", allowing a factor of 2 higher hit rates at the HL-LHC

New ASD in IBM 130 nm technology

2008 prototype of the analog part of a 4-chan. vs.
→ good matching of shape and gain (1,5%)
→ peaking time ~ 25ns instead of ~15 ns
2010 new version, incl. digital part (4 channels)
→ peaking time still > 15 ns
→ functional problems with Wilkinson AD
2013 cooperation MPI and Univ. Milano
→ modif. to reduce parasitic capacitances
→ redesign of Wilkinson and lvds driver
→ pre-tapeout tests: SPICE, PLX, LVS, PVT
2014 submission of new chip in november
2015 chips returned in febr. 2015, tests in april-september (still ongoing)

Verify chip performance

First use SPICE simulation, then, after layout, Post Layout eXtracted simulation (PLX) to check on the following parameters:

- Peaking time vs. Input charge
- Peak output volt. vs. Input charge
- Frequency response
- Transient noise

} Pre-amp, DA1, DA2, DA3

- Wilkinson discharge time vs. Input charge
- DISCR delay
- Serial interface and DACs

For all parameters:
check dependence on Process, Voltage and Temperature (PVT)

E.g.: PLX vs. SPICE simul. of peak time

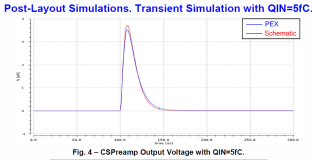
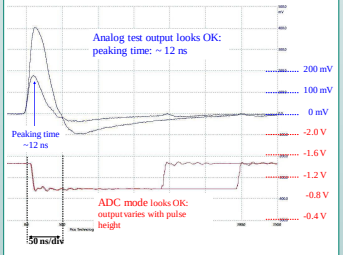


Fig. 4 – CSPreamp Output Voltage with QIN=5fC.

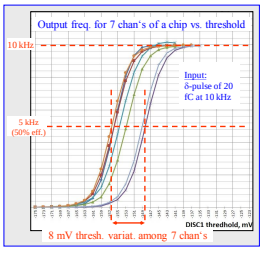
PARAMETERS	SCHEMATIC	PEX
Noise (in-Band Integrated)	547u	635.3u
Vdd1 Current Consumption	-4.173m	-4.238m
Preamp_peaking_time	8.529n	8.084n
DA1_peaking_time	9.404n	8.938n
DA3_peaking_time	10.52n	10.57n
Vpeak	3.75mV	3.5mV
PREAMP Sensitivity	0.74mV/fC	0.7mV/fC

Good match between Spice and Post-Layout Simulation (PEX), which takes e.g. stray capacitances into account.

First results testing the ASD vs. 4

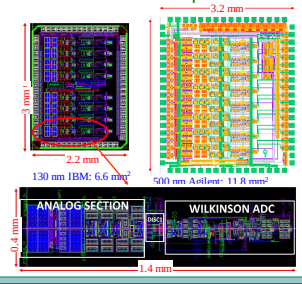


Threshold Scan of the ASD vs. 4

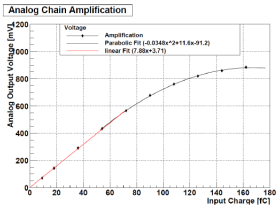


NB: ch. #7 (with analog output!) is off-scale by 30 mV

New and old Chip Layout



Range of linearity up to ~ 90 fC



Design aims for next submission:

- remove coupling from Discr. to Input
- improve ADC uniformity (pulse length vs. charge)
- improve dead-time uniformity
- fix some errors in the JTAG coding
- go for next submission in nov/dec
- go for production maturity by 2017
- chip to be used for new MDT readout electronics of the Muon Drift Tubes in Phase-II of the HL-LHC

Contact: richterr@mpp.mpg.de Sept 2015

Max-Planck-Institut für Physik
Föhringer Ring 6
80805 Munich, Germany

10.3 IEEE ICECS 2015

IC-PIX28:
a 28 nm read-out channel for pixel detector

F. Resta, M. De Matteis, G. Rota, A. Pezzotta, A. Pipino and A. Baschirotto
Physics Department University of Milano-Bicocca, Italy

Abstract

An Integrated Chip prototype for PIXel read-out, named IC-PIX28 and designed in 28nm CMOS technology, is here presented. The chip features a single channel including a cascade of a Charge-Sensitive-Amplifier (CSA) and a comparator, performing a Time-over-Threshold (ToT) operation. The IC-PIX28 comparator can operate with thresholds ≤ 3 mV, generated on-chip starting from an off-chip reference voltage. A few number of transistors allows processing an input charge within 0.1 fC $\div$ 5 fC range. With the minimum input charge, the CSA output peak voltage is 4.6 mV reached in 11 ns. In this condition, 44 mV/fC sensitivity and 0.029 fC (180 e^-) Equivalent-Noise-Charge (ENC) are achieved with 4.67 µA current consumption and 0.07 mm^2 area occupancy.

ScalTech28: INFN Project

- Integrated Circuits for High-Energy Physics experiments
  - Total Ionizing Dose (TID) up to 1Grad in 10 years
  - Large number of channels
- Present or under-development electronics could fail
- Low-Power and Rad-Hard circuits are needed
- CMOS 28nm
  - Bulk Technology
  - 0.9 V Supply Voltage
  - V_{DD}/V_{TH} ratio Reduction and
  - Output Swing Reduction
  - Transistor in subthreshold

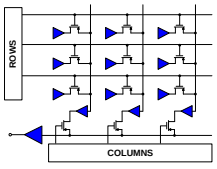
Read-Out Systems for Pixel

- Applications:
  - Physics Experiments
  - Photography
- CMOS Active Pixel Sensors (APSs)
  - Photon to Electron & Charge to Voltage conversions
  - Sensor and read-out electronic on-chip
    - * More compatibility
    - * More accuracy
    - * More complex
- Input Charge ≤ 6 fC
- Conventional Pixel Structures:
  - Matrix of n-rows and m-columns
  - Higher pixel cells to increase the resolution
  - Pixel cell smaller, low power and faster

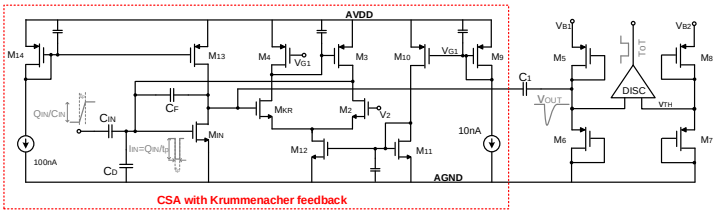
IC-PIX28: PIXel read-out

- Charge Sensitive Amplifier (CSA)
  - Only M_{IN} (common source stage) with R_F and C_F in feedback
  - Reduced Noise Contributions
  - Reduced Current Consumption
  - $V_{IN} = Q_{IN} / C_{IN}$, $I_{IN} = Q_{IN}/t_F$, gm_{IN} of 51 µA/V
- Krummenacher Feedback
  - $gm_{KR} = 800$ nA/V $\Longrightarrow R_F = 1.25$ MΩ
  - Fixed CSA input-output operating-point
  - Compensation of detector leakage current
- Discriminator Stage

PIXEL MATRIX

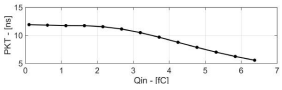


CHANNEL BLOCK SCHEME

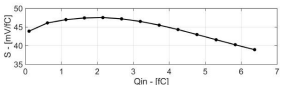


CSA with Krummenacher feedback

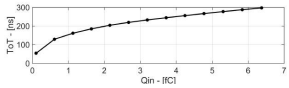
PeaKing Time delay vs. Input Charge



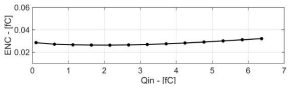
Sensitivity vs. Input Charge



Time of Threshold width vs. Input Charge

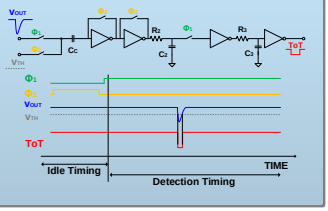


Equivalent Noise Charge vs. Input Charge

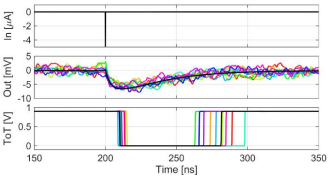


Discriminator Stage

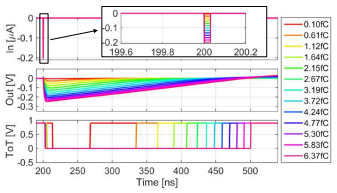
- Discriminator Stage based on inverter in chained
- Time-of-Threshold (ToT) operation in digital way
- RC nets for noise filtering
- Idle Timing for threshold loading



Input Current, CSA and DISC Output WITH and WITHOUT NOISE



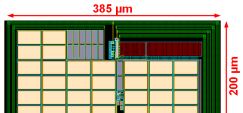
Input Current, CSA and DISC Output vs. Input Charge



Performance Resume

Parameter	[6]	[1]	IC-PIX28
CMOS Technology	130 nm	65 nm	28 nm
Supply Voltage	1.2 V	1.2 V	0.9 V
Channel Power Consumption	200 µW	6 µW	4.2 µW
Equivalent Noise Charge	250 e^-	200 e^-	180 e^-
Charge Sensitivity	80 mV/fC	40 mV/fC	44 mV/fC
Front-End Delay	25 ns	25 ns	11 ns
Detector Parasitic Capacitance	200 fF	100 fF	100 fF

Layout View



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Email: *federica.resta@mib.infn.it* – Phone: +39 0264482346 – Web: *https://fisica.mib.infn.it/mediaHomepages/applicataMicrolab/index.html*

10.4 IEEE SENSORS 2016

IEEE SENSORS 2016
ORLANDO, FL, USA | OCT 30 - NOV 2, 2016

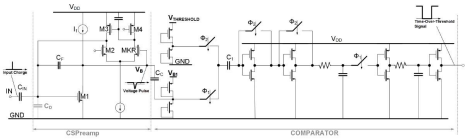
SCALTECH 28 — INFN — UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA

A 4.3µW 28nm-CMOS Pixel Front-End with Switched Inverter-Based Comparator

F. Resta, A. Pipino, A. Pezzotta, M. De Matteis, M. Croce, A. Baschirotto

Electrical characterization of a read-out front-end for high luminosity pixel detectors in 28nm bulk-CMOS technology is hereby presented. The proposed integrated circuit includes the cascade of ***a low-noise preamplifier stage*** and ***a switched-capacitor inverter-based comparator***. The selected technology process shows significant advantages in terms of radiation hardness, faster/low-power digital signal processing and whole chip area reduction.
The circuit has been realized within ScalTech28 project research of Milano Bicocca INFN.

CHANNEL BLOCK SCHEME



BULK CMOS 28nm TECHNOLOGY

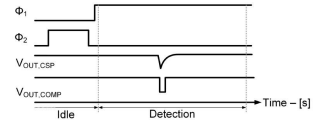
- V_{DD}/V_{TH} Ratio Reduction (0.9 V_{DD})
- Output Swing Reduction
- Transistor in Sub-Threshold
- More PVT Variations
- Layout Parasitic Effects not negligible
- Radiation Hardness (TID up to 1Grad)

CHARGE SENSITIVE PREAMPLIFIER

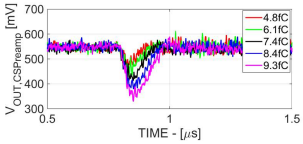
- Only M_{IN} (common source stage) with R_F and C_F in feedback
- Reduced Noise Contribution & Current Consumption
- Krummenacher Feedback
  - o Gm_{KR}=800nA/V → RF=1.25MΩ @ 60nA
  - o Fixed CSPreamp Input-output operating point (300mV_{DC} & 550mV_{DC})

COMPARATOR

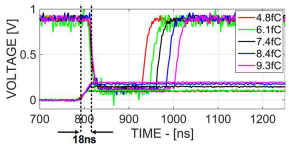
- Switched Inverter-Based Comparator → 4 Inverters in chained
- Digital Time-over-Threshold (ToT)
  - → Arrival Time Information
  - → Amount of Input Charge Information
- Idle Timing for threshold loading



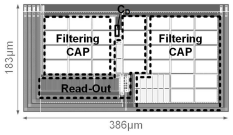
CSPREAMP OUTPUT VS. INPUT CHARGE



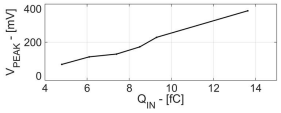
COMPARATOR OUTPUT VS. INPUT CHARGE



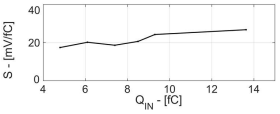
LAYOUT VIEW



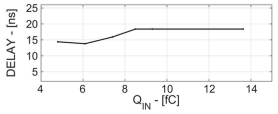
PEAKING VOLTAGE VS. INPUT CHARGE



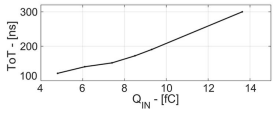
SENSITIVITY VS. INPUT CHARGE



COMPARATOR DELAY VS. INPUT CHARGE



TIME-OVER-THRESHOLD VS. INPUT CHARGE



PERFORMANCE RESUME

Parameter	Value
CMOS Technology	28nm
Supply Voltage	0.9V
Die Size	0.02mm²
Channle Power Consumption	4.3µW
Maximum Peak Voltage	365mV
Delay range	13.8ns–18.4ns
Time-over-Threshold range	121ns–300ns
Charge Sensitivity	20mV/fC
Detector Parasitic Capacitance	100fF
SNR@Minimum Input Charge	41dB
SNR@Maximum Input Charge	54dB

Part VI

Conclusions

11
Conclusions

This thesis is dedicated on the read-out front-ends for High Energy Physics (HEP) experiments. These topologies of the circuits have been implemented for many years with discrete components. Instead, in the last years, the integrated architectures are developed demonstrating reliability, robustness, reproducibility of results, area and power optimization. Typically, systems with more channels have been implemented and CMOS technology guarantees a good level of integration without loss in the performance. Integrated electronics changes with the application and working environment while most of the HEP experiments are held inside the LHC (Large Hadron Collider) at CERN (Geneva). The presence of very high radiation levels constitutes the main reason of performance degradation and failure events. Thus, it has been extremely important to study the radiation-induced effects in order to face radiation and design radiation-hard block.

Starting from this consideration, the core of this thesis concerned the development of two integrated circuits for HEP experiments. The first, named Octal MDT-ASD chip, is more complex and will be used in the HL-LHC Phase II Upgrade for muons detection. The second, named IC-PIX28, is a system with few functionalities thought to investigate on radiation hardness of the CMOS ultra scaled technology as Bulk CMOS 28 nm.

Octal MDT-ASD chip has been realized in IBM 130 nm in collaboration of Max Planck Institute (Munich). This is the Version 4 (V4) and aims to replace the chip currently used in 500 nm technology. Electronics more powerful is required to correctly work in presence of High Luminosity levels. Octal MDT-ASD V4 chip has been interfaced with the 'Mezzanine Board' in order to have a complete characterization in time and frequency domains. The most important performance have been compared (see Table 11.1) with the previous implementation [19]. The Octal MDT-ASD V4 power consumption is reduced of about 9 % without degrading sensitivity (charge-to-voltage conversion gain) and noise performance. In particular, the channel features an higher sensitivity at the Comparator input (14 mV/fC vs. 8.9 mV/fC), a lower ENC (0.6 fC instead of 1 fC), an higher SNR (about 4.1 dB higher than in previous design) and a lower peaking time delay (12 ns instead of 15 ns). These measured results demonstrate that the new design has a major sensing capability, a reduction of the bit error probability, an enhancement of the signal quality and a faster response.

Octal MDT-ASD V4 measurements were fundamental to investigate on issues not observed during the design but they were important to fix before chip replacement. For this purpose,

- the CSPreamp has been re-designed to improve the noise supply/ground rejection

- the BFMOAT layout layer has been introduce to improve substrate isolation limiting the analog and digital couplings
- the Channel#7 *BUFFER* is moved to near DA_3 output avoiding performance degradation and channels mismatch
- the Channel#7 *BUFFER* switch off has been introduced.

Octal MDT-ASD V5 aims to optimize the version 4 with a small increment of the area and the same power budget. Measurements of this chip are taking place in these weeks but the preliminary results seems to be encouraging.

At the end of this thesis, IC-PIX28 chip design and realization have been described. This the first prototype realized in Bulk CMOS 28 nm technology. In fact a single channel has been integrated and tested. The summary of the most important performance are reported in Table 11.2. Thanks to sub-threshold bias region of input transistor, the system performs around 30 mV/fC of sensitivity with 4.3 µW of power consumption and 0.9 V of supply voltage. The input charge range used for IC-PIX28 characterization, is 4 fC-20 fC and it is bound to measurements setup. Then 1 Grad-TID radiation exposure, the system detects charges from 7 fC and features smaller gain, slower times response and higher noise. Obviously, the system is strongly affected by radiation but, starting from this measurements, a new version will be designed able to limit performance degradation and to manage leakage current in the order of few tens nA.

Parameter	*Octal MDT-ASD V4*	*[19]*
CMOS Tech.	130 nm	500 nm
Total Die Area	6.38 mm^2	11.9 mm^2
Supply Voltage	3.3 V	3.3 V
Channel Current Consumption	10 mA	11 mA
Detector Parasitic Cap.	60 pF	60 pF
Shaping Function	Bipolar	Bipolar
Input Charge Range	5 fC - 100 fC	5 fC - 100 fC
Front-End Delay at 100 fC-Q_{IN}	12 ns	$\sim$15 ns
Front-End Sensitivity	14 mV/fC	8.9 mV/fC
ENC	0.6 fC	1 fC
SNR at minimum input charge	15 dB	10.9 dB

Table 11.1: MDT-ASD State-of-the-Art Comparison

Parameter	*PreRad Value*	*PostRad Value*
Input Charge Range	4 fC - 20 fC	4 fC - 20 fC
CSPreamp Min Peak Voltage	122.9 mV @ 4 fC	161.5 mV @ 4 fC
CSPreamp Max Peak Voltage	482.9 mV @ 20 fC	334 mV @ 20 fC
CSPreamp Min Peak Voltage	122.9 mV @ 4 fC	161.5 mV @ 4 fC
Average Sensitivity	30 mV/fC	22 mV/fC
Maximum PTD	31 ns	96 ns
Maximum ToT	258 ns @ 4 fC	1849 ns @ 7 fC
Minimum ToT	763 ns @ 20 fC	2717 ns @ 20 fC
Comparator Threshold	10 mV	10 mV
Maximum Comparator Delay	5 ns	20 ns

Table 11.2: Summary of IC-PIX28 Performance

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