UNIVERSITÀ DEGLI STUDI DI MILANO-BICOCCA
Dipartimento di Fisica "G. Occhialini"

Tesi di Dottorato in Fisica e Astronomia
Curriculum: Tecnologie Fisiche
Ciclo XXIX

Design of Analog Circuits in 28nm CMOS Technology for Physics Applications

Autore: ***Alessandra Pipino***

Tutor: Prof. Massimo Gervasi
Supervisore: Prof. Andrea Baschirotto
Coordinatore: prof.ssa Marta Calvi

Anno Accademico *2015/2016*

To Fabrizio

Abstract

The exponential trend of the complementary metal-oxide-semiconductor (CMOS) technologies predicted by Moore's law has been successfully demonstrated over the last three decades. A constant downscaling of CMOS technologies has been developed, in order to comply with requirements on speed, complexity, circuit density and power consumption of advanced high performance digital applications.

With the arrival of nanoscale (sub-100nm) CMOS technologies, digital performance improve further, but many new challenges have been introduced for analog designers. In fact, for the digital circuits CMOS scaling-down leads to several benefits: speed improvement, reduced power consumption, high integration and complexity level. The analog circuits, instead, strongly suffers from the ScalTech trend, because the MOS behavior dramatically changes through the different technological nodes. Especially for the ultra-scaled nodes, second order effects, previously negligible, become very important and start to be dominant, affecting the transistors performance. For instance, lower intrinsic DC-gain, reduced dynamic range, operating point issues and larger parameter variability are some of the problems due to the scaling of physical (length, oxide thickness, etc.) and electrical (supply voltage) parameters. Analog designers have to manage these problems at different phases of the design, circuital and layout, in order to satisfy the market high-performance requirements.

Despite that, the design of analog circuit in sub-nm technologies is mandatory in some cases or can be even strategical in others. For example, in mainly mixed-signal systems, the read-out electronic requires high frequency performance, so the choice of deep submicron technology is mandatory, also for the analog part. Other types of applications are the high-energy physics experiments, where read-out circuits are exposed to very high radiation levels with consequent performance degradation. Since radiation damage is proportional to gate oxide volume, smaller devices exhibit lower radiation detriment. It has been demonstrated in fact, that 28nm CMOS technology devices are capable to sustain 1Grad-TID exposure, not possible with previous technologies.

In this thesis, the main challenges in ultra-scaled technologies are analysed and then integrated circuits designed in 28nm CMOS technology are presented. The aim of this work is to show the design approach and several solutions to be applied in order to outermost the limits of silicon scaling, address the major scaling problems and guarantee the required performance.

The first circuit design, presented in the second chapter and integrated in 28nm CMOS technology, is a Fast-Tracker front-end (FTfe) for charge detection. The read-out system has been developed starting from the main specifications and circuital solutions already adopted for muon detection in ATLAS experiment. The proposed front-end is able to detect an event and soon after to reset the system in order to make the read-out front-end already available for the following events, avoiding long dead times. Moreover, exploiting a two thresholds crossing solution, the required

information can be collected, simplifying the architecture compared to the current.

The second circuit design presented and always integrated in 28nm CMOS technology, is a Chopper instrumentation amplifier. Instrumentation amplifiers are the key building blocks in sensor and monitoring applications, where they are used to sense and amplify usually very small (sub-mV) and low frequency signals. For this reason it is important to reduce or eliminate the input offset and flicker noise introduced by the amplifier itself, superimposing the main signal to be detected. The proposed amplifier use the classical modulation technique, called chopper, in order to meet the low offset and low flicker noise requirements. The use of an ultra-scaled technology ensures the amplifier employment in every mixed-signal system, with advantages also in terms of charge injection.

Contents

List of Figures

List of Tables

Introduction

In this thesis, the main key challenges in ultra-scaled technologies are analysed, and then integrated circuits designed in 28nm CMOS technology are presented.

The first chapter focuses on trends in device characteristics and how they influence the performance of nanoscale CMOS technologies circuits.

The second chapter shows the design in 28nm CMOS technology of a Fast Tracker Front-End (FTFE) for charge detection, starting from the requirements and the circuital solutions actually employed for ATLAS MDT detectors read-out electronic. The purpose of the project was to implement an efficient system, able to detect consecutive input events, avoiding long dead time e signal losses. The specific architecture is analysed and the resulting performance are shown.

In the third chapter a Chopper Instrumentation Amplifier designed in 28nm CMOS technology is presented. It is an amplifier characterized by the use of a modulation technique, called chopper, in order to meet the low offset and low flicker noise requirements, important in sensors and monitoring applications. In particular the three-stage operational amplifier has been designed to work in sub-threshold region, in order to address the scaling problems. After the architecture and the design procedure description, the results of the integrated prototype are shown.

At the end some conclusions are drawn.

Chapter 1

Device Trends of Technological Scaling-Down

1.1 Introduction

Nanometer CMOS technologies play a key role for the improvement of the mixed-signal systems, thanks to the high integration level of analog and digital circuits in the same die area. Even if digital signal processing is replacing some analog operations, the mixed-signal systems require anyway an analog front-end able to manage and convert the external signals. This means that the weak analog performance but also the advantages of the ultra-scaled technologies must be managed. In particular, the scaling-down of physical and electrical parameters leads to improvements for digital circuits on one side, while a lot of design issues for analog circuits on the other side. To cope with market requirements but also the analog design limits, advanced lithography techniques, new material like high-K/metal gate (HKMG), and new devices, as finfet or thinfet, have been introduced [3][4][5][6].

In the following subsections, the main trends in device characteristics due to the technological scaling-down will be analysed. Their influence on the design of nanoscale CMOS circuits will be shown, from both circuital and layout point of view.

1.2 Supply Voltage

Figure 1.1 shows that standard supply voltage V_{DD} of the analog devices decreases with the minimum transistor channel length [7]. Low supply voltage is a necessity in scaled technologies, in order to limit the channel electric field to a maximum acceptable value. In fact, the high intensity of the inside-silicon electric fields due to the smaller channel length can cause gate oxide and drain-to-source breakdown events, with consequent reliability problems [8]. As shown in Fig. 1.1, supply voltage for nanoscale technologies has reached almost the limit, with a value for the 28nm technological node of 0.9 V. Though this trend can be positive for digital power

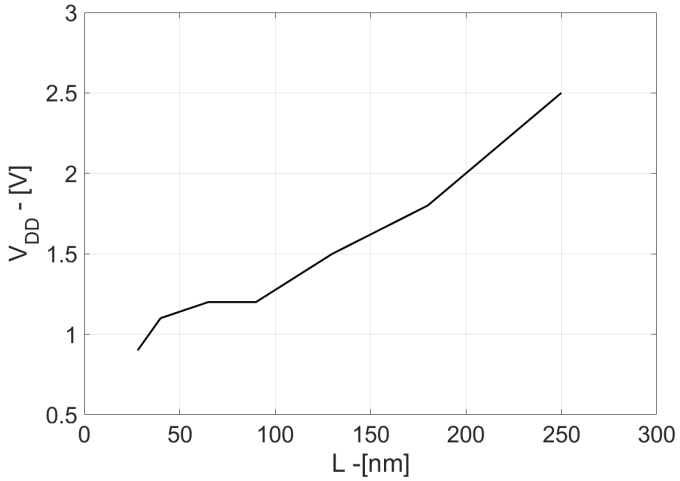


Figure 1.1: Supply variation with transistor length.

performance, it is not entirely true for the analog counterpart.

Lower supply voltage in digital CMOS circuits results in lower power consumption, since it depends on three components:

- the leakage current due to the reverse biased diodes formed between the substrate, the well and the diffusion regions of the transistors;
- the short circuit current from the supply voltage to ground when PMOS and NMOS transistors are simultaneously on for a short transition period;
- switching current due to the charging and discharging of the load capacitances.

The last component is the dominant one and the related dynamic power consumption $\mathrm{P_{dig}}$ is given by:

$$\mathrm{P_{dig}} = \mathrm{f_t} \cdot \mathrm{C} \cdot \mathrm{V_{DD}^2} \tag{1.1}$$

where $\mathrm{f_t}$ is the operation frequency and C is the capacitive load. From Eq. (1.1), digital power consumption reduces in scaled technologies, improving power performance in mixed-signal circuits.

On the contrary, for analog circuits the situation is very different, since lower supply voltage does not lead automatically to lower power consumption. The main reason is the reduced Signal-to-Noise ratio (SNR) at constant noise power, due to the smaller output signal swing. Let us consider one of the most simple single stage amplifier, i.e the common source circuit (Fig. 1.2). The maximum allowable output swing $\mathrm{V_{OUT,rms}}$ is:

$$\mathrm{V_{OUT,rms}} = \mathrm{V_{DD}} - 2\mathrm{V_{OV}} \tag{1.2}$$

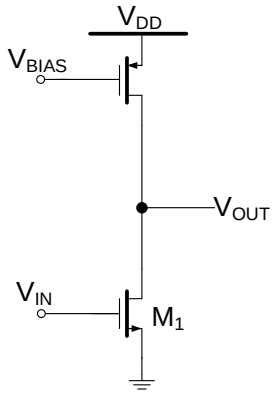


Figure 1.2: Common source circuit.

where $\mathrm{V_{OV}}$ is the transistor overdrive voltage, assumed equal for NMOS and PMOS devices. Considering only the $\mathrm{M_1}$ noise contribution and assuming dominant the thermal noise, the output in-band integrated noise is approximately given by:

$$\mathrm{V_{N,rms}^2} = \left(\frac{2}{3}4\mathrm{kT}\frac{1}{\mathrm{g_{m,M1}}}\right)\mathrm{A_V^2 BW} \tag{1.3}$$

where k is the Boltzmann constant, T is temperature, $\mathrm{g_{m,M1}}$ is the transistor $\mathrm{M_1}$ transconductance, $\mathrm{A_V}$ is the amplifier DC-gain and BW is the -3dB bandwidth. The SNR can be written as:

$$\mathrm{SNR} = \frac{\mathrm{V_{OUT,rms}^2}}{\mathrm{V_{N,rms}^2}} = \frac{\left(\mathrm{V_{DD}} - 2\mathrm{V_{OV}}\right)^2}{\left(\frac{2}{3}4\mathrm{kT}\frac{1}{\mathrm{g_{m,M1}}}\right)\mathrm{A_V^2 BW}} = \mathrm{I_1}\frac{\left(\mathrm{V_{DD}} - 2\mathrm{V_{OV}}\right)^2}{\mathrm{k_n}} \tag{1.4}$$

where $\mathrm{I_1}$ is the $\mathrm{M_1}$ drain-source current. As a result, at constant gain and bandwidth, the SNR is proportional to $\mathrm{I_1}$ by $\mathrm{V_{DD}^2}$. Lower is $\mathrm{V_{DD}}$, lower is the SNR, or alternatively in order to maintain the same SNR, when $\mathrm{V_{DD}}$ decreases, current consumption $\mathrm{I_1}$ must be increased, with larger power consumption. A numerical example can better highlight this problem, supposing to compare the 180nm and the 28nm technological nodes (assuming for simplicity that $\mathrm{k_n}$ is equal in both cases):

$$\mathrm{SNR_{180nm}} = \frac{\mathrm{I_1}}{\mathrm{k_n}}\left(1.8 - 2\cdot 0.2\right)^2 = 1.96\frac{\mathrm{I_1}}{\mathrm{k_n}} \tag{1.5}$$

$$\mathrm{SNR_{28nm}} = \frac{\mathrm{I_1}}{\mathrm{k_n}}\left(0.9 - 2\cdot 0.05\right)^2 = 0.64\frac{\mathrm{I_1}}{\mathrm{k_n}} \tag{1.6}$$

Notice that with the same current consumption, the SNR is 3 times lower in 28nm technology, or alternately the current should be 3 times higher than the 180nm case to obtain the same SNR. (The assumption of equal $\mathrm{k_n}$ parameter is not misleading, since it increases in scaled technologies, proving more the problem).

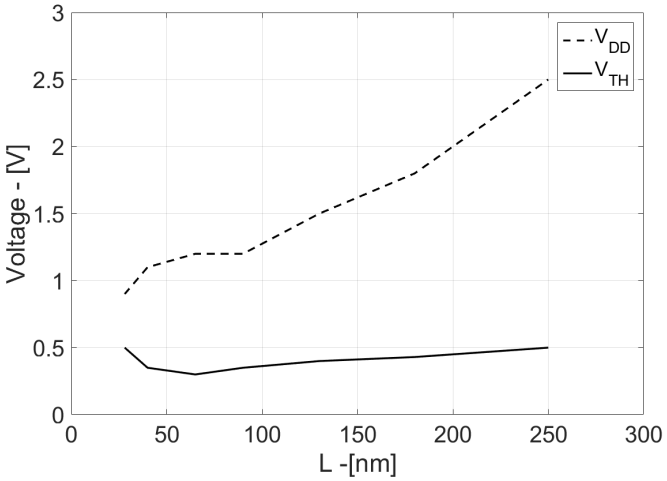


Figure 1.3: Threshold voltage variation with transistor length.

1.3 Threshold Voltage

As for supply voltage, technological scaling-down leads to a reduction of the transistor threshold voltage V_{TH} too, in order to ensure a high drive current capability. This trend is reported in Fig. 1.3. However, V_{DD} scales faster than V_{TH} and V_{TH} even approaches V_{DD}, inverting the decreasing trend of the last years, with a reduction of the V_{DD}/V_{TH} ratio. This happens in order to maintain low the transistors turn-off leakage current I_{off}, which increases with scaling-down process. This I_{off} current is mainly due to a subthreshold leakage [8] current which occurs when the gate voltage is lower than V_{TH} and can be written as follows:

$$I_{sub} = I_0 e^{-\frac{V_{TH}}{nV_t}} \left(1 - e^{-\frac{V}{V_t}}\right) \tag{1.7}$$

where I_0 is a technological dependent constant, n is the subthreshold slope, $V_t = kT/q$ is the thermal voltage. What can be deduced from (1.7) is that V_{TH} cannot be decreased significantly, but a minimum value is required, in order to avoid high leakage current.

As a results, while the V_{DD}/V_{TH} ratio in 0.25 µm CMOS technology was about 6, for 28 nm is about 2. This strong reduction makes critical the analog circuits design and leads to operating point and dynamic range issues:

- the overdrive voltage results to be small and less headroom is left to the output signals, with a dynamic range reduction;
- MOS transistors biasing in strong/moderate region becomes very difficult, so weak inversion region is an inevitable choice, where transistors current mismatch is critical and open loop linearity degraded because of the exponential characteristic;

- there is no margin for cascode topologies.

1.4 PVT Variations

As technology scales below 65 nm, manufactured dies began to exhibit a substantial spread of device performance across die and within each die due to Process, Voltage and Temperature (PVT) variations.

Process variation accounts for deviations in the semiconductor fabrication process. Variations in the process parameters can be impurity concentration densities, oxide thickness and diffusion depths, caused by non-uniform conditions during depositions and/or during diffusions of the impurities. Beside, variations in the device dimensions W and L can occur, mainly resulting from the limited resolution of the photo-lithographic process. Consequently, transistor parameters, such as threshold voltage, vary from the nominal value.

Also supply voltage can vary from the established ideal value during day-to-day operation, leading to different currents and circuital operating conditions, which must be taken into account during the design process.

Finally, temperature variation is an important aspect during circuit design. When a chip is operating, the temperature can vary throughout the chip and this is due to the power dissipation in the MOS-transistors, according also to the chip application. Of course, transistors characteristics are not the same at different temperatures and this trend seems to be worse in ultra-scaled technology.

During the analog circuits design, worst-case analysis are an important tool to analyse all these problems and to ensure expected performance even in the worst-case scenarios. The typical PVT cases to be considered are nominal, fast and slow for transistors process, $\pm 10\%$ of the supply voltage and $-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$ and $120\,^{\circ}\mathrm{C}$ for temperature. Table 1.1 gives the $\mathrm{V_{TH}}$ value in 28 nm CMOS technology for a NMOS device (W=300 nm, L=30 nm and $\mathrm{V_{GS}}$=600 mV) versus process, temperature and supply voltage variations. The nominal value of $\mathrm{V_{TH}}$ is 538.5 mV, but it changes with PVT from 389.1 mV to 677 mV, i.e. ± 150 mV ($\pm 25\%$), which is not negligible.

1.5 Mismatch Variations

The threshold voltage and the other transistor parameters are strongly influenced by any fluctuation or variation on MOS properties. This variations are classified into random and systematic ones [9]. Random variations can cause differences between identically designed and adjacent devices; it can be determined as the standard deviation of the differences for two closely spaced and identical devices. Systematic variations cause identical devices with the same layout, but not necessarily close to each other, to behave differently and to have a mean value difference of some parameters.

In deep sub-μm designs, especially 28 nm technology and lower, random local variations have become a significant part of the total variation and the related mismatch

		0.8 V	0.9 V	1 V
tt	**-40 °C**	582.2 mV	576.6 mV	571 mV
	27 °C	544.2 mV	538.5 mV	533 mV
	120 °C	491.4 mV	485.7 mV	480.1 mV
ff	**-40 °C**	484 mV	477.9 mV	471.8 mV
	27 °C	449.5 mV	443.3 mV	437.2 mV
	120 °C	401.5 mV	395.3 mV	389.1 mV
fs	**-40 °C**	508.8 mV	503.2 mV	497.6 mV
	27 °C	473.3 mV	467.6 mV	462.1 mV
	120 °C	424 mV	418.3 mV	412.7 mV
sf	**-40 °C**	656.4 mV	650.8 mV	645.2 mV
	27 °C	615.8 mV	610.2 mV	604.2 mV
	120 °C	559.5 mV	553.8 mV	548.2 mV
ss	**-40 °C**	677 mV	671.9 mV	666.8 mV
	27 °C	635.7 mV	630.6 mV	625.5 mV
	120 °C	578.5 mV	573.3 mV	568.2 mV

Table 1.1: PVT variations of V_{TH} in 28nm CMOS technology (V_{DD}=0.8, 0.9, 1 V, Temp=-40, 27, 120 °C, Process=tt, ff, fs, sf, ss).

decreases with the W and L scaling-down. Typical contributions [10][11][12][13] to the random events are:

- gate length variation
- line-edge roughness
- line width roughness
- random dopant fluctuations
- gate dielectric thickness variation
- defects and traps in the gate dielectric and gate dielectric-silicon interface
- patterning and proximity effects
- transistor strain
- polishing effects for the gate and Shallow Trench Isolation (STI)
- implant and annealing effects.

These random local events introduce statistical variation that can be analysed only in Monte Carlo simulations. In general random mismatch is inversely proportional to the device's dimension; the simple linear model is [14]:

$$\sigma^2 = \frac{A^2}{WL} + B + S^2 D_x^2 \tag{1.8}$$

where:

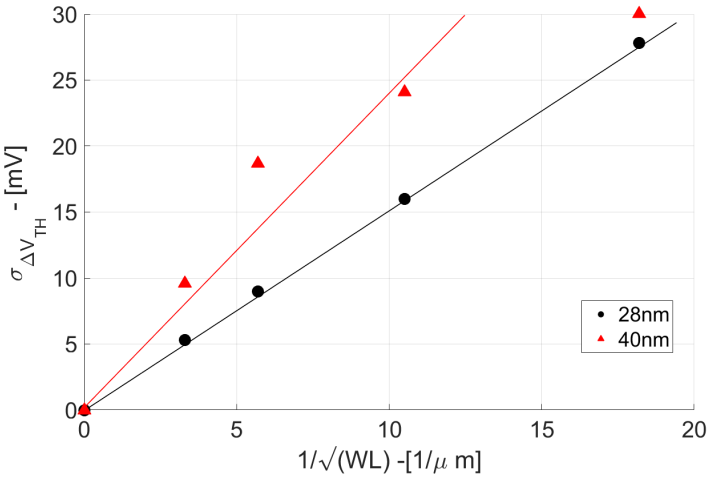


Figure 1.4: V_{TH} mismatch comparison between 40 nm and 28 nm technologies.

- A is the mismatch parameter depending on the technology, approximately depending on the MOS oxide thickness T_{ox};
- B is an offset of measurement (possibly low as possible);
- W and L are width and length of the device;
- S is the sensitivity parameter for different spaces between devices;
- D is the space between the two devices.

Neglecting the mismatch sensitivity to space devices, the simpler most used relationship is:

$$\sigma^2 = \frac{A^2}{WL} \tag{1.9}$$

For example, for threshold voltage the standard deviation results to be:

$$\sigma_{\Delta V_{TH}} = \frac{A_{\Delta V_{TH}}}{\sqrt{WL}} \tag{1.10}$$

This means that for the same device area, scaled technology features a better matching. As an example, in Fig. 1.4, the V_{TH} standard deviation is plotted versus $1/\sqrt{WL}$ for 40 nm and 28 nm technologies, obtained from an NMOS in saturation region with minimum length. The slope of the resulting lines corresponds to the terms $A_{\Delta V_{TH}}$ and it results to be 3.8 mV·µm and 1.54 mV·µm for 40 nm and 28 nm nodes, respectively. Thus, all the circuits whose power consumption is limited by the device matching can exploit the improved scaled technologies matching performance. However the V_{TH}

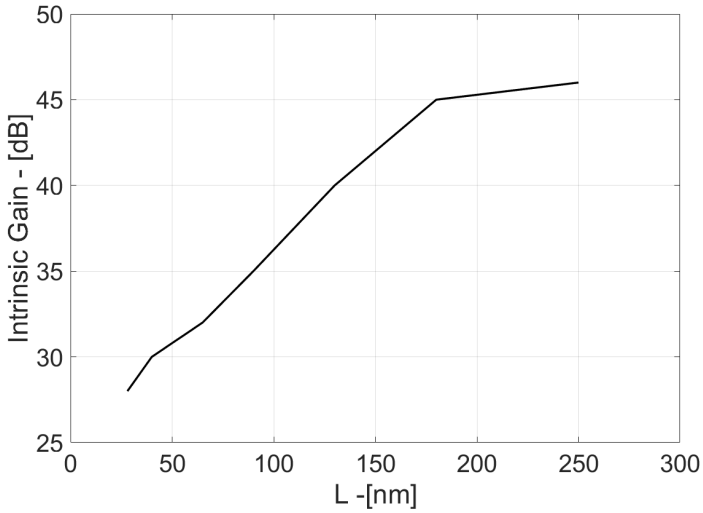


Figure 1.5: MOS intrinsic gain vs. transistor length (Voltage gain @ 5xL_{min}).

value is also affected by other layout dimension effects (LDE), typically negligible in larger devices, but severe and dominant in scaled technologies. The main LDE effects that introduce systematic mismatch are Well Proximity Effect (WPE), Poly Spacing Effect (PSE), OD Spacing Effect (OSE), Shallow Trench Isolation (STI) [12], which can be evaluated only through post-layout simulations, since they depends on the layout design.

1.6 Intrinsic Gain Reduction

Degradation of the transistors intrinsic gain, defined as the product $g_m r_{ds}$, where r_{ds} is the Mosfet output resistance, is one of the major challenges in the design of analog circuits in scaled technologies. In order to minimize the short channel effects and the drain induced barrier lowering (DIBL), the doping density close to drain and source wells is increased. In this way, leakage current during the switching phase in digital circuits is decreased, saving the switching capability [15]. However, the transistor output resistance strongly reduces and the resulting effect is a reduction of the gain. Maintaining the intrinsic gain across technology nodes is not feasible, as illustrated in Fig. 1.5. The intrinsic gain decreases of about 30 dB from 250 nm to 28 nm technology.

Analog designers have to use higher channel length to recover output resistance and mitigate this effect, otherwise they are forced to distribute horizontally the gain, since cascode topologies are difficult to bias, increasing complexity and number of poles.

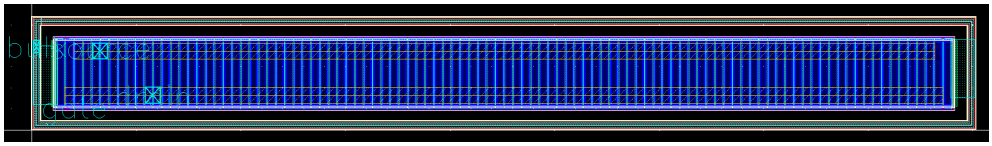


Figure 1.6: Example of NMOS layout in 28nm technology (100 fingers of 3 µm/1 µm to obtain a total NMOS of 300 µm/1 µm).

1.7 Restrictive Design Rules

Starting from the 28 nm technological node, the design rules are becoming much more complex in terms of device usage, density requirements and physical design limits. These restrictions have a significant impact on device selection as well as physical implementation of the circuit layout.

Double-pattern lithography and metal gate technologies have led to strict design rules, because poly and metal density must be kept very uniform across the die in order to fabricate the minimum channel length devices in a reliable way. Beside limits on the minimum and maximum poly density, there are also rules for the maximum poly area per device finger. This rules are challenging for digital circuits, but especially for analog designs, where large devices are used in order to improve matching or large decoupling capacitances for filtering are employed. As a consequence, large area devices must be fragmented to satisfy design rules, with an increase of analog circuits area in comparison with previous technological nodes.

Another requirement of the double-pattern lithography is that the gate orientation of all the devices must be uniform across the whole wafer, circuits rotation is strictly prohibited.

About devices geometries, other restrictions are: maximum transistor gate area, maximum transistor width W and length L and also a limited set of transistor W and L available. For example in 28 nm CMOS technology the maximum W and L for a single device finger are 3 µm and 1 µm, respectively. All this restrictions impose the use of a combination of smaller series and parallel transistors to create the desired transistor, as shown in Fig. 1.6 .

Moreover scaled technologies are characterized by a larger metal sheet resistance, up to 0.45 Ω/sq for the low metal layers in 28 nm technology, respect to 0.08 Ω/sq of old technologies as 180 nm and 250 nm. As a consequence, a careful approach to layout must be used, avoiding long and small metal paths, preferring the use of higher metal layers for long distances.

1.8 Intrinsic Transition Frequency

Sub-100 nm CMOS technologies are characterized by a MOS transistor frequency significantly higher than the past, entering the hundreds of GHz domain. Figure 1.7 shows the MOS transition frequency f_T trend vs. the minimum channel length [15]. The gate length reduction leads to a f_T above 300 GHz for 28 nm technology. To demonstrate the implication of an intrinsic speed increase with scaling-down, let

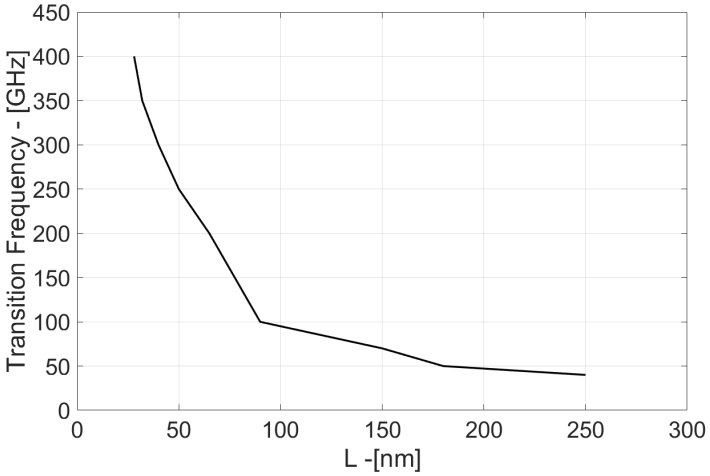


Figure 1.7: MOS transition frequency vs transistor length.

consider the approximate expression of the maximum operating frequency $\mathrm{f_{T,max}}$ of an amplifier:

$$\mathrm{f_{T,max}} = \frac{\mathrm{g_m}}{2\pi\left(\mathrm{C_{gs}} + \mathrm{C_{gd}} + \mathrm{C_{db}}\right)} \tag{1.11}$$

where $\mathrm{g_m}$ is the transistor transconductance, $\mathrm{C_{gs}}$ is the gate-source capacitance, $\mathrm{C_{gd}}$ is the gate-drain capacitance and $\mathrm{C_{db}}$ is the drain-bulk capacitance. As technologies are scaled-down, $\mathrm{g_m}$ tends to be larger while the capacitances reduce proportional to L. The result is an improved bandwidth capability, that for analog circuits design enables the implementation, for example, of broadband filters and amplifiers. However design in GHz domain leads to increased power consumption, noise and circuital complexity, challenges that the analog designer must deal with.

1.9 Radiation Hardness

Investigation in the CMOS technologies radiation hardening has become an important issue, especially for integrated circuits exposed to high level of radiations with consequent performance degradation [16]. In the next future, in many physical experiments at CERN (LHC, ATLAS, etc.), detector electronics close to the collision point will experience a cumulative total ionizing dose (TID) up to 1 Grad, a level of radiation never reached before. Until now, hardness-by-design techniques have been adopted, in order to mitigate the radiation damage effects: circuital dedicated solutions or custom transistors layout (enclosed-layout devices)[17]. However the circuital approaches don't solve completely the problems, while the layout solution is not feasible in sub-μm technologies, because of the restrictive design rules discussed before. The good news is that ultra-scaled technologies, and especially the 28 nm CMOS, results to be more radiation resistant than the others. In fact, radiation damage

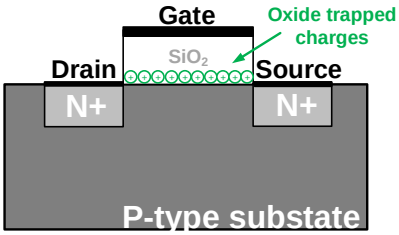


Figure 1.8: Oxide trapped charges in NMOS transistor due to ionization radiation.

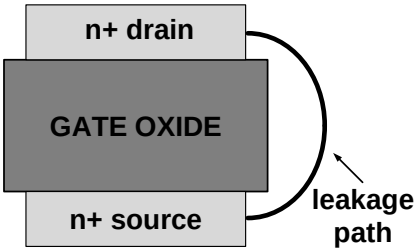


Figure 1.9: The source-drain leakage pah created by built-up charge in oxide.

is proportional to gate oxide volume, i.e. smaller devices exhibit lower radiation detriment. Moreover in ultra-scaled technologies, gate dielectric has been replaced with high-k materials, and this can be another advantage to avoid radiation damages.

In literature recent works on the technologies radiation characterization can be found, for 130 nm, 65 nm and 28 nm technologies [18][19], with also comparisons between different nodes. In particular, preliminary analysis show that standard Mosfets in 28 nm CMOS technology are tolerant to 1 Grad of TID. The main consequences caused by TID in Mosfets are trapped charges in the oxide and in the Si-oxide interface leading to a V_{TH} and subthreshold slope variation (Fig. 1.8), and trapped charges in the STI thick oxide creating an off-state leakage current path between source and drain (Fig. 1.9). While the global absolute V_{TH} variation for the 28 nm node is within 70 mV, for the 65 nm node this variation is higher up to 300 mV. Nevertheless, a considerable degradation has been observed for the drain leakage current respect to the previous technological nodes, while the trend of the subthreshold slope confirms the results of previous technologies. However, these are first promising results, which must be more investigated but give more incentive to exploit the 28 nm and beyond technologies in radiation and not applications.

Chapter 2

Fast Tracker Front-End for ATLAS MDT

2.1 Introduction

In the last years integrated circuits with deep sub-micron technologies have been widely employed in read-out electronic for high energy physics experiments. The main reason is to replace the current electronics used at CERN based on old CMOS processes. In this way, a higher density can be achieved thanks to the increased scaling, sensitivity/noise/power performance are improved and it is possible to exploit the intrinsic radiation hardness of the ultra-scaled technologies [20][18]. As a result, the development of efficient microelectronics read-out front-ends for high energy physics has become an interesting research field.

In this chapter, a read-out front-end for ATLAS Monitored Drift Tube (MDT) chambers is presented. After an overview of the ATLAS experiment and the MDT system, the electronic front-end design is described, from circuital and layout point of view. Then the test set-up will be discussed and front-end performance will be analysed.

2.2 ATLAS Monitored Drift Tube Chambers

ATLAS [1] (A Toroidal LHC ApparatuS) is a multi-purpose high-luminosity experiment which is part of the Large Hadron Collider (LHC) at CERN. The LHC [21] is the most powerful particle hadron accelerator and collider with a circumference of 27 km, located in a ring-shaped tunnel below the surface and consisting of eight straight sections. The high luminosity and increased cross-sections enable high precision tests of the Standard Model on QCD (i.e. quantum chromodynamics), electroweak interactions and flavour physics. Inside the accelerator, two high-energy particle beams, guided by a strong magnetic field maintained by superconducting electromagnets, travel at close to the speed of light before they are made to collide. Collisions happen at four locations around the accelerator ring, corresponding to the positions of four

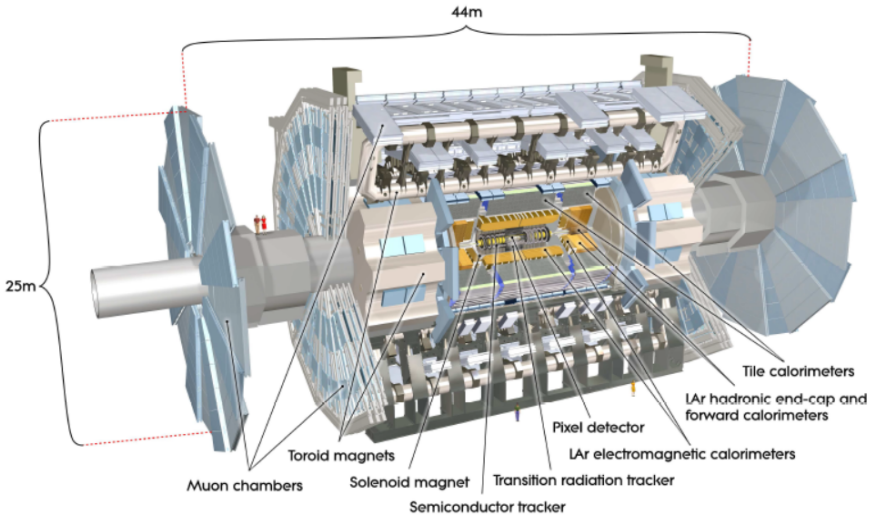


Figure 2.1: The ATLAS experiment at the Large Hadron Collider [1].

particle detectors – ATLAS, CMS, ALICE and LHCb.

The ATLAS detector investigates a wide range of physics topics, from the search for the Higgs boson and its properties to extra dimensions and particles that could make up dark matter. The high LHC luminosity and interaction rate imposed challenging requirements for the detectors and the read-out electronics in terms of radiation hardness and also resolution, since a lot of overlapping events per bunch crossing accompany the interesting event. The interactions in the ATLAS detectors create an enormous flow of data. As the read-out and storage capability is limited, ATLAS uses an advanced trigger system to select which events to record and which to ignore, without discharging interesting events.

The overall ATLAS detector layout is shown in Fig. 2.1. It is forward-backward symmetric with respect to the interaction point. A thin superconducting solenoid surrounds the inner-detector cavity, while three large superconducting toroids are located in the central barrel region and in the so-called end-caps. In the inner detector, high-resolution semiconductor pixel and strip detector, together with straw-tube tracking detectors, perform pattern recognition, momentum measurements and electron identification. Moreover high granularity liquid-argon (LAr) electromagnetic sampling calorimeters are present, providing electromagnetic and hadronic energy measurements.

The Muon Spectrometer is the main block of the ATLAS detector and defines the overall dimension. It measures the deflection of the muon tracks in the magnetic field generated by the large superconducting air-core toroid magnets, with a high-precision muon trigger and momentum measurement up to the TeV scale. The magnet configuration generates a field mostly orthogonal to the muon tracks, minimising

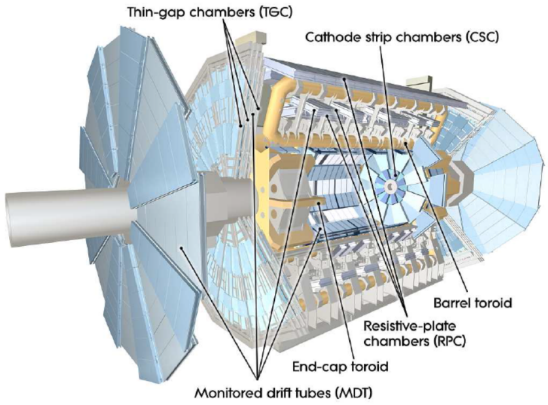


Figure 2.2: The ATLAS Muon Spectrometer [1].

the resolution degradation due to multiple scattering. An overview of the Muon Spectrometer is given in Fig. 2.2.

The primary momentum measurement in the muon system is provided by Monitored Drift Tube (MDT) [2] chambers which consist of aluminium pressured drift tubes with a diameter of 30 mm, filled with Ar/CO_2 gas at 3 bar. The MDT chambers are arranged in three cylindrical layers along the trajectory of the track, which allows a determination of the momentum from the sagitta of the track's curvature in the magnetic field. Most of the MDT chambers are composed of two multi-layers of drift tubes separated by support frames consisting of three cross plates interconnected by two long beams in tube direction. Apart from the length, all MDT tubes are identical. With an average tube resolution of 80 µm, a chamber resolution of 40 µm and 35 µm is achieved for 6 and 8 layer chambers, respectively. Electrons created by ionisation of the Argon atoms by traversing charged particles drift towards a gold-plate tungsten-rhenium anode wire with 50 µm diameter, kept at a potential of 3080 V. In this way, clusters of electron-ion pairs are created along the muon path; the moving ionisation charge multiplied in the avalanche close to the wire induces a current on the anode wire which is detected by the front-end electronics in order to measure the arrival time and ionisation charge of the hit. The signal of a single electron drops hyperbolically with a certain time constant that is on the order of few nanoseconds. As a consequence, the overall signal generated by a charged particle hit is the sum of the currents induced by all ion and electron ionisation clusters. Figure 2.3 shows a simplified illustration of a muon signal generated by three clusters.

Once the read-out front-end has measured the drift time, it can be translated into the drift radius at which the muon crossed the tube through a specific relationship and algorithms. Figure 2.4 shows the cross section of a MDT tube. The wall thickness is 0.4 mm and the inner radius is 14.58 mm (R_{max}). For each track, the electrons from the primary ionisation clusters drift to the central wire along radial lines, the corresponding drift lengths ranging from R_{min} to R_{max}. In the Ar/CO_2 gas the drift

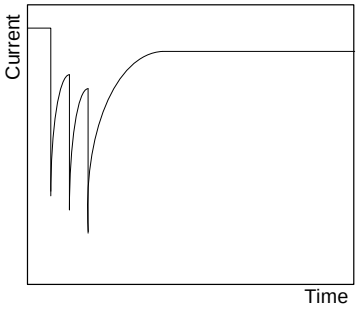


Figure 2.3: Illustration of a typical signal induced for example by three ionization clusters.

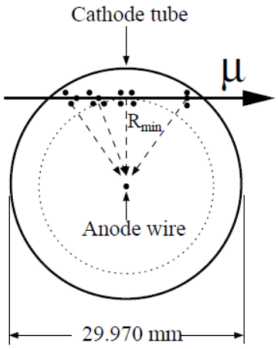


Figure 2.4: Cross section of an MDT tube [2].

velocity shows a strong dependence on the radius. The exact shape of the radius-to-drift time relation (r-t relation) depends also on parameters like temperature, pressure, magnetic field and total hit rate in the tube. For this reason this operating parameters have to be monitored with high precision and used in the calibration phase.

The main task of the readout electronics in the MDT chambers is to detect the arrival time of the hit and the relative charge, preserving the measurement accuracy of the tubes and facing with the expected high hit rate. While only electrons arriving earliest at the wire, namely those coming from the cluster created nearest to the anode wire, are used for the determination of the track coordinate, the subsequent ones will create additional threshold crossings, increasing the data volume to be read. Therefore, the electronics have to use programmable dead-time in order to disable the detection of multiple crossings. In addition electronics are necessary to control the readout system itself, to monitor the chamber environment and running conditions and to supply the necessary low and high voltage power.

2.3 ATLAS MDT Front-End Electronics

The current MDT front-end electronics comprise passive signal and high-voltage distribution boards, active read-out boards and monitoring units. Figure 2.5 shows a schematic drawing of the MDT drift tube connections to the electrical system. On the right chamber end there is the high-voltage hedgehog board, which connects the tubes to the high voltage supply with 383 Ω matching terminating resistor, in order to avoid reflections. The high-voltage hedgehog board contains also 1 MΩ resistor and 470 pF capacitor to filter noise above 500 Hz. At the left end there is the signal hedgehog board, which connects the tube to the "mezzanine" board containing the active read-out electronics. In particular, every mezzanine board performs amplification, shaping, discrimination and digital conversion of the signals coming from 24 drift tubes through the signal hedgehog board.

The architecture of the MDT read-out is shown in Fig. 2.6. The basic components of

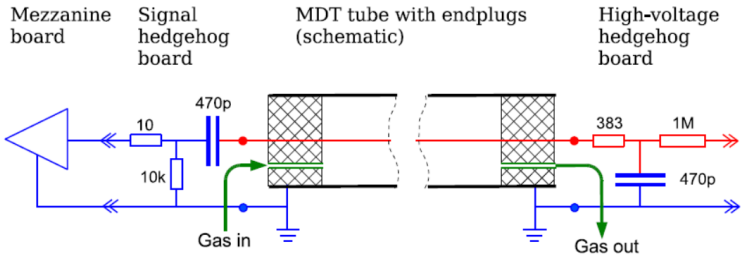


Figure 2.5: Electrical connections to an MDT drift tube [2].

the mezzanine board are three ASD (Amplifier-Shaper-Discriminator) blocks, which process 8 channels each, and a TDC (Time-to-Digital Converter), where the arrival times of leading and trailing edge are stored in a buffer memory of 256 words. Each time measurement is paired together with an identifier of the corresponding tube. The time is measured in units of the Timing, Trigger and Control (TTC) clock of 40.08 MHz, which is the bunch crossing (BC) frequency of the LHC machine. The MDT chambers contain up to 18 mezzanine boards which are controlled by a local processor, the Chamber Service Module (CSM), while the whole system is controlled and programmed by a JTAG.

In the current ASD block [22] (Fig. 2.7), which is the core of the active front-end before the digital conversion, after the amplification and the shaping stage, the signal passes a discriminator with a programmable threshold. The first threshold crossing time defines the arrival time of the signal.

Currently, the ASD can operate in two different modes: Time-over- Threshold (ToT) and charge measurement (ADC) mode. In ToT mode, the output logic signal remains high as long as the MDT shaped signal is above the first threshold; basically the leading edge and the trailing edge are taken into account in order to measure the electron arrival time and the ToT. In ADC mode the signal charge amplitude is measured in the rising edge with a proper analog-to-digital converter named Wilkinson ADC or short gate ADC. After integrating the shaped pulse for a given rate, the charge is stored on a holding capacitor, which is run down at a constant rate. The ADC output width thus encodes the rising edge charge information. The charge data is mainly used for the so-called "time slewing correction" [23].

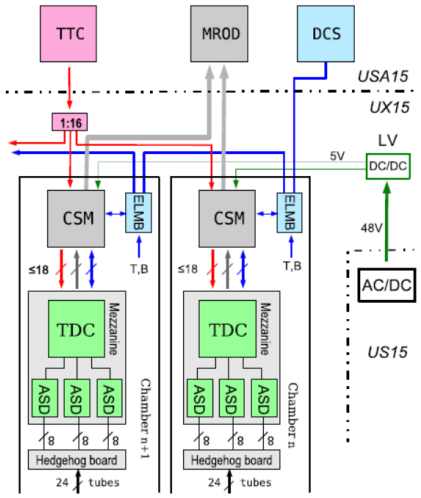


Figure 2.6: Schematic diagram of the MDT readout electronics [2].

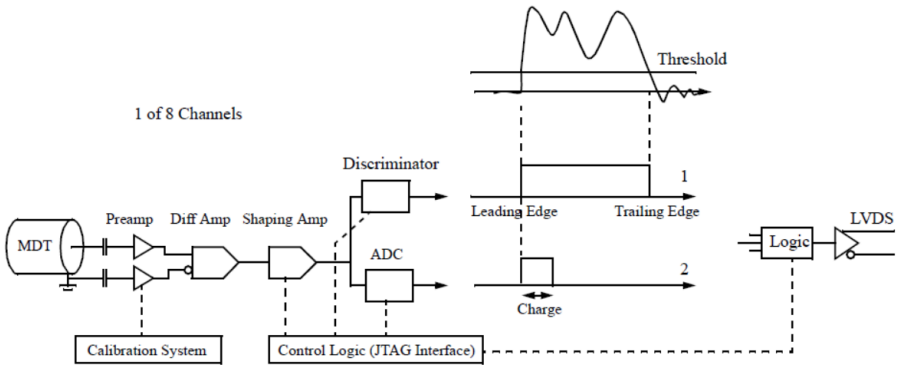


Figure 2.7: Block diagram of one current ASD channel [2].

The use of a fixed discriminator threshold for arrival time measurement introduces a dependence of the threshold crossing time on the pulse amplitude fluctuations, so called time slewing; the charge measurement through a short gate ADC allows for recovery of the resolution. Apart from this improvement, the charge measurement can also provide very useful information for monitoring purposes.

As highlighted before, the complicated shape of the MDT signals can cause multiple threshold crossings per hit increasing the read-out information size. For this reason, in order to mask multiple hits from the same track, a programmable dead-time, up to about 750 ns, is introduced. During this dead time, the front-end is blind at any other hit detection, in order to obtain a threshold crossing multiplicity very close to unity. The overall dead time value depends on the operation mode: in ToT mode is the time-over-threshold while in ADC mode is the time of integration. Typically the ASD user's manual [22] specifies it; the actual dead time varies in the range of 220 - 820 ns. However it reduces the efficiency of the front-end because good muon hits, which are masked by preceding background hits, could be lost. Therefore a trade-off exists between the loss of hit efficiency and the data volume to be stored.

The read-out front-end presented in this thesis has been designed starting from the ATLAS-MDT front-end characteristics described above. In the next section, design motivations and tasks will be discussed, followed by a detailed description of the proposed front-end.

2.4 Fast Tracker front-end Architecture

A Fast Tracker front-end (FTfe) has been designed in TSMC 28nm CMOS technology, starting from the requirements and the circuital solutions employed for the ATLAS-MDT detectors read-out electronics. The main task of this work was the implementation of a front-end characterized by a fast charge detection, avoiding the typical long dead times and loss of events described above. In particular, after a detailed analysis of the current system, the following front-end features have been

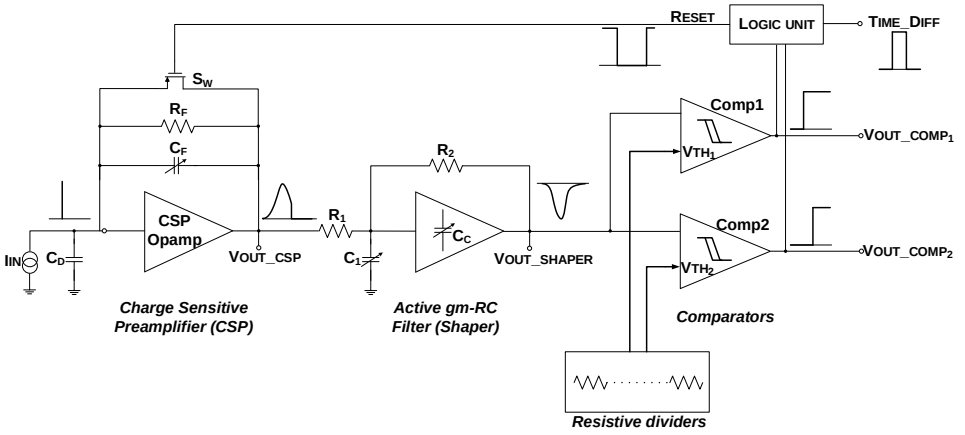


Figure 2.8: FTfe block diagram.

worked out:

- **Detection of the arrival time** of the event, taking into account a first threshold crossing time.
- **Measurement of the charge amplitude**, in order to correct the time-slewing effect, using a second threshold during the rising time; the resulting time difference pulse width will encode the charge information and the short gate ADC is no longer necessary.
- **Front-end reset** soon after charge detection, in order to made the system available for the next charge arrival, avoiding multiple threshold crossings per muon hit and reducing the required dead time and also the loss of events.

The block scheme of the proposed FTfe is shown in Fig. 2.8. The input current pulse coming from the muon detector is converted into a voltage signal by the Charge Sensitive Preamplifier (CSP), composed by a passive feedback net $\mathrm{C_F} - \mathrm{R_F}$, the reset switch $\mathrm{S_W}$ and the single-ended Opamp. By closing $\mathrm{S_W}$ it is possible to discharge the $\mathrm{C_F}$ capacitor and restore the CSP output at the common-mode voltage. The CSP output voltage is then shaped and amplified by an Active $\mathrm{g_m}$-RC Filter, in order to implement a unipolar shaping for tail cancellation, as will be discussed in detail later. The shaper output voltage is fed into two comparators, which compare it with two different thresholds generated by resistive dividers externally controlled. The Comp1 output pulse indicates the first crossing time, i.e. the charge arrival time. The Comp1 and Comp2 output pulses are then used in the Logic block to determine:

- the time difference pulse $\mathrm{TIME\_DIFF}$, which corresponds to the difference of the two crossing times during the shaper output rising edge and can be used to recover the charge information;

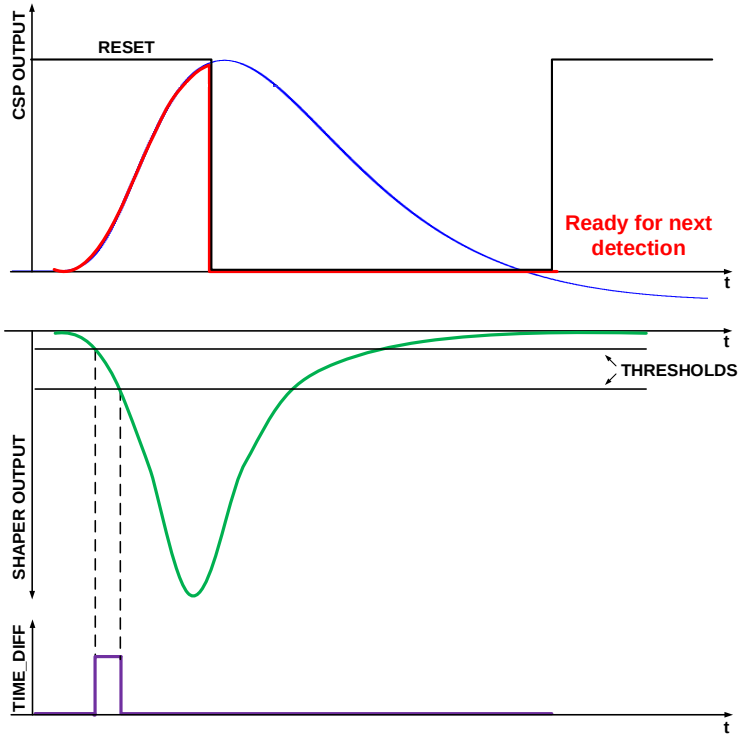


Figure 2.9: Simplified timing diagram of the FTfe.

- the reset signal for the CSP, whose interval depends on the input charge.

A programmable CSP feedback capacitor C_F has been implemented in order to control the CSP output pulse amplitude vs technology and temperature spread. Moreover, for a better control on the peaking time and to adjust the tail cancellation circuit for different technology behaviour, temperature and gases, the shaper time constants are programmable.

A simplified timing diagram of the desired front-end behaviour in response to the input current pulse is shown in Fig. 2.9. In particular, typical CSP and shaper output signals are represented, for a certain amount of input charge. After the two crossing times and the generation of the T_{IME_DIFF} pulse, the active-low reset signal closes the CSP switch S_W, bringing again the CSP output to common mode voltage. After a certain reset interval, smaller than the current dead times, the system returns to normal operation, waiting for the next arrival charge.

The starting specifications for the system to be developed are summarized in Table 2.1, in terms of input charge Q_{IN}, detector parasitic capacitance C_D, peaking time delay T_P, sensitivity S and Equivalent Noise Charge (ENC). The parameter T_P represents the time delay between the input charge arrival and the output voltage peak V_{PEAK}; basically it indicates the front-end capability to quickly detect the charge arrival,

Parameter	Value
Input charge Q_{IN}	5-100 fC
Detector capacitance C_D	10 pF
Peaking time delay T_P	$\leq$ 30 ns
Sensitivity S	$>$ 4 mV/fC
ENC	$<$ 0.5 fC

Table 2.1: FTfe specifications.

	CSP	Shaper
Peak Amplitude (for Q_{MIN} and Q_{MAX})	5-100 mV	25-500 mV
Peaking time delay	$\simeq$10 ns	$\simeq$30 ns
Output integrated noise	$<$ 400 μV_{RMS}	$<$ 2 mV_{RMS}

Table 2.2: FTfe specs distribution.

preserving a good MDT resolution in the drift time and distance measurements. The sensitivity S [24] is defined as the conversion ratio between output voltage peak and input charge, as indicated in Eq. (2.1):

$$S = \frac{V_{PEAK}}{Q_{IN}} \tag{2.1}$$

The ENC [24] is defined as the ideal charge to be injected at the CSP input able to generate a signal equal in amplitude to the Root-Mean-Square (RMS) output noise, resulting with a Signal-to-Noise ratio (SNR) equal to 1. It features a different way to represent the SNR and can be evaluated in terms of Coulombs or electrons as follows:

$$ENC = \frac{V_{nOUT,RMS}}{S} \tag{2.2}$$

$$ENC_{el} = \frac{ENC}{q} \tag{2.3}$$

where q indicates the electron charge of 1.6×10^{-19} C.

Starting from requirements indicated in Table 2.1, specifications as voltage peak (hence gain), peaking time delay and noise have been distributed among the front-end building blocks, basically CSP and shaper. The resulting specifications for each block are summarized in Table 2.2.

In the following subsections, the design of every FTfe block is described in detail, starting from the CSP circuit.

2.4.1 Charge Sensitive Preamplifier

The CSP block consists of an operational amplifier with the $C_F - R_F$ feedback net and a switch S_W for the reset operation (Fig. 2.10). Since C_D is quite large, as

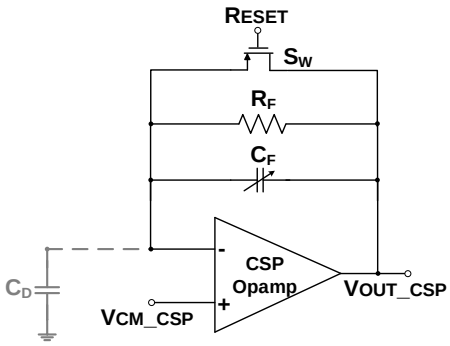


Figure 2.10: CSP block scheme.

indicated in Table 2.1, stability is critical for this design. Moreover during the reset interval, i.e. when S_W is closed, the Opamp is in buffer configuration with C_D as capacitive load, and this situation can be problematic for stability. As a consequence, a complete analysis of the circuit is necessary, in order to satisfy specifications and to fix every issue. The circuit behaviour, assuming an ideal opamp with infinite gain and bandwidth, depends only on the feedback net and in particular on C_F. In fact, the transfer function can be written as follows:

$$\frac{V_{OUT}}{I_D} = -\frac{R_F}{1 + sC_FR_F} \tag{2.4}$$

The detector signal is a narrow pulse having, in good approximation, a Delta-like shape, i.e. $I_D = Q_{IN}\delta(t)$, where Q_{IN} is the charge created in the detector after the hit. Consequently the output voltage becomes:

$$V_{OUT} = -\frac{R_F}{1 + sC_FR_F}Q_{IN} \approx -\frac{Q_{IN}}{sC_F} \rightarrow V_{OUT}(t) \approx -\frac{Q_{IN}}{C_F}e^{-t/C_FR_F} \tag{2.5}$$

From Eq. (2.5) it results that the feedback is dominated by the capacitance, and the output voltage peak depends only on the ratio between the Q_{IN} and C_F, while the detector impedance does not contribute. Thus, the ideal sensitivity results to be:

$$S = \frac{1}{C_F} \tag{2.6}$$

In a real design, opamp poles and finite gain together with the detector capacitance influence the CSP behaviour, affecting its performance. Assuming to express the gain of the opamp as $g_mR_L >> 1$ and that $R_F \simeq R_L$, the CSP transfer function in first approximation can be written as [25]:

$$\begin{aligned} \frac{V_{OUT}}{I_D} &= -R_F \frac{1 - s\frac{C_F}{g_m}}{\left(1 + sC_FR_F\left(1 + 2\frac{C_D}{C_Fg_mR_L}\right)\right)\left(1 + s\frac{C_D}{g_m}\right)} \\ &= -R_F \frac{1 - s\tau_z}{(1 + s\tau_{p1})(1 + s\tau_{p2})} \end{aligned} \tag{2.7}$$

Parameter	Value
$\mathbf{C_F}$	750 fF
$\mathbf{R_F}$	30 kΩ
CSP Opamp	Class A
input g_m	5 mA/V
DC Gain	42.5 dB
UGB	557 MHz
Dominant pole f_p	5.5 MHz

Table 2.3: CSP dimensioning.

A zero with time constant approximately equal to $\frac{C_F}{g_m}$ and two poles with time constants in first approximation depending on $C_F R_F$ (which determines the dominant pole) and $\frac{C_D}{g_m}$ (which defines the non-dominant pole) are introduced. The output voltage peak in this case results to be:

$$V_{OUT\_PEAK} = \frac{Q_{IN} R_F}{\tau_{p1} + \tau_{p2}} = \frac{Q_{IN} R_F}{\frac{C_D}{g_m} + C_F R_F \left(1 + 2\frac{C_D}{C_F g_m R_L}\right)} \tag{2.8}$$

and the sensitivity becomes:

$$S = \frac{R_F}{\frac{C_D}{g_m} + C_F R_F \left(1 + 2\frac{C_D}{C_F g_m R_L}\right)} \tag{2.9}$$

Moreover, also the peaking time delay T_P can be expressed as a function of the time constants as follows:

$$t_P = \left(\frac{\tau_{p1}\tau_{p2}}{\tau_{p2} - \tau_{p1}}\right) \log\left(\frac{\tau_{p2}}{\tau_{p1}}\right) \tag{2.10}$$

From Eq. (2.7) and Eq. (2.8), it is evident that C_D and opamp parameters influence the CSP output voltage in terms of gain (hence peak voltage) and time constants (hence peaking time and rise/fall time). The final dimensioning for the CSP design components in order to satisfy the CSP specifications are then listed in Table 2.3.

The operation amplifier, whose structure is shown in Fig. 2.11, is a classical two-stage Miller compensated opamp, operating in weak inversion region. The Miller capacitance C_M is equal to 1 pF, while the nulling resistor R_M value is 250 Ω. In order to maintain a good phase margin during the reset interval, when the opamp is in buffer configuration, and to avoid problematic ringing in the CSP output voltage during that phase, a capacitance of about 5 pF with a series switch controlled by the reset signal have been added in parallel with C_M. In this way, during the reset interval, the Miller effect is increased and stability is ensured.

About the feedback net, $C_F - R_F$ values are indicated in Table 2.3 also. A calibration for C_F has been implemented to compensate for technology and temperature spread. CMOS integration process leads to statical variations of parameters related to

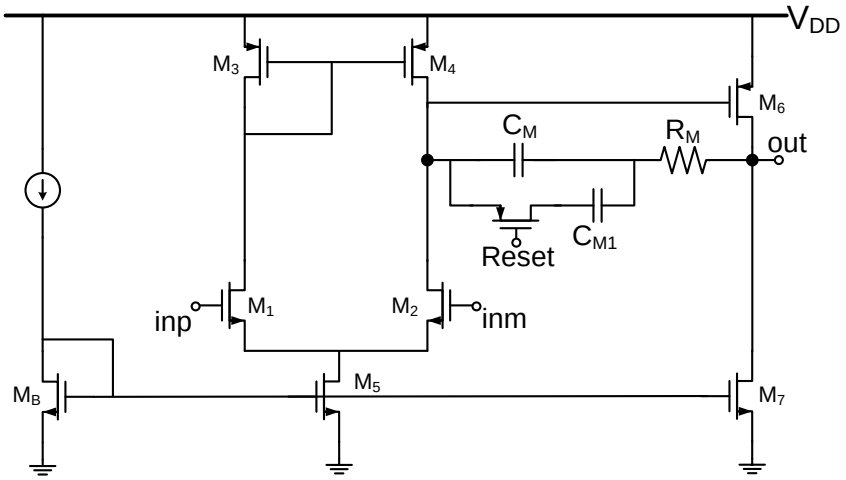


Figure 2.11: CSP Opamp schematic.

transistors, resistors and capacitors. Typically, capacitors mean standard deviation can reach 30% w.r.t. the nominal value; this variation must be taken into account during the design and eventually compensated if necessary for the circuit functioning. In the CSP circuit, capacitance $\mathrm{C_F}$ influences the output voltage evolution, especially the voltage peak, and then sensitivity. For this reason, a binary-weighted digital programmable capacitor array [26] has been implemented, where the calibration precision depends on the number of bits and the capacitors size. Changing the related digital word, a specific value for the $\mathrm{C_F}$ can be selected, in a reference range that must cover the maximum possible error. Calculation of the array capacitors is done through a Matlab® script. If $\mathrm{C_{nom}}$ is the nominal value of the capacitance, N is the number of bits and $\Delta\mathrm{C}$ is the maximum expected process variation of the capacitance value, the minimum $\mathrm{C_{min}}$ and maximum $\mathrm{C_{max}}$ values are:

$$\mathrm{C_{min}} = \mathrm{C_{nom}} \cdot (1 - \Delta\mathrm{C}) \tag{2.11}$$

$$\mathrm{C_{max}} = \mathrm{C_{nom}} \cdot (1 + \Delta\mathrm{C}) \tag{2.12}$$

As a results, the minimum capacitance step and so the maximum error ϵ achievable with the array depends on the number of bits as follows:

$$\epsilon = \frac{\mathrm{C_{max}} - \mathrm{C_{min}}}{2^{\mathrm{N}}} = \frac{\Delta\mathrm{C}}{2^{\mathrm{N}-1}} \tag{2.13}$$

Once known the maximum variation of the capacitance, the Matlab® script determines the array offset capacitor.

In this design, in order to compensate accurately the output voltage peak variation resulted from PVT simulations, the $\mathrm{C_F}$ capacitor has been replaced with 4-bits capacitor array (Fig. 2.12). Every process and temperature variation can be compensated by tuning the $\mathrm{C_F}$ value, with about 5% accuracy. As discussed also in the

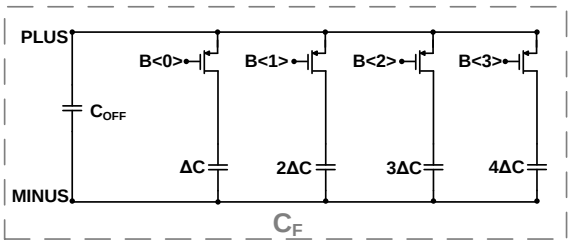


Figure 2.12: Schematic of the C_F capacitor array.

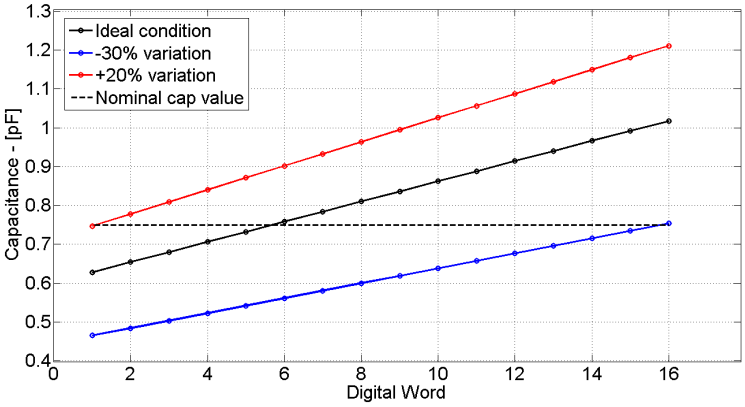


Figure 2.13: The capacitor values related to the digital words.

first chapter, ultra-scaled technologies are characterized by a larger and asymmetric variability of parameters, caused by physical and fabrication limitations. In Fig. 2.13 the digital word vs. capacitance relation is shown in nominal case together with about 20-30% positive and negative variation. In Fig. 2.14, the corresponding output voltage peak is shown vs. the digital word in the three cases.

2.4.2 Shaper

The CSP output signal is processed by a shaper stage, whose main tasks are:

- amplification of the signal;
- noise filtering;
- shaping of the signal in order to define the fall time, cancel the tail and restore quickly the signal to the baseline (reducing the dead time).

The commonly used signal shaping concepts are the so-called unipolar and bipolar shaping [27] [28]. The unipolar shaping is implemented with linear filters; the simplest way is to use the CR high-pass and RC-low-pass filter, but also more complex filter

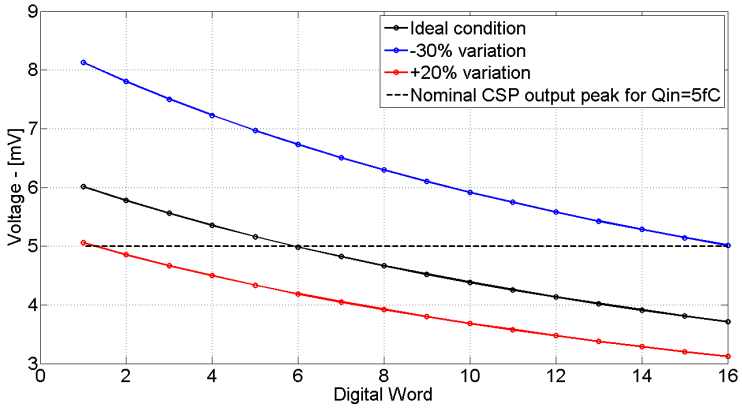


Figure 2.14: The CSP output voltage peak values related to the digital words.

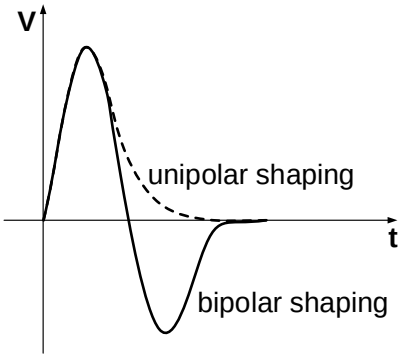


Figure 2.15: Front-end delta response for unipolar and bipolar shaping.

types can be used. Unipolar shaping is characterized by soft and slow decreasing falling edges that can cause a shift of the baseline at high counting rates. A solution can be the implementation of an active baseline restoration or an alternative can be the use of the bipolar shaping, which differentiates the signal suppressing low frequency. As a result, it provides baseline stability up to high rates, but causes an undershoot with a length corresponding to the length of the ion tail. In Fig. 2.15 typical δ-responses for unipolar and bipolar shaping are illustrated. A disadvantage of the bipolar shaping is the pile-up effect: muon signal pulses may be overlaid at high counting rates on top of the undershoot of preceding charge pulse, leading to a reduction of amplitude and rise time of the secondary muon pulse at the baseline. The signal pile-up effect leads to hit efficiency loss and degrade the time resolution. Only optimisation of the shaping or baseline restoration can suppress the problem.

In this design, since the dead time is reduced thanks to the reset operation which already performs a baseline restoration, a simple unipolar shaping has been chosen.

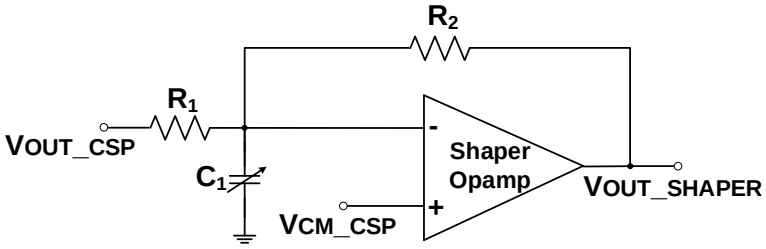


Figure 2.16: Active g_m- RC schematic used as shaper stage.

Parameter	Value
Filter type	Active g_m- RC
$\mathbf{R_1}$	2 kΩ
$\mathbf{R_2}$	20 kΩ
$\mathbf{C_1}$	2 pF
Shaper Opamp	Class A
input g_m	1 mA/V
DC Gain	53 dB
UGB	75 MHz
Dominant pole f_p	168 kHz

Table 2.4: Shaper dimensioning.

The shaping stage has been realized with an Active g_m- RC filter [26] topology, whose schematic is shown in Fig. 2.16. It is a biquadratic cell characterized by a closed-loop structure that exploits the opamp frequency response in the filter transfer function. In particular, the unity-gain-frequency (UGB) of the opamp is made comparable with the filter desired pole frequency. This reduces its power consumption w.r.t standard closed-loop structures, in which the opamp UGB should be much higher than the filter pole. Moreover, thanks to the closed-loop topology, high linearity and frequency response accuracy can be ensured. The transfer function of the Active g_m- RC can be expressed as follows:

$$T(s) = \frac{G}{\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1} \tag{2.14}$$

$$G = \frac{R_2}{R_1} \tag{2.15}$$

$$\omega_0 = \sqrt{\frac{\omega_{op}}{C_1 R_2}} \tag{2.16}$$

$$Q = \frac{1}{1+G}\sqrt{\omega_{op} C_1 R_2} \tag{2.17}$$

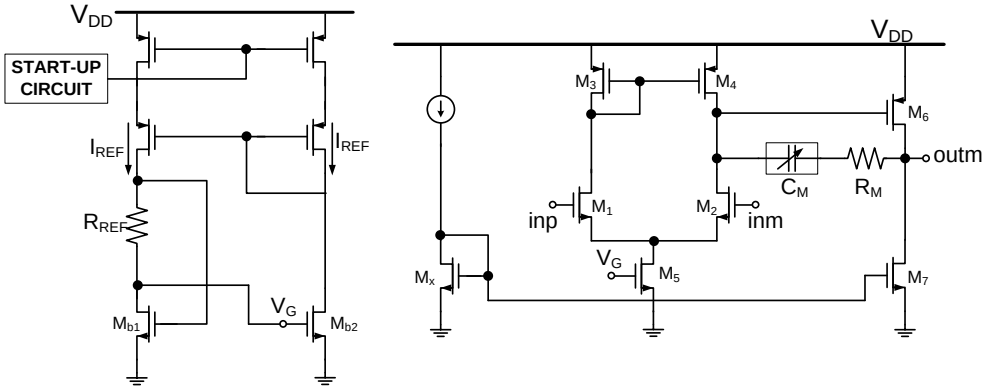


Figure 2.17: Shaper opamp schematic.

From the specifications of Table 2.1, a pole frequency at about 7 MHz and 20 dB gain have been chosen. Hence, the biquadratic cell has been dimensioned as indicated in Table 2.4. The opamp is based on the class-A Miller scheme, as shown in Fig. 2.17, similar to the CSP opamp. However it has a proper and dedicated bias circuit that matches the input stage $\mathrm{g_m}$ with an external resistor [26]. This enables the $\mathrm{g_m}$ to track the integrated resistor process deviation. At the right side of Fig. 2.17, the adjusting circuit is shown. Imposing the same current in the two paths and that:

$$\left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{\mathrm{Mb2}} = \mathrm{k}\left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{\mathrm{Mb1}} \tag{2.18}$$

through the matching between $\mathrm{M_{b1}}$ and the opamp input transistors $\mathrm{M_1}$ and $\mathrm{M_2}$, the input $\mathrm{g_m}$ is forced to be proportional to $1/\mathrm{R_{ref}}$, where $\mathrm{R_{ref}}$ is matched with the integrated resistances of the feedback net. This control on $\mathrm{g_m}$ allows full spread calibration of the filter pole by acting also on variable capacitors. In fact, all the capacitors of the shaping stage, i.e. $\mathrm{C_1}$ and the opamp Miller capacitance $\mathrm{C_M}$, have been replaced with 5-bits programmable capacitor arrays. In this way the overall filter frequency response can be controlled to compensate the cut-off frequency, i.e. the peaking time, variations due to technology and temperature spread. The capacitor arrays have been dimensioned using the same algorithm adopted for CSP feedback capacitance. In Fig. 2.18 the capacitance vs. digital word relation is shown in nominal case together with about $\pm$30% positive and negative variation. In Fig. 2.19, the corresponding pole frequency variation is shown vs. the digital word in the three cases.

2.4.3 Comparators and thresholds

The two comparators, one for the first threshold $\mathrm{V_{TH1}}$ and one for the second threshold $\mathrm{V_{TH2}}$, have the same structure, in order to reduce every possible difference in the response to the input signal coming from the shaper. They detect the presence of a

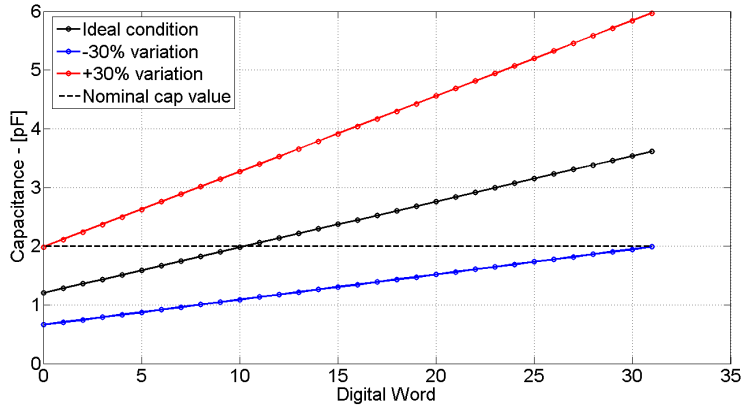


Figure 2.18: The Shaper capacitors values related to the digital words.

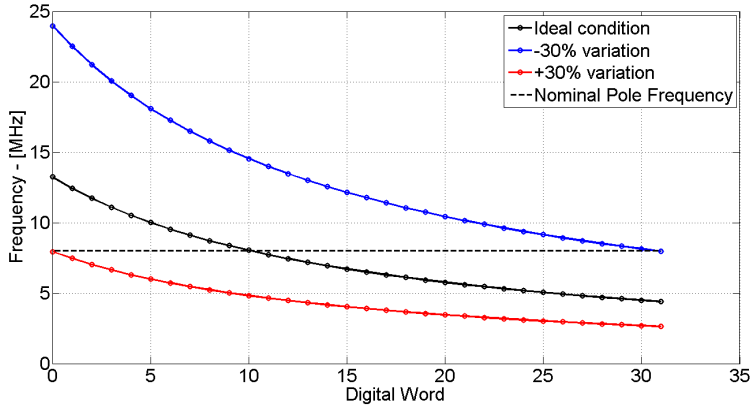


Figure 2.19: The Active g_m- RC pole frequency values related to the digital words.

specific charge and provide two output pulses containing the information about the two thresholds crossing times. Both the comparators have been implemented with a simple two-stage opamp topology.

The two thresholds have been realized with two identical resistive dividers composed by 20 equal smaller resistances of 10 kΩ, in order to ensure a good matching and a high accuracy of the voltages. The scheme is shown in Fig. 2.20. Voltages across every divider are externally controlled; in this way:

- it is possible to adjust $V_{TH1,2}$ w.r.t. the output shaper common mode voltage, controlling the middle output voltage of the dividers V_{CM};
- given that the minimum voltage step across a single resistance is $\Delta V_X = \Delta V_{DIV}/20$, V_{TH1} will be at ΔV_X from the output shaper signal baseline, while V_{TH2} will be always at $2\Delta V_X$ from the first threshold;

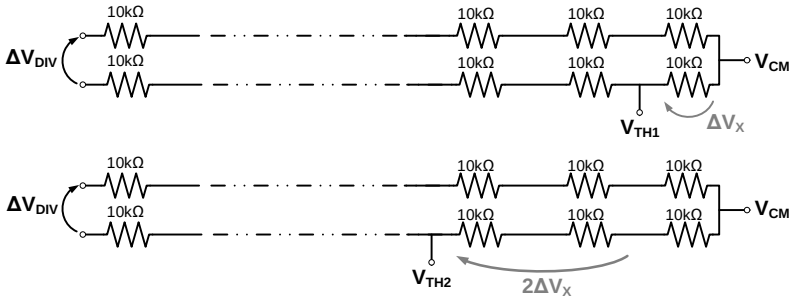


Figure 2.20: Resistive dividers schematics.

- it is possible to change the voltage distance between the two thresholds $V_{TH1,2}$ and between the thresholds and the output shaper signal baseline.

The nominal case of our set-up consists of a ΔV_{DIV} set to 100 mV around the output shaper common mode voltage and, as a consequence, the threshold voltages V_{TH1} and V_{TH2} at −5 mV_{DC} and −15 mV_{DC} respectively from the output shaper signal baseline.

The output signal V_{OUT_COMP1} of the first comparator contains the information about the V_{TH1} crossing time, which represents the charge arrival time. Moreover from this signal, also the Time-over-Threshold (ToT) information can be extracted if necessary, which corresponds to the interval between rising and falling edge times. Then, the two signals V_{OUT_COMP1} and V_{OUT_COMP2} are provided to the Logic block in order to determine the time difference pulse T_{IME_DIFF} and the reset signal.

2.4.4 Logic block

The reset signal is generated starting from the V_{OUT_COMP1} signal. In fact, using a chain of passive RC nets and inverters followed by a NOR logic gate, the reset pulse interval can be set. In particular, the RC time constants applied to V_{OUT_COMP1} make the reset signal starting about 17 ns after the first comparator switching. The reset interval length depends on the ToT of V_{OUT_COMP1}, i.e. on the input charge. A simplified schematic of the reset signal generation is illustrated in Fig. 2.21. When the reset voltage is low, the CSP feedback switch closes, since it is implemented with a PMOS transistor. Thanks to an additional NOR logic gate it is possible to force an external reset to the CSP.

The time difference pulse T_{IME_DIFF}, useful to extract the charge amplitude information, is provided by a NOR logic port which receives at input the inverted V_{OUT_COMP1} and V_{OUT_COMP2} (Fig. 2.21). The pulse width of T_{IME_DIFF} is equal to time difference between the first and the second thresholds crossing, proportional to the charge amplitude. It can be used to correct the time-slewing effect by the off-chip digital signal processing.

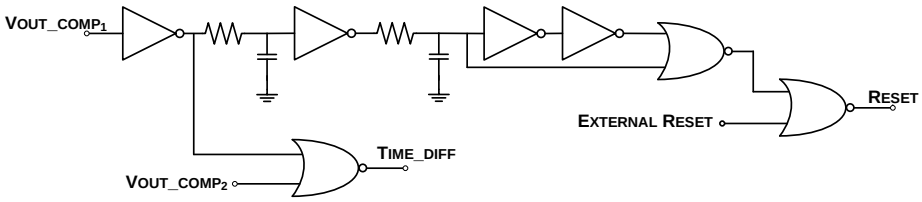


Figure 2.21: Schematic of the logic block with Reset and $\mathrm{T_{IME\_DIFF}}$ signals generation.

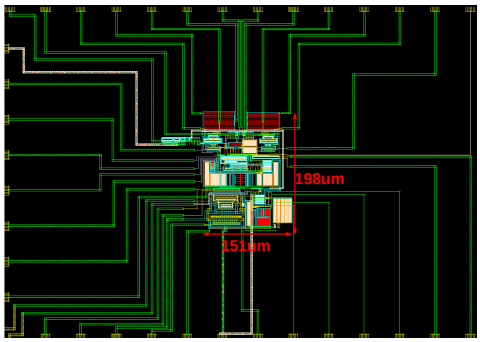


Figure 2.22: FTfe layout and routing to pads.

2.4.5 Output buffers

Analog and digital buffers have been included in the design in order to route out internal and output signals and avoid the effect of parasitic loads. In fact, pads, cables and other external components can affect the signal quality due to capacitive/inductive effects. In particular, two analog buffers, realized with a source-follower structure, have been used for the CSP and the shaper outputs signals. While for the digital output signals, i.e. $\mathrm{V_{OUT\_COMP1}}$, $\mathrm{V_{OUT\_COMP2}}$, $\mathrm{T_{IME\_DIFF}}$ and reset signal, digital buffers composed by a four-inverters chain have been employed.

2.5 FTfe Layout

After the front-end design, the layout of the entire circuit in CMOS 28 nm technology has been carried out. The total front-end area is 0.03 $\mathrm{mm^2}$. In Fig. 2.22 the chip layout is shown, included the routing to the pads.

Figure 2.23 presents the layout of the front-end only, highlighting the different blocks:

1. CSP part, which includes the CSP opamp, the $\mathrm{C_F - R_F}$ feedback net with the programmable capacitors array for $\mathrm{C_F}$, the reset switch and the buffer for the CSP output voltage. This part occupies an area of 0.008 $\mathrm{mm^2}$.

2. Shaper part with a 0.007 $\mathrm{mm^2}$ of area, which comprises the shaper opamp, the two programmable capacitors arrays for $\mathrm{C_1}$ and the opamp Miller capacitance,

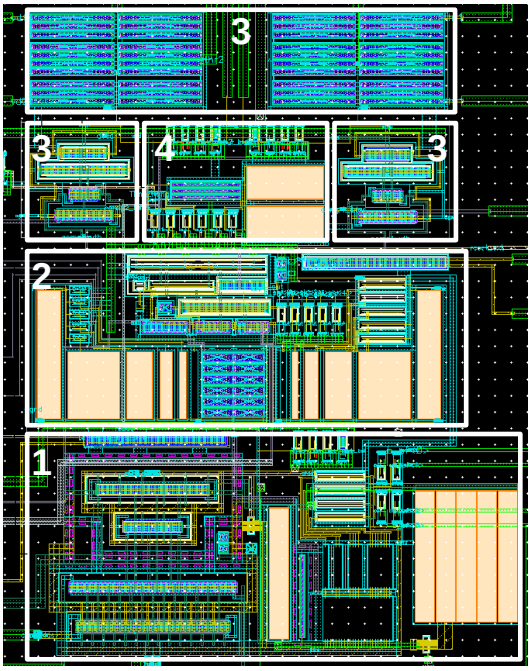


Figure 2.23: FTfe layout in detail.

the feedback resistances and the buffer for the shaper output signal.

3. Comparators and resistive dividers for the corresponding threshold voltages, which occupy an area of 0.006 mm^2.

4. Logic block and digital buffers, for a total area of 0.0022 mm^2.

In this technology, parasitics effects are not negligible and can easily compromise the circuit behaviour w.r.t. the schematic simulations. For this reason, a lot of attention must be paid in particular for supply, ground and substrate paths. For example, higher metals have been used for longer paths, since they are characterized by less parasitics resistances. Reduced number of vias have been adopted, for example in the substrate rings, since they are characterized by a high resistivity. For ground paths towards the pads, stacks of all metals have been used to filter and reduce every possible disturbs in the circuit, originated in the digital part. For this purpose, also separated supply lines are used for analog and digital blocks.

2.6 FTfe Performance

In Fig. 2.24 a diagram of the front-end with all input and output pins is shown. A list of them with their type and functionality is present in Table 2.5.

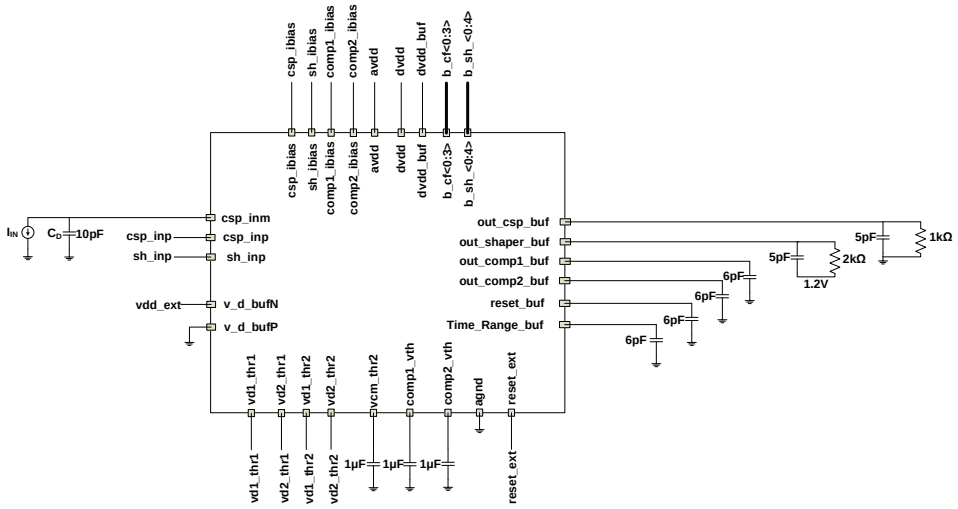


Figure 2.24: Chip pin diagram.

2.6.1 Signals settings

The muon detector is modelled with a current pulse generator and the detector capacitance C_D equal to 10 pF, as shown in Fig. 2.24. The input current pulse amplitude is fixed as Q_{IN}/Q_{TIME}, where Q_{TIME} is set to 30 ps and Q_{IN} is the input charge which can assume values from 5 fC (166 µA) to 100 fC (3.3 mA).

Capacitive loads towards ground of 6 pF are connected to the output digital signals (to model possible capacitances) and of 1 µF to the threshold voltages provided by the resistive dividers (to filter noise and every possible disturb). For the CSP and shaper analog buffers outputs, appropriate RC parallel nets are used.

All the other input voltages and currents values are listed in Table 2.5.

2.6.2 Results

After parasitic extraction, transient noise post layout simulations have been run in order to validate the FTfe functionalities.

CSP

Figure 2.25 shows the CSP frequency response, characterized by a DC Gain of 42.5 dB, a dominant pole at 6 MHz and 610 MHz of UGB.

Figures 2.26 and 2.27 show the transient noise simulation related to the CSP output signal generated from the minimum (5 fC) and the maximum (100 fC) input charge, respectively. In particular, input current pulse (blue line) and CSP output voltage (red line) are plotted together. Some peaking can be observed, correspondent to the switching instant of the digital blocks which disturbs the analog part, especially

Pin name	Description	Value
csp_inm	CSP negative input: input pulse current I_{in}	[166μ-3.3m]A
csp_inp	CSP Positive input	800mV
csp_ibias	CSP bias current	100μA
b_cf<0:3>	Word code for C_F calibration	0101
v_d_bufN	Drain of the NMOS buffer for CSP output	1V
out_csp_buf	CSP output voltage after buffer	Analog Out
sh_inp	Shaper opamp positive input	750mV
sh_ibias	Shaper bias current	100μA
b_sh<0:4>	Word code for Shaper cap calibration	01010
v_d_bufP	Drain of the PMOS buffer for Shaper output	0V
out_shaper_buf	Shaper output voltage after buffer	Analog Out
comp1_ibias	Comparator1 bias current	100μA
comp2_ibias	Comparator2 bias current	100μA
out_comp1_buf	Output voltage of Comparator1 after buffer	Digital Out
out_comp2_buf	Output voltage of Comparator2 after buffer	Digital Out
comp1_vth	Threshold voltage V_{TH1} of Comparator1	Analog Out
comp2_vth	Threshold voltage V_{TH2} of Comparator2	Analog Out
vd1_thr1	High voltage of V_{TH1} resistive divider	775.6mV
vd2_thr1	Low voltage of V_{TH1} resistive divider	675.6mV
vd1_thr2	High voltage of V_{TH2} resistive divider	775.6mV
vd2_thr2	Low voltage of V_{TH2} resistive divider	675.6mV
vcm_thr2	Voltage at half V_{TH2} resistive divider	Analog Out
Time_Range_buf	Time difference output pulse after buffer	Digital Out
reset_buf	Internal reset signal after buffer	Digital Out
reset_ext	External reset signal (1V→OFF, 0V→reset)	1V
avdd	Supply voltage for analog part	1V
dvdd, dvdd_buf	Supply voltages for digital part	1V
agnd	Ground voltage	0V

Table 2.5: Pin list, with description and set up in nominal value.

through ground paths. They have been reduced using different supply voltages, but more isolation and filtering should be added in a next optimisation. Table 2.6 summarizes the main important parameters for both cases.

Figure 2.28 reports the CSP output peak amplitude Δ_{PEAK_CSP} vs. the input charge. Note that the characteristic is linear.

The output integrated noise results to be 125 μV_{RMS}.

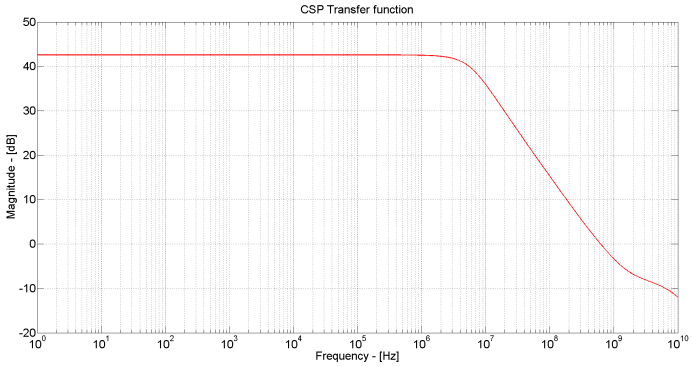


Figure 2.25: CSP frequency response.

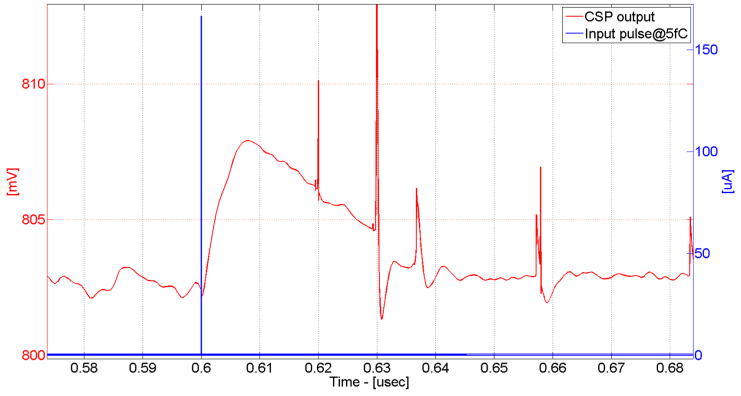


Figure 2.26: Input current pulse (blue) and CSP output voltage (red) for 5fC input charge.

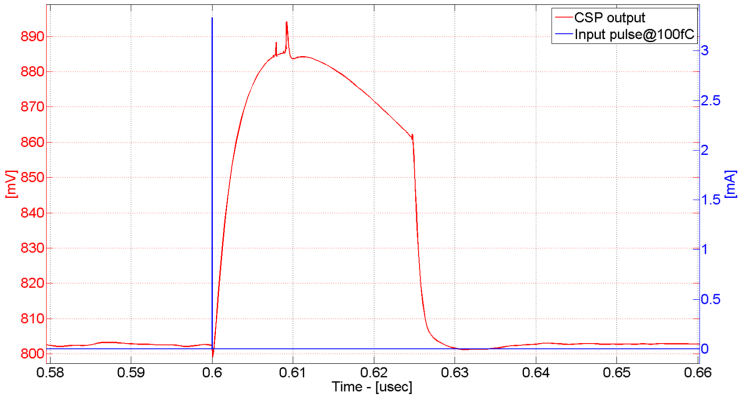


Figure 2.27: Input current pulse (blue) and CSP output voltage (red) for 100fC input charge.

Input charge Q_{IN}	**5fC**	**100fC**
Input current pulse I_{IN}	166 µA	3.3 mA
CSP output common mode V_{CM_CSP}	802.4 mV	802.4 mV
CSP output voltage peak V_{PEAK_CSP}	807.9 mV	885 mV
CSP output peak amplitude Δ_{PEAK_CSP}	5.05 mV	82.6 mV
CSP peaking time delay T_{P_CSP}	11 ns	11 ns

Table 2.6: CSP transient noise results summary.

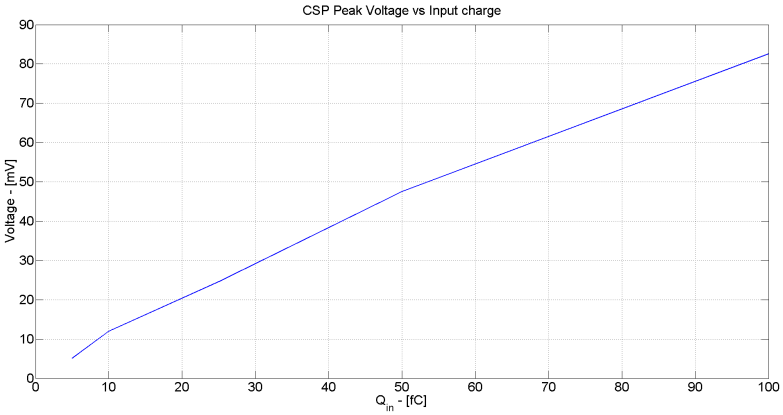


Figure 2.28: CSP output peak amplitude vs. input charge.

Shaper

The frequency response of the Active g_m- RC is shown in Fig. 2.29. The DC Gain is 19.5dB, the dominant pole is at 7.6MHz and the UGB is equal to 420MHz.

Transient noise simulation about the Shaper output voltage is reported in Figs. 2.30 and 2.31 for 5fC and 100fC of input charge, respectively. Table 2.7 summarizes the main important parameters for both cases.

CSP and Shaper have also been tested for 5 different input charge values (5, 10, 25, 50, 75, 100 fC). The resulting time domain waveforms are shown in Fig. 2.32.

Figure 2.33 reports the Shaper output peak amplitude Δ_{PEAK_SH} vs. the input charge. The characteristic results to be very linear. Shaper peaking time delay T_{P_SH} is almost constant respect to different input charges, as shown in Fig. 2.34. Peaking time specification is satisfied, since it is equal to 28 ns (<30 ns). The total noise density at Shaper output is equal to 1.18 mV_{rms}.

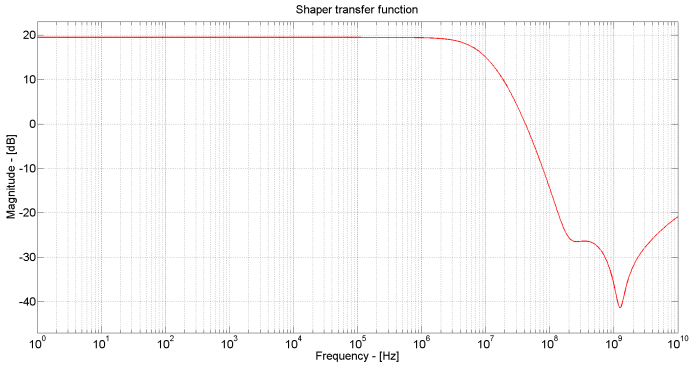


Figure 2.29: Shaper frequency response.

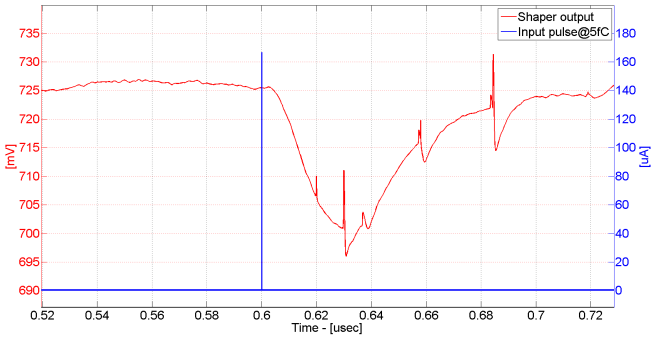


Figure 2.30: Input current pulse (blue) and Shaper output voltage (red) for 5fC input charge.

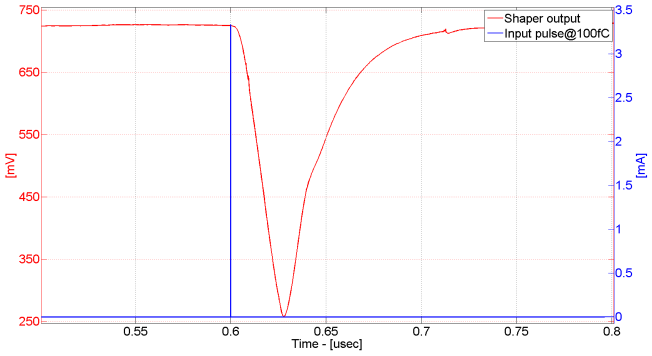


Figure 2.31: Input current pulse (blue) and Shaper output voltage (red) for 100fC input charge.

Input charge Q_{IN}	**5fC**	**100fC**
Input current pulse I_{IN}	166 μA	3.3 mA
Shaper output common mode V_{CM_SH}	725.6 mV	725.6 mV
Shaper output voltage peak V_{PEAK_SH}	701 mV	256 mV
Shaper output peak amplitude Δ_{PEAK_SH}	24.6 mV	469.6 mV
Shaper peaking time delay T_{P_SH}	28 ns	28 ns

Table 2.7: Shaper transient noise results summary.

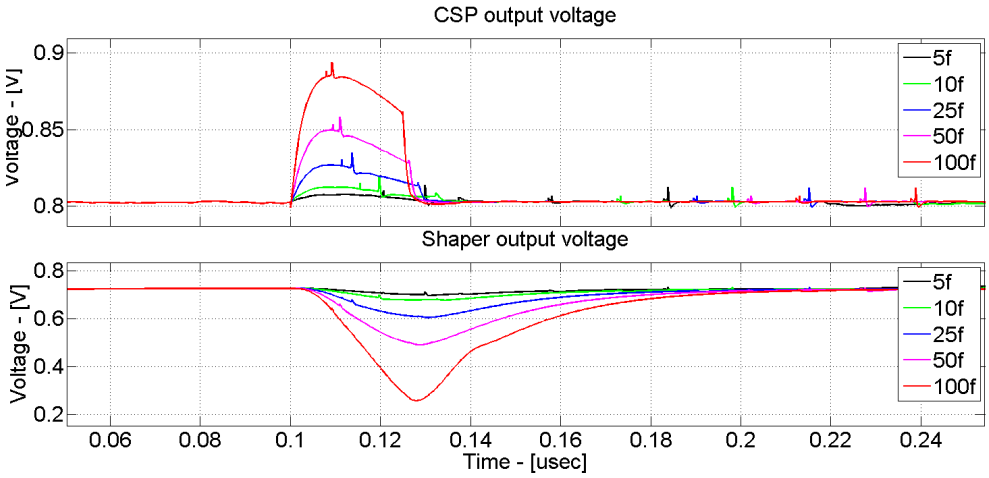


Figure 2.32: CSP and Shaper output signals for different input charges (5÷100 fC).

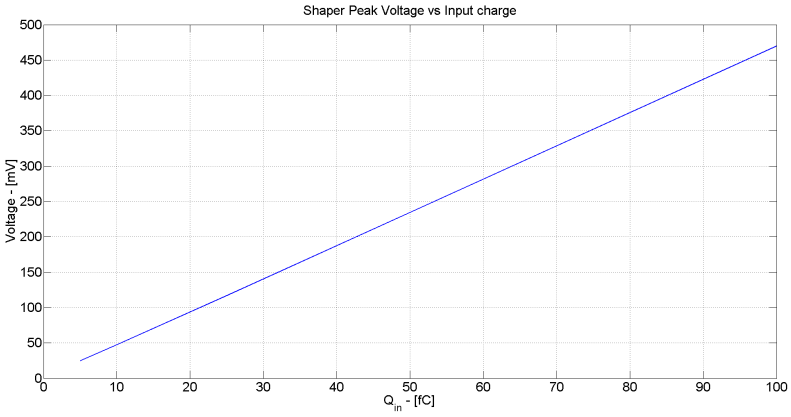


Figure 2.33: Shaper output peak amplitude vs. input charge.

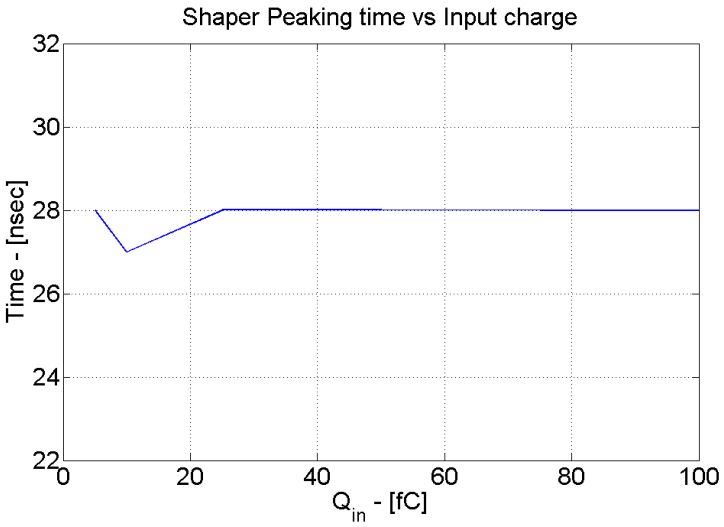


Figure 2.34: Shaper peaking time delay vs. input charge.

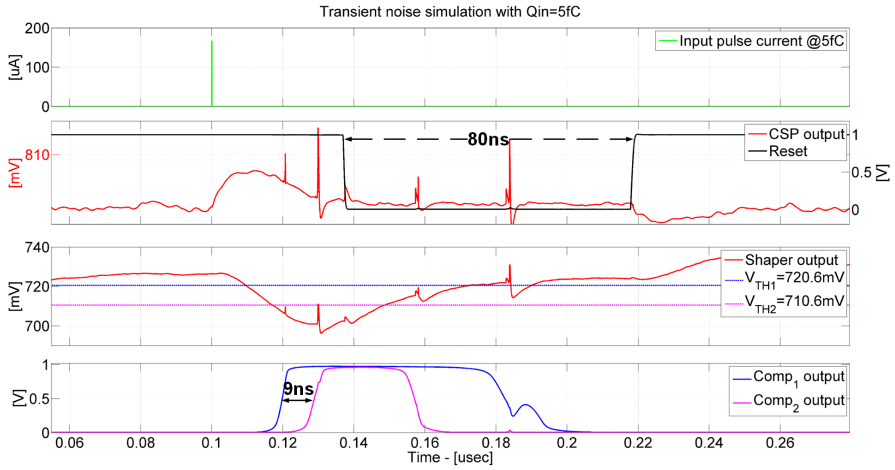


Figure 2.35: CSP, Shaper, Comparators and Reset signals at 5fC input charge.

Comparators

Comparators response is shown in Figs. 2.35 and 2.36. Together with the input pulse, the analog (CSP and Shaper outputs and threshold voltages) and digital outputs (Reset and Comparators outputs) are reported for minimum and maximum charge cases, respectively. Notice that the reset interval depends on the input charge and varies in the range of [80 - 160] ns. Soon after the Reset signal switches to zero, the CSP output signal is restored to the common mode voltage. The V_{TH1} and V_{TH2} crossings of the Shaper output signal are detected by the two comparators. At minimum charge, when slope is soft, the two comparators switches with a delay of 9 ns each other; at

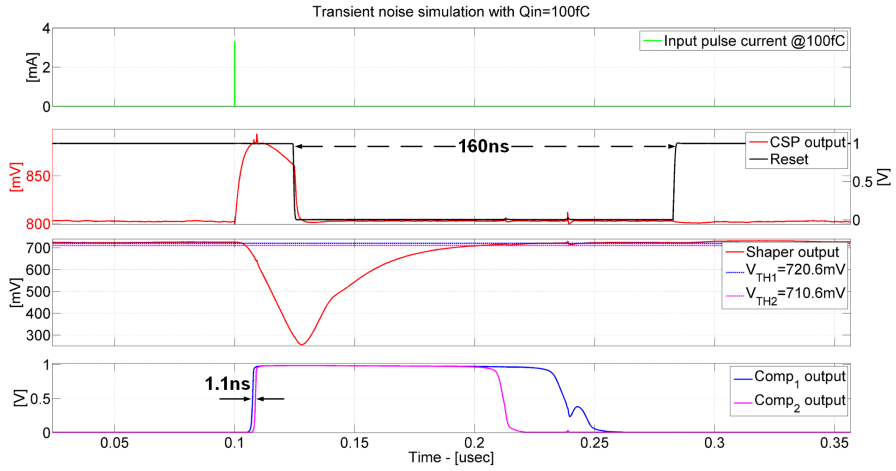


Figure 2.36: CSP, Shaper, Comparators and Reset signals at 100fC input charge.

maximum charge, when slope is steeper, the delay between the two comparators switching instants decreases to 1.1 ns.

Logic block

Figures 2.37 and 2.38 show the $\mathrm{T_{IME\_DIFF}}$ signal related to the switching instants of the two comparators, for minimum and maximum charge respectively. This signal contains the information about the charge amplitude.

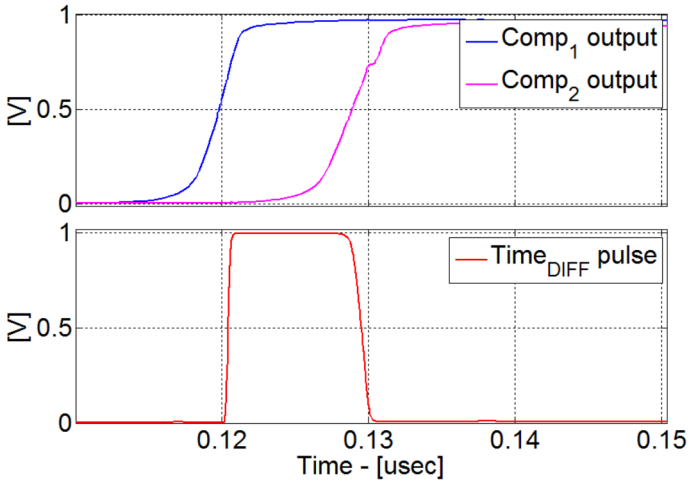


Figure 2.37: Time difference pulse at 5fC input charge.

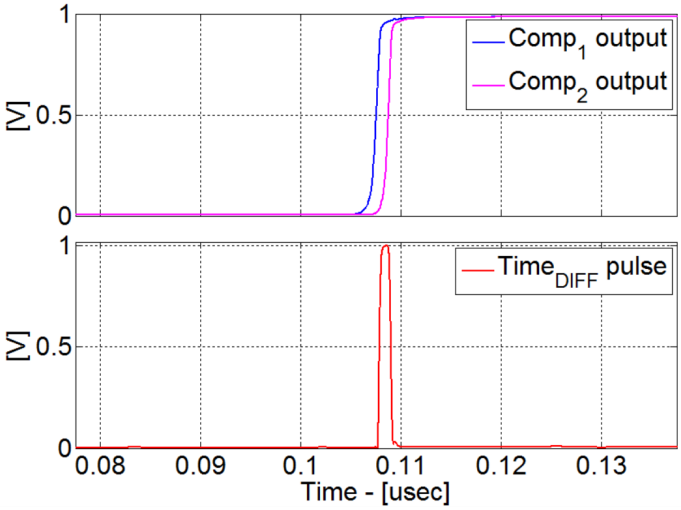


Figure 2.38: Time difference pulse at 100fC input charge.

Front-end Characteristics

The FTfe has been characterized in terms of sensitivity S, ENC and SNR. The sensitivity is quite constant over the input charge range, as illustrated in Fig. 2.39. It is >4 mV/fC, as required by the front-end specifications. Also the ENC parameter is almost constant (Fig. 2.40) with a value around 0.25 fC, less than the requirement of 0.5 fC. Finally, The SNR vs. input charge is plotted in Fig. 2.41 and it increases with the input charge. All the characteristics have been evaluated at the Shaper output.

A summary of the main FTfe parameters are listed in Table 2.1, while a comparison with a state-of-the-art ASD for ATLAS MDT chambers is reported in Table 2.9. The performance of the proposed front-end are in line with the state-of-the-art, with a better behaviour in terms of area, power consumption, ENC and SNR. This advantages derives especially from the different technology used and from the simpler architecture employed. In fact, the reference work presents a front-end which includes more amplifier stages and the short gate ADC, with an higher supply voltage of 3.3V.

In the current ASD system, the TDC uses an input clock frequency of 40 MHz provided by the LHC to synchronize the acquisition of detector signals to the bunch crossings of the LHC machine. The time resolution is 250 ps, required to measure the drift time. In our case, the total time range in which can be encoded the charge amplitude information is of 8 ns (i.e. difference between the maximum and minimum charge time difference pulse width). Assuming to use the same current TDC and to maintain the same time resolution, the resulting ENOB is 5.3. However, in the next future, exploiting the ultra-scaled technology, as the 28 nm itself, better resolutions can be achieved, improving conversion accuracy [29][30].

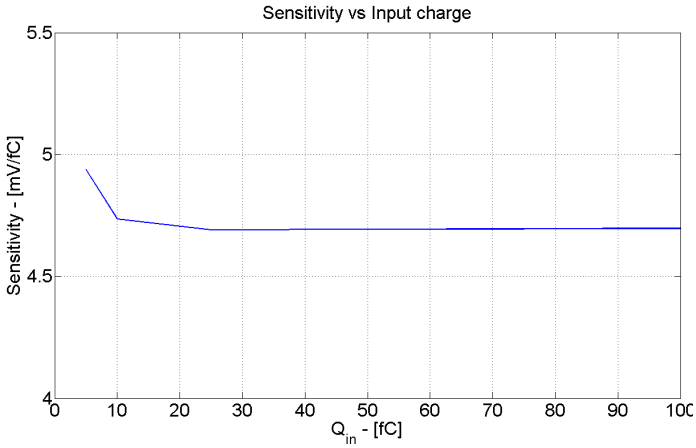


Figure 2.39: Sensitivity vs. input charge.

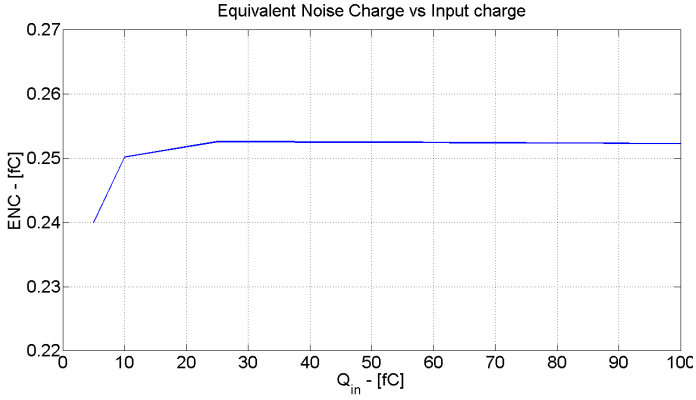


Figure 2.40: ENC vs. input charge.

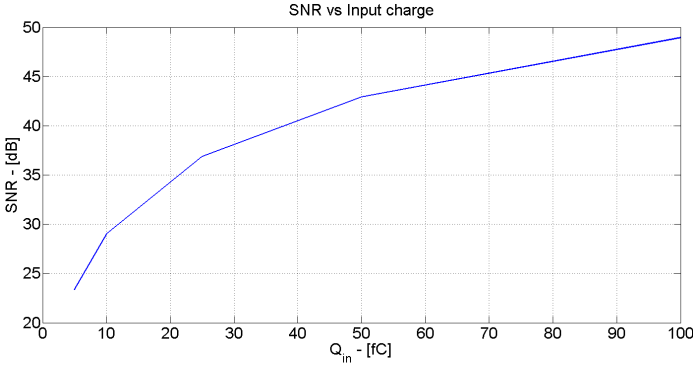


Figure 2.41: SNR vs. input charge.

Input charge	[5-100] fC
Input detector capacitance	10 pF
CSP peaking amplitude	[5-82] mV
CSP peaking time delay	11 ns
Shaper peaking amplitude	[24.6-469.6] mV
Shaper peaking time delay	28 ns
Shaper output rms noise	1.18 mV_{RMS}
Sensitivity	[4.93-4.69] mV/fC
ENC	[0.24-0.25] fC
SNR	[23.3-48.9] dB
Reset interval	[80-160] ns
Technology	CMOS 28nm
Supply voltage	1 V
Power consumption	2.6 mW

Table 2.8: FTfe results summary.

Parameter	This Work	[31]
CMOS Technology	28nm@1V	0.13 µm@3.3V
Area	0.03 mm^2	0.7 mm^{2*}
Power Consumption	2.6 mW	33 mW
Detector Capacitance	10 pF	60 pF
Input Charge	5fC-100fC	5fC-100fC
Peaking Time Delay	28 ns	12 ns
Sensitivity	4.7 mV/fC	14 mV/fC
ENC	0.24 fC	0.6 fC
SNR	23.3 dB	15 dB

*extrapolated

Table 2.9: State-of-the-art comparison.

Chapter 3

Chopper Instrumentation Amplifier

3.1 Offset Compensation Techniques

In many measurement systems, such those dedicated to biomedical applications or read-out electronic for different kind of sensors [32][33], small signals of few nV or μV are processed. These low frequency sub-microvolt signals require a large but precise amplification, so they can be handled by an Analog-to-Digital Converter (ADC). A simplified diagram of such a system is shown in Fig. 3.1. However operational amplifiers have several non-idealities in DC and at low frequency, which are input offset voltage and flicker noise [34], characterized by the same order of magnitude of the weak sensor signals. In order not to saturate the amplifier or limit the accuracy of the sensor read-out system, input offset and flicker noise have to be properly reduced.

Offset in CMOS amplifier is a DC error defined in general as the input signal that forces the system output to zero. In a real opamp, as illustrated in Fig. 3.2, even when input voltages are shorted, a DC voltage is present at output. It is defined input offset

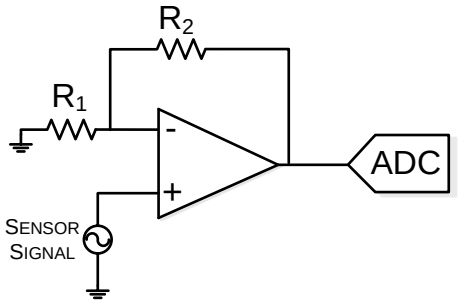


Figure 3.1: A simplified sensor read-out diagram.

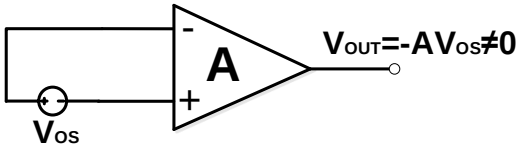


Figure 3.2: Amplifier with input offset source.

voltage V_{OS}, and modelled like a voltage source at the amplifier input, the signal required to force the amplifier output voltage to zero. The input offset signal can be due to asymmetric paths in the circuital topology and it is called systematic offset; or it is originated by random mismatches caused by lithographic imperfections and it is called random offset. Offset is also a time-varying signal that can drift as a function of temperature, voltage supply, input level and ageing. The main consequences of offset signal are threshold voltage V_{TH} and drain current I_{DS} variations. In particular, two identical MOS exhibit a V_{TH} mismatch [14] given by the following expression:

$$\sigma^2_{\Delta V_{TH}} = \frac{A^2_{\Delta V_{TH}}}{WL} + S^2 D_x^2 \tag{3.1}$$

where $A_{\Delta V_{TH}}$ and S are the Pelgrom constants dependent on CMOS technology used in the fabrication process, W is the MOS channel width, L is the MOS channel length and D_x is the distance between them. Pelgrom formula shows that V_{TH} variation is inversely proportional to the area and directly proportional to the distance. Hence, the variation in I_{DS} caused by a threshold voltage mismatch is given by:

$$\sigma_{\frac{\Delta I_D}{I_D}} = \sqrt{\sigma^2_\beta + \left(\frac{g_m}{I_{DS}}\sigma_T\right)^2} \tag{3.2}$$

where σ_β and σ_T represent the variations of the current factor and the threshold voltage between two identical devices (always dependent on area and distance), while the ratio g_m/I_{DS} defines the MOS efficiency and it is inversely proportional to the overdrive voltage V_{OV}. In order to decrease current mismatch, V_{OV} should be increased. Therefore mismatch current can be minimized by proper saturation region biasing, while threshold voltage mismatch can be reduced increasing the MOS area. Both approaches cannot be used so directly, especially in ultra-scaled and low-voltage design, where signal swing is small and parasitic capacitances cannot be no more neglected.

As mentioned before, at low frequency operational amplifiers contribute also with the flicker noise (1/f). It is a type of noise coming from the mechanism of generation and recombination of carriers activated by localized energy levels that reflect the discontinuity at the MOS surface. Basically, some electrons escape from the channel and are trapped in the MOS gate oxide. This phenomena is characterized by a large time constant, so its power is concentrated at low frequency. The power density of

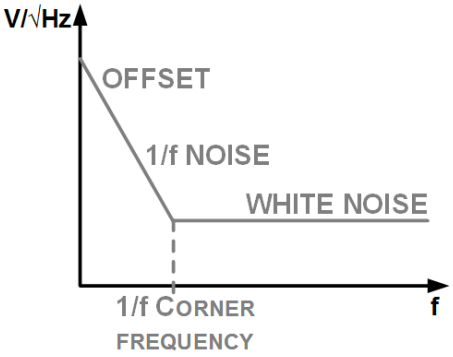


Figure 3.3: Low frequency noise behaviour of a CMOS amplifier.

the 1/f noise is:

$$S_{n,fl}(f) = \frac{k_f}{WL}\frac{1}{f} \tag{3.3}$$

where k_f is the flicker noise coefficient dependent on the amount of impurity in the silicon. The equation shows that flicker noise is inversely proportional to MOS area and frequency; so good performance could be obtained with large area devices (but increasing also MOS capacitance). If we extend 1/f noise down to zero frequency, it becomes a constant error signal: offset. The typical low frequency noise behaviour of an amplifier is shown in Fig. 3.3. Offset and 1/f noise dominate at low frequency, while thermal noise dominates at higher frequency; the corner frequency is between the region dominated by the flicker noise and the white noise.

Instead of increasing the transistor size to improve offset behaviour, it can be considered to add extra circuitry for offset trimming or dynamic offset compensation. Calibration or trimming during production is a possible solution to achieve a low offset, but this approach doesn't take care of offset drift due to temperature and ageing, limiting the accuracy. The best alternative is to compensate for the offset dynamically, during the amplifier lifetime, reducing also the offset drift due to time and temperature. Moreover, most of the techniques used to cancel offset removes also flicker noise, improving the system accuracy. There are two commonly used dynamic offset compensation techniques [34][35][36]: auto-zeroing and chopping. Auto-zero is a sampled-data technique, while chopper is a modulation method; both satisfy the low offset requirements, however with advantages and drawbacks which will be analysed in the following subsections.

3.1.1 Auto-zero Technique

Auto-zero is a sampled-data technique; the basic idea is to sample offset and flicker noise in one phase and then to subtract them from input signal in a second phase. Figure 3.4 illustrates one of the possible architecture named Auto-Zeroing Output Offset Storage (AZ OOS). It consists of a capacitor C placed at the output of an amplifier and

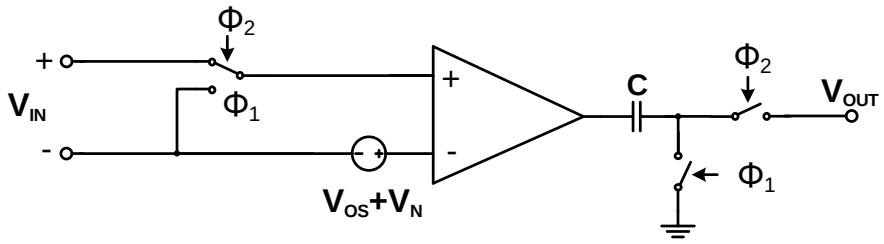


Figure 3.4: Auto-zero technique block diagram.

some switches to control the required phases. During the sampling phase (ϕ_1 closed, ϕ_2 open) opamp inputs are shorted and the offset voltage $\mathrm{V_{OS}}$ and flicker noise $\mathrm{V_n}$ are sampled and stored in the capacitor C. During this time, the amplifier cannot be used. In the amplification phase (ϕ_1 open, ϕ_2 closed) input signal is amplified while offset and noise stored before are subtracted at the amplifier output.

A first drawback of this technique is that input signal path is disconnected during the sampling phase and so the input signal cannot be amplified continuously. Although this may be not compatible with continuous-time applications, it is well suited to sampled-data systems such as switched-capacitor circuits where all the signals are sampled at the end of a phase and held during the complementary time interval. Moreover, because of the sampling operation, this topology suffers from the thermal noise folding back into the signal band, increasing the overall input-referred noise [37]. The auto-zero technique is also limited by charge injection due to the switches, resulting in a residual offset voltage which can be reduced using a large capacitor C. As a consequence, power consumption increases, because driving large capacitive loads leads to large bias currents. All these disadvantages make this method unsuitable, especially for low power applications.

3.1.2 Chopper Technique

The chopper technique exploits a modulation function to shift offset and signal to different frequencies. Figure 3.5 illustrates an idealized chopper modulated amplifier. It consists of a commutating mixer, or chopper, followed by an ideal amplifier and another chopper. Signals $\mathrm{m_1(t)}$ and $\mathrm{m_2(t)}$ are two non-overlapping clock signals with period $\mathrm{T = 1/f_{chop}}$, where $\mathrm{f_{chop}}$ is called chopper frequency.

The input signal is modulated by the first chopper and transposed to high frequency, in particular to the odd harmonics of the modulation signal. Then, offset voltage and $1/\mathrm{f}$ noise are added to the modulated signal and amplified by the gain stage. After amplification, the signal is demodulated back to the baseband by the second chopper, while offset and flicker noise are modulated once for the first time and transposed to high frequency, leaving the chopper amplifier ideally without any offset and flicker noise signals. Figure 3.6 depicts the spectra of the signals involved

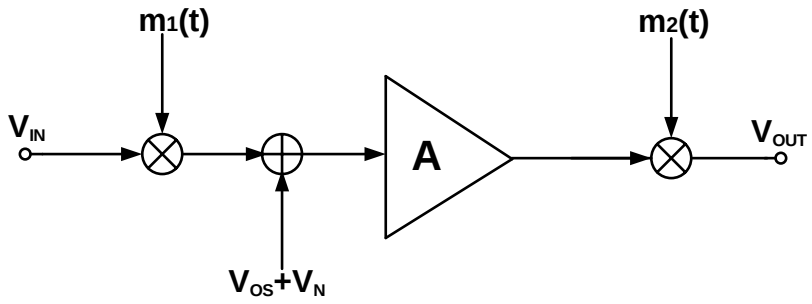


Figure 3.5: Simplified chopper technique diagram.

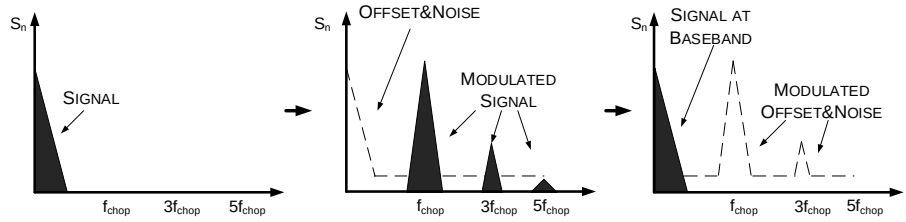


Figure 3.6: Frequency operation of the chopper technique.

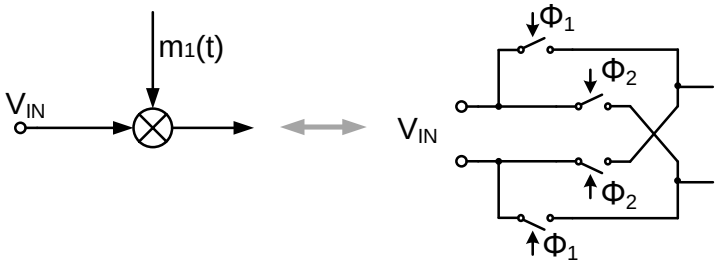


Figure 3.7: Polarity-reversed switch schematic.

in the relevant points of the processing chain. The chopping frequency f_{chop} should be greater than the corner frequency, in order to reduce as much as possible 1/f noise contribution, and it must have 50% duty-cycle.

The modulation process is implemented by a polarity-reversed switch driven by a square wave with a chopper frequency f_{chop}, shown in Fig. 3.7; at every period input signal is inverted and the result is a modulated signal at f_{chop}.

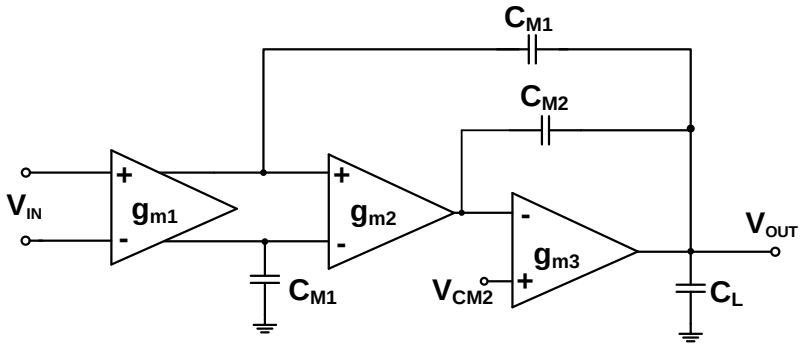


Figure 3.8: Continuous-time amplifier schematic.

Unlike auto-zero technique, chopper method does not introduce aliasing of the white noise, because there is not a sample and hold operation, but noise is only periodically inverted without changing its properties. For this reason also input signal is always processed, so the chopper technique is better used in continuous-time applications. However also the chopper technique introduces residual offset, mainly caused by the charge injection mismatch demodulation from the clock lines driving the switches and the input of the amplifier. Residual offset increases with f_{chop}, so lower chopper frequency should be used, also to ensure a higher gain of the overall amplifier, since the amplifier itself loses gain after the dominant pole. However, higher f_{chop} modulates input signals far from the corner frequency, improving noise performance. Therefore, a trade off exists between gain, residual offset and noise, which leads to find the optimized value for f_{chop} according to the architecture and its specifications. It is also necessary to put effort in the layout phase of the differential choppers and clock lines, in order to reduce parasitic capacitances mismatches and the proportional residual offset.

3.2 Chopper Amplifier: Prototype 1

In this section, the design and implementation of a chopper amplifier in 28nm CMOS technology is presented. First, the continuous-time version of the amplifier will be described, followed then by a description of the chopped one. At the end, layout and results will be analysed.

3.2.1 Continuous-time opamp design

The continuous-time opamp architecture is shown in Fig. 3.8. It is characterized by three gain stages (indicated by their input transconductance g_{mi}) with a classical Nested Miller compensation implemented through capacitors C_{M1} and C_{M2}, required to achieve closed-loop stability of the overall amplifier. The first stage has been

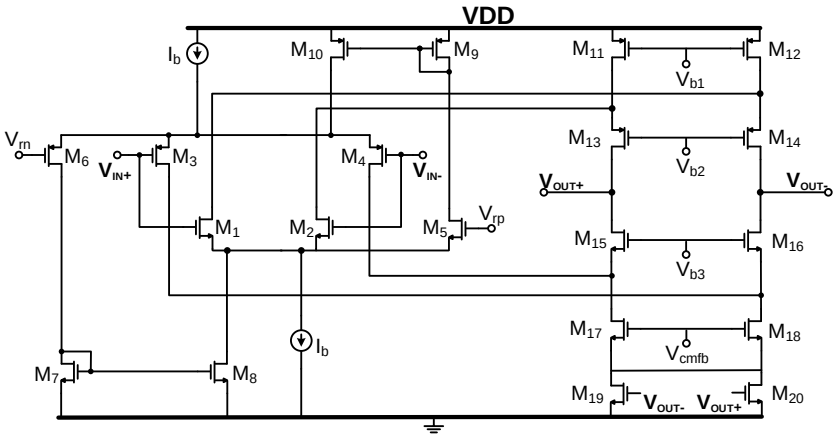


Figure 3.9: First stage input rail-to-rail folded cascode schematic.

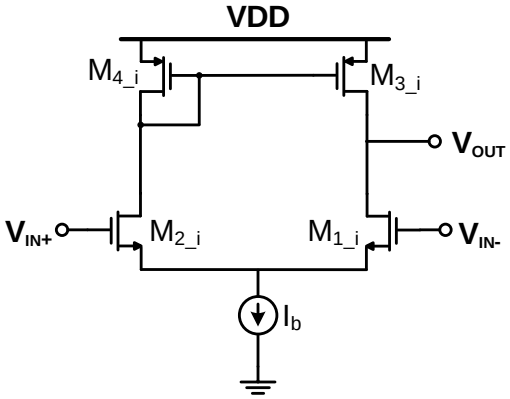


Figure 3.10: Second and third stages differential amplifiers schematic.

designed as a rail-to-rail input folded cascode amplifier shown in Fig. 3.9, while the second and third stages are simple differential amplifier illustrated in Fig. 3.10 (they will be discussed in detail later).

The high number of stages is due to the high gain requirement, typical for instrumentation amplifier together with low offset and 1/f noise requirements. Since ultra-scaled technologies are characterized by a reduced intrinsic gain, as already discussed in the first chapter, a horizontal gain distribution is mandatory in this systems, in order to obtain high DC gain. Moreover MOS transistors operating in subthreshold region must be adopted, because of the low voltage, reduced swing, reduced supply-threshold voltage ratio constraints which characterize scaled technologies as the CMOS 28nm and analysed in the first chapter. In fact, exploitation of

the subthreshold region increases signal swing, improving dynamic range, exhibits higher MOS transconductance efficiency g_m/I_D and lower distortion. The drawbacks of working in that region are larger current mismatch and reduced bandwidth. About the mismatch, in this case it is not a problem, since a proper dynamic offset compensation technique is adopted; regarding the low bandwidth, in this type of applications (i.e. biomedical, instrumentation, sensors), high frequency operation is not a requirement and a few kHz-bandwidth is generally enough. In fact, the main improvement brought by ultra-scaled technology, the high transition frequency, in this type of systems is not really necessary due to the low-frequency operation. Nevertheless in mainly mixed-signal systems [33], where signal processing requires high frequency performance, the readout electronics often consists of an instrumentation amplifier that precedes an ADC. Since the RF front-end drives the choice of deep sub-micron technologies, it will be the same for the analog baseband front-end. For this reason, the design of a chopper amplifier in ultra-scaled technology is an interesting research activity.

The typical design procedure for multi-stage amplifiers working in strong inversion cannot be adopted in this case, because of the different behaviour of transistors in the sub-threshold region. In particular, in the subthreshold regime, the drain current I_D and the threshold voltage V_{TH} for an n-channel MOS are [38][39]:

$$I_D = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left(1 - e^{\frac{-V_{DS}}{nV_T}}\right) \approx I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_T}} \tag{3.4}$$

$$V_{TH} = V_{TH0} - \lambda_D V_{DS} - \lambda_B V_{BS} \tag{3.5}$$

where I_0 is a technology-dependent parameter, W/L is the aspect ratio of the transistor, V_{GS} and V_{DS} are the gate-source and drain-source voltages respectively, n is the subthreshold slope constant which depends on technology, V_T is the thermal voltage, V_{TH0} is the threshold voltage at room temperature with zero bias ($V_{BS} = 0V$), and λ_D and λ_B are the Drain-Induced Barrier Lowering (DIBL) and Body effect coefficients respectively. From Eqs. 3.4 and 3.5, the small signals transistor parameters can be derived for the subthresold region; they are summarized in Table 3.1, compared with their value in saturation region of strong inversion. In Table 3.1 also the power spectral density for the input referred noise (thermal noise) $S_{n,in}$ is indicated in both cases (in the expressions shown in table, $K = \mu_n C_{ox}$, λ is the channel length modulation coefficient, T is the absolute temperature, k_B is the Boltzmann constant and q is the elementary charge).

Considering Eqs. 3.4 and 3.5 together with the expressions listed in Table 3.1 and the guidelines given in [39][40] about the opamp design in subthreshold region, the transfer function of the circuit can be written as:

$$H(s) = \frac{A_0}{\left(1 + \frac{s}{p_d}\right)} \frac{N(s)}{D(s)} \tag{3.6}$$

where A_0, p_d, N(s) and D(s) are DC gain, dominant pole, numerator and denominator, respectively. They are given by:

	Subthreshold	Strong inversion
$g_m = \frac{\delta I_D}{\delta V_{GS}}$	$\frac{I_D}{nV_T}$	$\sqrt{\frac{2KWI_D}{L}}$
$r_{DS} = \frac{\delta V_{DS}}{\delta I_{DS}}$	$\frac{nV_T}{I_D \lambda_D}$	$\frac{1}{\lambda I_D}$
$A_0 = g_m r_{DS}$	$\frac{1}{\lambda_D}$	$\frac{1}{\lambda}\sqrt{\frac{2KW}{I_D L}}$
$S_{n,in}$	$\frac{2q}{I_D}(nV_T)^2$	$\frac{8k_B T}{3}\sqrt{\frac{L}{2KWI_D}}$

Table 3.1: Small signals transistor parameters (saturation region).

$$A_0 = -g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3} = \frac{1}{(2\lambda_{14_1}\lambda_{12_1})(\lambda_{1_2}+\lambda_{3_2})(\lambda_{1_3}+\lambda_{3_3})} \tag{3.7}$$

$$p_d \approx \frac{1}{C_{M1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3}} \tag{3.8}$$

$$N(s) = 1 - \frac{C_{M2}}{g_{m3}}s - \frac{C_{M1}C_{M2}}{g_{m2}g_{m3}}s^2 \approx 1 - \frac{C_{M1}C_{M2}}{g_{m2}g_{m3}}s^2 \tag{3.9}$$

$$D(s) = 1 + \left(\frac{C_{M2}}{g_{m2}} - \frac{C_{M2}}{g_{m3}}\right)s + \frac{C_{M2}C_L}{g_{m2}g_{m3}}s^2 \tag{3.10}$$

where g_{mi} and R_{oi} are the transconductance and the output resistance of the i-th stage, C_L is the load capacitance and the factor λ_{n_i} represents the DIBL effect coefficient of transistor M_n of the i-th stage (as illustrated in Figs. 3.9 and 3.10). Eq. 3.7 relates the DC gain only to the λ values of the contributing transistors, which are related to transistors lengths. As a consequence, the minimum lengths of the involved mosfets can be estimated in order to reach the desired DC gain. From Eq. 3.10, there are two LHP non-dominant complex and conjugated poles that can be expressed as:

$$p_{2,3} \simeq -\frac{g_{m3}}{2C_L}\left(1 + \sqrt{1 - 4\frac{\frac{g_{m2}}{C_{M2}}}{\frac{g_{m3}}{C_L}}}\right) \tag{3.11}$$

and two zeros real and opposite, given by Eq. 3.12, whose phase contribution is negligible and also their gain contribution if they are greater than the UGB.

$$z_{1,2} \approx \pm\sqrt{\frac{g_{m2}g_{m3}}{C_{M1}C_{M2}}} \tag{3.12}$$

The amplifier specifications used as starting point for the design are listed in Table 3.2. The procedure starts from the noise requirement; as well known, the noise in multistage amplifiers is dominated by the first stage, which in this case is a rail-to-rail

Parameter	Value
Technology	CMOS 28nm
Supply voltage V_{DD}	0.9 V
Capacitive load C_L	100 pF
Input referred noise IRN	150 nV/$\sqrt{Hz}$
Bandwidth GBW	340 kHz
Phase Margin Φ	70 °
DC Gain A_0	110 dB

Table 3.2: Chopper amplifier specifications.

Parameter	Value
I_b	500 nA
g_{m1}	15 μA/V
g_{m2}	15 μA/V
g_{m3}	500 μA/V
A_{01}	50 dB
A_{02}	25 dB
A_{03}	35 dB
C_{M1}	7 pF
C_{M2}	2 pF

Table 3.3: Amplifier dimensioning.

folded cascode working in subthreshold region. Hence the input thermal noise PSD can be expressed as:

$$S_{n,in} = 4\frac{qn^2V_T^2}{I_b}\left[1 + \frac{I_{17,18}}{I_b} + \frac{I_{11,12}}{I_b}\right] \tag{3.13}$$

where n has been considered equal for NMOS and PMOS to 1.35, I_i is the current flowing through the i-th transistor. About the bandwidth specification, it can be expressed as follows:

$$GBW = \frac{g_{m1}}{2\pi C_{M1}} = \frac{I_b}{2\pi n V_T C_{M1}} \tag{3.14}$$

According to Eqs. 3.4 - 3.14 and Table 3.1, the resulting opamps small signal parameters and capacitors value are summarized in Table 3.3. Notice that the higher value of g_{m3} than $g_{m1,2}$ is due to the large load capacitor C_L to be driven, while the Miller capacitance C_{M2} choice derives from the phase margin specification.

Stage 1

As mentioned before, the first stage is an input rail-to-rail folded cascode amplifier. This choice has been done in order to implement an input common-mode rail-to-

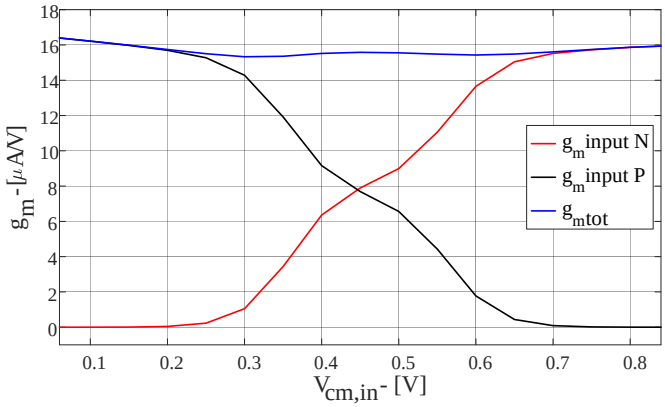


Figure 3.11: Rail-to-rail operation of the input stage.

rail capability and maximize the Signal-to-Noise Ratio (SNR), since ultra-scaled technologies are characterized by a small allowable signal swing. The rail-to-rail operation is guaranteed by the use of a complementary input stage [41], which means an input stage with both n-ch and p-ch input pairs, as shown in Fig. 3.9. This technique ensures that above the entire common mode range there is always at least an input pair operating:

- for input common-mode close to either supply voltage, only one input pair is active and the total transconductance is the g_m of the correspondent input transistors;
- in the middle voltage range, both input pairs work and the total transconductance is doubled.

However, in a rail-to-rail operation, it is necessary to hold every performance parameter constant over the entire input common mode range, in particular DC gain and bandwidth, which highly depend on the input transconductance. For this reason it is necessary to implement specific techniques that keep the input g_m constant for the entire common mode range. There are several constant g_m techniques in literature [42][43][44][45][46], which uses maximum/minimum selection circuits or input DC level shifter. Since the transistors work in subthreshold region, where the g_m is proportional to the drain current (Table 3.1), the basic idea in this design is to double the input g_m over the entire common-mode interval, also when only one active pairs is working, simply doubled the bias currents. In particular, as illustrated in Fig. 3.9, current switches M_5 and M_6 are used:

- when the input common-mode is close to the V_{DD}, only n-type input pair works and the bias current of the input pair off flows through current switch M_6, doubling the total current and also the total g_m;

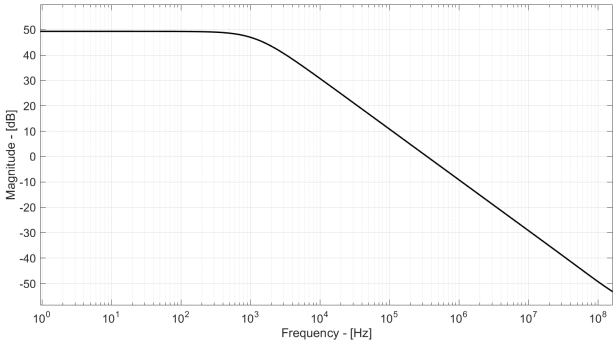


Figure 3.12: Transfer function of the first stage.

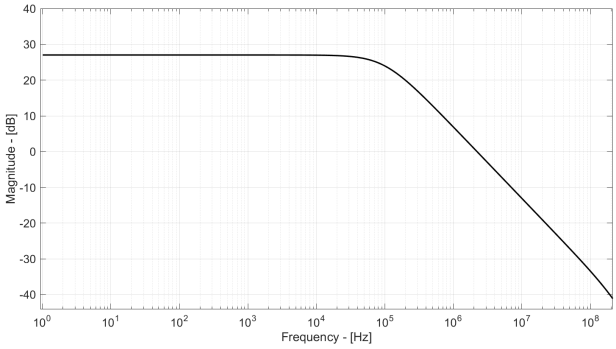


Figure 3.13: Transfer function of the second stage.

- when the input common-mode is close to ground, only p-type input pair works and the bias current of the input pair off flows through current switch $\mathrm{M_5}$, doubling the total current and also the total $\mathrm{g_m}$.

Figure 3.11 illustrates the simulated input total $\mathrm{g_m}$ kept almost constant to about 15 µA/V, as a function of the input common-mode voltage. The transfer function is shown in Fig. 3.12, with a DC Gain of 49 dB and a UGB of 350 kHz. The current consumption is 26 µA.

Stage 2 and 3

The second and third stages are simple differential opamp with n-type input pair, already illustrated in Fig. 3.10. The bias currents are 1 µA and 33 µA for second and third opamp respectively. Figures 3.13 and 3.14 illustrate their transfer function. The second stage exhibits a DC Gain of 27 dB with 2.2 MHz of UGB, while the third stage is characterized by 35 dB DC Gain and a UGB of 780 kHz.

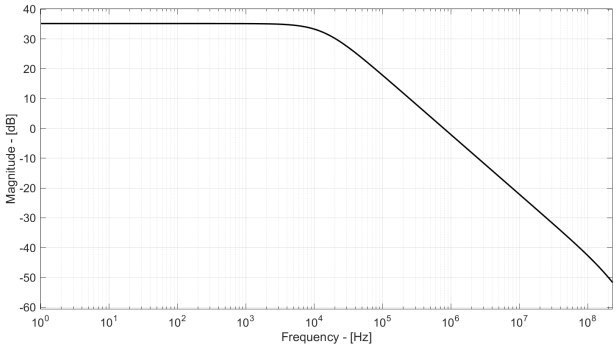


Figure 3.14: Transfer function of the third stage.

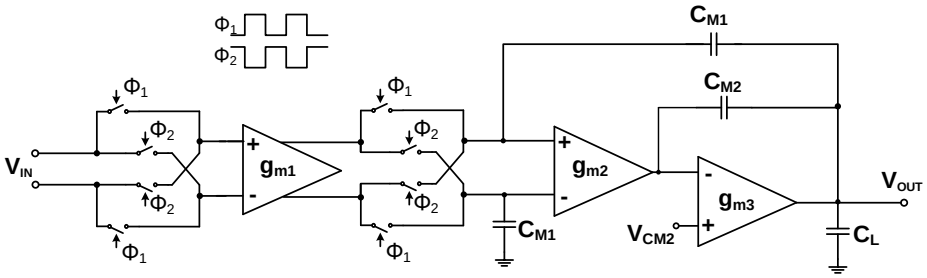


Figure 3.15: Chopped amplifier schematic.

3.2.2 Chopped opamp design

The complete schematic of the chopper amplifier is shown in Fig. 3.15. Two choppers are placed across the first gain stage in order to reduce its offset and flicker noise contribution, with a lower corner frequency. Since the amplifier need to handle rail-to-rail input signals, every switch of the chopper has been realized with a transmission gate structure [47], shown in Fig. 3.16, which is made of both PMOS and NMOS devices. In general, they should be driven with four non-overlapping phases to drive correctly the two modulators and to prevent noise leakage. This clock contains a short period of time where neither signal is propagated through the chopper block to avoid noise leakage during switching. The phases should also be close to a 50% duty cycle for proper modulation. Moreover, the use of complementary switches with scaled channel length helps to reduce charge injection, since the gate-source capacitances are small and the charge injected by the two transistors approximately cancels each other. In particular, aspect ratios of 1 µm/30 nm and 2 µm/30 nm have been used for complementary switches NMOS and PMOS, respectively.

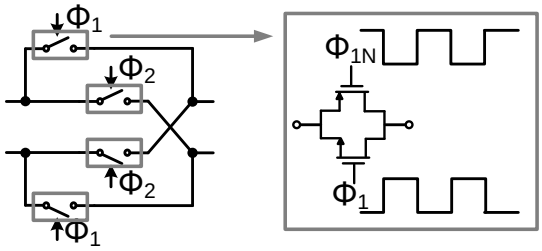


Figure 3.16: Transmission gate structure used for chopper switches.

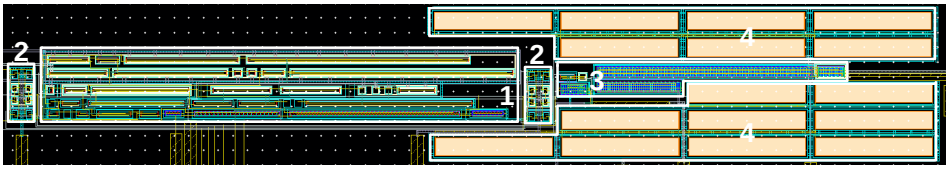


Figure 3.17: Chopper amplifier layout.

3.2.3 Layout

After the amplifier design, the layout of the entire circuit in CMOS 28nm technology has been carried out. The total area is 0.014 mm^2. Figure 3.17 shows the layout of the chopper amplifier, highlighting the different blocks:

1. The input stage with a 0.0038 mm^2 of area;

2. Choppers, which occupies together an area of 0.0003 mm^2;

3. Second and third stages for an area of 0.0008 mm^2;

4. Miller capacitances C_{M1} and C_{M2}, realized as parallel of 1 pF minimum capacitance, with a total 0.0063 mm^2 of area.

3.2.4 Results

In Fig. 3.18 a diagram of the chopper amplifier with all input and output pins is shown. A list of them with their type and functionality is present in Table 3.4.

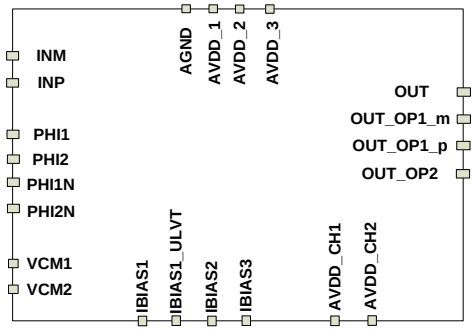


Figure 3.18: Chopped amplifier pin diagram.

Pin name	Description	Value
INM	Amplifier negative input	Analog In
INP	Amplifier positive input	Analog In
PHI1	Phase 1 for the choppers	Digital In
PHI2	Phase 2 for the choppers	Digital In
PHI1N	Complementary Phase 1 for the choppers	Digital In
PHI2N	Complementary Phase 2 for the choppers	Digital In
VCM1	Common mode voltage for stage 1	450 mV
VCM2	Common mode voltage for stage 3	450 mV
IBIAS1	Stage 1 first bias current	100 nA
IBIAS1_ULVT	Stage 1 second bias current	100 nA
IBIAS2	Stage 2 bias current	1 μA
IBIAS3	Stage 3 bias current	1 μA
AVDD_CH1	Supply voltage for chopper 1	0.9 V
AVDD_CH2	Supply voltage for chopper 2	0.9 V
AVDD_1	Supply voltage for stage 1	0.9 V
AVDD_2	Supply voltage for stage 2	0.9 V
AVDD_3	Supply voltage for stage 3	0.9 V
OUT	Amplifier Output (to be connected to 100 pF)	Analog Out
OUT_OP1_m	Negative output of stage 1 after chopper	Analog Out
OUT_OP1_p	Positive output of stage 1 after chopper	Analog Out
OUT_OP2	Output of stage 2	Analog Out
AGND	Ground voltage	Analog In

Table 3.4: Pin list, with description and set up in nominal value.

Post-layout simulations

The total current consumption is 60 µA. Figure 3.19 shows the simulated transfer function in comparison with the expected one. The final DC Gain is 106 dB, about

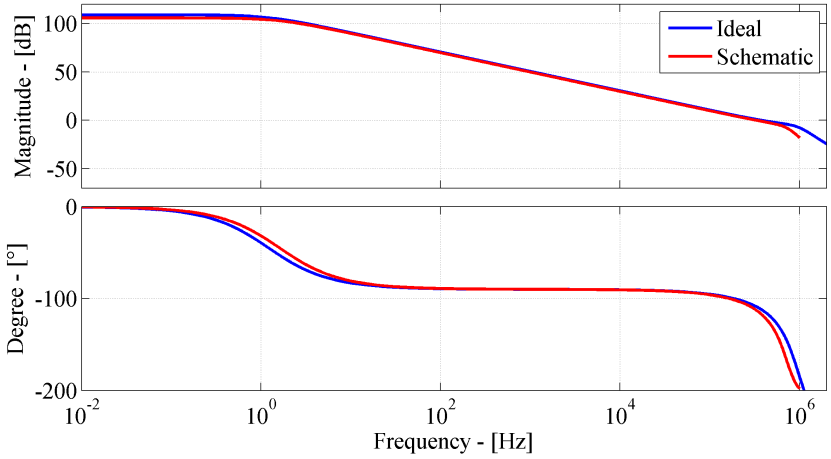


Figure 3.19: Chopped amplifier bode diagram.

4 dB below the expected 110 dB, due to the chopping effect. The GBW is 329 kHz, with a phase margin of 68 ° and the dominant pole is at about 1.2 mHz.

Figure 3.20 shows the low frequency periodic noise simulation in case of continuous-time and chopped amplifier. The result is a decrease of the corner frequency from 11.5 kHz to 50 Hz, with consequently a reduction of the flicker noise.

The result of the input referred offset distribution after 50 Montecarlo runs is illustrated in the histogram in Fig. 3.21; the standard deviation is 2.2 µV.

Figure 3.22 shows the transient step response in unity-gain closed-loop configuration.

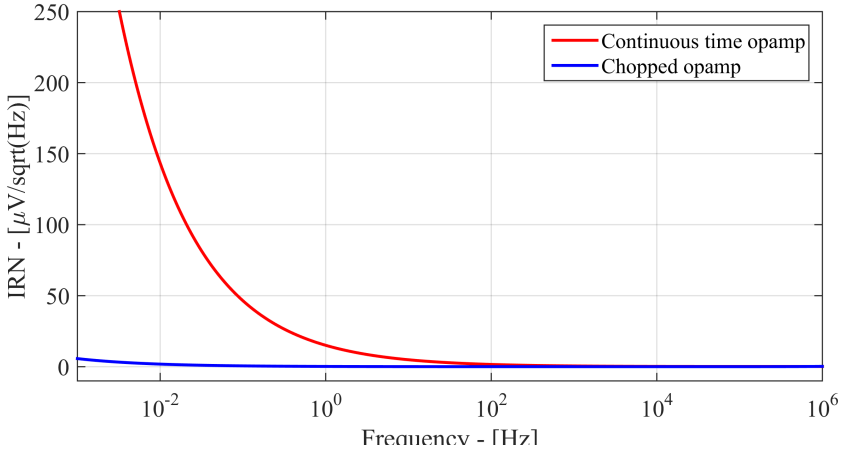


Figure 3.20: The periodic noise simulation result for the continuous-time and the chopped amplifier.

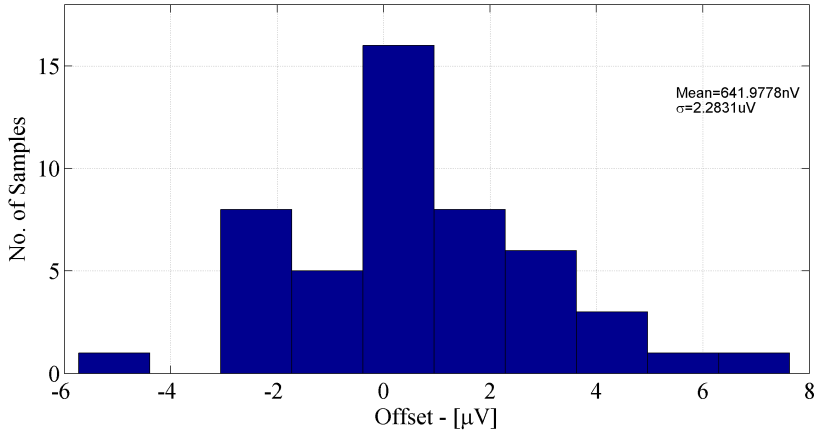


Figure 3.21: Input referred offset distribution of the chopper amplifier.

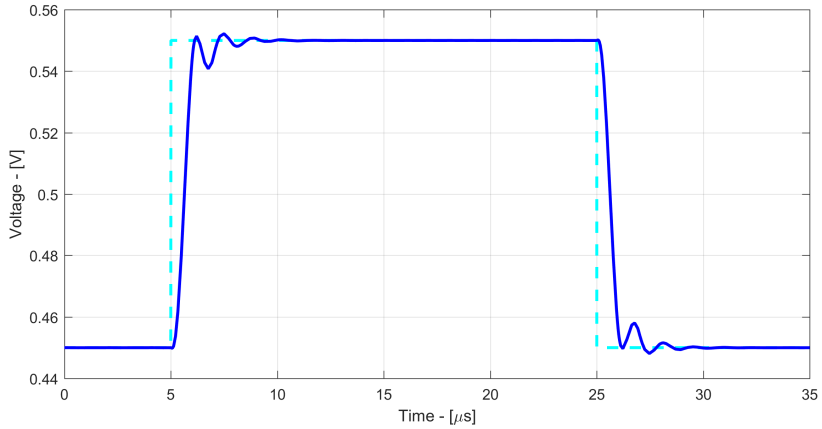


Figure 3.22: Chopped amplifier step response.

Measurements

In order to characterize the prototype, a board has been designed with a proper and dedicated software named Altium® . A photograph of the board is shown in Fig. 3.23. For this prototype, the voltage references have been provided externally with resistive dividers, while the four non-overlapping phases of the choppers have been generated externally through a FPGA, in on and off state. Moreover, the board allows to measure the chopper amplifier in different configurations, buffer or inverting/non-inverting with a gain of 2/3.

Unfortunately, some problems have been faced during the measurement phase, most of them related to the chopper four phases generation. In fact, the direct connection of the FPGA pins to the chopper switches leads to extra impedance parasitic

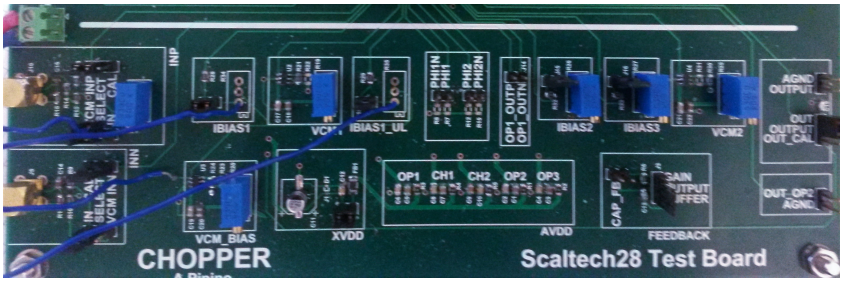


Figure 3.23: Photograph of the chopper amplifier test board.

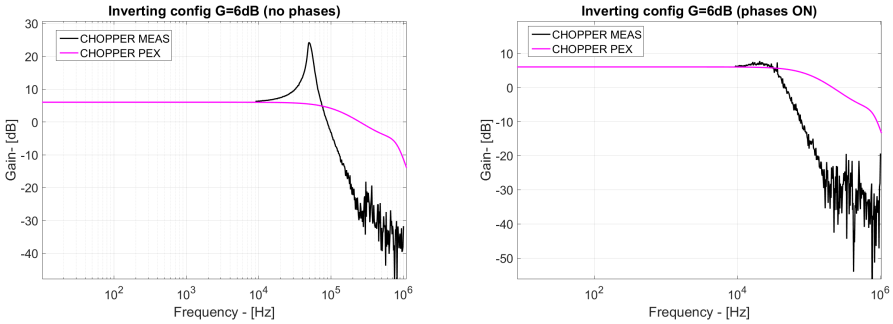


Figure 3.24: Measured frequency response with the amplifier in inverting configuration and 6 dB of gain compared to simulations: phases off (right), phases on (left).

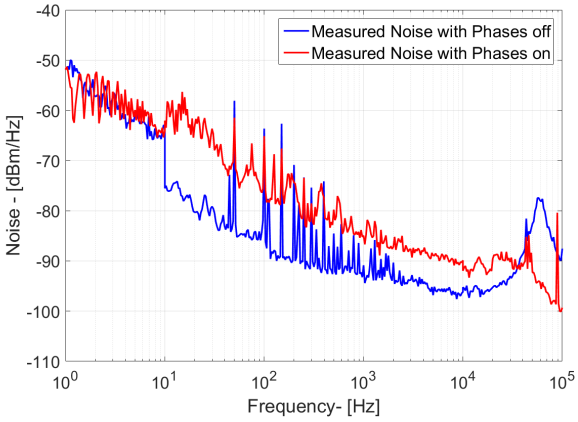


Figure 3.25: Noise measurement with phases off and off.

loads and cross interferences with inputs and outputs of the first stage. The first consequence is that the input stage does not work properly when the choppers are on, but more bias current is necessary. However, the measured frequency response

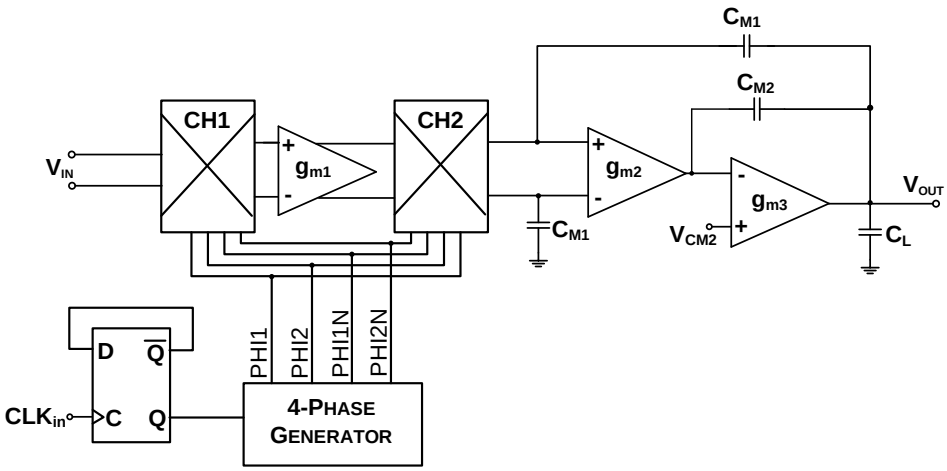


Figure 3.26: Diagram of the chopper amplifier second prototype.

in buffer configuration (or others) has a reduced bandwidth than the simulated case and a high not expected Q-peaking appears, as shown in Fig. 3.24. Second, the chopper effect on offset and flicker noise with/without choppers is not evident, as demonstrated in Fig. 3.25. This problem has been verified also through a Cadence® simulation, adding some parasitic loads to the phases inputs.

For this reason, a second prototype has been integrated, including a block for the internal generation of the four non-overlapping phases for the choppers.

3.3 Chopper Amplifier: Prototype 2

The second prototype of the Chopper Amplifier, integrated with the same 28nm CMOS technology used for the first prototype, includes the four-phase non-overlapping clock signal generator. Other improvements to the circuit are the use of resistive dividers for the reference voltages and buffers to route out the output signals of the internal amplifiers. The final schematic of the second prototype is shown in Fig. 3.26.

3.3.1 Four-phase Generator

The circuit diagram of the four-phase non-overlapping clock signal generator [48] is illustrated in Fig. 3.27. In order to obtain equal pulse widths of complementary clock signals with 50% of duty cycle, the input reference clock is applied to a divide-by-2 circuit based on a D flip-flop. The resulting signal and its complementary are then applied to a cross-coupled section including two NOR gates, two phase delay blocks and two phase disoverlap blocks. The phase delay blocks are realized by two inverters connected in series with 1 pF grounded capacitor between them, as indicated in Fig. 3.27. Each phase disoverlap block includes a series of four inverters with 1 pF

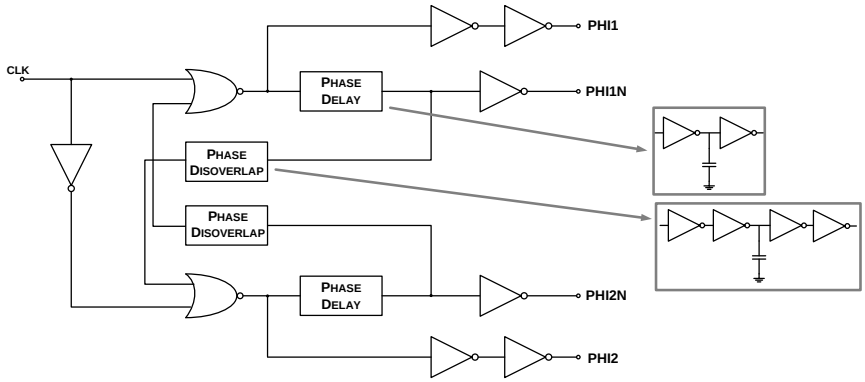


Figure 3.27: Four-phases generator schematic.

grounded capacitor between the two couples. These delay blocks determine the time disoverlap between the four-phase signals, required to drive the four complementary switches.

Figure 3.28 shows the plot of the phase generator output signals with a frequency of 150 kHz. The minimum delay between the switching instants is about 1.5 ns, as highlighted in Fig. 3.29.

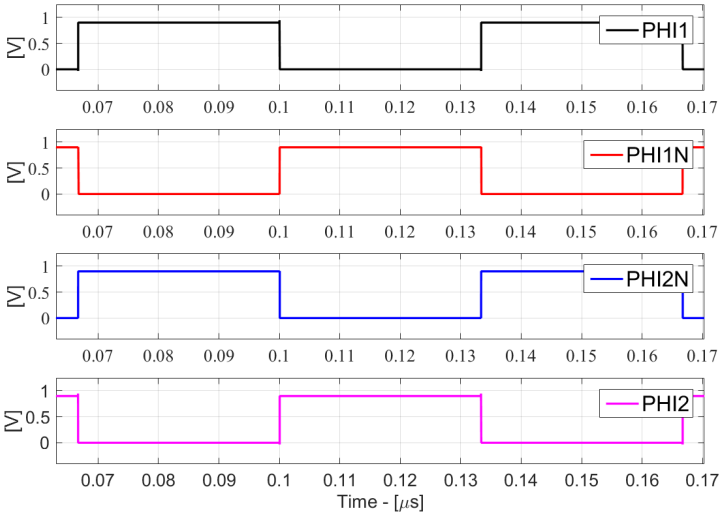


Figure 3.28: Four phases time transient.

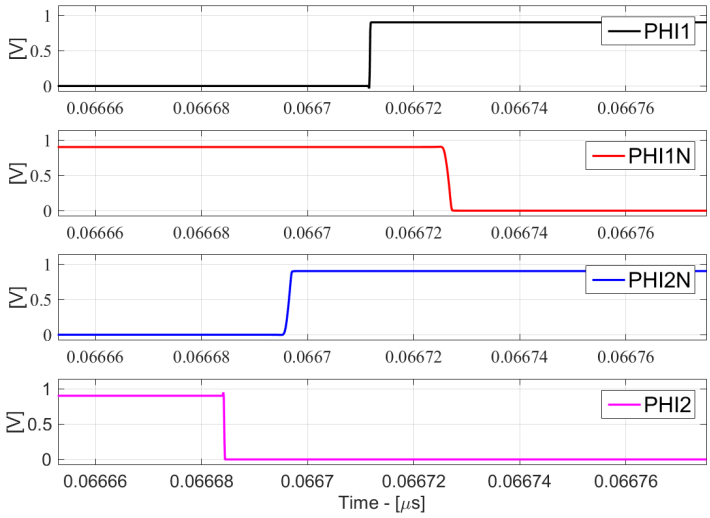


Figure 3.29: Detail of the time disoverlap between the four phases.

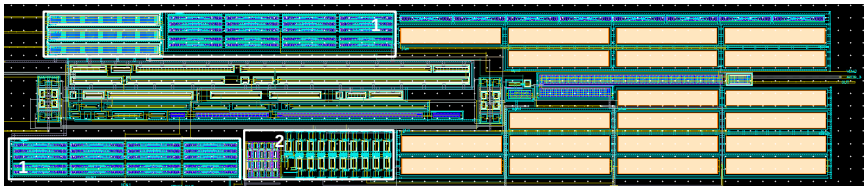


Figure 3.30: Layout of the chopper amplifier second prototype.

3.3.2 Layout

The layout of the second prototype in CMOS 28nm technology has a total area of 0.023 mm^2. Figure 3.30 shows the layout of the chopper amplifier, highlighting the new blocks:

1. D flip-flop and four-phase generator for an area of 0.0012 mm^2;
2. Resistive dividers and buffers with an area of 0.0041 mm^2.

3.3.3 Results

The pin diagram of chopper amplifier second prototype is the same of the first one, except for the phases pins not present in this case. A list of the pins with their type and functionality is present in Table 3.5.

The total current consumption is 70 µA. Figure 3.31 shows gain and corner frequency for different chopping frequency. There is a trade-off between those factors; the chosen chopping frequency is 150 kHz because ensures good compromise be-

Pin name	Description	Value
INM	Amplifier negative input	Analog In
INP	Amplifier positive input	Analog In
VCM1	Common mode voltage for stage 1	450 mV
VCM2	Common mode voltage for stage 3	450 mV
IBIAS1	Stage 1 first bias current	1 μA
IBIAS1_ULVT	Stage 1 second bias current	1 μA
IBIAS2	Stage 2 bias current	2 μA
IBIAS3	Stage 3 bias current	1 μA
AVDD_CH1	Supply voltage for chopper 1	0.9 V
AVDD_CH2	Supply voltage for chopper 2	0.9 V
AVDD_1	Supply voltage for stage 1	0.9 V
AVDD_2	Supply voltage for stage 2	0.9 V
AVDD_3	Supply voltage for stage 3	0.9 V
OUT	Amplifier Output (to be connected to 100 pF)	Analog Out
OUT_OP1_m_buf	Negative output of stage 1 after chopper&buffer	Analog Out
OUT_OP1_p_buf	Positive output of stage 1 after chopper&buffer	Analog Out
OUT_OP2_buf	Output of stage 2 after buffer	Analog Out
AGND	Ground voltage	Analog In

Table 3.5: Pin list, with description and set up in nominal value.

tween gain (108.4 dB) and corner frequency (560 mHz).

Figure 3.32 shows the amplifier transfer function. The final DC Gain is 108.4 dB, the GBW is 375 kHz, with a phase margin of 76 ° and the dominant pole is at about 1.3 Hz.

Figure 3.33 shows the low frequency periodic noise simulation in case of continuous-time and chopped amplifier with 150 kHz chopping frequency. The result is a decrease of the corner frequency from 27.5 kHz to 560 mHz, with consequently a reduction of the flicker noise. The input-referred noise at 10 kHz is 147 nV/$\sqrt{\text{Hz}}$.

The result of the input referred offset distribution after 50 Montecarlo runs is illustrated in the histogram in Fig. 3.34; the standard deviation is 26 µV.

Next step of measurements could validate the proposed architecture and design procedure, showing the potentialities of a chopper amplifier in 28nm CMOS technology.

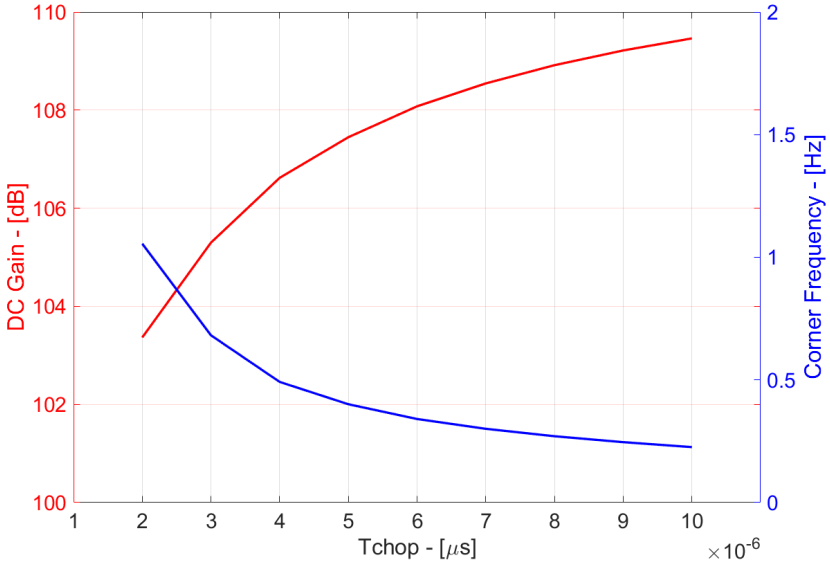


Figure 3.31: Simulated DC Gain and corner frequency for different chopping period.

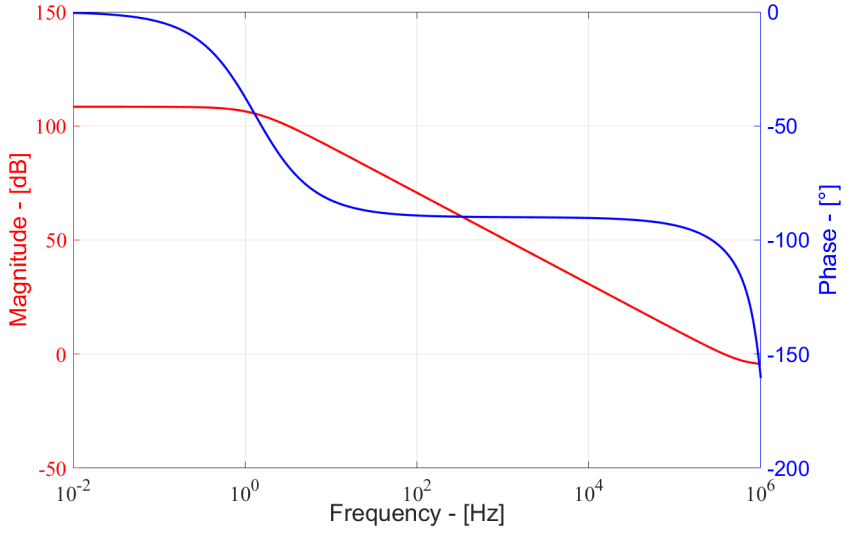


Figure 3.32: Bode diagram of the chopper amplifier second prototype.

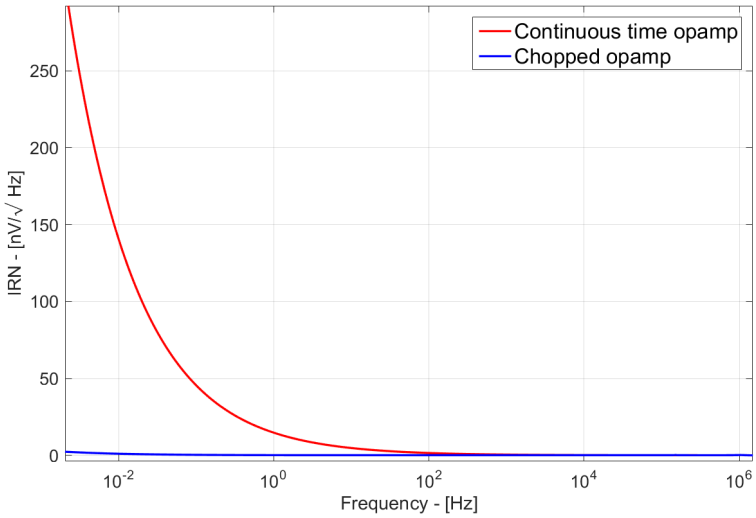


Figure 3.33: Input referred noise of the chopper amplifier second prototype.

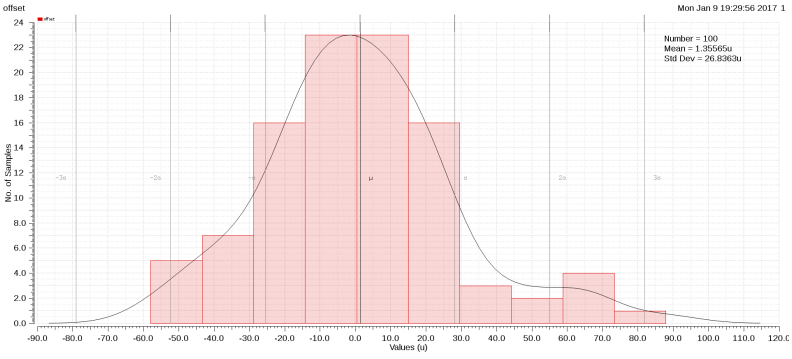


Figure 3.34: Input referred offset distribution of the chopper amplifier second prototype.

Chapter 4

Papers

A paper and a poster on the first prototype of the Chopper amplifier are listed in the next pages. They have been presented at the IEEE International Conference on Electronics, Circuits and Systems (ICECS 2015) held in Cairo (Egypt).

4.1 IEEE ICECS 2015: Paper

A Rail-to-Rail-Input Chopper Instrumentation Amplifier in 28nm CMOS

A. Pipino, A. Pezzotta, F. Resta, M. De Matteis and A. Baschirotto
Department of Physics, University of Milano-Bicocca, Italy
Email: a.pipino1@campus.unimib.it

***Abstract*—This paper presents a chopper instrumentation amplifier designed in 28nm CMOS technology. The operational amplifier has a rail-to-rail folded cascode input stage, which ensures a constant g_m over the available common-mode range. It is characterized by a Nested Miller compensation. All transistors operate in sub-threshold region; thus the opamp has been designed through a specific procedure for sub-threshold operation. The chopper technique is exploited to reduce the input referred offset and noise. The circuit operates with 0.9V supply voltage and exhibits a simulated 106dB DC gain and 329kHz GBW. Montecarlo simulations demonstrate an offset distribution with 2.2µV standard deviation. The input noise spectral density is equal to 27nV/√Hz, giving a noise efficiency factor of 8.**

***Keywords*—chopper technique, nested miller compensation, sub-threshold operation, instrumentation amplifier**

I. INTRODUCTION

Instrumentation Amplifiers (IAs) are the key building blocks in sensor and monitoring applications. The analog input signal to be amplified is usually a low frequency sub-mV signal. Accordingly, IAs must be designed to achieve low input referred offset and noise, especially flicker noise, and high gain, in order not to compromise system performance. Autozero or chopper techniques are often exploited [1]-[3] to meet the low offset requirement. In particular chopping is a modulation technique in which the signal and the offset are modulated to different frequencies and in this way the offset, as well as flicker noise, can be filtered out.

Nowadays deep nanometers CMOS technologies with sub-1V supply voltages are available. Scaling-down is not a primary requirement in chopper IA implementation. First of all, it brings to a reduction of the supply voltage, but threshold voltages doesn't decrease with the same trend. The decreasing V_{dd}/V_{th} ratio results in operating point issues and a smaller allowable signal swing. Exploitation of the sub-threshold (or weak inversion) region and rail-to-rail input stage operation [4]-[8] address both problems and allow to use all the possible voltage headroom, improving dynamic range and signal-to-noise ratio. Moreover the intrinsic gain decreases and consequently distributing horizontally the gain is mandatory to match requirements. On the other hand scaled-down technologies enable to design choppers with better performance in terms of charge injection, implementing minimum size transistors. The main improvement brought by ultra-scaled technology, the high transition frequency, in this type of systems is not necessary due to the low-frequency operation. Nevertheless in mainly mixed-signal systems [9], where signal processing requires high frequency performance, analog circuits must comply with these issues. In fact the readout electronics in some systems often consists of an IA that precedes an ADC. The RF front-end requires an efficient implementation in terms of area and power efficiency and for this reason it drives the choice of deep submicron technologies, in which also the analog part must be realized.

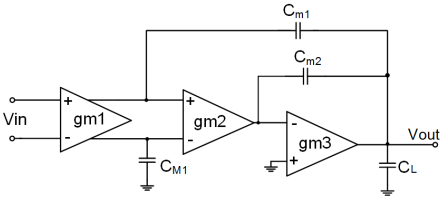


Fig. 1. Continuous time opamp

In this scenario, this paper presents a three-stage chopper amplifier working in sub-threshold region, with a Nested Miller compensation (NMC) and a rail-to-rail folded cascode input stage. The amplifier, designed in 28nm CMOS technology, is able to drive 200pF of capacitive load.

This paper is organized as follow. Section II describes the design of the opamp using specific equations for sub-threshold region and the chopper schematic. Section III shows the simulation results. Finally conclusions are carried out in Section IV.

II. OPAMP CIRCUITAL TOPOLOGY

Figure 1 shows the scheme of the continuous-time opamp only, characterized by three stages and a classic Nested Miller compensation. The first stage, whose schematic is shown in fig. 2, is a rail-to-rail input folded cascode opamp. The complementary input stage ensures a rail-to-rail input range with constant transconductance g_m, thanks to the control of bias currents made by two current switches (M6 and M5). The second and third stages are simple differential stages with active load, as shown in fig. 3.

A. Continuous Time Opamp Design

The typical design procedure for multi-stage amplifiers working in strong inversion cannot be adopted in this case, because of the different behavior of the sub-threshold region.

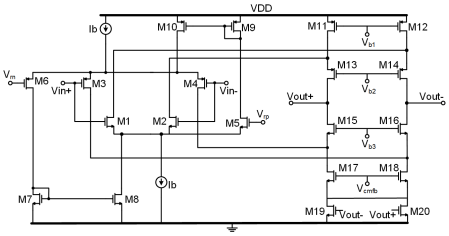


Fig. 2. Schematic of the rail-to-rail folded cascode stage.

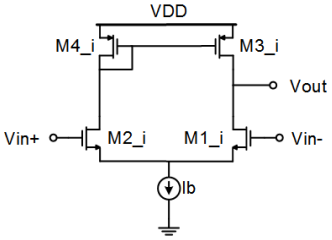


Fig. 3. Schematic of the second and third stage (i=2,3).

Considering the guidelines given in [5][10] for opamp analysis in sub-threshold region, the loop gain transfer function of the circuit can be written as:

$$H(s) = \frac{A_0}{\left(1+\frac{s}{p_d}\right)}\frac{N(s)}{D(s)} \tag{1}$$

where DC gain, dominant pole, numerator and denominator are given by

$$A_0 \approx -g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3} \approx \approx -\frac{1}{(2\lambda_{14\_1}\lambda_{12\_1})(\lambda_{1\_2}+\lambda_{3\_2})(\lambda_{1\_3}+\lambda_{3\_3})} \tag{2}$$

$$p_d \approx \frac{1}{C_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3}} \tag{3}$$

$$N(s) = 1-\frac{C_{m2}}{g_{m3}}s-\frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2 \approx 1-\frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2 \tag{4}$$

$$D(s) = 1+\left(\frac{C_{m2}}{g_{m2}}-\frac{C_{m2}}{g_{m3}}\right)s+\frac{C_{m2}C_L}{g_{m2}g_{m3}}s^2 \tag{5}$$

Note that the DC gain is related to the DIBL effect coefficient of transistors and, consequently, to the transistors lengths. According to this, their lengths have been estimated in order to obtain a gain distribution of 50dB, 25dB and 35dB for the first, second and third stage respectively. From eq.(5), there are two LHP non-dominant complex and conjugated poles that can be expressed as

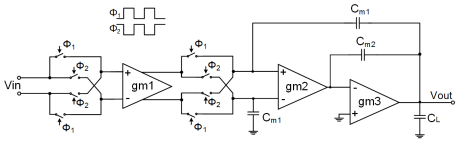


Fig. 4. Schematic of the chopper amplifier.

$$p_{2,3} \cong -\frac{g_{m3}}{2C_L}\left(1\pm\sqrt{1-4\frac{\frac{g_{m2}}{C_{m2}}}{\frac{g_{m3}}{C_L}}}\right) \tag{6}$$

and two zeros real and opposite, given by (7), whose phase contribution is negligible:

$$z_{1,2} \approx \pm\sqrt{\frac{g_{m2}g_{m3}}{C_{m1}C_{m2}}} \tag{7}$$

Also their gain contribution can be negligible if they are greater than the GBW.

Let assume as starting points of the design an input referred noise IRN of 150nV/√Hz and the desired GBW of 340kHz. Noise is dominated by the first stage, which in this case is a rail-to-rail folded cascode working in sub-threshold region, shown in fig. 2; hence the input thermal noise PSD can be expressed as [5]:

$$S_{n,in} = 4\frac{qn^2V_t^2}{I_b}\left[1+\frac{I_{17,18}}{I_b}+\frac{I_{11,12}}{I_b}\right] \tag{8}$$

where q is the electron charge, n is the sub-threshold slope that we approximate equal for NMOS and PMOS to 1.35, V_t is the thermal voltage and I_i is the current flowing through the i-th transistor. The GBW is:

$$GBW = \frac{g_{m1}}{2\pi C_{m1}} = \frac{I_b}{2\pi n V_t C_{m1}} \tag{9}$$

where g_{m1} and I_b are the transconductance and current of the first stage, and C_{m1} is the external Miller capacitor. According to the previous expressions, we set I_b, g_{m1} and C_{m1} respectively equal to 500nA, 15µA/V and 7pF. Then, g_{m3} has to be bigger than g_{m1} and g_{m2} (also equal to 15µA/V), since the load capacitor C_L is very large and equal to 100pF. Thus, g_{m3} has been set equal to 500 µA/V. Finally in order to have a phase margin Φ of about 70° [5], we set C_{m2} equal to 2pF.

B. Chopper Opamp

Figure 4 shows the overall chopper amplifier. The circuit has two chopper blocks across the first gain stage. In this way the signal is modulated, amplified and then demodulated again. The modulation is done by a square-wave signal with frequency f_{chop}, through a polarity-reversing switch. Offset and flicker noise, added by the first stage, are modulated once and shifted to high frequency. The results are less input offset

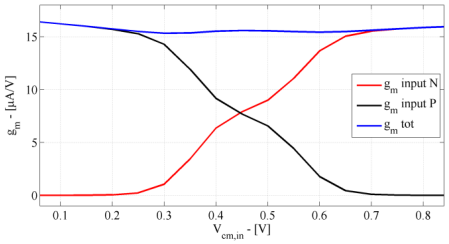


Fig. 5. Rail-to-rail operation of the input stage.

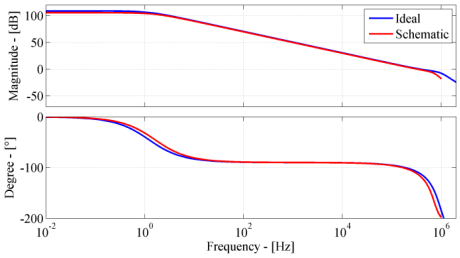


Fig. 6. Opamp transfer function.

voltage, a lower corner frequency and only a white noise floor. Since the first stage has a rail-to-rail input and in order to reduce charge injection, transmission gate (i.e. complementary) switches with minimum size transistors have been used. The chosen chopping frequency f_{chop} is 500kHz.

III. Post-Layout Simulation Results

The proposed chopper amplifier has been implemented using the 28nm CMOS technology with a supply voltage of 0.9V. The total current consumption I_{tot} is 60µA. The performance over the available common mode range are constant thanks to rail-to-rail input stage that maintains a constant g_{m1}, as shown in fig. 5.

Figure 6 shows the simulated transfer function in comparison with the expected one. It has about 106dB of DC gain instead of 110dB, probably due to the chopping effect, with a dominant pole at 1.2Hz. The GBW is 329kHz with a phase margin of about 68°. Figure 7 shows a low frequency periodic noise simulation with and without chopper. The result of the chopper operation is a lower corner frequency which scales from 11.5kHz to 50Hz, less flicker noise and also white noise that has a final value of 27nV/√Hz.

The histogram in fig. 8 shows the simulated input referred offset distribution after 50 Montecarlo runs of the circuit in inverting configuration. The obtained standard deviation is 2.2µV. The transient step response in unity-gain closed-loop configuration is reported in fig. 9 and it is characterized by a

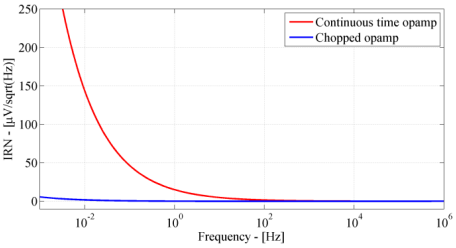


Fig. 7. Input referred noise voltage.

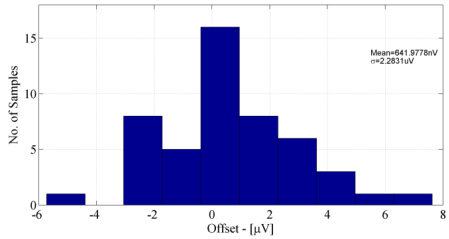


Fig. 8. Input referred offset distribution.

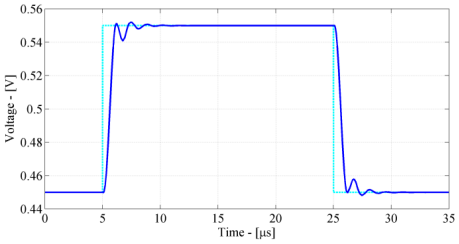


Fig. 9. Amplifier step response.

slew-rate SR of about 0.1V/µs. PSRR is reported in fig. 10, while CMRR is equal to 70dB.

In order to compare noise reduction due to the chopper technique with other works, the Noise Efficiency Factor [11] (NEF) is typically employed. It is defined as:

$$NEF = V_{n,in}\sqrt{\frac{2I_{tot}}{\pi V_t 4kT}} \qquad (10)$$

where $V_{n,in}$ is the input referred noise density, I_{tot} is the total current consumption, k is the Boltzmann constant and T is the absolute temperature. The resulting NEF is 8. The layout of the proposed amplifier is shown in fig. 11 and it occupies an area of 0.014mm^2.

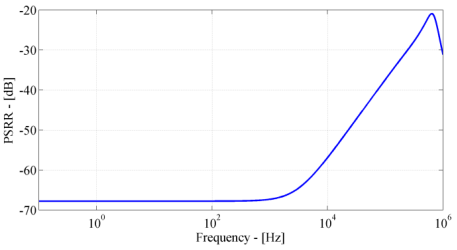


Fig. 10. PSRR frequency response.

Table I summarizes the main performance of the proposed chopper amplifier and provides a comparison with other similar works present in literature. Performance results to be competitive in terms of noise, offset and NEF, even if designed in a challenging scenario with an ultra-scaled technology. Moreover area occupation is 10 times smaller than other works.

IV. Conclusions

In this work a chopper instrumentation amplifier is presented, designed in a 28nm CMOS technology with 0.9V supply voltage. It is characterized by a rail-to-rail input stage, a Nested Miller compensation and the exploitation of the chopper technique in order to reduce input referred offset and noise. Due to the employment of an ultra-scaled technology, a careful design has been carried out since the operational amplifier works completely in sub-threshold region. The results are 106dB DC gain and 329kHz GBW with about 68° phase margin. The circuit operates with 500kHz chopping frequency and achieves a distribution of the offset voltage with 2.2µV standard deviation, obtained over the 50 available samples. The input referred noise density is 27nV/√Hz. Finally the proposed opamp achieves a NEF of 8.

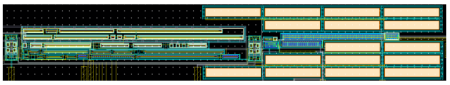


Fig. 11. Layout of the chopper amplifier.

TABLE I. COMPARISON WITH THE STATE OF ART CHOPPER AMPLIFIER

	This Work	[12]	[13]
Year	2015	2010	2010
Technology	28nm	0.18-0.5µm	0.7 µm
Supply voltage	0.9V	1.8/5V	5V
Chopping frequency	500kHz	500kHz	30kHz
DC Gain	106dB	168dB	>100dB
GBW	329kHz	260kHz	900kHz
Input referred offset standard deviation	2.2 µV	1.94 µV	2 µV
IRN	27nV/√Hz	27nV/√Hz	21nV/√Hz
Supply current	60µA	14.4 µA	143µA
Power	54µW	26/72µW	715µW
NEF	8	5.5	9.6
Area	0.014mm^2	1.14mm^2	1.8mm^2

References

[1] C. Enz and G. Temes, “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization”, Proceedings of the IEEE, vol. 84, no. 11, pp. 1584–1614, 1996.

[2] C. Enz, E. Vittoz, and F. Krummenacher, “A CMOS chopper amplifier,” IEEE J. Solid-State Circuit, vol. 22, no. 3, pp. 335–342, 1987.

[3] K. A. Makinwa, Dynamic offset compensated CMOS amplifiers. Springer, 2009.

[4] E. Vittoz and J. Fellrath, “CMOS analog integrated circuits based on weak inversion operations”, IEEE J. Solid-State Circuit, vol. 12, no. 3, pp.224-231, Jun. 1977.

[5] A. Grasso, D. Marano, G. Palumbo and S. Pennisi, “Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability”, IEEE Trans. on Circuits and Systems-I:Reg. Papers, vol. 62, no. 6, pp.1453-1462, May 2015.

[6] L. Magnelli, F. A. Amoroso, F. Crupi, G. Cappuccino, and G. Iannaccone, “ Desgin of a 75-nW, 0.5-V subthreshold complementary metal-oxide-semiconductor operational amplifier”, Int. J. Circuit Theor. Appl., vol. 42, no. 9, pp.967-977, Sept. 2014.

[7] T. Stockstad and H. Yoshizawa, “A 0.9-V 0.5-um rail-to-rail CMOS operational amplifier,” IEEE J. Solid-State Circuits, vol. 37, no. 3, pp. 286–292, Mar. 2002.

[8] S. Yan, J. Hu, T. Song, and E. Sanchez-Sinencio, “Constant-gm techniques for rail-to-rail CMOS amplifier input stages: a comparative study”, IEEE International Symposium on Circuits and Systems, 2005, pp. 2571–2574 Vol. 3, 2005.

[9] Q. Fan, F. Sebastiano, J. H. Huijsing and K. A. A. Makinwa, “A 1.8 W 60 nV Hz Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes”, IEEE J. Solid-State Circuits, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.

[10] S. P. A. D. Grasso, G. Palumbo, “Analytical comparison of frequency compensation techniques in three-stage amplifiers,” IEEE Journal of Solid-State Circuits, vol. 36, no. 1, pp. 53–80, 2008.

[11] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, “A micropower low-noise monolithic instrumentation amplifier for medical purposes,” IEEE J. Solid-State Circuits , vol. SC-22, pp. 1163–1168, Dec. 1987.

[12] M Belloni, E. Bonizzoni, A. Fornasari and F. Maloberti, “A Micropower Chopper-CDS Operational Amplifier”, IEEE J. Solid-State Circuits , vol. 45, no. 12, pp. 2521–2529, Dec. 2010.

[13] Q. Fan, J. H. Huijsing, and K. A. A. Makinwa, “A 21 nV/√Hz chopper-stabilized multipath current-feedback instrumentation amplifier with 2µV offset,” in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2010, pp. 80-81.

4.2 IEEE ICECS 2015: Poster

A Rail-to-Rail-Input Chopper Instrumentation Amplifier in 28nm CMOS

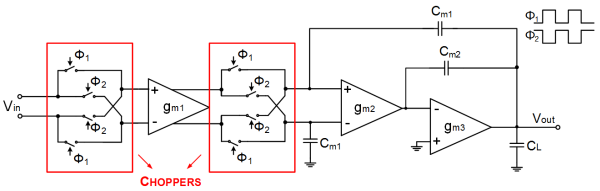
A. Pipino[1], A. Pezzotta[1], F. Resta[1], M. De Matteis[1] and A. Baschirotto[1]
[1]*Department of Physics & INFN, University of Milano-Bicocca, Italy*

Abstract

This paper presents a chopper instrumentation amplifier designed in 28nm CMOS technology. The operational amplifier has a rail-to-rail folded cascode input stage, which ensures a constant gm over the available common-mode range. It is characterized by a Nested Miller compensation. All transistors operate in sub-threshold region; thus the opamp has been designed through a specific procedure for sub-threshold operation. The chopper technique is exploited to reduce the input referred offset and noise. The circuit operates with 0.9V supply voltage and exhibits a simulated 106dB DC gain and 329kHz GBW. Montecarlo simulations demonstrate an offset distribution with 2.2μV standard deviation. The input noise spectral density is equal to 27nV/Hz, giving a noise efficiency factor of 8.

ScalTech28 Project: Description

- Three-stage instrumentation amplifier (IA)
  - Input Folded cascode opamp as first stage
  - Differential opamp as second and third stage
- Chopper technique in order to meet the low offset requirement of IAs
- Sub-threshold operation and dimensioning of the overall amplifier
- Rail-to-rail input stage with constant g_m through bias current control
- Nested Miller Compensation through C_{m1} & C_{m2}
- 100pF of capacitive load

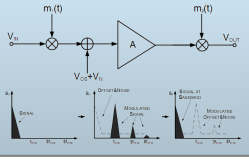


Scaled Technology Issues

- Mixed-signal systems requires the use of scaled technology also for analog blocks
  - Reduction of the V_{DD}/V_{TH} ratio
    - Less signal swing ☹
    - Operating point issues ☹
  - Reduced intrinsic gain $g_m r_o$
    - Horizontal gain distribution ☹
    - Increased power consumption ☹
- Solution → **Subthreshold operation** ($V_{GS} \leq V_{TH}$)
  - Increased signal swing ☺
  - Higher efficiency g_m/I_D ratio ☺
  - Larger current mismatch ☹ → dynamic offset compensation!

Chopper technique

- Dynamic offset cancellation technique
- Offset & 1/f noise reduced through modulation:
  - Signal is modulated, amplified and then demodulated again
  - Offset&1/f noise are modulated once and shifted to high frequency
- $m_1(t)$ is a square wave signal with period $T_{chop}=1/f_{chop}$
- Modulator is a polarity reversing switch



Specifications

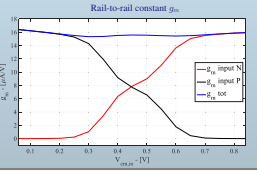
Parameter	Value
CMOS Technology	28 nm
Supply Voltage	0.9 V
Capacitive load	100 pF
DC Gain	110 dB
Gain Bandwidth	340 kHz
Input Referred Noise	150 nV/Hz
Phase Margin	70°

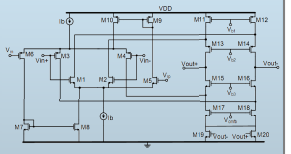
Dimensioning

Parameter	Value
I_b	500 nA
g_{m1}	15 µA/V
g_{m2}	15 µA/V
g_{m3}	500 µA/V
C_{m1}	7 pF
C_{m2}	2 pF
A_{01}	50 dB
A_{02}	25 dB
A_{03}	35 dB

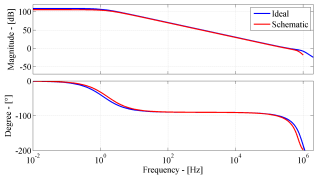
First stage

- Input rail-to-rail folded cascode opamp
- Constant transconductance g_m over signal swing:
  - input MOS working in weak inversion
  - control of the bias current made by two current switches M5&M6
  - $g_m = \alpha \cdot I_D \Rightarrow g_{mtot} = g_{mP} + g_{mN} = \alpha \cdot (I_P + I_N)$

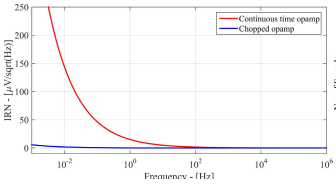




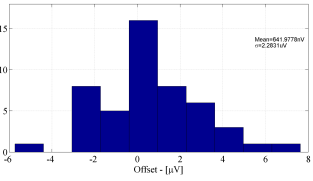
Opamp Frequency Response



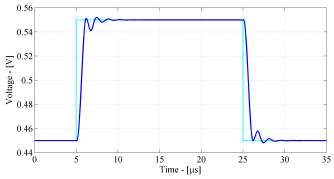
Input Referred Noise Voltage



Input Referred Offset Distribution



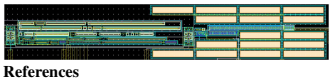
Step response



Performance Resume

Parameter	This Work	[3]	[4]
Year	2015	2010	2010
CMOS Technology	28 nm	0.18/0.5 µm	0.7 µm
Supply Voltage	0.9 V	1.8/5 V	5 V
Chopping frequency	500 kHz	500 kHz	30 kHz
DC Gain	106 dB	168 dB	>100 dB
GBW	329 kHz	260 kHz	900 kHz
Input offset standard deviation	2.2 µV	1.94 µV	2 µV
IRN	27 nV/Hz	37 nV/Hz	21 nV/Hz
Power Cons.	54 µW	26/72 µW	715 µW
NEF	8	5.5	9.6
Area	0.014 mm^2	1.14 mm^2	1.8 mm^2

Layout View



References

[1] K. A. Makinwa, *Dynamic offset compensated CMOS amplifiers*, Springer, 2009

[2] A. Grasso et al., *Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability*, IEEE Trans. on Circuits and Systems-I:Reg. Papers, vol. 62, no. 6, pp.1453-1462, May 2015

[3] M Belloni et al., *A Micropower Chopper-CDS Operational Amplifier*, IEEE J. Solid-State Circuits , vol. 45, no. 12, pp. 2521–2529, Dec. 2010

[4] Q. Fan et al., *A 21 nV/Hz chopper-stabilized multipath current-feedback instrumentation amplifier with 2µV offset*, IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2010, pp. 80-81

Email: *alessandra.pipino@mib.infn.it* – Phone: +39 0264482346 – Web: *https://fisica.mib.infn.it/media/homepages/applicata/microlab/index.html*

Conclusions

In this thesis, integrated circuit designs in 28 nm CMOS technology have been presented, with different application fields. The aim of this works was to study and analyse the advantages and especially the limits of the ultra-scaled technologies, as the 28 nm CMOS technology. Supply and threshold voltage ratio reduction, reduced intrinsic gain, worse PVT variations, restrictive layout rules, but also better transition frequency, mismatch variation and radiation hardness, have been described. Improvements for digital circuits on one side, a lot of analog design issues on the other side, characterize the scaled technologies, because of the poor analog performance. Different solutions and approaches have been used to face with the technology issues, circuital and of layout.

The first developed system is a read-out front-end for muon detection in the ATLAS experiment. In the last years, integrated circuits have been widely used in the high-energy physics experiments in order to improve the read-out performance. Because of the gradually CERN systems upgrade, read-out circuits will be exposed to increasingly radiation levels (up to 1Grad), with consequent damages. For this reason, the exploitation of ultra-scaled radiation hardness technologies has become a challenging research activity. The proposed solution for the read-out electronic is different from the current one used in the ATLAS detector, because it reset the front-end soon after the detection, in order to be available for next events, without loss of information. Thanks to a double threshold architecture, all the required information in terms of arrival time, charge amplitude and ToT are collected. The preliminary post-layout results seems to be promising and in line with the typical ATLAS detectors requirements. In particular, the read-out front-end exhibits almost 5 mV/fC of sensitivity, 0.2 fC of ENC and a peaking time delay of 28 ns. The test board has already been realized and the next step, after the arrival of the chips expected in short time, will be the measurements, in order to validate the proposed architecture.

The second design is a Chopper instrumentation amplifier in 28 nm CMOS technology. Instrumentation amplifiers are used in a wide range of applications, sensors, biomedical or RF mixed-signals; as a consequence, they must be integrated in scaled technology to follow the required systems performance. The proposed Chopper amplifier consists of a three stages Nested Miller compensation architecture, with two chopper across the first gain stage. It has been completely dimensioned in subthreshold region, with a rail-to-rail input stage and able to drive 100 pF of capacitive load.

A second prototype has been integrated including the four-phase non-overlapping clock generator and it is characterized by 108 dB DC Gain and a low corner frequency of 560 mHz. The next step will be to measure the chip and to verify that problems have been solved, validating the performance.

Bibliography

[1] G. A. e. a. ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider," *Journal of Instrumentation*, vol. 3, p. S08003, 2008.

[2] Y. A. et al., "ATLAS Muon Drift Tube Electronics," *Journal of Instrumentation*, vol. 3, p. P09001, 2008.

[3] T. Skotnicki *et al.*, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *IEEE Circuits and Devices Magazine*, vol. 21, no. 1, pp. 16–26, 2005.

[4] L. Chang *et al.*, "Moore's law lives on [CMOS transistors]," *IEEE Circuits and Devices Magazine*, vol. 19, no. 1, pp. 35–42, 2003.

[5] D. Hisamoto *et al.*, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *Electron Devices, IEEE Transactions on*, vol. 47, no. 12, pp. 2320–2325, 2000.

[6] M. M. Frank, "High-k/metal gate innovations enabling continued CMOS scaling," in *In ESSCIRC (ESSCIRC), 2011 Proceedings of, IEEE*, pp. 50–458, IEEE, 2011.

[7] A. Baschirotto *et al.*, "Low power analog design in scaled technologies," 2009.

[8] X. Qi *et al.*, "Efficient subthreshold leakage current optimization-Leakage current optimization and layout migration for 90-and 65-nm ASIC libraries," *IEEE Circuits and Devices Magazine*, vol. 22, no. 5, pp. 39–47, 2006.

[9] . T. H. P. de Gyvez, J. P., "Threshold voltage mismatch and intra-die leakage current in digital CMOS circuits," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 1, pp. 157–168, 2004.

[10] K. Kuhn *et al.*, "Managing Process Variation in Intel's 45nm CMOS Technology," *Intel Technology Journal*, vol. 12, no. 2, 2008.

[11] M. Koh *et al.*, "Limit of gate oxide thickness scaling in MOSFETs due to apparent threshold voltage fluctuation induced by tunnel leakage current," *Electron Devices, IEEE Transactions on*, vol. 48, no. 2, pp. 259–264, 2001.

[12] Y. Sheu *et al.*, "Modeling the well-edge proximity effect in highly scaled MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 53, no. 11, pp. 2792–2798, 2006.

[13] H. T. B. . L. Y. M. Johnson, J. B., "Analysis and modeling of threshold voltage mismatch for CMOS at 65 nm and beyond," *Electron Device Letters, IEEE*, vol. 29, no. 7, pp. 802–804, 2008.

[14] D. A. C. . W. A. P. Pelgrom, M. J., "Matching properties of MOS transistors," *Solid-State Circuits, IEEE Journal of*, vol. 24, no. 5, pp. 1433–1439, 1989.

[15] P. Dautriche, "Analog design trends and challenges in 28 and 20nm CMOS technology," in *In ESSCIRC (ESSCIRC), 2011 Proceedings of, IEEE*, pp. 1–4, IEEE, 2011.

[16] H. Hughes and J. Benedetto, "Radiation effects and hardening of MOS technology: devices and circuits," *Nuclear Science, IEEE Transactions on*, vol. 50, no. 3, pp. 500–521, 2003.

[17] W. Snoeys *et al.*, "Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 439, no. 2, pp. 349–360, 2000.

[18] F. Faccio *et al.*, "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," *Nuclear Science, IEEE Transactions on*, vol. 62, no. 6, pp. 2933–2940, 2015.

[19] A. Pezzotta *et al.*, "Impact of GigaRad Ionizing Dose on 28 nm bulk MOSFETs for future HL-LHC," in *Solid State Device Research Conference, 2016. ESSDERC 2016. 46th European*, pp. 146–149, IEEE, 2016.

[20] W. Dabrowski, "Challenges and benefits of designing readout ASICs in advanced technologies," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 579, no. 2, pp. 821–827, 2007.

[21] L. Evans and P. Bryant, "LHC Machine," *Journal of Instrumentation*, vol. 3, p. S08001, 2008.

[22] E. H. C. Posch and J. Oliver, *MDT-ASD User's Manual*. ATL-MUON-2002-003, 2007.

[23] W. R. et al., *MDT Resolution Simulation Frontend Electronics Requirements*. ATL-MUON-97-137, 1997.

[24] L. Rossi, P. Fischer, T. Rohe, and N. Wermes, *Pixel detectors: From fundamentals to applications*. Springer Science & Business Media, 2006.

[25] M. De Matteis *et al.*, "An 8-channels 0.13um-CMOS front-end for ATLAS MDT-detectors," in *IEEE SENSORS 2015*, pp. 1–4, IEEE, 2015.

[26] S. D'Amico, V. Giannini, and A. Baschirotto, "A 4th-Order Active-Gm-RC Reconfigurable (UMTS/WLAN) Filter," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 7, pp. 1630–1637, 2006.

[27] M. A. W. Riegler, *Bipolar versus unipolar shaping of MDT signals*. ATL-MUON-99-003, 1999.

[28] W. R. Blum, Walter and L. Rolandi, *Particle detection with drift chambers.* Springer Science & Business Media, 2008.

[29] B. Shen *et al.*, "An 8.5 mW, 0.07 mm 2 ADPLL in 28 nm CMOS with sub-ps resolution TDC and< 230 fs RMS jitter," in *2013 Symposium on VLSI Circuits*, pp. C192–C193, IEEE, 2013.

[30] S. J. Kim *et al.*, "A 0.63 ps, 12b, synchronous cyclic TDC using a time adder for on-chip jitter measurement of a SoC in 28nm CMOS technology," in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, IEEE, 2014.

[31] M. D. M. et al., "Performance of the new amplifier-shaper-discriminator chip for the atlas mdt chambers at the hl-lhc," *Journal of Instrumentation*, vol. 11, p. C02087, 2006.

[32] . Z. Y. Han, D., "A chopper stabilized instrumentation amplifier with dual DC cancellation servo loops for biomedical applications," in *Solid State Circuits Conference (A-SSCC), 2012 IEEE Asian*, pp. 49–52, IEEE, 2012.

[33] S. F. H. J. H. . M. K. A. Fan, Q., "A 1.8 W 60 nV Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 7, pp. 1534–1543, 2011.

[34] K. A. Makinwa and J. H. Huijsing, *Dynamic offset compensated CMOS amplifiers.* Springer, 2009.

[35] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization.," in *Proceedings of the IEEE 84.11*, pp. 1584–1614, 1996.

[36] C. Enz, E. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," *Solid-State Circuits, IEEE Journal of*, vol. 22, no. 3, pp. 335–342, 1987.

[37] . K. W. J. Pertijs, M. A., "A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 10, pp. 2044–2056, 2010.

[38] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," *Solid-State Circuits, IEEE Journal of*, vol. 12, no. 3, pp. 224–231, 1977.

[39] A. Grasso, P. G. Marano, D., and S. Pennisi, "Design Methodology of Subthreshold Three-Stage CMOS OTAs Suitable for Ultra-Low-Power Low-Area and High Driving Capability," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 62, no. 6, pp. 1453–1462, 2015.

[40] L. Magnelli *et al.*, "Design of a 75-nW, 0.5-V subthreshold complementary metal-oxide-semiconductor operational amplifier," *International Journal of Circuit Theory and Applications*, vol. 42, no. 9, pp. 967–977, 2014.

[41] H. J. S. T. . S.-S. E. Yan, S., "Constant-g m techniques for rail-to-rail CMOS amplifier input stages: a comparative study," in *IEEE International Symposium on Circuits and Systems*, pp. 2571–2574, IEEE, 2005.

[42] W. Redman-White, "A high bandwidth constant gm and slew-rate rail-to-rail CMOS input circuit and its application to analog cell for low voltage VLSI systems," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 5, pp. 701–712, 1997.

[43] J. M. Carrillo *et al.*, "Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 8, pp. 1364–1372, 2003.

[44] C. Hwang, A. Motamed, and M. ismail, "Universal constant-gm input stage architecture for low-voltage op amps," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 42, no. 11, pp. 886–895, 1995.

[45] S. Sakurai and M. Ismail, "Robust design of rail-to-rail CMOS operational amplifiers for a low power supply voltage," *Solid-State Circuits, IEEE Journal of*, vol. 31, no. 2, pp. 146–156, 1996.

[46] R. Hogervorst *et al.*, "A compact power-efficient 3-V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *Solid-State Circuits, IEEE Journal of*, vol. 29, no. 12, pp. 1505–1513, 1994.

[47] F. Maloberti, *Analog design for CMOS VLSI systems*. Springer Science & Business Media, 2006.

[48] . M. K. Johns, D. A., *Analog integrated circuit design*. John Wiley & Sons., 2008.

Acknowledgements

Prima di tutto vorrei esprimere la mia gratitudine al prof. Andrea Baschirotto e Marcello De Matteis, per avermi dato l'opportunità di fare questi tre anni di dottorato presso l'Università di Milano-Bicocca e per il continuo supporto e incoraggiamento nella mia attività di ricerca.

In questa esperienza ho avuto la fortuna di avere accanto ottimi colleghi con cui condividere le ore di lavoro, le pause, i dubbi, i momenti più difficili e anche quelli positivi. Per cui grazie a Antonio, Federico, Fulvio e Tommaso. Un ringraziamento speciale va alle due persone che più mi hanno accompaganata e sostenuta in qualsiasi momento, fuori e dentro l'ufficio, Federica e Alessandro. Senza di loro questi tre anni di dottorato non sarebbero stati gli stessi.

Grazie anche a Salvatore, Gianpaolo e Michela per la loro preziosa amicizia e per rendere i momenti fuori dall'ufficio così divertenti e spensierati!

Infine un doveroso ringraziamento va come sempre alla mia famiglia, papà, mamma e mia sorella, che, nonostante la lontananza, mi ha comunque sempre appoggiata e sostenuta. E a Fabrizio non posso che volgere il grazie più speciale, dedicandogli questa tesi, per essermi stato davvero accanto dall'inizio alla fine, per aiutarmi e sostenermi sempre. Ritrovarsi a casa la sera migliora ogni giornata, alleviando tutti i pensieri. Con lui ogni cosa diventa possibile e da sola non so se ce l'avrei fatta.

Grazie!