UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA

SCUOLA DI DOTTORATO

UNIVERSITÀ DEGLI STUDI DI MILANO-BICOCCA

Department of Materials Science

PhD program in Materials Science and Nanotechnology Cycle 29°

Functional analysis of In-based nanowires for low power phase change memory applications

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ACADEMIC YEAR 2015/16

To my wife

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Preface

Phase change memories (PCMs), based on chalcogenide alloys (mainly $Ge_2Sb_2Te_5$), are the most promising candidate for the realization of “Storage Class Memories”, which would fill the gap between ‘‘operation’’ and ‘‘storage’’ memories. PCMs are also one of the few currently available technologies for the implementation of nanoeletronic synapses in high density neuromorphic systems. The main improvements needed in order to exploit the full potential of PCMs in these innovative applications are the reduction of the programming currents and power consumption, and further cell downscaling. Thanks to their nano-sized active volume to be programmed and self-heating behavior, phase change nanowires (NWs) are expected to exhibit improved memory performances with respected to commonly used thin-film/heater-based structures.

This Ph. D. Thesis reports the study of the phase change properties of ultra-thin In-based NWs for low power consuming PCMs, exploring the more promising features of this class of materials with respect to the commonly considered Ge-Sb-Te alloys.

In particular, the self-assembly of In-Sb-Te, In-doped Sb and In-Ge-Te NWs was successfully achieved by Metal Organic Chemical Vapour Deposition (MOCVD), coupled to vapour-liquid-solid mechanism, catalysed by catalyst nanoparticles. The parameters influencing the NW self-assembly were studied and the compositional, morphological and structural analysis of the grown structures was performed. In all cases, NWs of several μm in length and with diameters as small as 15 nm were obtained. The experimental contribution of the

manuscript's author to the NWs growth study has mainly focussed on the substrates preparation, catalyst deposition and, morphological and elemental analysis of the grown samples. Moreover, the author has then performed the functional analysis of $In_3Sb_1Te_2$ and In-doped Sb NW-based PCM devices. To conduct that analysis, a suitable fabrication procedure of the devices and an appropriate electrical measuring set-up have been identified. Reversible and well reproducible phase change memory switching was demonstrated for $In_3Sb_1Te_2$ and In-doped Sb NW devices, showing low working parameters, such as RESET voltage, current and power.

The results that will be described in this manuscript support the conclusion that In-based ultra-thin NWs are potential building blocks for the realization of ultra-scaled, high performance PCM devices.

This Thesis work was carried out at the Laboratorio MDM (Materials and Devices for Microelectronics), part of the Institute for Microelectronics and Microsystems of the National Research Council of Italy, located in Agrate Brianza (Italy). Two short traineeships (of about three months), consisting of experimental research, were conducted at the Tyndall National Institute, Cork (IE), and the Institut für Festkörper-elektronik (FKE), TU Vienna, Vienna (AT), respectively.

Chapter 1 : Introduction to electrical phase-change memory technology

In this chapter will be given a short introduction to the electrical phase-change memory (PCM) technologies, useful for an understanding of the topics covered in this PhD thesis. A comprehensive and thorough review of PCM technologies, including a complete discussion of material and device issues, can be found elsewhere [1]–[11].

Ovshinsky, in 1968, described two kinds of switching mechanisms observed in chalcogenide alloys, threshold switching and memory switching [12]. Threshold switching is the sudden drop in resistance of an amorphous chalcogenide alloy positioned between two electrodes when a specific applied voltage is exceeded. This resistance drop to a lower resistance state is an electronic effect and it is reversible if the voltage is removed fast enough. Memory switching, instead, is the reduction in resistance that remains after when the current is totally removed. This memory effect is caused by a change in the atomic structure of the chalcogenide from the amorphous phase to the crystalline phase induced by Joule heating. Remarkably, it is possible to return from the conductive crystalline structure to the resistive amorphous phase by melting and very rapid cooling (quenching). This reversible memory switching between the two described physical states is the foundation of PCM.

Early phase-change alloys were characterized by relatively long crystallization times and it took the breakthrough discovery of fast (i.e., nanosecond time scale) switching materials along the pseudo-binary line between GeTe and Sb_2Te_3 [13], notably the most studied and utilized $Ge_2Sb_2Te_5$ (GST), to enable phase-change storage technology [9]. Non-volatile random-access PCM is now the most mature of the emerging memory technologies. After demonstrating that large-scale manufacture was possible, PCM products are entering volume production [6]. However, currently PCM are in commercial production but still remain limited to niche applications relative to stand-alone data storage to replace Flash memory.

In the future, advanced PCM is expected to effectively replace some Flash and embedded memories [7]. PCMs are also being considered as a potential disruptive solution for the realization of a new Storage Class Memory [14], which would fill the gap between ‘‘operation’’ and ‘‘storage’’ memories. Moreover, PCMs are one of the few currently available technologies for the implementation of artificial nanoeletronic synapses and neurons in high density neuromorphic systems [15]–[17]. The main improvements needed in order to exploit the full potential of PCMs in these applications are lower operation currents and power consumption, and further cell downscaling.

1.1 Principles of phase change memory

As mentioned before, electrical PCM is based on the repeatable switching of a phase-change material between its amorphous and the crystalline states accompanied by a large resistance change. Memory information is stored in the atomic configuration of the material and is read by measuring the resistance of the PCM cell. Figure 1 illustrates the principle.

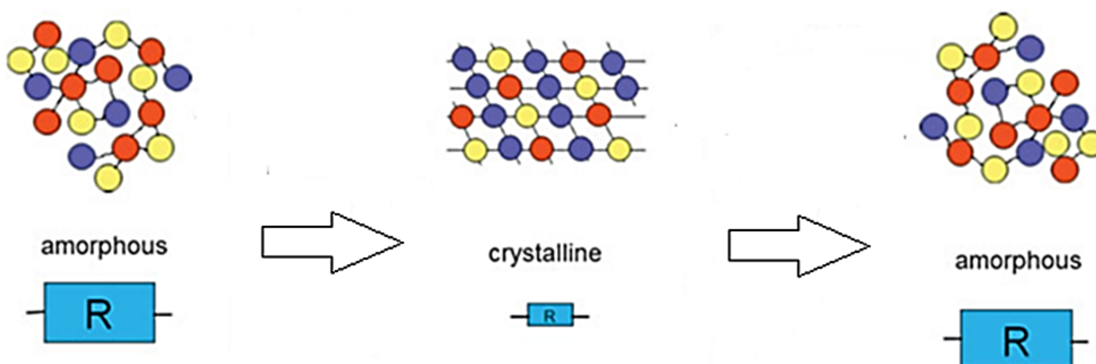


Figure 1-1: Principle of phase change memory. [9]

To set the cell into its low-resistance state (SET state), an electrical pulse is applied to heat a significant portion of the cell above the crystallization temperature of the phase-change material. This is only possible because of the threshold switching effect that leads to a drastic and sudden (within nanoseconds) reduction of the resistance of the amorphous phase when a certain electric field is surpassed, at a given threshold voltage (V_{th}). Otherwise, it would be impossible to heat the amorphous material using Joule heating with reasonably low voltages. This set operation tends to dictate the write speed performance of PCM technology, since the required duration of this pulse depends on the crystallization speed of the phase-change material. In the reset operation a more intense electrical pulse is applied in order to melt the central portion of the cell. If this pulse is cutoff abruptly enough, the molten material quenches into the amorphous phase, producing a cell in the high-resistance state (RESET state). Due to the relative high melting temperature (e.g. melting temperature of the GST is about 620 °C), high reset currents (100-500 µA) are typically required. The resistance state of the memory cell is read with a sufficiently small electrical pulse, which does not modify the state of the memory cell. These operations are summarized in Figure 2.

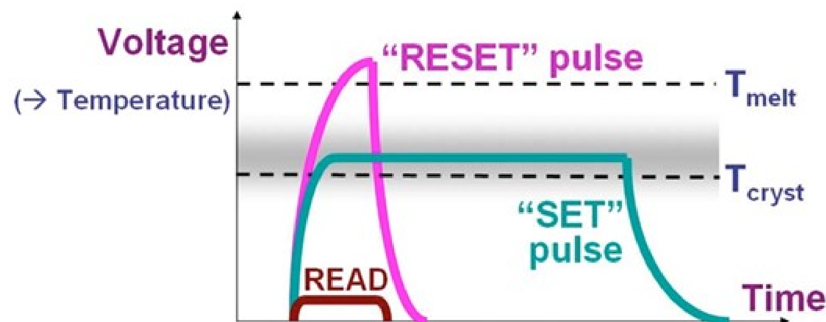


Figure 1-2: Programming and sensing operations of a PCM device by application of electrical pulses. [5]

The current pulses are provided by a selector device, which also isolates the memory cell during programming and sensing operations. Field-effect transistors [18],bipolar junction transistors [19], and diodes [20] have been employed as selector devices, and, in most cases, the size of the selector is larger than the PCM cell in order to provide sufficient current, ultimately limiting the storage density. Considerable development efforts have been devoted to optimizing the cell design that leads to reduced reset current, thus to reduced size of the selector and increased storage density.

Figure 3 shows the typical pulsed current–voltage (I-V) curves of the SET and RESET states, indicating a large resistance difference between the two states that guarantees reliable bit

discrimination at low voltages (READ region). The RESET state is in the high-resistance state below Vth (subthreshold region) and shows electronic threshold switching behavior at Vth, i.e., a negative differential resistance. This is reversible if the voltage pulse is removed very quickly. But if the voltage is applied for longer than the crystallization time it leads to memory switching and the cell reaches the low-resistance state for an applied voltage larger than Vth.

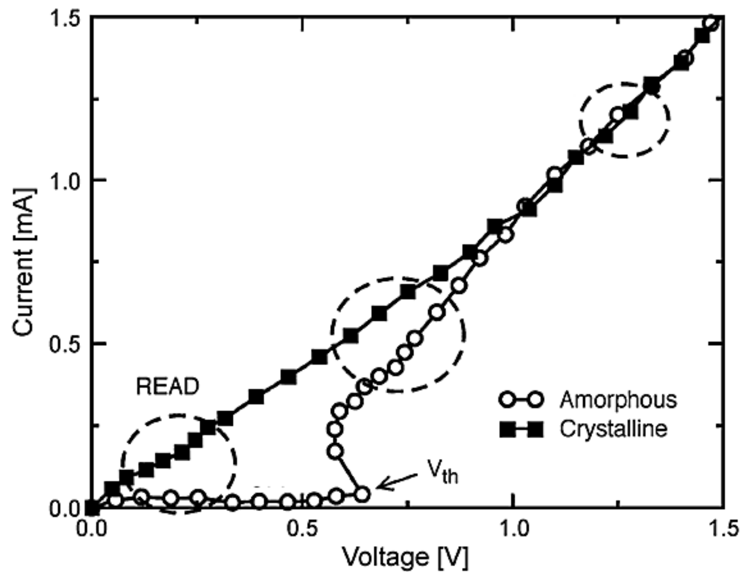


Figure 1-3: Experimental pulsed I–V curve of a PCM cell in the crystalline and in the amorphous state. [21]

1.2 The reference materials for phase-change electronic storage

A phase change material is useful for technological applications if it fulfills a large set of material requirements which depend on the application. Storage technologies based on phase-change materials require very fast (nanosecond time scale) crystallization of the amorphous phase during writing but very high stability of the amorphous phase against spontaneous crystallization (archival lifetime of 10 years). For these reasons only very few materials are actually technologically useful phase-change materials.

The industrial development of PCM arrays started with the use of GST ($Ge_2Sb_2Te_5$) [22]. The active material has a critical impact on device performance, and therefore other options are being actively investigated, aimed at increasing speed, improving retention and cycling endurance, and lowering power consumption. However, GST is still considered as a reference material for phase change electronic storage.

In the crystalline phase, GST has a metastable rock-salt structure, characterized by Te atomic planes interleaved with Ge/Sb planes with 20 % vacancies (Figure 4). Vacancies are essential for the energy stability of the octahedral structure and are responsible for p-type conduction [8].

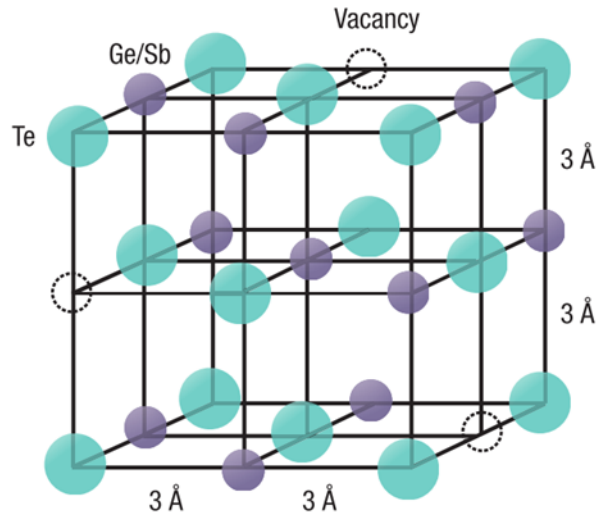


Figure 1-4: Schematic image of the crystal structure of the rock-salt-like phase of GST. [8]

The crystalline phase can be transformed into an amorphous phase by heat-induced melting-quenching, resulting in the loss of the long range order and in the development of a covalently bonded structure [23]. However, unlike other amorphous solids, the short-range atomic arrangement also changes [7].

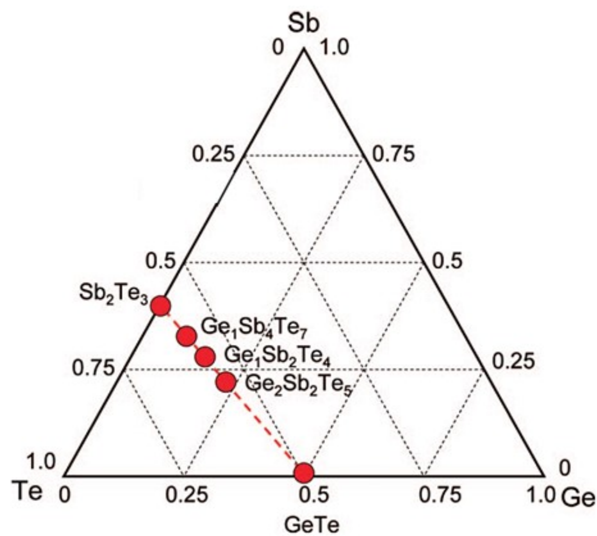


Figure 1-5: Stoichiometries of interest along the pseudo-binary line [10]

As GST, most of the conventional alloys which are applied as phase-change materials lie on the GeTe-Sb_2Te_3 pseudo-binary line (Figure 5).

The electrical properties of phase-change materials is crucial for the application of these materials in solid state memory devices. The electronic band structure of ternary Ge-Sb-Te alloy depends on stoichiometry and phase, and can be simplified as a band-gap with localized energy levels in between (Figure 6). In the crystal phases, the Fermi level is approximately located closely to, or inside of the valence band. This corresponds to semiconductor-like and metallic behavior respectively. In the amorphous phase, no band gap can be defined; rather, a high density of localized states is present within the mobility gap, with the Fermi level calculated to be approximately pinned at the center thereof ($Ge_2Sb_2Te_5$ at T=0 K) [24]. In this regard, electronic transport mechanisms in the amorphous phase are still being debated.

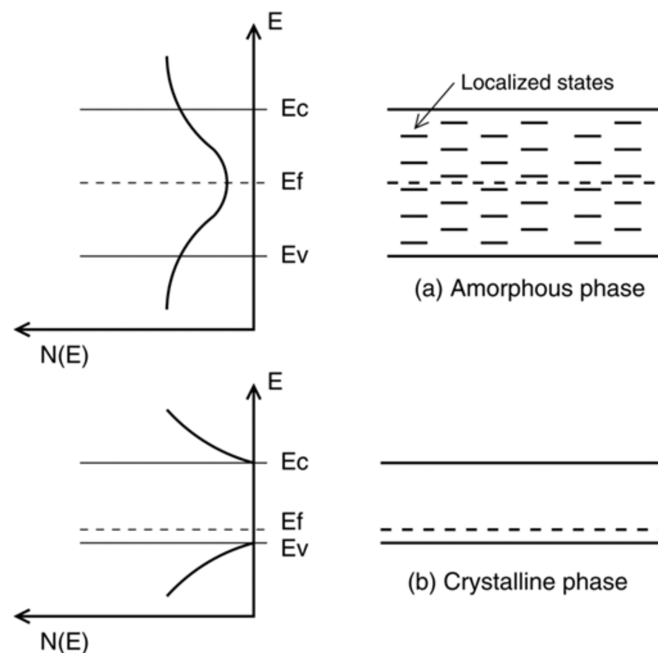


Figure 1-6: Schematic band diagrams and density of states as a function of energy for the amorphous phase (top) and the crystalline phase (bottom) of the Ge-Sb-Te alloys. [25]

In many aspects, the described ternary Ge-Sb-Te alloys are good constituents for electrical PCM, for example they have a relatively low melting point, very low thermal conductivity, and relatively high resistance in the amorphous and the crystalline phase, but in other aspects they do not perform very well. The crystallization temperature is low for certain PCM applications such as embedded memory or automotive applications, the crystallization times are too long and cycle numbers are not sufficient for other potential PCM applications such as dynamic random access memory (DRAM) replacement. Even if wide materials research has been already performed to find phase-change materials that are better suited for PCM,

further efforts are necessary to find phase-change materials that really fulfill all the technological requirements.

1.3 Typical PCM cell structures

Typical technological implementations of PCM devices are based on a heater-based cell architecture. The early developed and most simple type of PCM cell (called ‘‘mushroom’’ type) is shown in Figure 7. In this cell, the bottom electrode, which is produced by filling a small via, is optimized to act as a heater, largely confining the high-temperature zone to a region close to the bottom electrode interface. After the via is filled by the heater material, which is often TiN, a polishing is applied to planarize the wafer, followed by phase-change thin-film deposition. Before the top electrode deposition, the deposited film is patterned into “islands” using conventional lithography to form individual cells (for each heaters of the device), and isolated and encapsulated using thermally insulating dielectric materials, such as Si_3N_4.

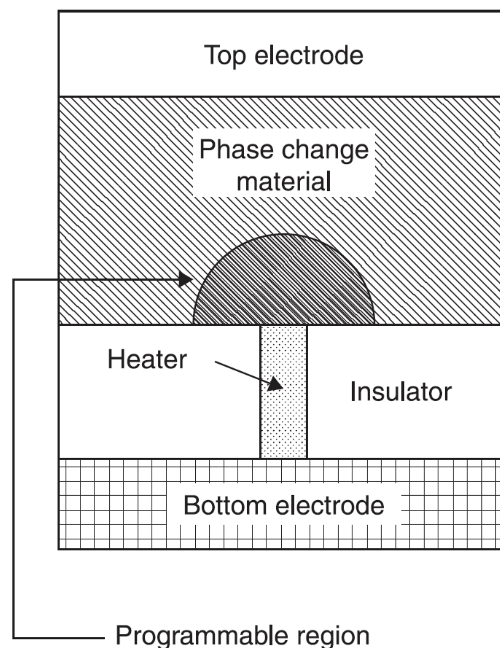


Figure 1-7: Schematic cross- section of ‘‘mushroom’’ PCM cell. Current crowding at the heater to phase change material contact results in a programmed region illustrated by the “mushroom” boundary. [2]

As introduced briefly above, the large programming current is still a key issue that limits the adoption of PCM in many applications. Furthermore, large programming current forces a strict requirement on the current delivered by the cell selector of the PCM. In order to provide enough current to switch the states of PCM, the area of the cell selector may not be scaled down as fast as the memory cell itself, thus the size of the cell selection device becomes

the limiting factor for the device density. Therefore, reducing the programming current is necessary for achieving both high-density and low power consumption of PCM.

Reference	Structure	TN (nm)	I_{reset} (μA)	Schematic view
Pellizzer *et al.* 2006	Mushroom	90	700	
Ha *et al.* 2003	Edge	240	200	
Pirovano *et al.* 2005, Pellizzer *et al.* 2006	μTrench	180 90	450 400	
Pirovano *et al.* 2007	Self-aligned μTrench	90	300	
Breitwisch *et al.* 2007	Pore	180	250	
Lee *et al.* 2007	Confined	45	260	
Song *et al.* 2006	Ring-shaped contact	100	450	

Table 1-1: Characteristics of different PCM cell designs. TN is the technology node, Ireset is the reset current. [1]

To decrease the reset current, many different cell designs were developed in the last decade. In general, a PCM cell is designed so that the only current path across the device passes through a small aperture. As this aperture shrinks in size down to sub-lithographic dimension, the programmable region of the cell it is drastically reduced. In turn, this decreases the power (and thus the current) requirements. Depending on how this sub-lithographic aperture is implemented, PCM cell structures belong to one of two general categories: those which control the cross section by the size of the heater electrode (contact minimized) and those which minimize the size of the phase change material itself at some point within the cell (volume

minimized, also known as confined) [5]. The confined cell structures tend to be a bit more thermally efficient, offering the potential for lower reset current requirements [26]. A summary of the technology characteristics of some of the various PCM cell designs is reported in Table 1.

Moreover, programming current and programming energy gracefully scale with cell size thus making possible to match low power/low energy requirements with nanoscale devices. It is demonstrated that a reduction of the reset current can be achieved by scaling the device dimensions. In particular, by shrinking all the linear dimensions by a factor k, the reset current should decrease by the same factor [11]. Scaling is therefore the main enabler of programming current/power performance improvement in PCM devices.

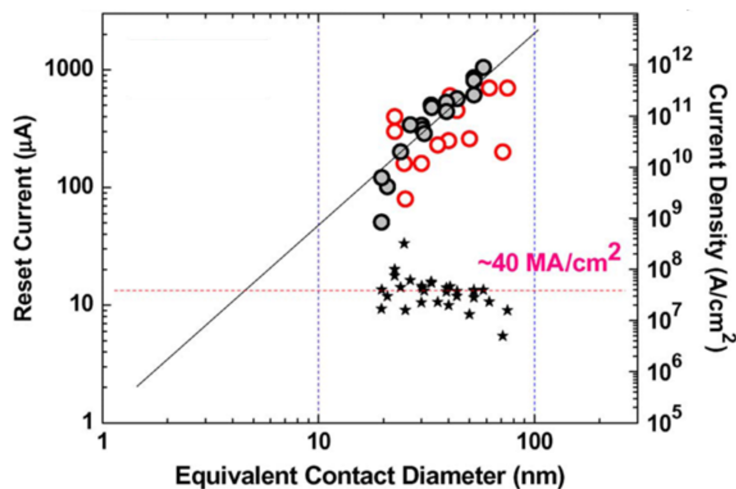


Figure 1-8: Reset current as a function of equivalent contact diameter. [2]

Figure 8 summarizes PCM programming current as a function of the equivalent diameter of a circular contact for different cell structures. It is clearly visible that the reset current scales with the effective contact area of the PCM and that a constant current density ~40 MA/cm^2 is necessary to program the average PCM cell.

1.4 Nanowire PCM devices

An alternative method for reducing programming volumes and contact size areas is to employ phase-change nanomaterials, synthesized either by top- down or bottom- up approaches. The use of 1D phase-change structures, such as NWs, makes it possible to fully exploit the scaling properties of the PCM device. The phase-change NW growth and its diameter, composition and crystallinity can be controlled. In this way, a NW can form a nano PCM cell itself [1].

The idea of a NW-PCM device is very simple, based on the transformation of the active phase-change layer in a planar cell into a 1D cell. The 1D cell is formed by a NW, whose metallic contacts at both tips form the top and bottom electrodes, respectively. A nanocell is therefore obtained in which the NW is a self-heating resistor [27]. A portion of it undergoes a phase transition from amorphous to crystalline, as the current flows through it. A proper dielectric material is needed to passivate the NW, not only to insulate it, but also to protect it from evaporating during the phase transitions. Figure 9 displays the scheme of a NW-based PCM cell.

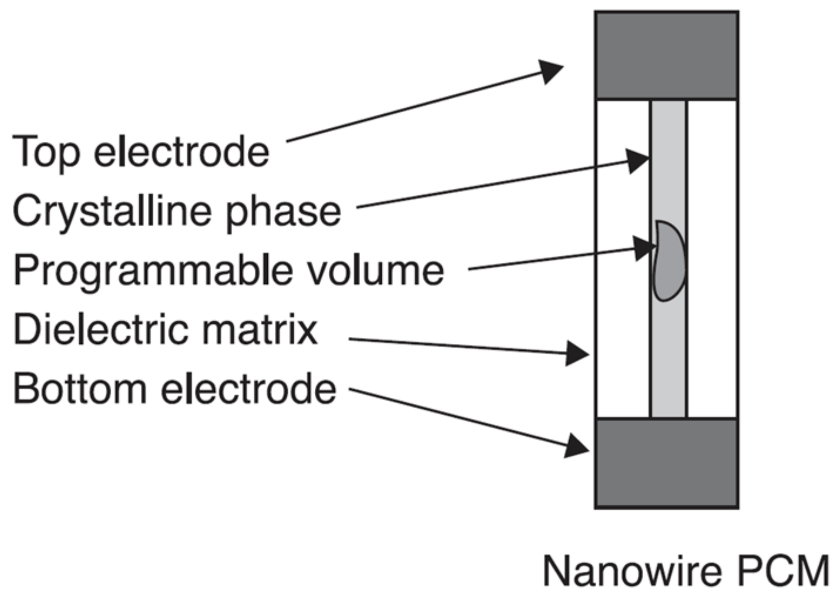


Figure 1-9: NW-based PCM cell. [1]

The energy required to induce the phase transition is lowered, not only because of the good structural properties of these nanostructures (which can be defect- free when the NWs are self-assembled) and the high geometrical scaling, but also due to other aspects related to size effects. The list below summarizes the main size effects that can be observed in phase-change NWs [28]–[35]:

- reduction of melting temperature;
- reduction of crystallization temperatures;
- reduction of activation energy for re-crystallization;
- reduction of thermal conductivity,
- reduction of proximity disturbance,
- reduction of resistance drift (if induced stress effects are not present);
- reduction of writing currents and power consumption;
- lower data retention.

In Figure 10 is reported the thickness-dependent behavior of the reset (amorphization) current for GST and GeTe NWs. It is clearly visible a systematic shift toward lower programming currents (corresponding to a reduction of the power) required for amorphization, when decreasing the NWs diameter.

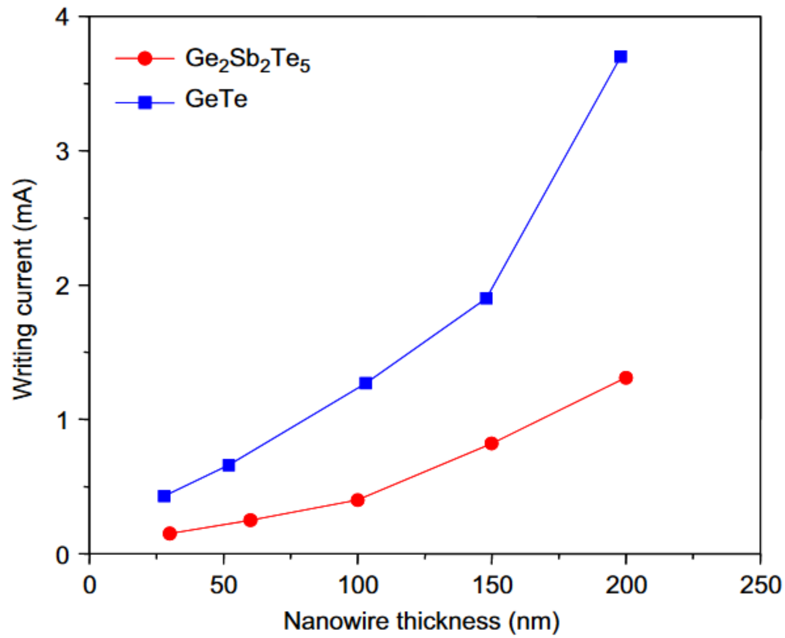


Figure 1-10: GST and GeTe NW scaling effect on writing (reset 9 current). [31]

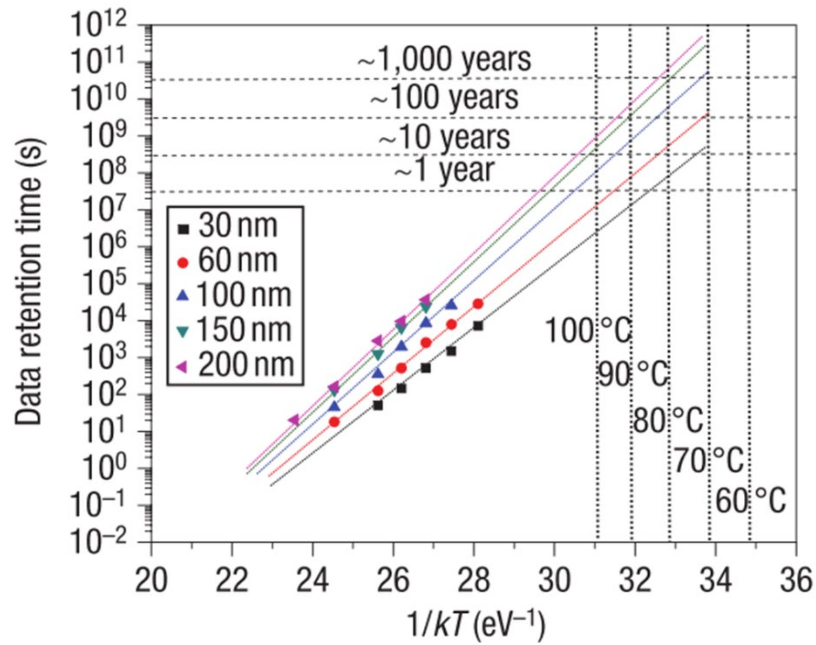


Figure 1-11: NW thickness- dependent Arrhenius plots of recrystallization or data retention time (t) versus (1/kT) of amorphous-state NW-based devices, measured from 140–220 °C. [30]

On the other hand however, scaling down PCM cells from thin films to NWs requires solutions specific to each of the reliability problems introduced by the reduced length scale. In particular, the reduction in data retention time as a function of the NW diameter (Figure 11), have to be taken into account. In this regard, one possibility to improve the data retention should be given by the use of high-crystallization temperature phase-change materials.

Only a smart combination of scaling and material engineering will be able to allow the opening of new perspectives for the PCM technology. "Scaling can be used as a straightforward way for power consumption design and is thus a key enabler of low power applications in the memory market. Phase change material engineering represents instead the key enabler of reliability and performance features of the PCM technology, thus likely supporting the widening of the PCM application spectrum" [36].

1.5 In-based phase-change materials

In addition to the successful prototype family of alloys originates from the pseudo-binary line of GeTe-Sb_2Te_3, there are other families of phase-change materials. Among them, In-based phase-change materials, namely those belonging to the In-Sb-Te and In-Ge-Te systems, display higher thermal stability of the amorphous phase respect to the Ge-Sb-Te alloys [37], [38], due to higher crystallization temperatures (> 270 °C). This property is crucial to enhance the data retention capability of the PCMs and it is particularly appealing for the development of ultra-scaled devices. Recently, PCM cells assembled with In-based chalcogenide thin-film have been fabricated and characterized [39]–[42], demonstrating good resistance contrast, high endurance, and multiple resistance levels. Although, very few reports of nano-sized In-based PCM devices have been reported [43].

Among compounds of the In–Sb–Te ternary alloys, the $In_3Sb_1Te_2$ composition (IST) has been extensively investigated and it was shown that it is metastable at low temperature (< 420 °C) and it has a cubic rock salt structure [44]. This chalcogenide alloy not only shows extremely high contrast with respect to the drop in resistivity, but also excels in terms of thermal stability (crystallization temperature > 290 °C) and exhibits a totally different composition [45][46], which sets it apart from established phase-change systems. An IST PCM cell was fabricated with 6 × 6 μm^2 contact dimension and the electrical characteristics were measured [40]. That IST cell showed three obvious current steps in the crystalline state during the voltage sweep (Figure 12), clearly indicating a multi-level memory capability. Later, the same researchers were successful in demonstrating that the observed multi resistance states were due a stable multi-phase change mechanism [41]. In particular, Sb and Te atoms co-exist on the (1/4, 1/4,

1/4) sites in the zincblende structure of InSb when IST is transformed at the first crystallization state. These Sb and Te atoms move to (1/2, 1/2, 1/2) sites, forming rock salt structured IST at the second phase transformation. At the third phase changing state, In_3SbTe_2 separates into InTe and InSb, and only InTe appears in the crystallized phase.

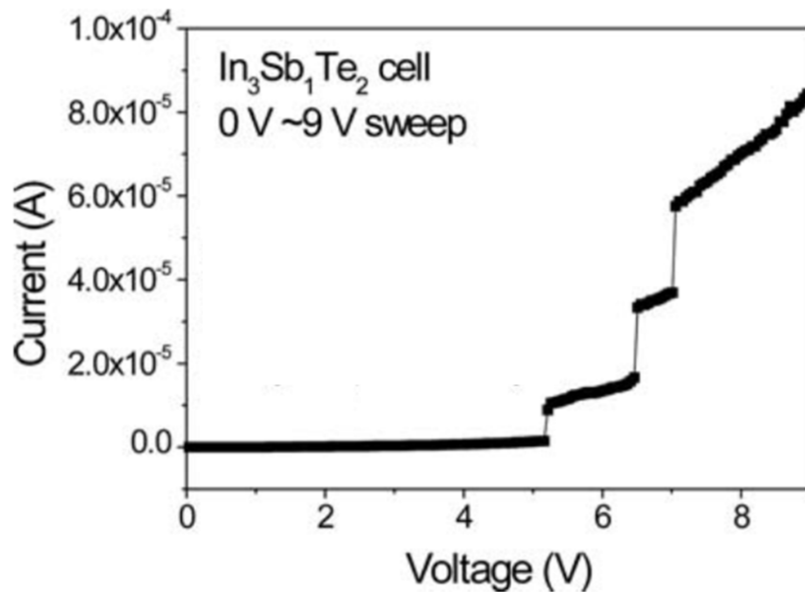


Figure 1-12: I–V curve of the IST PCM cell measured in Ref [40].

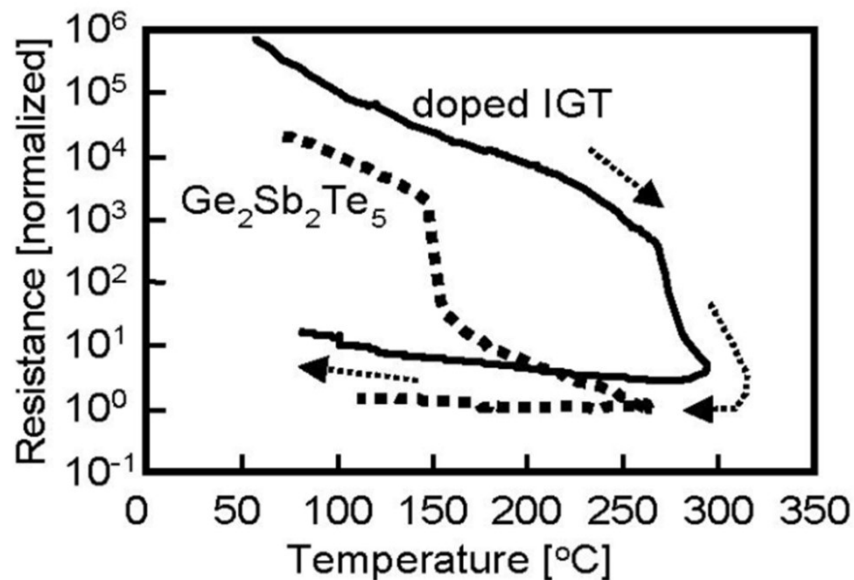


Figure 1-13: Dependence of resistance on temperature in amorphous films of GST and doped IGT. [42]

Doped $InGeTe_2$ (IGT) has been proposed as a candidate for automotive use since it reaches a crystallization temperature of 276 °C, about 130 °C higher than GST (Figure 13). It

has been also demonstrated that PCM devices based on doped IGT are able to reach 10 years' retention at temperatures higher than 150 ◦C [42].

Recently, a model of the liquid and amorphous phases of $InGeTe_2$ has been provided [38]. While the liquid is metallic, the amorphous phase is a semiconductor with a band gap of 0.5 eV. The local structure of amorphous IGT is similar to that of GST as concerns Ge and Te atoms. Atoms of In are, instead, mostly fourfold coordinated in $InTe_4$ tetrahedra, similarly to the crystalline phase of InTe and In_2Te_5. According to this model, the higher crystallization temperature measured for IGT compared to that of the GST, might be the result of two concurring effects. On one hand, a crystallization temperature higher than in GST is expected because of the higher melting point of IGT (Figure 14). On the other hand, if tetrahedra are absent in the crystalline IGT cubic phase, the large fraction of $InTe_4$ tetrahedra in its amorphous phase should hinder the crystallization, resulting in a further increase in the crystallization temperature. This property might be shared with other phase change alloys containing In, such as IST.

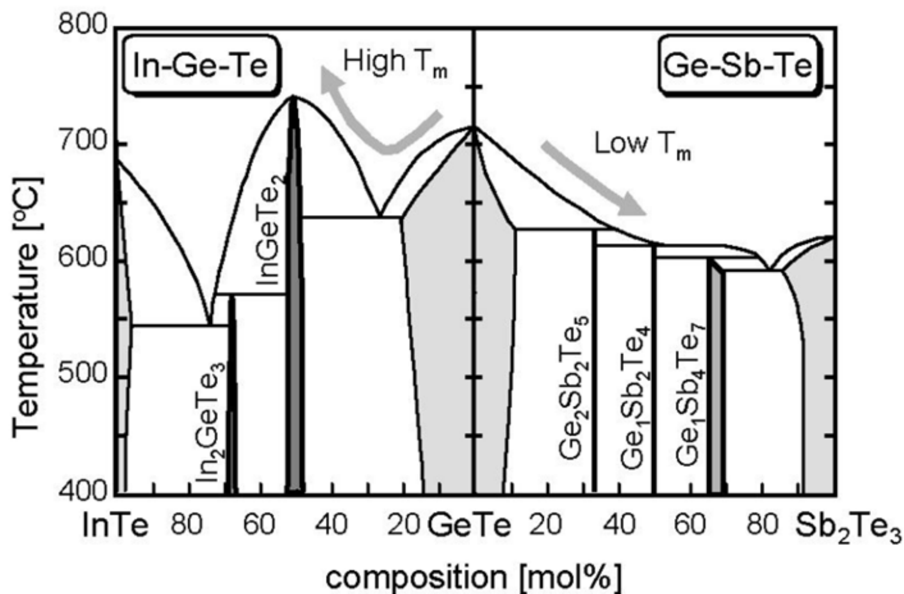


Figure 1-14: Pseudo-binary phase diagrams of GeTe-InTe and GeTe-Sb_2Te_3 systems. [42]

A Te-free class of phase-change materials, that combine fast crystal growth with excellent amorphous stability at room temperature, has been proposed at the beginning of the new millennium for high-data-rate optical recording applications [47]. These phase-change materials are composed mainly of antimony and contain dopants like germanium, indium, gallium, or combinations thereof (5%– 25%). In particular, it is demonstrated that In-doped Sb alloys have both a high crystallization speed and a reasonable thermal stability (Figure 15),

along with limited power consumption (because of its relatively low melting point and thermal conductivity) [48]. For this reasons, this alloys should be promising candidates for the developing of an ultra-fast electrical PCM. In this regard, very recently, SiC-doped Sb alloy was proposed and explored for PCM applications [49], showing long data retention, fast switching speed and low programming voltages of the tested devices.

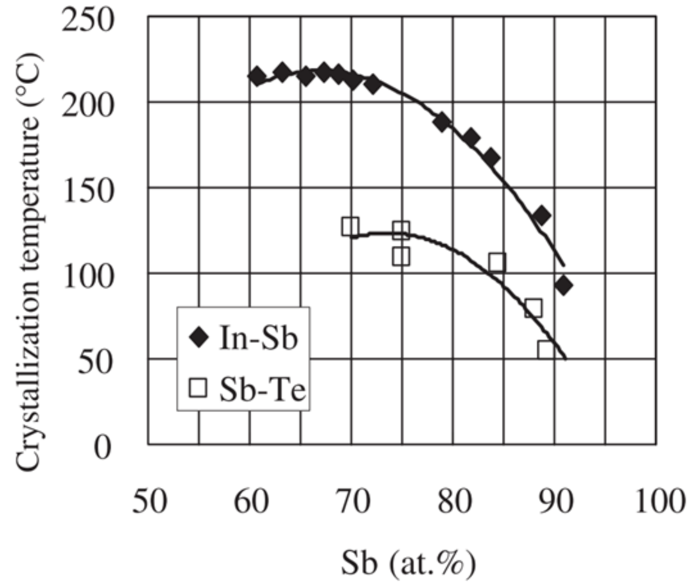


Figure 1-15: Crystallization temperature measured by DSC at 10 °C/min. [48]

Chapter 2 : Experimental techniques

2.1 The metal-organic chemical vapor deposition technique

Chemical vapor deposition (CVD) is a versatile process suitable for the manufacturing of coatings, powders, fibers, and nanostructures. With CVD, it is possible to produce most metals, many nonmetallic elements such as carbon and silicon as well as a large number of compounds including carbides, nitrides, oxides, intermetallics, chalcogenides and many others [50]. CVD may be defined as the deposition of a solid on a heated surface from a chemical reaction in the vapor phase. It belongs to the class of vapor-transfer processes which is atomistic in nature, as the deposition species are atoms or molecules or a combination of these. Beside CVD, they include various physical-vapor deposition processes (PVD) such as evaporation, sputtering, molecular beam epitaxy, and ion plating. Advantages and disadvantages of PVD and CVD are summarized in Table 1.

Feature	PVD	CVD
Purity	medium	high
Growth rate	high	medium
Step coverage	poor	excellent
Hazard	low	medium
Complexity, cost	low	medium

Table 2-1: Comparison of growth techniques [51]

The main advantage of CVD over PVD is the low defect density: since the bonding of atoms to one another is driven by the chemistry of the species, incorporation of external species is not favored. This is especially useful when growing nanostructures. In addition, CVD delivers a good step coverage and conformality in the deposition of thin films, that is crucial for the filling of high aspect ratio trenches such as in integrated circuit processing. The main drawback of the CVD is the increased complexity: while PVD requires only high-purity elemental precursors ('target' or powders), CVD employs complex molecular precursors. Moreover, the number of chemical reactions used in CVD is considerable and include thermal decomposition (pyrolysis), reduction, hydrolysis, disproportionation, oxidation, carburization, and nitridation. These reactions can be activated by several methods. The most important are as follows:

- Thermal activation, which typically takes place at high temperatures (> 900 °C), although the temperature can also be lowered considerably if metal-organic precursors are used.
- Plasma activation, which typically takes place at much lower temperatures (300–500 °C).
- Photon activation, usually with shortwave ultraviolet radiation, which can occur by the direct activation of a reactant or by the activation of an intermediate .

Metal-Organic CVD (MOCVD) is major area of CVD which is rapidly growing, particularly in semiconductor and optoelectronic applications. MOCVD (also known as Metal-organic vapor phase epitaxy, MOVPE) differs from conventional CVD in the usage of precursors that contain metals and organic ligands (C, H). In particular, metal-organics are compounds in which the atom of an element is bound to one or more carbon atoms of an organic hydrocarbon group. Many of the elements used in MOCVD are the metals of groups IIa, IIb, IIIb, IVb, Vb, and VIb, which are non-transitional. Actually, the term metal-organic is used somewhat loosely in CVD jargon, since it includes compounds of elements, such as silicon, phosphorus, arsenic, selenium, and tellurium, that are not considered metallic.

Ultra-pure precursors (as far as 99.9999% purity) shall be utilized to preserve the final purity of the grown film/nanostructure. The growth process involves the heating of the precursors up to a given temperature and at a given vacuum pressure when they are inside a proper container

(bubbler), into which the carrier gas (typically hydrogen or nitrogen) is compelled to flow, thus becoming saturated with the precursor vapors. The bubbler temperature, internal pressure, and gas mass flow ultimately set the concentration and amount of precursor that volatilizes to take part in the reaction. The mixture of carrier gas and precursor vapors is used to transport the reactants from the bubbler to the deposition chamber, controlling the molar flow of each precursor with a precision of the order of µmol/min. Parameters vary from precursor to precursor and do not depend on the final element to be deposited. Upon approaching the surface of the sample, the precursor dissociates into: 1) the element to be deposited, and 2) one or more additional molecules, typically hydrocarbons, as byproduct of the reaction. For the dissociation to be activated, energy has to be supplied to the molecule in the form of: heat. The deposition occurs when the partial pressures of the species to be deposited inside the reaction chamber reach a thermodynamic supersaturation condition with respect to the temperature and pressure: the system is therefore induced to restore equilibrium by lowering the concentration of the species in the vapor phase, namely realizing the "vapor to solid" transition. In the usual working conditions (normally controlled by mass transport or kinetics) the higher the growth temperature, the higher the deposition (i.e. dissociation) rate. The principle of the deposition process is sketched in the Figure 1.

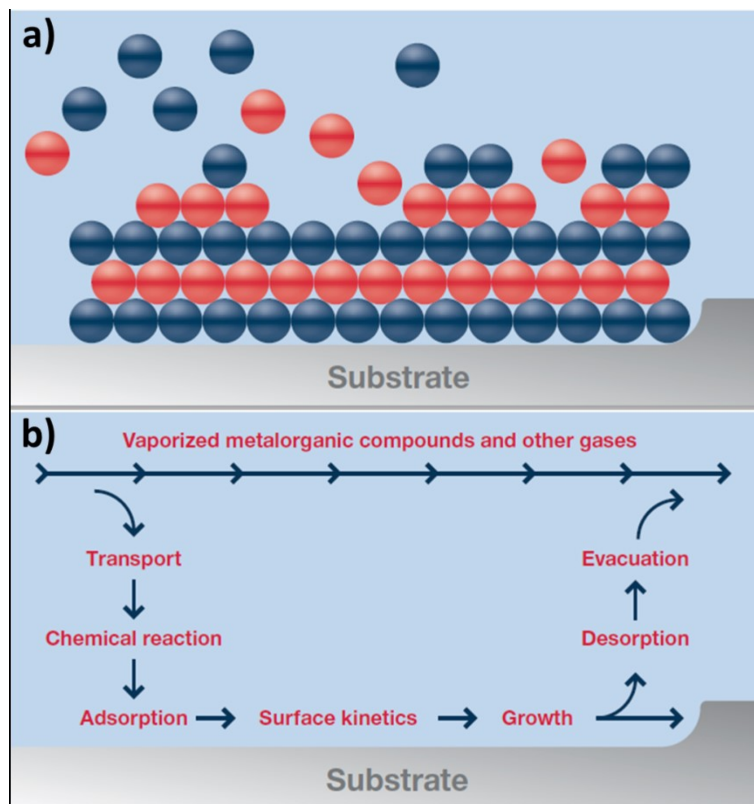


Figure 2-1: (a) Deposition process takes place on the substrates. (b) Surface processes while growing layers (or nanostructures) on the substrate. [52]

A thermal MOCVD AIX 200/4 reactor (Figure 2) at the Laboratorio MDM of CNR-IMM, Agrate Brianza (Italy) has been employed in this work to prepare samples of nanostructures of phase-change material, particularly NWs. Manufactured by AIXTRON SE (Germany), this reactor was developed for R&D and low scale production. Installation AIX 200/4 is based on horizontal low pressure reactor with gas rotation of the wafers. Our AIXTRON system it features up to four precursors lines, a heated growth chamber, a nitrogen gas glove box, and a pumping system. All deposition process is computer controlled. In this reactor the carrier and process gas is nitrogen. It must be noted that the use of N_2 brings the advantage of a simpler, safer operating condition than normal reactors where H_2, hydrides, or ammonia are used. However N_2 is inert at the growth temperatures employed, the activation rate of the deposition is remarkably lower than normal. The N_2 purity requirements are: concentration below 0.1 ppb for H_2O and below 0.5 ppb for O_2.

Figure 2-2: The MOCVD reactor and growth chamber (inset) at Laboratorio MDM

2.1.1 VLS mechanism for nanowires self assembly

As mentioned in the first Chapter, storage capacity and power reduction of PCMs can be basically achieved by acting on the phase-change material and/or on the programming volume size, meaning scaling down the memory cells. The use of 1D phase-change structures, such as NWs, makes it possible to fully exploit the scaling properties of the PCM device. The phase-change NW growth and its diameter, composition and crystallinity can be controlled. In this way, a NW can form a nano PCM cell itself. The energy required to induce the phase transition is lowered, not only because of the good structural properties of these nanostructures

(which can be defect- free when the NWs are self- assembled) and the high geometrical scaling, but also due to other aspects related to size effects.

Among the various techniques for the growth of self-assembled NWs, Vapor-Liquid-Solid (VLS) mechanism is the well established and the most widely accepted model. The VLS mechanism was reported by Wagner and Ellis in 1964 to explain the growth of Si whiskers using Au as a metal catalyst [53]. The name VLS it refers to the fact that the source material from the vapor passes through a liquid droplet and finally ends up as a solid. So, the VLS process can be divided into three steps. First, nanoparticles of catalyst (gold, platinum, or other alloys are suitable, according to the specific reaction) are deposited onto the growth substrate. The substrate is then loaded into the growth chamber and heated up to an appropriate temperature, so that the vapor-phase precursors mix with the nanoparticle to form a liquid eutectic mixture, according to the phase diagram of the considered system. The second step is the crystal nucleation upon gas adsorption and supersaturation. The last step is the axial growth from the crystalline seeds to form NWs.

Figure 3 schematically illustrates the bottom-up synthesis of NWs by the VLS process [54].

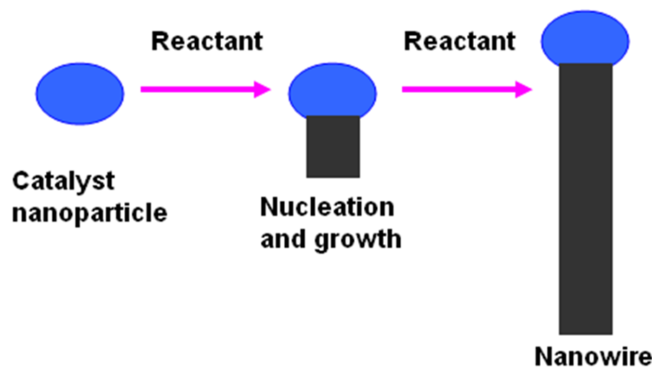


Figure 2-3: Schematic illustrations of the NW growth process by the VLS mechanism.[54]

According to the VLS mechanism, the diameter of the NWs is well controlled by the size of the catalytic nanoparticles.

In this work, several typologies of NWs, interesting for the realization of innovative PCM devices, have been synthesized by MOCVD coupled with VLS technique, using nanometer-sized gold nanoparticles.

2.2 The scanning electron microscope

The invention of the Scanning Electron Microscope (SEM) in the 1930s represented a revolution in nanotechnology because it extended imaging capabilities to unprecedented resolution. SEM can be considered the evolution of optical microscope, where electrons, instead of photons, are employed. In the SEM, the morphology of the sample surface is probed by collecting the electrons scattered back to the sensor while sweeping the electron-beam. Two reasons guarantee a higher resolution than optical microscope. First, electrons can be accelerated to higher energies and, therefore, smaller equivalent de Broglie wavelength:

$$\lambda_e = \frac{1.226}{\sqrt{E_e}} \,[\mathrm{nm}] \qquad (2.1)$$

ùwhere E_e is the electron energy in eV. That corresponds to a wavelength of 0.012 nm for 10 keV. Second, the electron-beam can be sharply focused by electromagnetic plates, and even swept in a raster. Therefore details can be resolved up to a minimum feature size equal to the theoretical beam focusing spot, its size being the limiting factor. Imaging magnification is achieved by shrinking the raster-scan width, and is therefore dependent on the resolution of the electromagnetic deflector plates, rather than the beam spot size. Up to 500,000 times magnification can be achieved in modern SEM that fit a 16 bit resolution analog-to-digital controller of the beam deflection.

The SEM schematic operation principle is shown in Figure 4. Electrons are produced at the top of the column, by a combination of thermoionic and field emission from a metal cathode (tungsten or LaB6). Then they are accelerated down and passed through a combination of lenses and apertures to produce a focused beam of electrons which hits the surface of the sample. The sample is mounted on a stage in the chamber area and, unless the microscope is designed to operate at low vacuums, both the column and the chamber are evacuated by a combination of pumps. The level of the vacuum will depend on the design of the microscope. The position of the electron-beam on the sample is controlled by scan coils situated above the objective lens. These coils allow the beam to be scanned over the surface of the sample. This beam rastering or scanning, as the name of the microscope suggests, enables information about a defined area on the sample to be collected. As a result of the electron-sample interaction, a number of signals are produced. These signals are then detected by appropriate detectors.

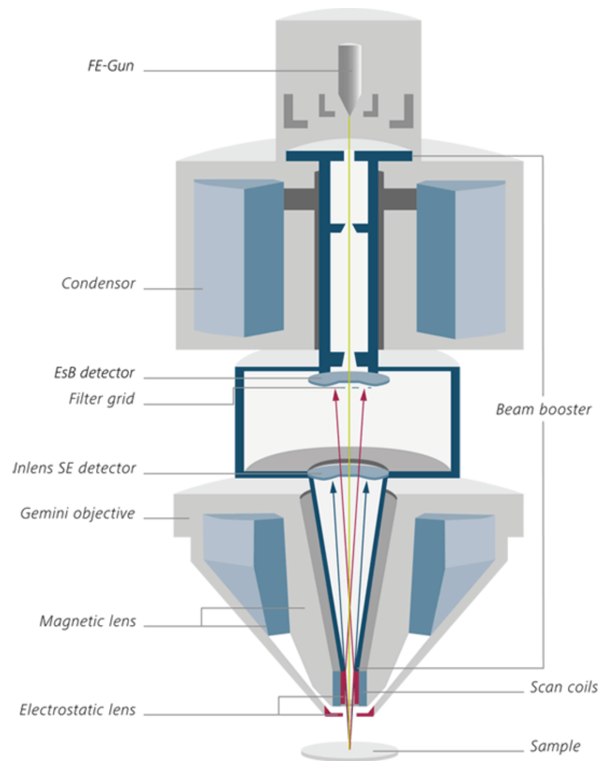


Figure 2-4: Schematic cross section of Gemini optical column. [55]

In particular, upon impacting the sample, the electrons of the beam (primary electrons, PE) are subject to several scattering events in which they release energy and momentum to the sample atoms and electrons. Because of their high energy, small mass, PE penetrate the sample, according to a distribution of trajectories exhibiting a distinctive ”pear” shape (and eventually collect into the sample forming a negatively charged region). In the PE-sample interaction, other electrons are extracted from the sample. Part of these electrons are the highly energetic, elastically back-scattered electrons (BSE) originating from both the surface and depth. Other PE cause the emission of electrons from the atomic core or electrons of the atomic shell of the sample material in inelastic scattering events, causing the emission of weakly energetic secondary electrons (SE), mainly from the sample surface. In general, as a consequence of electron emission, sample ionization occurs locally. If the sample is a dielectric or electrically insulated from the surrounding, a positive charge builds up on the samples surface. The charge buildup on the sample’s surface can be detected as a darker area; conductive paste is used to ground the sample potential to earth and avoid the shading effect. A schematic summary of electron-sample interactions is detailed in the following Figure. Note that the emission of Backscattered electrons, X-rays, and Auger electrons (occurring upon removal of an inner shell electron from the sample) is beyond the scope of this work and will be neglected.

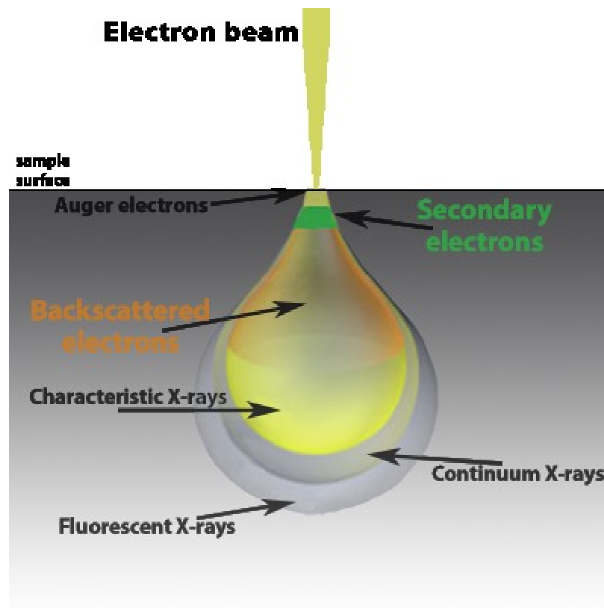


Figure 2-5 – Summary of electron-sample scattering events in a SEM. [56]

For imaging, two different detectors are employed in this work. An annular detector (in-lens) is located along the booster column. This detector allows an extremely efficiently detection of the secondary electron (SE) signal emitted from the sample. The low energy, SEs generated at the impact point of the PE beam are intercepted by the weak electrical field at the sample surface. They are then accelerated to a high energy by the field of the electrostatic lens and focused on the annular in-lens detector inside the beam booster located above the objective lens. While the in-lens detector provides the best high resolution information, a lateral SE detector in the specimen chamber provides optimum topographical information. Signals from both detectors may be mixed to deliver optimum image quality.

In the present work, a Zeiss SUPRA 40 FE-SEM of the MDM Labortorio of Agrate Brianza was employed for both imaging and electron-beam lithography (detailed in the next paragraph). The SUPRA 40 is a general purpose high resolution FE-SEM based on the 3rd generation GEMINI® column. Excellent imaging properties combined with analytical capabilities makes this workhorse suitable for a wide range of applications such as materials development, failure analysis, process control, nanotechnology and analytical applications.

2.3 Electron-Beam Lithography

Electron-beam lithography (EBL) is a technique used for the fabrication of micro- and nanostructures, based on the chemical modification of polymer resist films caused by electron irradiation. Two varieties of resist exist: positive and negative. Upon exposure to the e-beam, the positive (negative) resist solubility increases (decreases), as a result of the dissociation of C-

C bonds in the polymeric chain, and it is formed a highly stable structure, because of bond cross-linking. The ultimate resolution of EBL is not set by the resolution of electron optical systems, which can approach 0.1 nm, but by the resolution of the resist and by the subsequent fabrication process. EBL is unique amongst the non-local probe methods in this characteristic. Provided the highest resolution resists are used, the resolution of the other methods (e.g. optical lithography) is limited by the resolution of the imaging systems [57]. Mainly, the EBL resolution limit is due to the well-known proximity effect [58]. This effect is created by the forward-scattering of electrons in the resist and the backscattering of electrons from the substrate. The electron scattering leads to undesired exposure (e-beam energy deposited) of the resist in the unexposed regions adjacent to those exposed by the e-beam, which in turn causes changes in the dissolution rate of the resist. Therefore, the unexposed regions receiving the scattered electrons are also partially developed, which results in designed patterns with dimensions different from the target ones.

One of the main concerns in EBL preparation is the deposition of a flat, uniform, thin film of resist. These requirement can be met by spin coating the sample surface. The final thickness of film depends on: amount of resist, sample size, spin time, spin speed, and resist specific molar weight. As a matter of fact, higher molar weight resist have lower sensitivity. Subsequent curing is needed for stabilization and hardening of the film. Afterwards the resist is ready for exposure to the e-beam. To success in the fabrication of suitable micro- and nanostructures, a fine calibration of the e-beam operational parameters is mandatory: in particularly, electron high voltage (EHT), and aperture size (AP). The former should be as high as possible to improve beam focusing; the latter sets the beam current (I_{beam}). In combination with the raster sweep dwell time per step (T_{dwell}), and step size ($\Delta x \Delta y$) these parameters eventually set the electron dose per unit area (Dose), in $\mu C/cm^2$ according to the formula 2.2:

$$Dose = \frac{I_{beam}}{\Delta x \cdot \Delta y} T_{dwell} \quad (2.2)$$

Finally, beam magnification (MAG) and working distance (WD) set the exposed area width, height and step size.

A Zeiss Supra 40 SEM (described in the previous paragraph) equipped with a Raith Elphy Plus lithographic attachment of the Laboratorio MDM has been employed to fabricate some of the metallizations and electrodes required to prepare NW-based devices. The Raith Elphy Plus is a beam-blanker and pattern generator that remotely controls the SEM column during the EBL exposures. Lateral and vertical correction routines are available from the built-

in software, allowing high precision focusing and placement of the electron-beam during the exposure.

At the Center for Micro- and Nanostructures (ZMNS) of the TU of Vienna, a Raith e-LiNE has been used to manufacture other NW-based devices studied in this work. The e-LiNE is an electron beam lithography tool with a 100 mm by 100 mm travel range. It uses thermal field emission filament technology and a laser-interferometer controlled stage. The column voltage varies from 100 eV to 30 keV and the laser stage moves with a precision of 2 nm. There are six apertures on the system: 7.5, 10, 20, 30, 60, and 120 µm. The electron beam current is controlled by selecting the appropriate aperture. The system is equipped with a load lock. Typically, large area patterns are divided into small writing fields that are stitched together. The individual fields are written one by one by scanning the beam within the field.

2.4 The transmission electron microscope

The high-resolution TEM (HR-TEM) resolution is unsurpassed by any other probing tool at the atomic level. Contrarily to the SEM, here the electron beam source and the detector are located on opposite sides with respect to the sample. The e-beam crosses the section of the specimen before being collected by the sensor. The interaction between the small equivalent de Broglie wavelength and the lattice delivers an image, with resolution as small as ≈ 0.18 nm. The TEM can discern the position of lattice planes in a crystalline solid. Moreover, a lattice diffraction pattern can be obtained by computing the Fast Fourier Transform (FFT) on the HR-TEM image. The diffraction patter reveals information on the lattice spacing, and orientation. However, for the e-beam to cross the sample, complex sample preparation is required to produce thin slices (< 500 nm thick) by micro or nano machining.

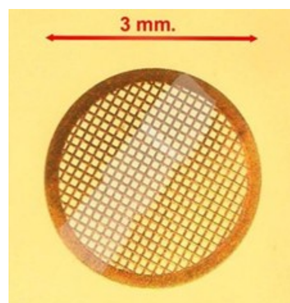


Figure 2-6: TEM grid

The TEM is convenient for imaging NWs, which have diameter smaller than 200 nm, thus requiring no special preparation. To this end, the NWs need to be dispersed on dedicated, micromachined holey carbon grids for the observation (see Figure 6). The grid is available with pitches of as little as 1 µm. After depositing the NW, it stick to the grid by electrostatic force

and it can be looked for in the microscope. The sample holder makes it possible to vary the incident angle of the electron beam, thus investigating the different crystallographic directions.

Additional capabilities are available in TEM equipped with scanning e-beam. In this tool, called STEM, the e-beam is swept in a raster over the sample. The rastering of the beam across the sample makes these microscopes suitable for analysis techniques such as mapping by energy dispersive X-ray (EDX) spectroscopy and annular dark-field imaging (ADF). These signals can be collected simultaneously, allowing direct correlation of image and quantitative data.

Analytical and conventional Transmission Electron Microscopy (TEM) studies were performed on selected NWs in a High Resolution (0.18 nm) Field Emission JEOL 2200FS, equipped with energy filter, 2 high angle annular dark field detectors and X ray microanalysis available at Istituto dei Materiali per l'Elettronica ed il Magnetismo (IMEM-CNR) in Parma, Italy.

2.5 X-ray grazing-incidence diffraction

The X-Ray diffraction (XRD) is a non-destructive technique for the qualitative and quantitative analysis of the crystalline materials, in form of powder or solid. Basically XRD is obtained as the "reflection" of an X-ray beam from a family of parallel and equally spaced atomic planes, following the Bragg's law: when a monochromatic X-ray beam with wavelength λ is incident on lattice planes with an angle θ, diffraction occurs if the path of rays reflected by successive planes (with distance d) is a multiple of the wavelength. Qualitative analysis (phase analysis) can be done thanks to the comparison of the diffractogram obtained from the specimen with a huge number of patterns included in the official databases. Single phases and/or mixtures of phases can be analysed with the programs available today. Moreover, this tool is especially useful for providing information on the orientation, axis, and size of crystal grains

Some of the samples of phase-change NWs in the present work have been characterized by X-ray diffraction (XRD) experiments, in grazing-incidence configuration by means of an ItalStructures HRD3000 diffractometer available at Laboratorio MDM.

Grazing-incidence diffraction (GID) is a scattering geometry combining the Bragg condition with the conditions for X-ray total external reflection from sample surfaces. This provides superior characteristics of GID as compared to the other diffraction schemes in the studies of thin films or nanostructure grown on the sample surface, as NWs. However, because the probing beam has a diameter of about 5 mm, this instrument can only probe large areas of samples, giving an average information generated from the contribution of several nanostructures grown on the surface of the sample. Nevertheless it is usually possible to

discriminate, for example, the contribution of different kind of NWs and therefore achieve useful information on the phase and growth orientation of them.

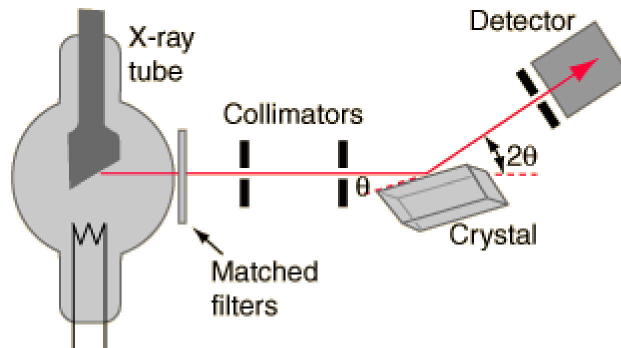


Figure 2-7: X-ray Bragg spectrometer.

2.6 The total reflection X-ray fluorescence technique

Total Reflection X-Ray Fluorescence (TXRF) is a surface elemental technique that can be used for compositional analysis of particles or nanostructures on smooth surfaces. TXRF is an energy dispersive technique. An incident X-ray beam impinges on a sample fixed on a polished substrate at very small angles (< 0.1°) in order to achieve a total reflection of the beam within the sample and the obtained fluorescence photons from the sample are detected. This setup increases the excitation efficiency of the sample and reduces the adsorption and scattering of the X-ray beam within the sample leading to a reduced background noise and a higher sensitivity. Moreover, the extreme grazing incidence geometry allows placing the detector very close to the sample surface. This results in a large solid angle for the detection of the fluorescence radiation.

In Figure 8 is sketched simplified the principle of the X-ray fluorescence spectroscopy. The specimen is excited with the primary X-radiation. In the process electrons from the inner electron shells are knocked. Electrons from outer electron shells fill the resultant voids emitting a fluorescence radiation that is characteristic in its energy distribution for a particular material. This fluorescence radiation is evaluated by the detector. In the reported Figure, one electron from the K shell is knocked. The resultant void is filled by either an electron from the L shell or an electron from the M shell. In the process the K_α and K_β radiation is generated, which is characteristic for the particular material.

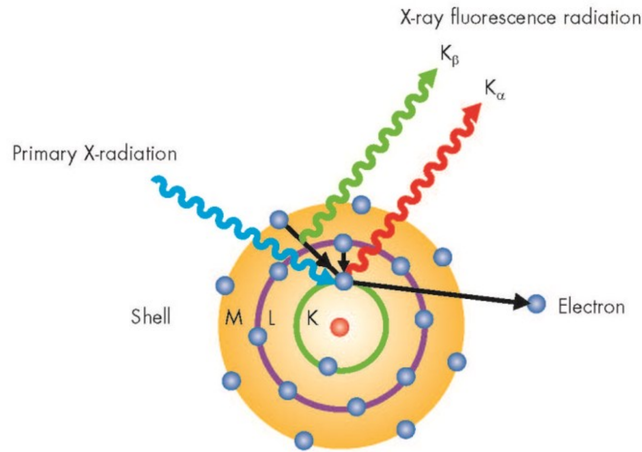


Figure 2-8: The Principle of the X-Ray Fluorescence Spectroscopy (XRF). [59]

The compositional analysis of the MOCVD growth samples was performed by TXRF spectra. X-ray fluorescence measurements were done using an ItalStructures XRR-TXRF 3000 system.

2.7 Metallization

NW-based devices preparation requires the deposition of metal electrodes or pads, in several process steps. The most straightforward and highest yield method to realize metallization is the evaporation technique. In this work it has been exploited the electron beam evaporation.

Electron beam evaporation is a PVD technique whereby an intense, electron beam is generated from a filament and steered via electric and magnetic fields to strike source material and vaporize it within a vacuum environment. At some point as the target material is heated via this energy transfer its surface atoms will have sufficient energy to leave the surface. At this point they will pass through the vacuum chamber, at thermal energy (less than 1 eV), and can be used to coat a substrate located above the evaporating material. Since thermal energy is so low, the pressure in the chamber must be below the point where the mean free path is longer than the distance between the target and the substrate (average distances are 300 mm to 1 meter). Allowing evaporated atoms/molecules to traverse the distance between source and substrate undisturbed by other atoms/molecules ensures "line of sight" arrival of material which is ideal when some type of masking is employed. Moreover, the low arrival energy is also advantageous for sensitive sample. In figure 9 is shown a scheme of an electron beam evaporator.

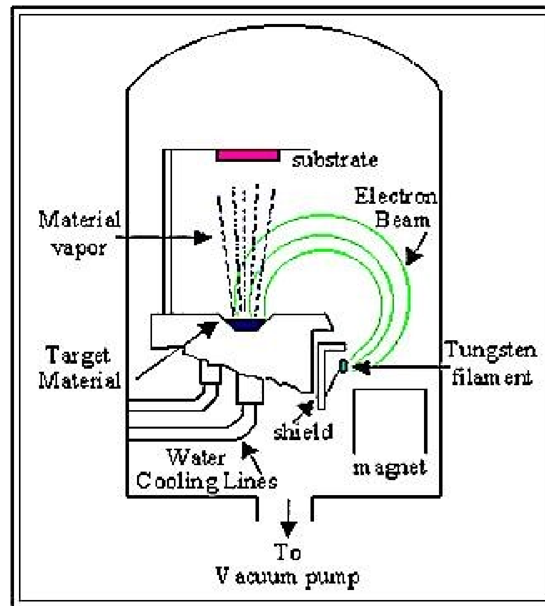


Figure 2-9: Scheme of an electron beam evaporator. [60]

A Leybold e-beam evaporator of the ZMNS of the TU of Vienna was used to perform most of the metal evaporations in this work. This system is a turbo pumped thin film evaporator with four water-cooled evaporation sources. Due to the capability to change targets under vacuum conditions, multi-layer films can be evaporated without exposing to air. Evaporation rates are controlled manually by varying the cathode current of the e-beam source. Rates are monitored with a standard 6MHz crystal oscillator. A nitrogen baffle for cooling the sidewalls of the machine is available in order to speed up the pump process.

2.8 Nanofabrication by dual beam (FIB/SEM) system

For some of the NW-based devices implemented in this work, the electrical contacts between the NWs and the microelectrodes were achieved with the help of an electron- and ion-beam-assisted direct-write nanofabrication process (see chapter 4 for additional details). To perform this process, a dual focused ion/electron beam equipped with a gas injection system has been employed.

The dual beam incorporates both a focused ion beam (FIB) column and a SEM column in a single system. The typical dual beam column configuration is a vertical electron column with a tilted ion column. Figure 10 shows such a configuration with the ion beam at 52° tilt to the vertical. To enable ion induced deposition (or milling) and electron imaging of the same region, dual beams typically have a coincident point where the two beams intersect with the

sample. With the sample at the coincident point, the advantages of the dual beam compared to a single-beam FIB become apparent.

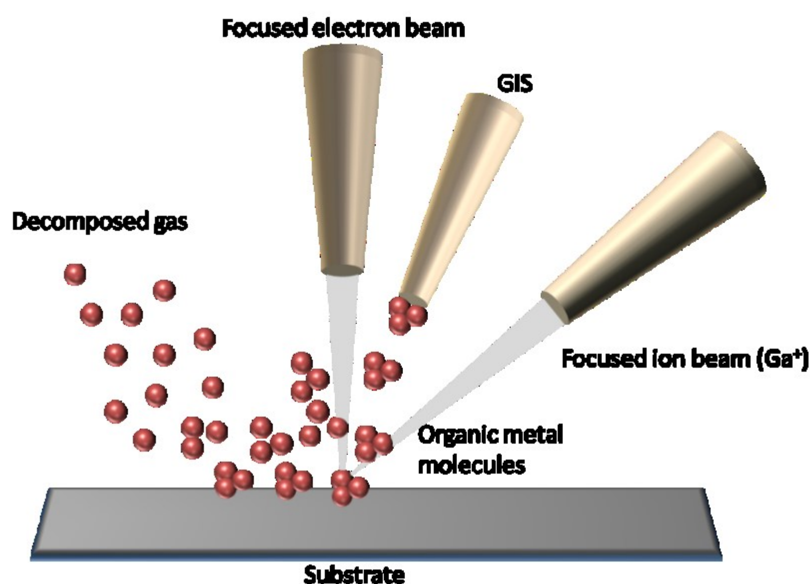


Figure 2-10: Illustration of deposition process in dual-beam instruments via electron beam-induced deposition and ion beam-assisted deposition. [61]

The electron beam (e-beam) is provided by a SEM column, the setup of which has been described in a previous paragraph, whereas the ion column employs a gallium Liquid Metal Ion Source (LMIS) to focus Ga+ ions into a narrow beam (i-beam) by means of magnetic lenses, which serve also for sweeping the beam in a raster. [62].

Selective material deposition (also called focused induced deposition) is one of the most powerful feature of dual beam FIB/SEM technologies. Deposit materials are often supplied by an internal gas delivery system that locally exposes a chemical compound close to the surface impact point via GISs, incorporated into the dual beam platforms. The chemical gas compound is usually in the precursor form and consists of organometallic molecules. When this compound is exposed to the region of interest, ion/electron beam performs a raster sweep. Upon impacting the precursor molecule, the i-/e-beam delivers energy to dissociate it and cause the deposition of the material into desired microstructures with nanometric resolution. The thickness of the deposition is controlled by both aperture size (i.e., current) and accelerating voltage (i.e., energy) of the selected beam.

To nanofabricate some of the phase-change NW-based devices investigated in this work, dual beam contacting was carried out using a standard Pt precursor ($C_9H_{16}Pt$). The benefit of dual beam (FIB/SEM) based direct-write technique for the rapid fabrication of site-specific Pt

contacts to NWs, however, has the drawback of the poor quality of the metal deposition. According to several Authors, FIB deposition produces a polycrystalline platinum, rich in contamination by: gallium (from the ion beam), carbon (from the precursor gas), and oxygen (when the base pressure is not optimal) [63]. Most of contaminants gather at the grain boundaries, with a detrimental effect on electrical conductivity. In addition, Pt deposited by e-beam has lower electrical conductivity (0.8 vs. 0.0045) and higher carbon contamination than that deposited by i-beam (60–75% vs. 40–55%) [64]. In both cases, it was demonstrated that the resistance of the deposited Pt structures can be decreased by thermally annealing treatments. However, the improvement of the metal quality is small, while the risk of contaminating the contacted NWs is high.

Some of the devices characterized in the present manuscript have been prepared in a FEI Helios NanoLab 600i Dual Focused Electron/Ion Beam during an author's internship at the Tyndall National Institute of Cork (IE).

2.9 Electrical measurement systems

To evaluate their conductivity, as-fabricated NW-based devices were tested using an Agilent 4156B semiconductor parameter analyser, at room temperature and ambient dark conditions. The source electrode was grounded, and a highly doped silicon substrate served as the back gate electrode. The results of this characterization are reported in the Chapter 4. The Agilent 4156B Precision Semiconductor Parameter Analyzer is fully, automatic, high performance instruments designed to measure, display graphically, and analyze the dc parameters and characteristics of electronic devices.

The characterization of nanoscaled PCM devices requires the use of programming pulses with very short duration (ns range) and very fast pulse falling time, which is crucial for the amorphization of phase-change materials, because a rapid quenching is required to avoid recrystallization. To perform the functional analysis on the phase-change NW-based devices the Transmission Line Pulse (TLP) technique has been exploited, using a HPPI® system. The results of this analysis will be presented in the chapter 5. The classical Transmission Line Pulse (TLP) measurement system consists of a 50 Ω high voltage pulse generator, a high speed digital oscilloscope, a Source Meter Unit (SMU) and a control computer. The typical range of the pulse waveform parameters are: output voltage amplitude in the range of up to ±4 kV, output currents up to ± 80 A, pulse width in the range of 1 ns up to 1.6 µs, pulse rise time in the range from 100 ps to 50 ns. The transient voltage and currents in the device under test (DUT) are recorded using a high speed digital oscilloscope with e.g. 12 GHz bandwidth and 40 GS/s sampling rate [65].

In this work, the differential voltage was measured directly at the device under test by the four-point Kelvin method (Figure 11). In addition, to measure the device resistance, direct current (d.c.) measurements were performed after each pulse, using a switch configuration with the SMU.

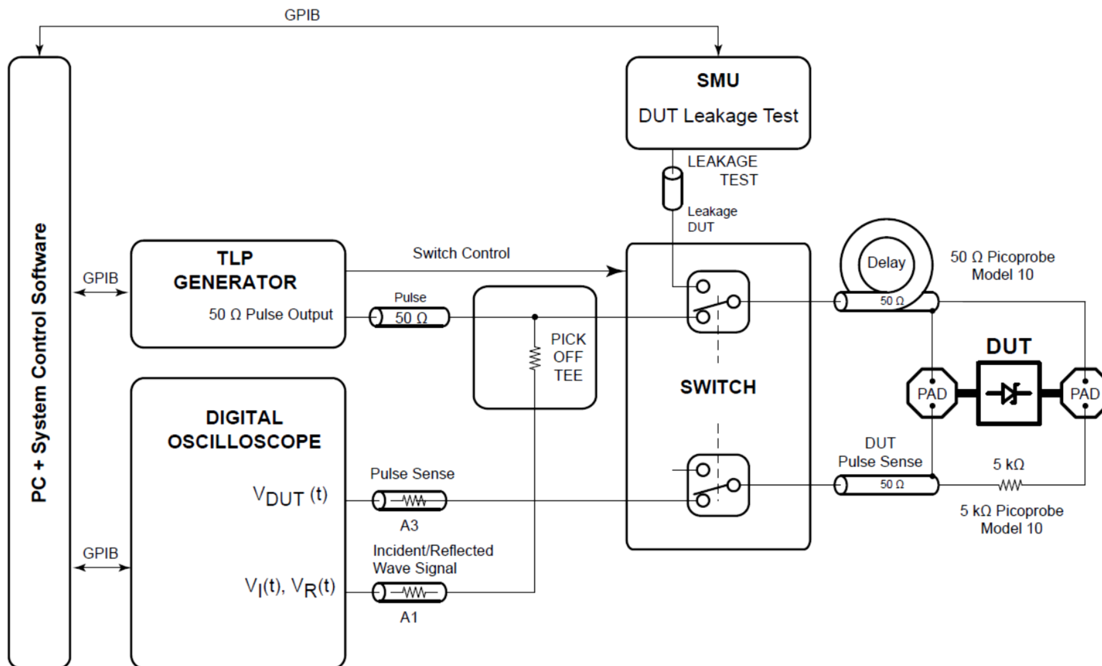


Figure 2-11: Four point Kelvin TLP method including dc leakage measurement. [65].

On the pulse force line a standard 50 Ω ground-signal type RF probe tip is used. The discrete current sensor should be located as close as possible to the DUT, typically not more than 5 cm far away. Thus, the setup is suitable for pulse with a duration > 5 ns. The sense probe tip has an integrated resistive divider, which enables the voltage to be measured with minimal parasitic loading (1-5 kΩ). The bandwidth of the high impedance probe is 7 to 11 GHz depending on the probe tip model. To ensure differential voltage measurement directly at the device sheath waves should be suppressed on the transmission lines with ferrite cores and the ground of the probe tip holder should be isolated from the chuck and DUT fixture surrounding grounds. The switch configuration with the source meter unit (SMU) is used to perform a dc (spot) current measurement in the pA to mA range after each current pulse.

Chapter 3 : Self-assembled In-based nanowires

As described in detail in the chapter 1, typical implementations of PCM devices are generally based on a heater/chalcogenide thin film architecture and exploit alloys of the pseudo-binary line between Sb_2Te_3 and GeTe [9], such as $Ge_2Sb_2Te_5$. In the last 15 years the research it is mainly focused on the continuing downscaling of size and cost of the PCMs. The scaling potential of PCM devices is subjected to three main challenges: (i) the physical downscaling of the cell by improvement of the technology, such as lithography, etching and deposition techniques, (ii) the programming current reduction by efficient cell downscaling, heat/current confinement and material optimization, and (iii) matching of reliability requirements, such as 10 years data retention in a specified temperature and failure probability range, or immunity to thermal interference in the array [66]. To overcome these challenges the investigation of ingenious fabrication processes, innovative memory cell geometry and unconventional phase change materials is required.

In this work it is proposed the use of self-assembled In-based NWs to realize extremely scaled PCM devices for low power applications. The reasons justifying the choice to exploit NWs and In-based phase change materials are discussed systematically in the chapter 1 of this thesis. In the introduction of this third chapter, however, it is useful to recall some of the benefits associated with this choice. First, self-assembly of NWs is a relatively simple

fabrication method that allow a tremendous downscaling of cell sizes. Moreover, self-assembled NWs have sufficiently high aspect-ratio to enable the self-heating approach, which is expected to be the most efficient for PCM applications [27]. In addition, NWs grown by bottom-up techniques are typically defect-free structures, whereas the conventional top-down approach with multiple lithographic and etching steps generally leads to structural/chemical degradation of the phase-change materials, which is detrimental to the high scalability, low power consumption and non-volatility requirements. Moreover, low programming currents have been already demonstrated in $Ge_2Sb_2Te_5$ and GeTe NW-based PCM cells [30], [67]. However, recrystallization studies showed a reduction of the activation energies and data retention times depending on the NW diameter [30]. One way to counteract this effect is given by the use of In-based phase change alloys, such as $In_3Sb_1Te_2$, which exhibit a higher crystallization temperature with respect to Ge-Sb-Te alloys [37], [68], [69]. This may help PCM face the scaling challenges in terms of reliability, as well as offer more opportunities for PCM devices to enter high-T applications, such as the automotive segment.

3.1 Synthesis by metal organic chemical vapour deposition

In this section is presented the MOCVD growth of In-based NWs. The growth was performed in a MOCVD AIX 200/4 thermal reactor, exploiting the VLS mechanism induced by Au metal-catalyst. Notably, the MOCVD growth allows high compositional control and relatively high deposition rates [70], while the VLS technique is useful to obtain defect-free mono-crystalline NWs with high aspect ratios [53][71] and very small diameters [30]. The VLS process, explained in chapter 2, is briefly described in Figure 1.

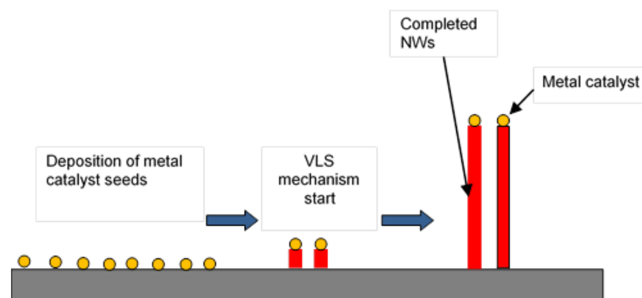


Figure 3-1: Schemes illustrating VLS path to obtain the nanowires.

In the VLS mechanism metal catalyst seeds are used on flat or structured substrates, to induce the 1D growth [53].

In this work two families of alloys containing Indium have been investigated:

- In-Sb-Te alloys
- In-Ge-Te alloys

The effect of different substrates, catalysts dimension, deposition parameters (e.g. substrate temperature and reactor total pressure) on the grown structures composition, morphology, microstructure, growth mode and selectivity were studied. In particular, the morphological analysis of the samples was operated by a Zeiss ® Supra 40 field emission Scanning Electron Microscopy (SEM), while their average compositional analysis was achieved by Total reflection X-Ray Fluorescence (TXRF) using an ItalStructures XRR-TXRF 3000 system, and an ItalStructures ® HRD3000 X-Ray Diffraction (XRD) system was used to evaluate the average crystal structure and growth orientation.

In this section are also reported the results of the microstructural and the selected area compositional analyses performed on the most interesting grown NWs. The local NW microstructure, growth direction and composition were characterized by High Resolution Transmission Electron Microscopy (HR-TEM), performed with a JEOL ® 2200FS microscope with point resolution of 0.18 nm, equipped with in-column Ω energy filter, 2 high-angle annular dark-field (HAADF) detectors and X-ray microanalysis (EDX). Such investigations were performed on tens of NWs of any grown sample to improve the statistics for all the results presented in this work.

3.2 Substrates preparation

Au nanoclusters were chosen as catalysts for the VLS process on Si(001), Si(111), Si(011) and SiO_2/Si(100) substrates. Au nanoclusters can be obtained both from the deposition of Au NPs dispersed in colloidal solutions and by thermal evaporation; this makes them suitable for their combination with the lithographic processes required for the fabrication of low and high density ordered arrays.

3.2.1 Catalysts obtained from colloidal solution of Au NPs

Commercially available BBI ® colloidal suspensions of Au NPs of sizes: 10, 20, 30 and 50 nm, were used. The p+ doped-Si (001), p+ doped-Si(111) and p+ doped-Si(011) substrates were first cleaned by HF 5% aqueous solution from native oxide and then a mixture of [colloidal suspension of Au] : [HF 1%] = 1:1 was dropped onto the substrate for 30s. The samples were then rinsed in DI water and dried with N_2. For the SiO2/Si(100) substrates, the samples were first treated with poly-L-lysine (PLL) solution to change the surface pH and favor the Au NP attachment to the substrates, and then exposed to the colloidal solution (without HF), in order to exploit the adsorption phenomenon that involves positively charged PLL and

negatively charged Au NPs. This process resulted in a dispersion of Au NPs on the substrate surface with surface densities in the order of 10^8 – 10^{10} cm^{-2} (Figure 2). Such values of surface NPs density are suitable for the NWs growth study targeted in the present work.

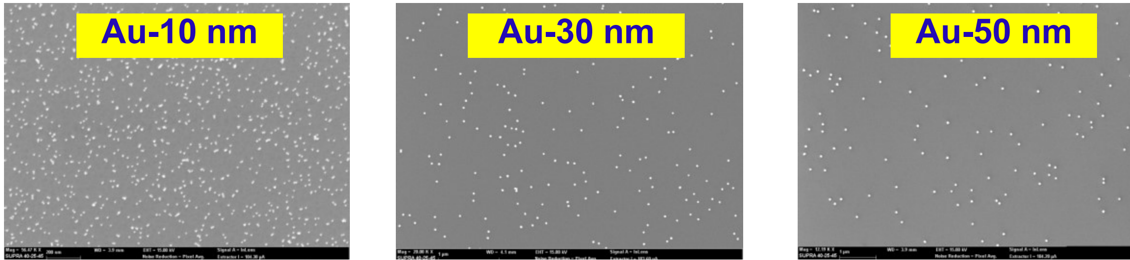


Figure 3-2: SEM images of catalytic nanoclusters on Si(100) obtained from the use of a colloidal solution of Au NPs of different sizes.

3.2.2 Catalysts obtained by evaporation of Au nano-islands

Au nanoclusters were obtained also by Au evaporation. For proper evaporated thicknesses, the Au deposition induced Au nanoislands with suitable sizes for the VLS process. The evaporation process, although more complex for the necessity of tuning the amount of evaporated material, is readily transferrable to a process involving EBL or photolithography, for the fabrication of ordered arrays of catalysts. The evaporation process led to higher density of Au clusters; on the other hand, a relatively wide variation of Au particle sizes is obtained (Figure 3).

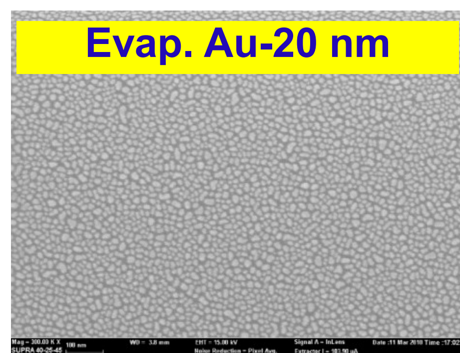


Figure 3-3: SEM image of catalytic nanoclusters obtained by Au evaporation on Si(100).

The most effective process for the preparation of catalytic nano-particles for the VLS process resulted to be the one making use of colloidal solutions of Au NPs. In fact, this procedure is relatively quick and provides nanoparticles with precise size and sufficient surface

density on all the substrates considered. This method was therefore chosen for the study of the MOCVD growth of NWs, object of the present chapter.

3.3 In-Sb-Te growth

In this section is reported the results of the growth of self-assembled In-Sb-Te nanostructures by MOCVD. The used metalorganic precursors were electronic grade Dimethylaminopropyl-dimethyl-Indium ($C_7H_{18}InN$, DADI), Antimony trichloride ($SbCl_3$,) and Bis(trimethylsilyl) Telluride ($Te(SiMe_3)_2$, DSMTe) provided by Air Liquide ®. The precursor vapours were transported to the reactor by the aid of ultra-purified N_2 carrier/process gas. Precursors partial pressures in the vapour phase were varied:

- from 1×10^{-3} to 9×10^{-2} mbar for DADI
- from 4×10^{-3} to 3.7×10^{-2} mbar for $SbCl_3$
- from 7×10^{-3} to 5.4×10^{-2} mbar for DSMTe

Total gas flow was 4.5 L/min; deposition time was 60 min. Different deposition runs were performed in the temperature range of (300−425)°C and pressure range of (300−750) mbar.

A systematic study for the MOCVD synthesis of In-Sb-Te nanostructures was performed on Si(001)/SiO_2, Si_{p+}(001) and Si $_{p+}$(111) substrates. The growth parameters were optimized on the basis of morphological and compositional analysis, thus identifying the best route to obtain In-Sb-Te NWs appealing for the realization of PCM devices. In particular, the final goal of the growth parameters optimization was to obtain NWs with a cross sections below 30 nm, in order to study the phase change behavior at extremely scaled size.

3.3.1 Growth study on $Si(100)/SiO_2$ substrates

Compositional, morphological and microstructural variation of In-Sb-Te growth on $Si(100)/SiO_2$ substrates as a function of different deposition parameters, such as: precursors molar flow rate (flux), reactor temperature and pressure, are reported in this paragraph.

The TXRF measured composition of the grown nanostructures as a function of In and Sb molar flow rates, keeping Te molar flow rate constant and fixed reactor temperature and pressure, is reported in Table 1.

As it can be seen, a decrease of the Sb molar flow rate is accompanied by a decrease of Te content in the NWs; incorporation of Sb and In do not seem to compete with each other. The morphology of these samples was characterized by SEM and is reported in Figure 4.

The change in molar flow rate produces a change in the grown structures, as well as of their composition, with NWs being obtained for the highest value of Sb molar flow rate and for the lowest values of the In molar flow rate (sample #600 in Table 1). The effect of the reactor temperature on the NW composition under the precursors molar flow rates of sample #600 was studied and is reported in Figure 5. The main results, also reported in the figure, indicated that the temperature can have an effect on the reduction of by products (background crystals) and on improving the morphology of the NWs.

Sample	Te flux [mol/min]	Sb flux [mol/min]	In flux [mol/min]	Composition (from TXRF)
#596	1.4E-5	2E-5	1.1E-5	$In_{0.76}Sb_{0.08}Te_{0.17}$ ($In_3Sb_{0.31}Te_{0.61}$)
#597	1.4E-5	4.9E-6	1.1E-5	$In_{0.78}Sb_{0.10}Te_{0.12}$ ($In_3Sb_{0.36}Te_{0.47}$)
#598	1.4E-5	4.9E-6	5E-6	$In_{0.74}Sb_{0.12}Te_{0.14}$ ($In_3Sb_{0.48}Te_{0.58}$)
#599	1.4E-5	2E-5	5E-6	$In_{0.70}Sb_{0.08}Te_{0.21}$ ($In_3Sb_{0.36}Te_{0.92}$)
#600	1.4E-5	2E-5	2.5E-6	**$In_{0.59}Sb_{0.11}Te_{0.31}$ ($In_3Sb_{0.54}Te_{1.58}$)**

Table 3-1: TXRF measured composition of IST nanostructures as a function of precursors molar flow rates (reactor T = 375 °C, reactor p = 750 mbar). Both atomic % and atomic formula of the measured composition are reported.

The formation of NWs is maximized at 350 °C, while there are more background crystals at 375 °C, accompanied by an increase of indium incorporation in the growth products. Regular NWs disappear at 425 °C, when bigger irregular wires and spheres are present on the substrate after the growth. This study evidenced that the temperature significantly influences the morphology of the growth products. Moreover, a pressure of at least 750 mbar is required to obtain deposition of nanostructures on the $Si(100)/SiO_2$ substrate and the temperature window

allowing the NW self-assembling was narrow, e.g. NWs were present in the (350-375)°C temperature range for a growth pressure of 750 mbar.

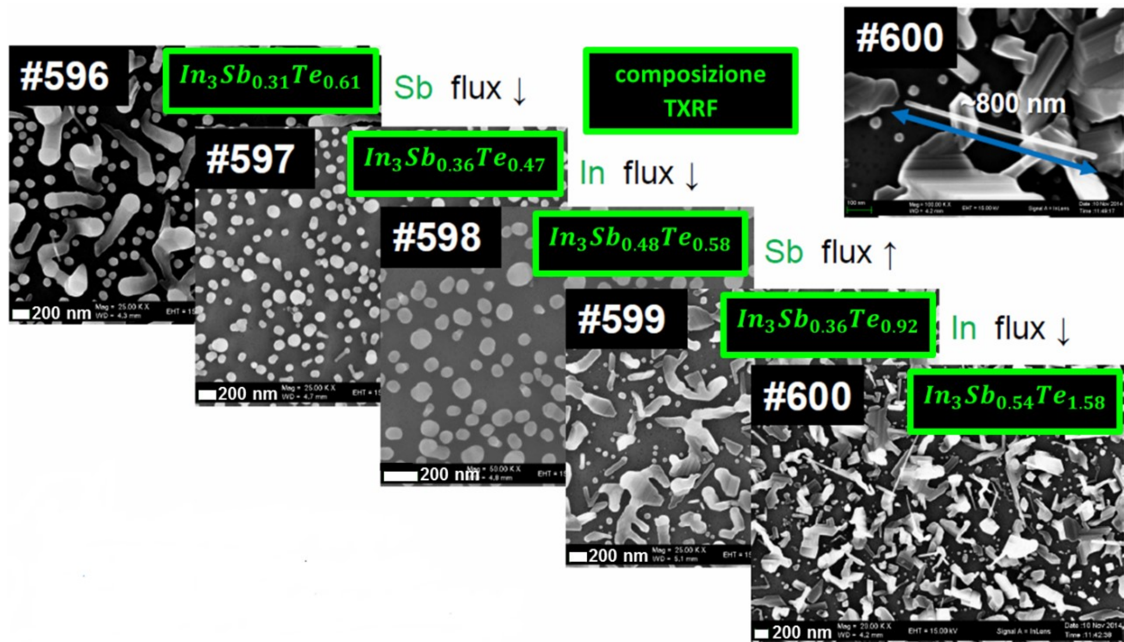


Figure 3-4: SEM and TXRF characterization of samples in Table 1. Reactor T = 375 °C, reactor p = 750 mbar.

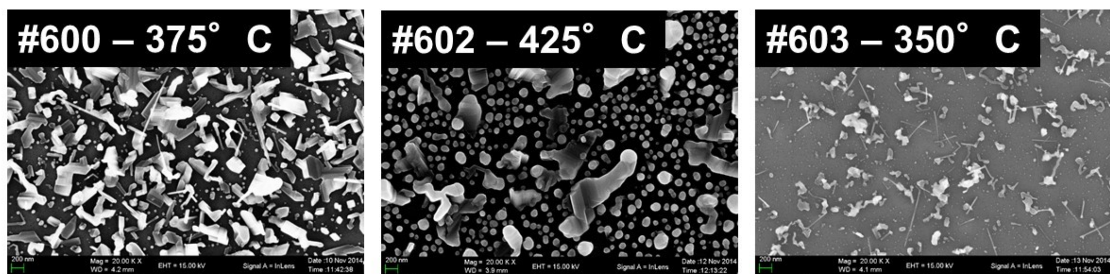


Figure 3-5: Grown nanostructures morphology for different values of reactor temperatures (molar flow rates in mol/min: In = 2.5×10^{-6}, Sb = 2×10^{-5} and Te = 1.4×10^{-5}; reactor p = 750 mbar).

3.3.2 NWs on silicon oxide substrates

In the following, it is presented the morphological and microstructural characterization of the optimized NWs (T = 350°C, p = 750 mbar) synthesized on the silicon oxide substrates. On the top of the Figure 6 is shown a low resolution TEM image of one entire NW, where a droplet, most likely the Au seed, on top of the NW is clearly visible, as expected by the VLS mechanisms. While the high resolution TEM images, shown on the bottom of the Figure 6, of

several NWs with different diameters demonstrated that the optimized NWs have good crystallinity and <110> growth direction.

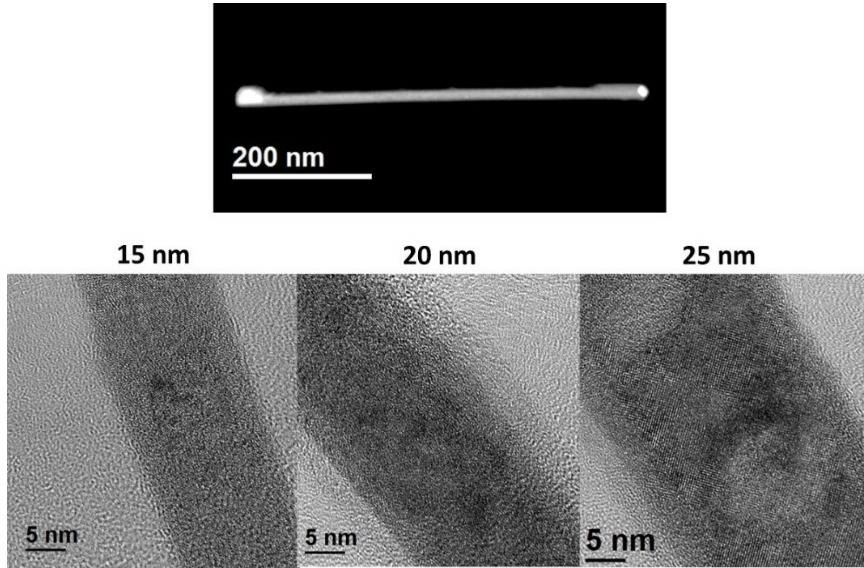


Figure 3-6: Low resolution TEM image of one entire NW (top) and high resolution TEM images of NWs with different size.

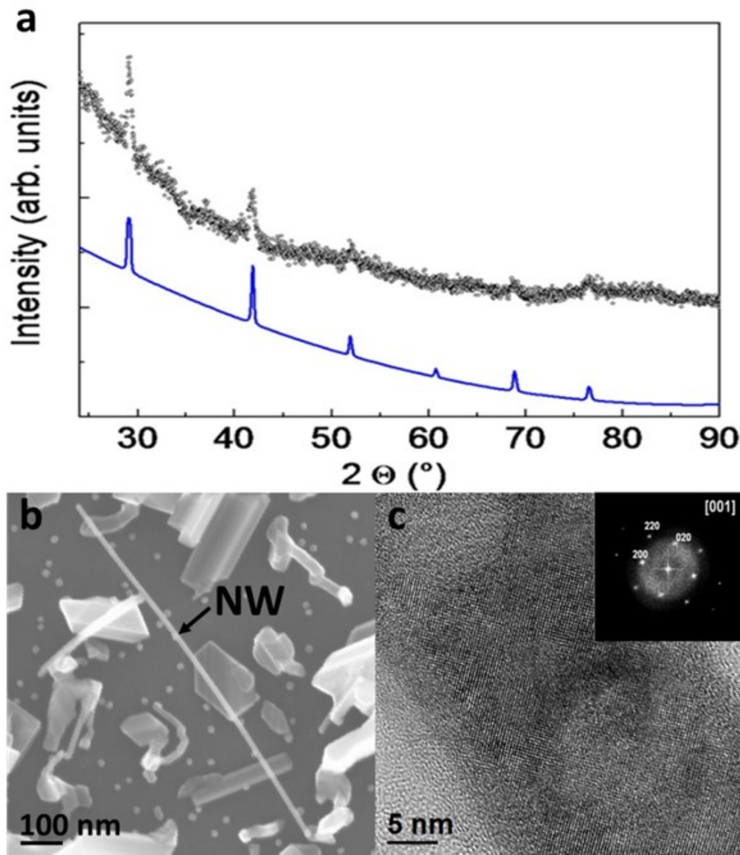


Figure 3-7: Structural and morphological analysis performed on In-Sb-Te sample grown on Si(001)/SiO_2 substrates at T = 350 °C, p = 750 mbar: (a) XRD data (dots) and expected diffraction pattern of the $In_3Sb_1Te_2$ stable phase (blue line), (b) SEM top view image showing a $In_3Sb_1Te_2$ NW and nanocrystals, (c) HRTEM image of a $In_3Sb_1Te_2$ NW and its fast Fourier Transform inset. [72]

Figure 7a shows the XRD analysis performed on a sample grown at 350 °C and 750 mbar on Si/SiO_2 substrate. The diffracted maxima can be identified as belonging to the $In_3Sb_1Te_2$ phase. It is worth noting that not only NWs, but also the other In−Sb−Te growth products concur to the XRD signal. The TXRF quantitative compositional measurement gave an overall In−Sb−Te composition for the deposited material in the proportion of $In_{3.0}Sb_{0.7}Te_{1.4}$. Since TXRF is a large area analysis technique, the contributions of the NWs and the background crystals could not be separated. The SEM top view image (Figure 7b) displays the morphology of the grown sample, where NWs with uniform diameter, with the Au NP at their tip, indicating the VLS mechanism, are present together with undesired nanocrystals and unreacted Au NPs. SEM cross section images have shown NWs randomly tilted with respect to the substrate surface. These NWs have an average diameter and length of 20 nm and 1 μm, respectively, being the average aspect ratio 50 (AR = length /diameter). The EDX spectra of the optimized NWs give a composition of $In_{63}Sb_8Te_{28}$ atom percentage (i.e. $In_3Sb_{0.4}Te_{1.3}$ after normalization to In), within a 2 at.% error. Figure 7c shows the HRTEM image of a single NW, demonstrating that it is partially crystalline, with the inclusion of some amorphous zones. In addition, by means of the fast Fourier transform pattern, reported as the inset in (Figure 7c), the 002 atomic spacing was measured and the value d_{002}= 3.04 Å was obtained, which is in good agreement with the literature values for $In_3Sb_1Te_2$ and with the presented XRD analysis.

The above results showed that the optimized NWs (T = 350°C, p = 750 mbar), obtained after the growth study performed on silicon oxide substrates, are $In_3Sb_1Te_2$ NWs with diameters as small as 15 nm and length up to 1 μm. The main drawback encountered using Si(001)/SiO_2 substrates was the impossibility to increase the NWs density and reduce the growth by-products on the surface. This would require a much lower deposition pressure, which in our case is detrimental for the NW growth rate, so that no deposition occurs.

3.3.3 Growth study on Silicon substrates

In-Sb-Te growth was then studied on Si_{p+}(100). Again, the effect of precursors flow rates, reactor temperature and pressure was investigated. Actually analoguos studies were performed on Si_{p+}(111) substrates, obtaining similar results. Here we focus on Si_{p+}(100), since it is of technological interest, even in view of the realization of ordered arrays of NWs.

The growth of nanostrutures on Si(100) substrates was found to be more efficient than on SiO_2. This allowed the reduction of the reactor pressure from 750 mbar down to 300 mbar. In particular, MOCVD growth studies were carried out at 450 mbar and 300 mbar. It is known that the NWs formation by VLS mechanism depends on the deposition pressure, which influences the reactants partial pressure and thus the concentration of the growth species inside the Au

catalysts, and generally a reduction of the growth pressure allows a better morphological quality of the grown NWs [70].

The effect of the precursors flow rate for a fixed value of reactor pressure and temperature was first addressed (Figure 8).

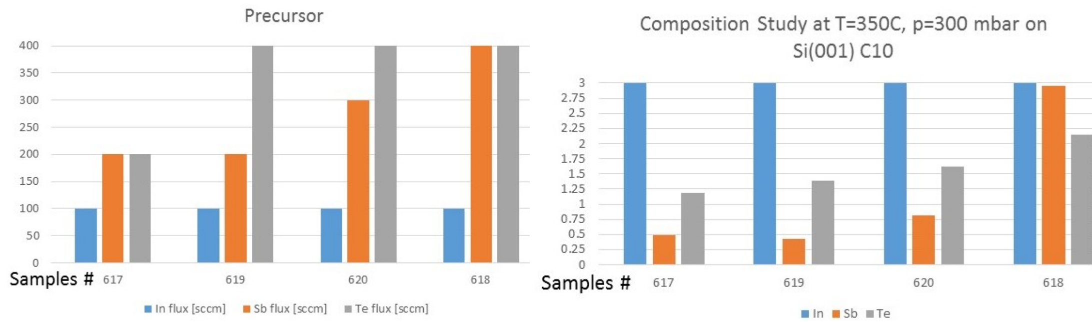


Figure 3-8: Effect of precursor flow rate (left) on TXRF measured composition (right). (reactor T = 350 °C, reactor p = 300 mbar).

The results indicate that the Sb/Te ratio increases monotonically as a function of the Sb flow rate for a constant Te flow rate (see Figure 9).

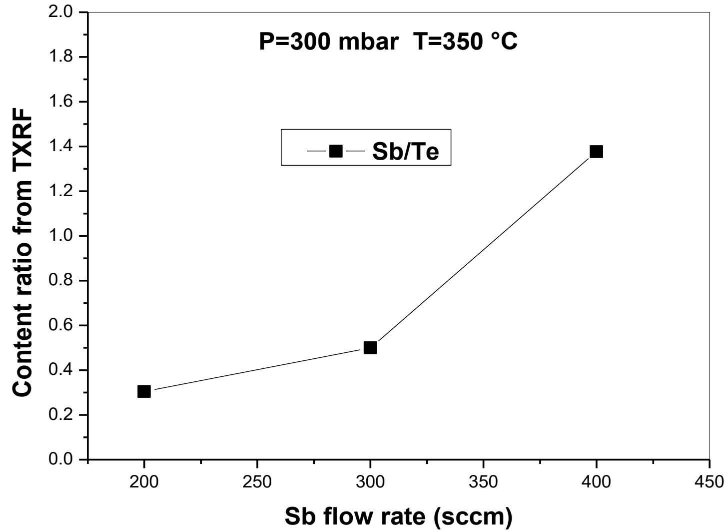


Figure 3-9: Change of Sb/Te content in the grown nanostructures (from TXRF) as function of Sb flow rate, for reactor p = 300 mbar and reactor T = 350 °C.

The effect of reactor temperature on the composition of NWs for fixed values of flow rate and reactor pressure are shown in Figure 10. The In content in the NWs monotonically increases with temperature with respect to both Sb and Te contents. The same trend was observed for reactor p = 450 mbar as reported in Figure 11.

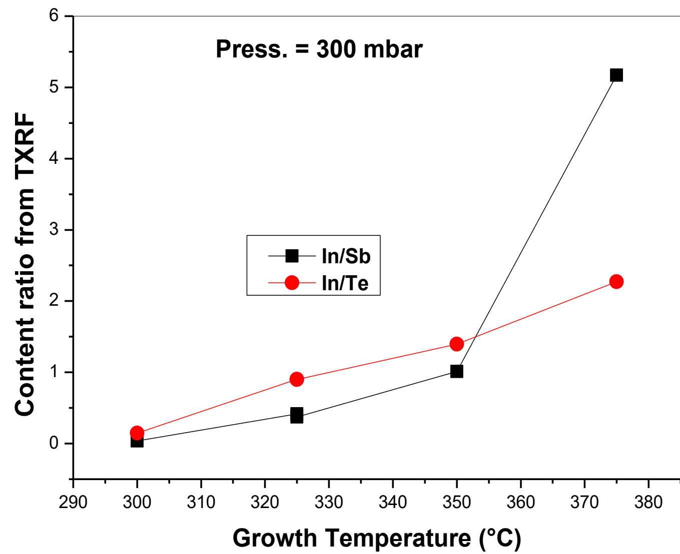


Figure 3-10: Change of In/Sb and In/Te content in the grown nanostructures (from TXRF) as function of reactor temperature (In, Sb, Te flow rates = 100, 400, 400 sccm, respectively; reactor p = 300 mbar).

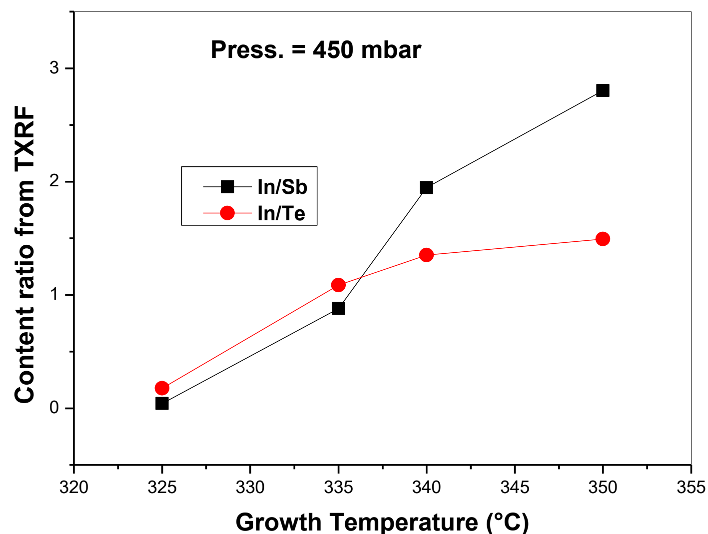
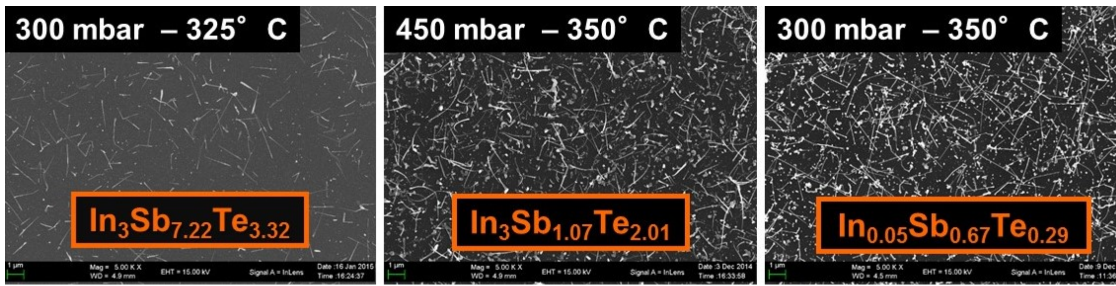


Figure 3-11: Change of In/Sb and In/Te content in the grown nanostructures (from TXRF) as function of reactor temperature (In, Sb, Te flow rates = 100, 800, 200 sccm, respectively; reactor p = 450 mbar).

NWs were obtained under a relatively wide range of above mentioned process parameters, including Au nanoparticles sizes. This allowed the growth of NWs with different morphology and different compositions. In Figure 12 some examples of NWs with a relatively large range of composition (measured by TXRF) are reported.



Sample #621; Au NPs 10nm   Sample#608; Au NPs 10nm   Sample #618; Au NPs 20nm

Figure 3-12: SEM images and TXRF measured compositions of In-Sb-Te NWs obtained for different growth parameters (including different Au NPs sizes).

As it can be seen, relatively dense, long (several microns) and thin (down to 10 nm diameter) NWs were obtained, with a relatively large range of In, Sb, Te contents.

In terms of NWs alignment, NWs grow with different angles with respect to the surface, as it can be seen in Figure 13.

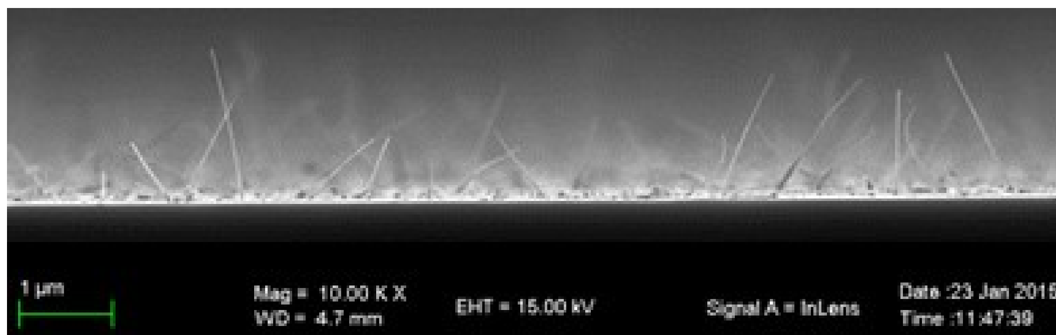


Figure 3-13: SEM cross section view of In-Sb-Te NWs.

In terms of NWs morphology, a change of the growth parameters produces a change in the NWs. It was for instance observed that, for fixed values of precursor flow rates and reactor pressure, an increase of reactor temperature of 25 °C led to a change of the NWs shape from uniform and very thin (≈ 15 nm diameter), to tapered NWs (Figure 14). In both cases NWs can be several microns long.

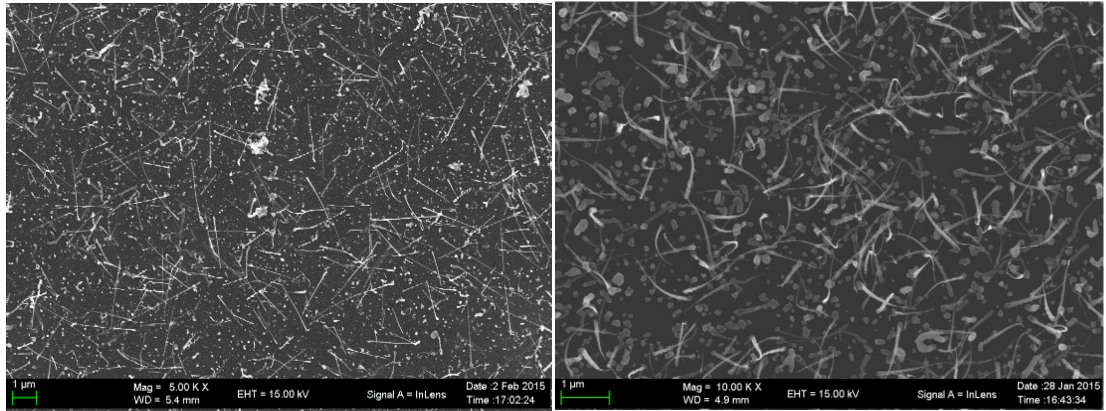


Figure 3-14: SEM images of two samples with In-Sb-Te NWs with different morphologies obtained with different reactor temperatures: uniformly thin for T = 335 °C (left) and tapered for T = 350 °C (right). (Other growth parameters are fixed).

The two different morphologies are more clearly shown in the SEM cross sections of Figure 15, showing uniformly thin NWs with constant diameter and tapered NWs. It should be noticed that in some cases, both types of morphologies are present on the same sample.

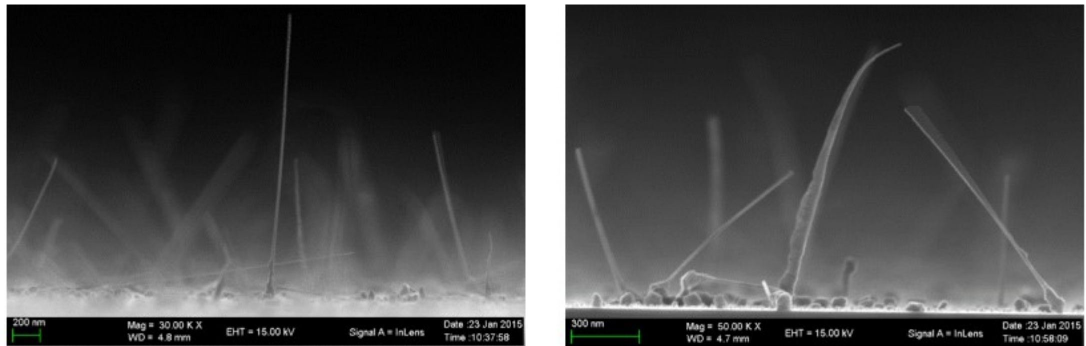


Figure 3-15: SEM cross view of NWs with different morphologies: uniformly thin (left) and tapered (right).

3.3.4 In-Sb-Te NWs on Silicon

In this paragraph is presented the characterization of the different typologies of NWs successfully synthesized on silicon substrates changing the growth parameters and the catalysts size. Thorough TEM observations of NW morphology, microstructure (by selected area diffraction) and composition (by EDX) analysis were performed on each of the observed NWs types.

3.3.4.a NWs grown with 10 nm Au nanoparticles

In this section it is reported the results obtained using gold nanoparticles with diameter of 10 nm as catalysts for the NWs growth. The grown In-Sb-Te NWs can be divided into four categories (Figure 16):

1. Thick (150–200 nm cross section) NWs with irregular morphology. Composition: (atomic %) $In_{50}Sb_{16}Te_{34}$ ≈ (atomic formula) $In_3Sb_1Te_2$.
2. Short, thick, regular and tapered NWs. Cross section ranging from 200 nm (at the bottom) trough 0 (at the top). Composition: (atomic %) $In_{48}Sb_{16}Te_{36}$ ≈ (atomic formula) $In_3Sb_1Te_2$.
3. Thin NWs (≈ 15 nm diameter). Composition: (atomic %): $In_{45}Sb_{20}Te_{35}$ ≈ (atomic formula) $In_3Sb_1Te_2$.
4. Thin (≈15 nm diameter) and long NWs. Composition (atomic %): $In_XSb_{80}Te_{20-X}$ ≈ (atomic formula) In-doped (< 6 %) Sb_4Te_1.

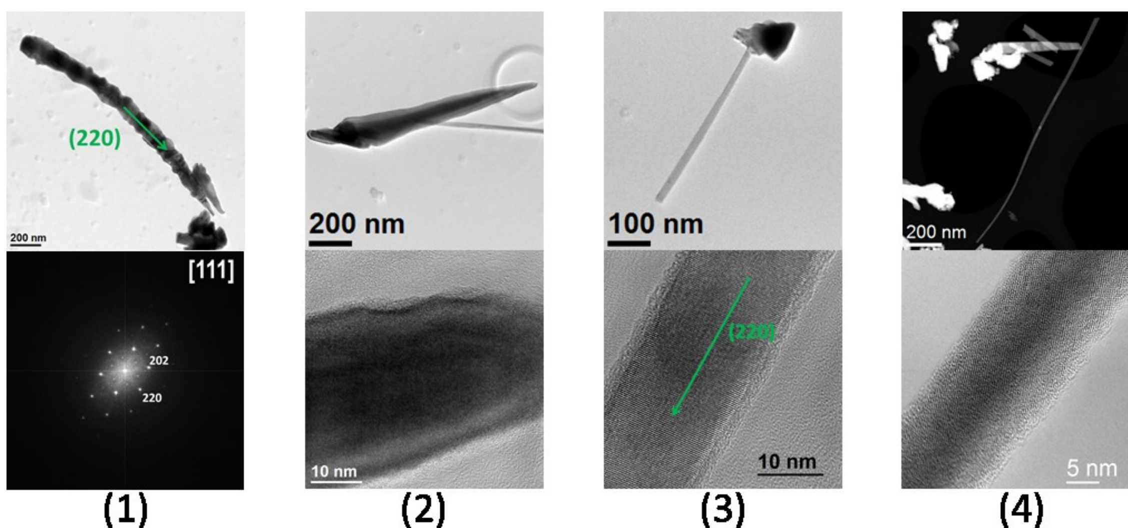


Figure 3-16: LRTEM (top) and HRTEM images or corresponding fast Fourier Transform (bottom) of different types of In-Sb-Te NWs grown on silicon substrate using 10 nm Au nanoparticles. Growth direction is indicated by a green arrow.

According to diffraction by TEM, NWs are generally single crystalline. In some cases, NWs are defected with morphological features probably connected to the presence of staking faults (e.g. type (1) NWs of Figure 16). Elemental analysis of the NWs indicated that mainly two compositions are formed varying the growth parameters, whereas a wider range of compositions was obtained from TXRF measurements preformed on the studied samples. On the one hand, the TEM investigation, unlike TXRF and XRD, provides exact information on the NWs, rather than values mediated over the all deposited structures (i.e. including byproducts and large crystals). On the other hand, the statistics of TEM is limited, as the number of analyzed NWs cannot be very large. However, comparison of SEM, XRD, TXRF and TEM results confirms that ternary In-Sb-Te NWs were obtained with morphologies and compositions determined by deposition parameters. In particular, the phase associated with each NW type was determined by electron diffraction and EDX. The $In_3Sb_1Te_2$ phase is found for NWs of type 1, 2 and 3 and the phase In-doped Sb_4Te_1 (atom percentage of In < 6 %) for NWs of type 4.

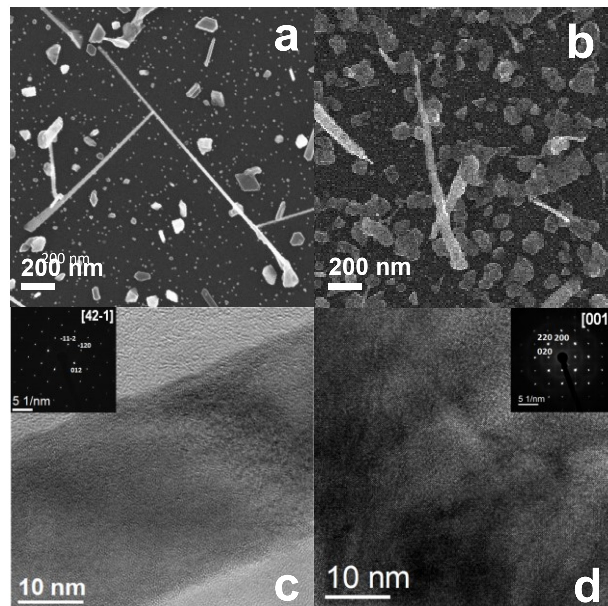


Figure 3-17 Morphological and structural analysis performed on In-Sb-Te NWs grown on Si(001) substrates at p=450 mbar and at different temperatures: (a) and (b) SEM top view images showing In-Sb-Te NWs and nanocrystals grown at 325 °C and 335 °C, respectively; (c) and (d) corresponding HRTEM images of a In-Sb-Te NW and their electron diffraction patterns inset.[72]

In particular, at 450 mbar NWs were present in the (325-350)°C temperature range. Such NWs exhibit different morphologies and chemical compositions, depending on the growth temperature. Notably, two different types of NWs were obtained. The first kind of NWs, grown at 325 °C, are thin and regular as shown in the SEM image of Figure 17a. These NWs have a diameter between 15-80 nm and a length between 1-3 µm, with an AR value up to 200. The second type of NWs, obtained in the range of temperature between 335 °C and 350 °C, are thick, conic and irregular (Figure 17b) with a maximum cross section in the range of 70-300 nm

and a length of 0.5-1.5 μm. It is worth noting that in such temperature range many nanocrystals also appeared, while their number is drastically reduced when the growth is performed at 325 °C. Moreover, the EDX measurement performed on single NWs indicated that "thin" NWs, such as those in Figure 17a, have a Sb_4Te_1 composition, with an In atomic percentage ranging between 4.5 and 5.5. Instead, "thick" NWs, such as those in of Figure 17b, have a $In_{2.76}Sb_{0.68}Te_2$ composition (after normalization of Te to 2). Figures 17c and 17d show the HRTEM images of a "thin" and a "thick" NW, respectively, each with its electron diffraction pattern. It has to be noted that the NW in Figure 17c has a high crystalline quality, while the one in Figure 17d is highly defected. Therefore, In-doped Sb_4Te_1 single crystal NWs were obtained at 325 °C and defective $In_3Sb_1Te_2$ NWs were obtained in the range between 325 °C and 350 °C.

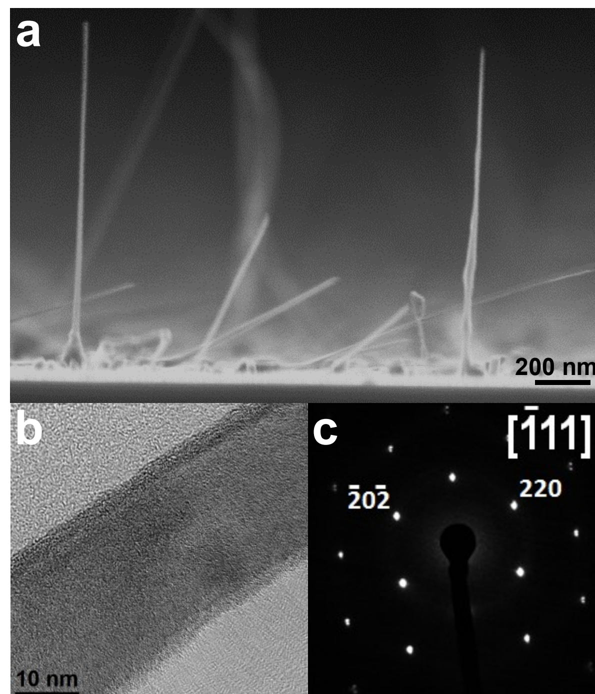


Figure 3-18 Morphological and structural analysis performed on In-Sb-Te NWs grown on Si(001) substrates at p = 300 mbar and 325 °C: (a) SEM cross view image of $In_3Sb_1Te_2$ NWs on Si(001), (b) HRTEM image of a $In_3Sb_1Te_2$ NW, and (c) its electron diffraction pattern.[72]

It has to be recalled that, for the purpose of PCM operation, the initial crystalline quality of the NWs is supposed not to be crucial. However, we observed that an improved NW morphology and crystal structure could be obtained by decreasing the reactor pressure to 300 mbar. Therefore, a further study of NWs grown at temperature among (300-375)°C was carried out at p=300 mbar. In addition to the two types of NWs obtained at 450 mbar, a new kind of NWs, with interesting features, has been grown at 325 °C, 300 mbar. Figure 18a shows a SEM cross view image of some of these $In_3Sb_1Te_2$ NWs grown on a Si(001) substrate. The NWs were randomly tilted with respect to the silicon surface and their average diameter was 15 nm, while

their length varied between 1 and 3 µm. Consequently, their AR varies between 70 and 200. The EDX spectroscopy revealed that the chemical composition is $In_{45}Sb_{20}Te_{35}$ atomic percent ($In_3Sb_{1.3}Te_{2.3}$ after In normalization to 3), while electron diffraction pattern on a single NW (Figure 18c), indicated a crystalline structure compatible with the rock salt phase of $In_3Sb_1Te_2$. In addition, the HRTEM images, (Figure 18b), highlighted that $In_3Sb_1Te_2$ NWs, grown at 300 mbar and 325 °C on Si(001) surface, are high quality single crystals. Finally, it is important to notice that low growth pressures, such as 300 mbar, significantly increase the NW density and reduce the number of larger crystals and other by-products.

It is worth to emphasize that, among the different NWs typologies, synthesized on silicon substrates using 10 nm Au nanoparticles, the ultra-thin defect-free $In_3Sb_1Te_2$ and In-doped Sb_4Te_1 NWs (with diameters down to 15 nm) were the most promising for the realization of PCM devices for low power applications, due to their morphology and chemical composition.

3.3.4.b NWs grown with 20 nm Au nanoparticles

In this section it is reported the results obtained using gold nanoparticles with diameter of 20 nm as catalysts for the NWs growth on silicon substrates.

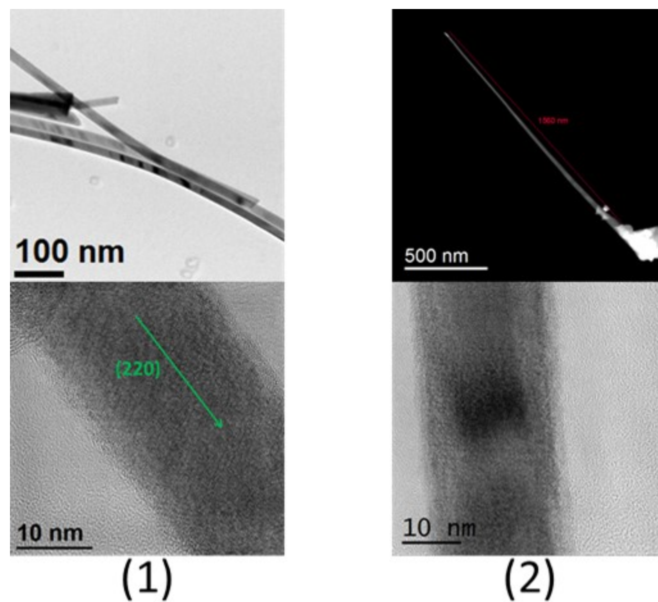


Figure 3-19: LRTEM (top) and HRTEM (bottom) images of In-Sb-Te (1) and In-doped Sb (2) NWs grown on silicon substrate using 20 nm Au nanoparticles. Growth direction is indicated by a green arrow.

These NWs can be divided into two categories:

1. Regular, thin (≈25 nm diameter) and long $In_XSb_{80}Te_{20-X}$ NWs.
2. Regular, thin (≈25 nm diameter) and long In_XSb_{1-X} NWs.

Figure 19 shows LRTEM and HRTEM images of both categories of the grown NWs. According to TEM analysis, both these typologies of NWs are high quality single crystals. Whereas, EDX

analysis of the NWs indicated that two compositions are formed varying the growth parameters. In particular, for the MOCVD growths performed at 450 mbar and in the temperature range of (325-350) °C, the chemical composition of the NWs is $In_XSb_{80}Te_{20-X}$, like that of the "type 4" NWs described in the previous paragraph, with an Indium content of about 3%. While, for the growths developed at 300 mbar and 325 °C, the NWs exhibit an In_XSb_{1-X} composition with an Indium content ranging from 5% and 15%. Notably, this kind of NWs have not been obtained using 10 nm Au nanoparticles, for the explored growth parameters in this work. Regarding the description of the morphology and the microstructure of the $In_XSb_{80}Te_{20-X}$ NWs, refer to the analysis performed on "type 4" NWs grown using 10 nm Au nanoparticles in the previous section of this chapter. In the following it is reported the morphological and microstructural analysis of the grown In_XSb_{1-X} NWs.

These NWs were randomly tilted with respect to the silicon surface and their average diameter was 25 nm, while their length varied between 1 and 6 µm. The In doped Sb NWs showed very regular shape. In particular, they were slightly tapered and exhibited well defined faceting (squared section). Figure 20 reports a HRTEM image of an In_XSb_{1-X} NW and its fast Fourier Transform. Lattice parameters and diffraction pattern are all consistent with the rhombohedral structure of the metallic Antimony. In particular, the measured cell parameter is about 4% longer than that reported in the literature for the metallic Antimony, probably due to the doping with Indium. Therefore, the In-doped Sb phase has been assigned to the grown In_XSb_{1-X} NWs.

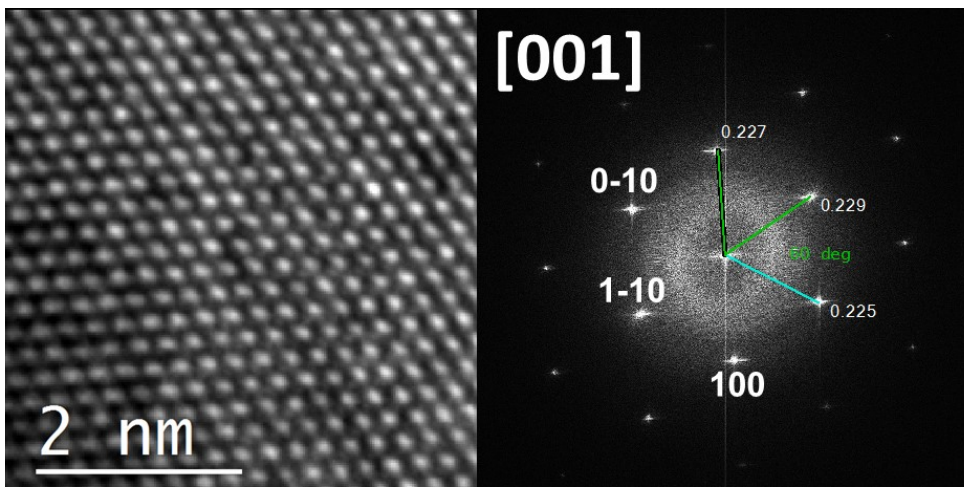


Figure 3-20: HRTEM image of an In-doped Sb NW (left) and its fast Fourier Transform (right).

3.4 In-Ge-Te growth

In this section are reported the results of the growth of self-assembled In-Ge-Te NWs by MOCVD. The NWs growth was performed exploiting the VLS mechanism induced by Au metal-catalyst NPs with average sizes of 10, 20, respectively. The Au NPs were dispersed on Si(100), Si(111) and Si(110) 1 cm^2 substrates, according to the procedure explained at the beginning of this chapter.

The metalorganic precursors were electronic grade dimethylaminopropyldimethylindium ($C_7H_{18}InN$), and tetrakisdimethylaminogermanium ($Ge[N(CH_3)_2]_4$) and bis(trimethylsilyl)telluride ($Te(SiMe_3)_2$) provided by Air Liquide® and were transported to the MOCVD reactor by an ultra-purified N_2 carrier/process gas. For each size of the Au NPs catalysts, a wide range of MOCVD process parameters was evaluated. The partial pressures in the vapor phase of dimethylaminopropyldimethylindium (P_{In}), tetrakisdimethylaminogermanium (P_{Ge}) and bis(trimethylsilyl)telluride (P_{Te}) were varied in the range $5 \cdot 10^{-4}$ to $2 \cdot 10^{-3}$, $1 \cdot 10^{-2}$ to $5 \cdot 10^{-2}$ and $5 \cdot 10^{-3}$ to $5 \cdot 10^{-2}$ mbar respectively, while the reactor temperature (T_R) and reactor pressure (P_R) were varied in the range of 350 to 500 °C and 400 to 500 mbar, respectively. The deposition times (t_{dep}) ranged from 60 to 210 min.

3.4.1 Growth study

For all combinations of trialed MOCVD growth parameters, NW-like growth was obtained only for $P_{In} = 5 \cdot 10^{-4} - 2 \cdot 10^{-3}$ mbar, $P_{Ge} = 1 \cdot 10^{-2} - 5 \cdot 10^{-2}$ mbar, $P_{Te} = 5 \cdot 10^{-3} - 5 \cdot 10^{-2}$ mbar and T_R = 400-450 °C. The variation of the P_R in the investigated range did not have any effect on the morphology of the deposits. In Figure 21 (a) an SEM top view image of a typical NW-like growth on a Si(100) substrate is reported. A very dense growth of NWs is obtained when 10 and 20 nm Au-NPs are used. NWs lengths are generally in the range of 1.5 – 2 µm, while diameters are in the range of 15 – 20 nm. From Figure 21, it can also be seen that the NWs are aligned along some preferential directions with respect to the substrate. Measurements of the inclination angle with respect to the substrates using top and side view SEM images showed that the NWs are directed along the <110> directions of the Si(100) substrate. The same holds when Si(111) substrates were used. Consistently, when we used Si(110) oriented substrates, a fraction of vertically aligned NWs was obtained (Figure 21 (b)). It has to be remarked that the possibility of controlling the orientation of the NWs by, e.g., epitaxy can represent an important advantage for their technological applications.

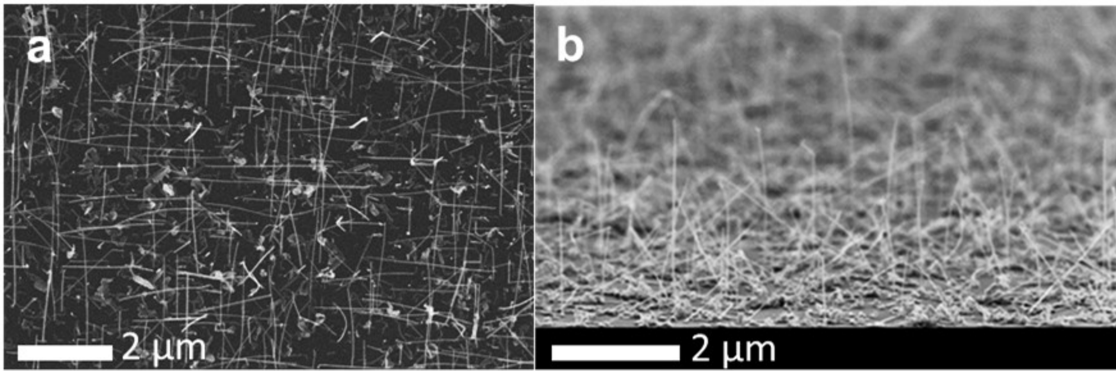


Figure 3-21: a) SEM top view image of a 10 nm Au NPs catalyzed In-Ge-Te NWs growth on a Si(100) substrate; b) SEM tilted view of 20 nm Au NPs catalyzed In-Ge-Te NWs growth on a Si(110) substrate.

The size of the Au NPs strongly influences the morphology of the deposits. In particular, the density and alignment of the NWs decreases with increasing Au NPs sizes. Also, larger NPs produces NWs with larger diameters, consistently with the VLS growth mechanism. However, the most striking effect of the precursors' size is on the microstructure of the NWs.

3.4.2 In-Ge-Te NWs

HR-TEM analysis revealed that two main types of NWs are obtained, depending on the dimeter of the Au NPs.

3.4.2.a NWs grown with 10 nm Au nanoparticles

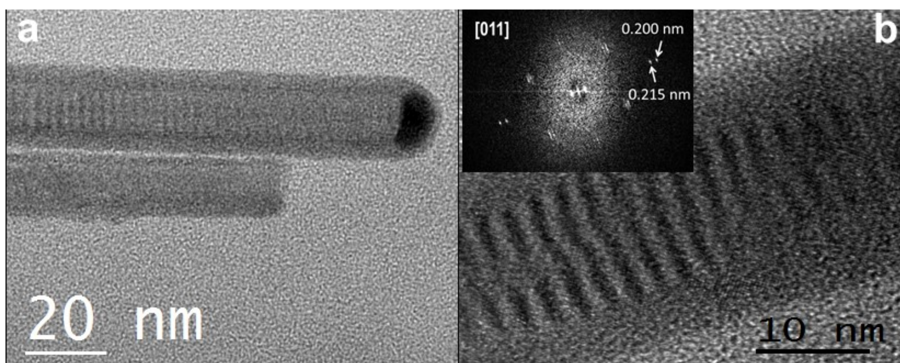


Figure 3-22: (a) TEM image of one Ge/In_2Te_3 core/shell NW. (b) HRTEM image of an Ge/In_2Te_3 NW and its fast Fourier transform (inset).

The first type is represented by Ge/In_2Te_3 core/shell NWs. This is the dominant type of NWs when 10 nm Au NPs are used. Figure 22 (a) reports a TEM image of one of these NWs, where is clearly visible its core/shell structure.

TEM imaging and corresponding fast Fourier transform (FFT) evaluation, along with EDX compositional analysis, revealed that this type of NWs is formed by a single crystalline cubic Ge core, with a <110> growth direction, surrounded by a crystalline In_2Te_3 cubic phase shell. Figure 22 shows some results of the performed TEM characterizations. In particular, in the inset of Figure 22 (b) is reported the FFT of a core/shell NW where are visible two distinct diffraction patterns. These patterns have lattice parameters equal to 0.200 nm, compatible with the d_{220} of the cubic Ge, and 0.215 nm, consistent with the d_{220} of the cubic In_2Te_3 [73], respectively. EDX analysis allowed to assign the Ge cubic phase to the core of the NWs and the In_2Te_3 cubic phase to their shells. Figure 23 (a) reports the microstructural characterization of a Ge/In_2Te_3 core/shell NW on which compositional map (Figure 22 (b)) and longitudinal profile (Figure 22 (c)) were also measured by EDX.

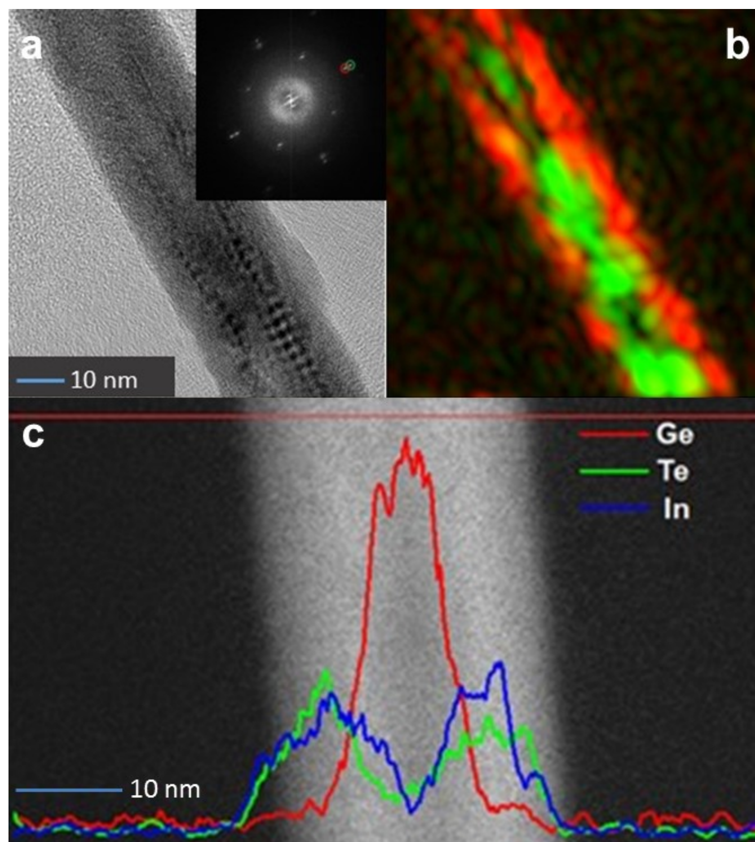


Figure 3-23: Ge/In_2Te_3 core/shell NW (a) HRTEM image and its FFT, (b) EDX compositional map, (c) EDX longitudinal profile analysis.

Remarkably, the collected FFTs also showed that the core and the shell of this type of NWs are in epitaxial relationship. In addition, Moiré fringes, formed by the overlap of different crystalline lattices, have been observed in the TEM images of these NWs, for example in Figure

22 (b). This phenomenon further confirm that these NWs have a core/shell structure with a cube on cube growth of In_2Te_3 on Ge.

3.4.2.b NWs grown with 20 nm Au nanoparticles

Besides of core/shell NWs, Ge-doped InTe NWs are also observed when 20 nm Au nanoparticles have been used to catalyze the MOCVD growing.

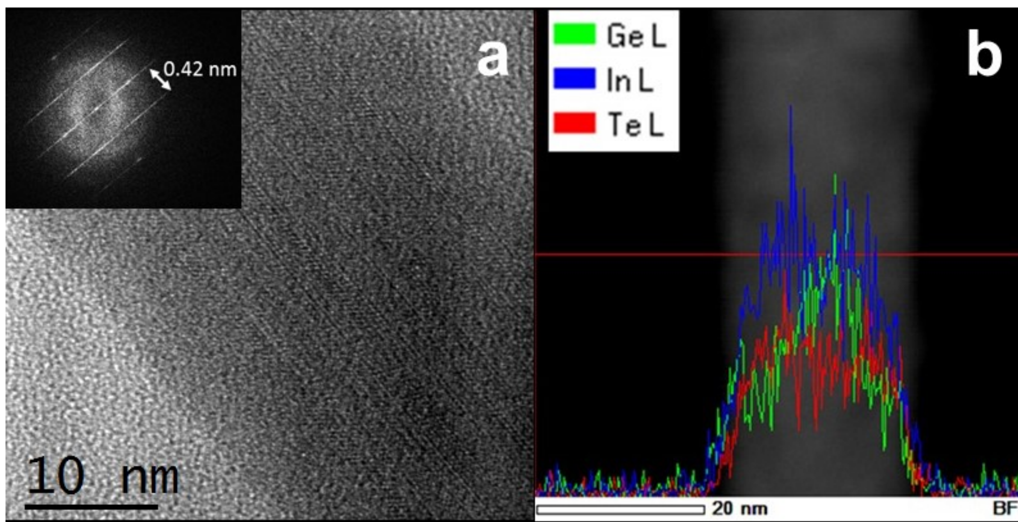


Figure 3-24: Ge-doped In_2Te_3 NW (a) HRTEM image and its FFT, (b) EDX longitudinal profile.

Figure 24 (a) displays a HRTEM image of one NW belong to this second typology and its FFT (inset). As it can be seen from the reported TEM image, these NWs exhibit a relatively high atomic disorder, hampering a conclusive phase identification by TEM characterization. In fact, the stripes in the FFT pattern indicates the lack of order along one of the two investigated directions. However, the measured spacing between the lattices planes along the direction of growth is equal to 0.42 nm, as indicated in the inset of Figure 24 (a). This value is consistent with the d_{200} interplanar spacing of the tetragonal phase of the InTe [74]. NWs with compositions $Ge_xIn_{1-x}Te_1$ with average x = 0.2 have been observed. Moreover, EDX linescan analysis performed along the longitudinal profile of this type of NWs (Figure 24 (b)) showed that the three elements form a ternary Ge-In-Te alloy, thus excluding the presence of a core/shell structure. Therefore, these NWs could be identified as Ge-doped InTe structures.

It is worth noting that neither of the $InGeTe_2$ nor In_2GeTe_3 stable ternary phases described in the phase diagrams reported in Ref. [42], were observed in the NWs for the

presently used growth conditions. It is worth noting here that alloys of the In-Ge-Te system are being investigated for their potential applications in phase change memory (PCM) devices with improved thermal stability. However, there are no reports on the bottom-up synthesis of In-Ge-Te NWs. Despite the absence of NWs with the composition and phase of the high melting temperature alloys of the In-Ge-Te system, Ge-doped InTe NWs such as those presently obtained might represent an interesting alloy for PCM application.

Chapter 4 : Implementation

This Chapter focuses on the NW-based PCM cells implementation and their preliminary electrical characterization, carried out in order to find suitable devices on which perform the functional analysis of the phase-change properties of the designed memory cells. In particular, two terminal devices formed by $In_3Sb_1Te_2$, In-doped Sb and In-Ge-Te NWs were investigated. The first part of the Chapter is dedicated to the devices fabricated using the FIB induced deposition technique, while the second part concerning devices manufactured using EBL approach.

4.1 Device microfabricated by focused induced deposition

Table I summarizes the different sets of samples manufactured by FIB technique.

Name	**Au catalyst size**	**NWs type**	**Metallization**
F8	20 nm	GeTe	Pt

#626	10 nm	$In_3Sb_1Te_2$	Pt
#632	10 nm	$In_3Sb_1Te_2$	Pt
#680	20 nm	In-doped Sb	Pt

Table 4-1: List of samples with harvested NWs electrically characterized after FIB electrodes deposition

This work focused on the study of In-based phase-change NWs. The GeTe NWs were used initially to optimize the contacting approach.

4.1.2 Nanowires harvesting

The NWs harvesting is carried out by bringing the surface of a receiving substrate in contact with the surface of a substrate with the NW forest and rubbing them together. The receiving substrate presents pre-patterned metal structures by optical lithography (Figure 1). These structures, which provide large area (~100x100 μm^2) pads for electrical testing using probe stations, will be subsequently contacted to the harvested NWs using FIB Pt deposited tracks. Figure 1 shows examples of different patterned substrates. The harvested NWs are randomly dispersed on the surface, and only those located between two pads are suitable for contacting. The pads separation will determine the length of Pt track and therefore the overall resistance of the structure.

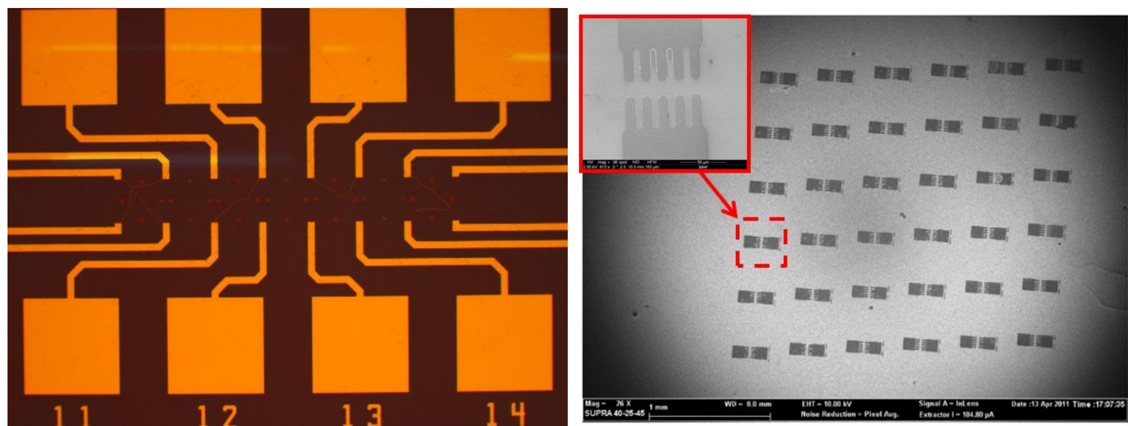


Figure 4-1: Pre-defined metal patterns on SiO_2/Si substrates by optical lithography.

4.1.3 Devices microfabrication

The NW contacting was achieved by FIB deposition of Pt between the pre-existing metal pattern and the NW. A dual beam FIB system (descripted in Chapter 2) was used to locate and contact suitable NWs using a combination of both electron and ion beam (Ga ions) Pt

deposition. Contacting was carried out using a standard Pt precursor ($C_9H_{16}Pt$), with deposition times of the order of 1–5 minutes. Initial contacting (first 50 nm) to a NW was made using a low energy (5kV) electron beam with a relatively low beam current (< 5.5 nA). Following this initial pass, the electron beam current was increased to 5.5nA for the remaining 100–150 nm of Pt deposition. This initial Pt contact was to ensure that the NW did not move during further FIB processing. It also served to protect the NW against ion beam damage during the final contacting with the FIB. Final contact to the pre-defined metal pads was made using the ion beam. Traces were defined using the FIB software, taking account of any obstacles (dirt) on the surface. Pt tracks with heights of 150 nm to 1 μm and widths of 200 nm to 2 μm were experimented with. Ion beam depositions were carried out at 30 kV, using currents ranging from 9.7 pA to 2.8 nA.

The optimization of the Pt tracks involved deposition of Pt bridges between two existing metal pads and measuring the resistance as a function of deposition conditions (Figure 2). The E-beam deposition of Pt is used for low energy deposition that will not affect the underlying surface while ion beam assisted deposition is more effective at producing Pt tracks but could cause more damage to the substrate and the NW.

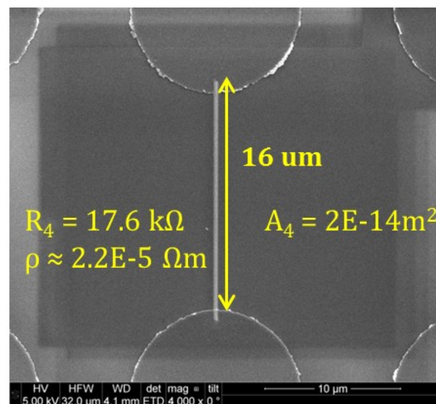


Figure 4-2: SEM image showing an example of Pt bridge structure between two large metal pads.

Several recipes were tested and are summarized in Table II. The E-beam only process results in very high resistivity values, which improve when the E-beam current is increased. The resistivity is reduced dramatically when the E-beam is combined with the ion beam deposition.

The best resistivity achieved for the deposited Pt tracks is still two orders of magnitude higher that the bulk resistivity of pure Pt, which is 1.06 x 10^{-9} Ωcm. The value achieved (2.2 x 10^{-7} Ωcm) translates into a resistance value of 17 kΩ for a 16 μm long track. It is very important to quantify the contribution of the Pt tracks to the overall resistance when a NW is included. This contribution should be minimized in order to minimize the voltage drop across the Pt tracks. However, as we will see in the electrical characterization section, aspects other than the resistance of the metal tracks must be considered.

Site #	E-beam Field (kV)	E-beam Current (nA)	Ion beam Field (kV)	Ion beam Current (nA)	Width (nm)	Height (nm)	Time (s)	Resistivity (Ωcm)
1	5	1.4	-	-	100	50	50	0.04
2	5	1.4	-	-	200	50	89	0.04
3	5	5.5	-	-	500	416	460	$5x10^{-4}$
4	5	1.4	30	0.028	200	100	89+72	$5.4x10^{-7}$
5	5	5.5	30	0.028	200	100	5+14	$2.2x10^{-7}$

Table 4-2: FIB Pt deposition conditions and resulting resistivity. Note the significant difference in deposition time between site 4 and 5 is due to the shorter gap for site 5 (16µm) as compared to site 4 (90µm).

In order to contact the NWs, the pre-patterned sample surface with randomly harvested NWs is inspected by SEM. When a NW with the appropriate morphology and dimensions is located in suitable site (Figure 3 left and center) then Pt tracks are deposited by FIB to contact it to the pads (Figure 3 right).

The example presented in figure 3 illustrates this approach, the GeTe NW properties are not the focus of this study but it helped developing the NW contacting method for the $In_3Sb_1Te_2$, In-doped Sb and In-Ge-Te NWs. The GeTe d.c. electrical characteristics were investigated (Figure 4). The overall measured resistance was ~50 kΩ, assuming the deposited Pt resistivity to be the same as previously extracted, this result shows that the GeTe NW resistance accounts for approximately half of the overall resistance.

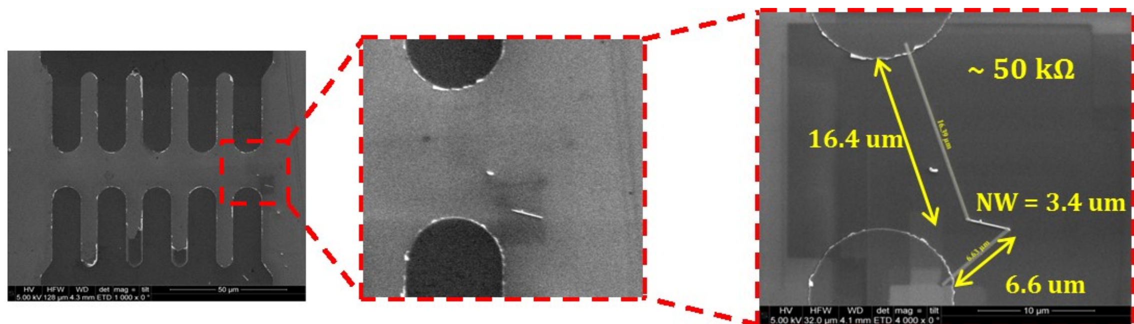


Figure 4-3: SEM images showing a GeTe NW between two metal pads before Pt FIB contacting (left and center) after Pt FIB contacting (right).

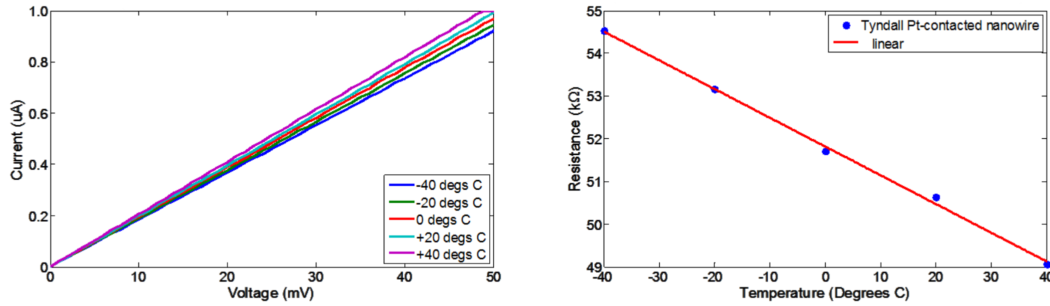


Figure 4-4: GeTe NW Current Voltage characteristics at different temperatures (right). The resistance as function of temperature is showing a negative temperature coefficient of resistance consistent with a non-metallic behavior.

4.1.4 Voltage pulsing

Once the NWs electrically contacted to the external probing pads and their d.c. properties assessed, the successful NW candidates are then subjected to voltage pulses in order to evaluate their phase-change behavior.

The characterization procedure consists of successive programming pulses with increasing voltage amplitude, each pulse followed by a d.c. measurement of the NW resistance using a very small voltage range to prevent the d.c. measurement from inducing change in the NW properties. This procedure enables the SET and RESET resistances to be extracted, as well as the V_{th} and the current required for the SET-to-RESET transition.

The approach adopted in this study is not fully automated, here the programming and measurement are carried out manually. The samples studied present small numbers of suitable NW candidates as opposed to fully processed wafers with large numbers of identical PCM cells which allow the full parameter space to be explored including the pulse width, the pulse rise time and fall time as well as the pulse height. The effort to develop a fully automated is not justified here in view of the number of NWs available for electrical pulsing.

Figure 5 shows a schematic of the NW voltage pulsing setup, a pulse generator (Agilent 81110A) is used to apply a voltage pulse to the NW. The instrument can deliver +/-10V, the pulse current is dependent on the load resistance which is comprised of the NW resistance and Pt track resistance. A separate source measure unit is used to monitor the resistance after every voltage pulse. The pads structures are probed alternatively using two pairs of probes: one pair to apply the pulse and the other pair to measure the resistance (figure 6 right).

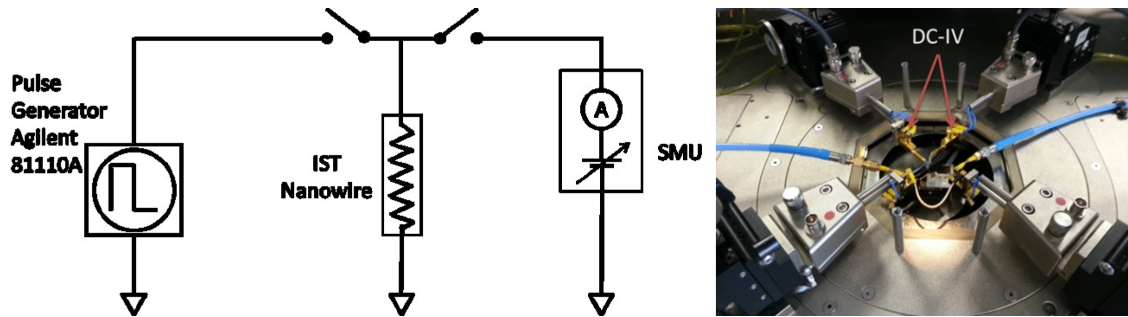


Figure 4-5: Schematic of the NW pulsing setup (left). Picture (right) showing the probe station used for pulsing NWs. One pair of probes is used for pulsing and the other for measuring the resistance after the pulse.

4.1.5 Devices electrical characterization

4.1.5.a $In_3Sb_1Te_2$ NW-based devices

Several $In_3Sb_1Te_2$ NWs of sample #626 were contacted (Figure 6). The recipe developed for contacting the GeTe NWs was applied to the #626 NWs. All contacted NWs exhibited open circuit except one, characterized in d.c. (Figure 7). The current-voltage characteristic of this $In_3Sb_1Te_2$ NW-based device is perfectly ohmic and its total resistance (including electrodes and contact resistances) is about 460 kΩ. The NW is approximately 1 µm long and has a diameter of 80 nm, the extracted resistivity is 200 mΩ cm. This resistivity value is much higher (~ three order of magnitude) than published data on crystalline $In_3Sb_1Te_2$ film [75]. However, the contribution of electrodes and contact resistance to the measured resistance may reasonably explain this difference.

Sample #632 presented several suitable $In_3Sb_1Te_2$ NWs for contacting (Figure 8). A total of four yielded ohmic characteristics. A four point contacting configuration (Figure 9 right) was explored on one of the sites. Using this configuration allows resistance of the Pt tracks to be excluded from the measurement [76]. The I-V of site 11-1 in Figure 9 is obtained using the four Pt track method. Considering the NWs geometry and resistance, the resistivity was found around 20 mΩ cm. Also in this case the contact resistance affected the resistivity calculation, explaining the difference with $In_3Sb_1Te_2$ resistivity reported in Ref. [75].

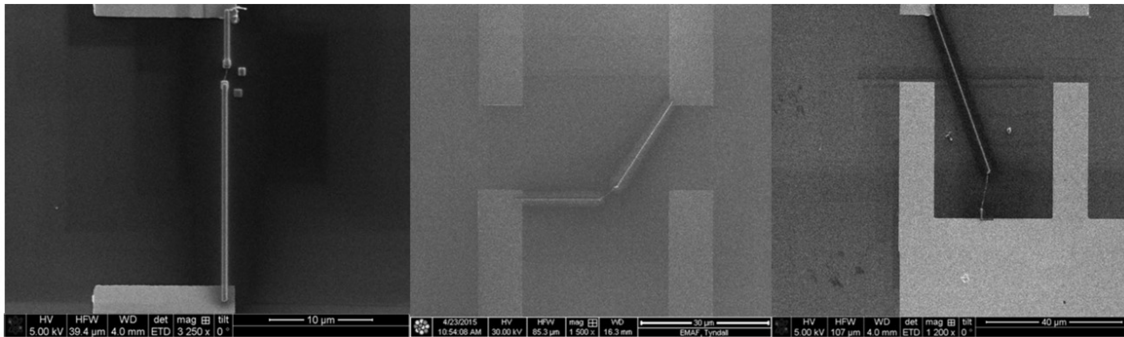


Figure 4-6: Sample #626 examples of FIB contacted NWs.

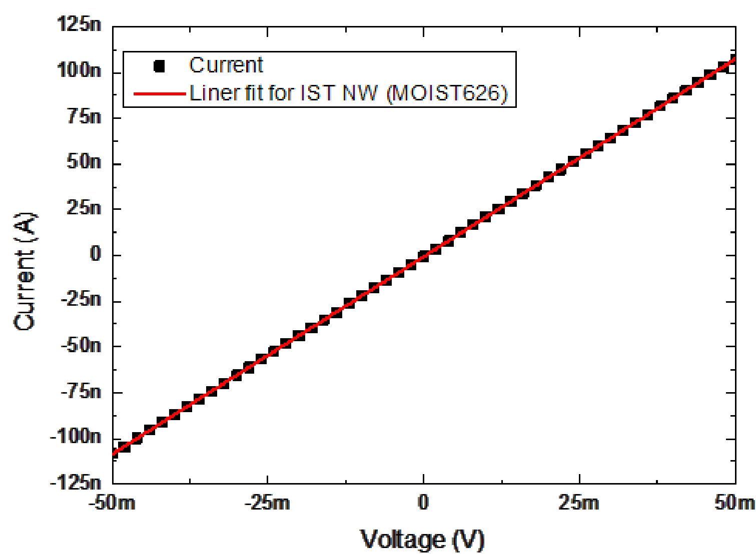


Figure 4-7: $In_3Sb_1Te_2$ NW-based device I-V characteristic. The total resistance is 460 kΩ.

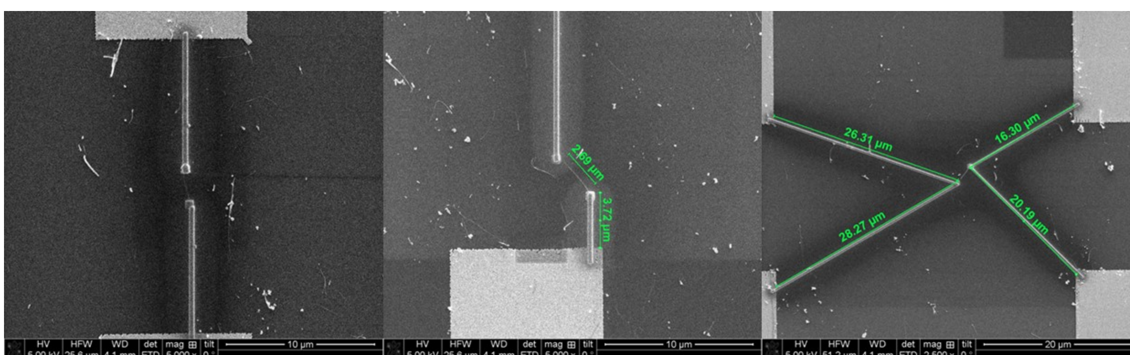


Figure 4-8: Sample #632. Examples of FIB contacted $In_3Sb_1Te_2$ NWs. Four point contact configuration (right) was also explored.

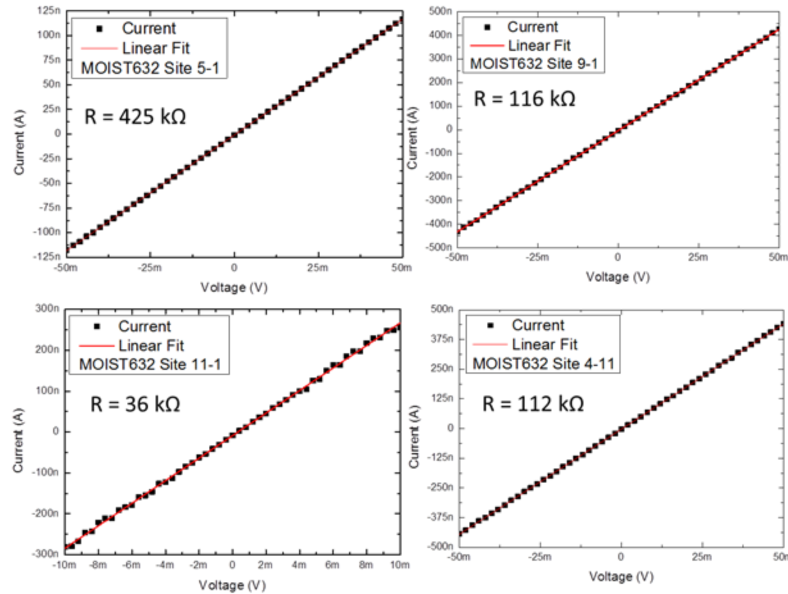


Figure 4-9: Sample #632. $In_3Sb_1Te_2$ NW-based device I-V characteristic of four different test structures.

Two devices (sites 5-1 and 9-1) were selected for pulsing. The devices d.c. characteristics were re-measured prior to pulsing. Two weeks after the initial d.c. measurement the resistance of both devices doubled from 425 kΩ up to 1.18 MΩ for site 5-1 and from 116 kΩ to 205 kΩ for site 9-1. The oxidation of the NWs could explain this resistance increase, however this is an unlikely possibility considering the time elapsed between the d.c. measurements and the much longer time between the NW growth and harvesting and the first resistance measurement. Figure 10 shows the device resistance as a function of pulse voltage. The harvested NWs are expected to be in the crystalline phase, as described in Chapter 3. Therefore, short pulses with fast rise and fall time should be applied to amorphize (RESET) the NW. Constant width (50ns) pulses are applied across the NW with the same rise time and fall time of 2ns. The device resistance was monitored after every pulse and the pulse voltage incremented.

The resistance is stable up to approximately 6 V, at higher voltage values the resistance reduces from ~1 MΩ to ~500 kΩ. The origin for this resistance decrease is unclear and the NW did not show the expected resistance increase associated with the switch to the amorphous state. Much longer pulses (1µs) were subsequently applied to this NW in an attempt to crystallize it (in case it was in the unlikely amorphous phase). The rise and fall time used were 100ns. The resistance showed a further initial decrease and then sharply increased after a 9V amplitude pulse.
The other NW (9-1) on this sample was subjected to 100 ns pulses, the results (not shown) were very similar to the previously pulsed NW, an initial resistance decrease was observed followed by a sharp resistance increase around 8V. Note, the current levels measured after the sharp resistance increase are more consistent with an open circuit than high resistance state due to a phase change from crystalline to amorphous.

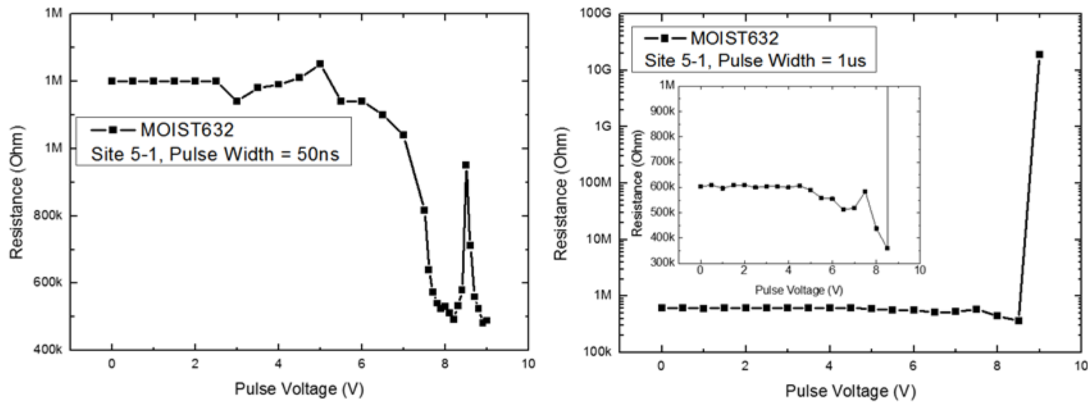


Figure 4-10: NW resistance as a function of voltage pulse height for sample #632 site 5-1. The RESET pulse width was 50ns (left), the pulse width was increase to 1µs (right) in an attempt to induce phase change in the NW.

Upon thorough inspection using high resolution SEM (Figure 12) both NWs present a defect that could explain this open circuit behavior.

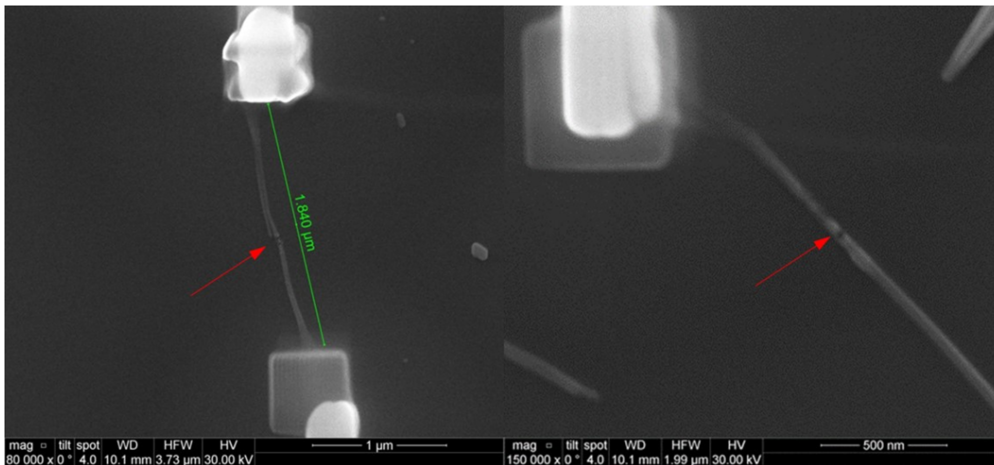


Figure 4-11: High resolution SEM images of NW of 5-1 (left) and 9-1 (right) site, showing possible NW failure after pulsing.

Several possible reasons can be speculated for the absence of phase change in these NW-based devices:

- When the short pulses (50 ns) are applied, pulse amplitude required to induce the phase change is higher than 10 V (instrument maximum voltage).

- As the pulse width is increased (1µs), possible hot spots along the length of the NW could result in material being locally vaporized (Figure 11). A possible solution to this issue is to cap the NWs with oxide.

- Another possible issue preventing the phase switching from occurring could be related to the not sharply defined Pt tracks deposited by FIB. As the ions and electrons are scattered on the substrate they induce Pt deposition around the Pt metal track. Figure 12 (left) shows a 'halo' around the Pt tracks. This could create a current path parallel to the NW and hence shorting it. A modified contacting method will be developed to prevent this issue.

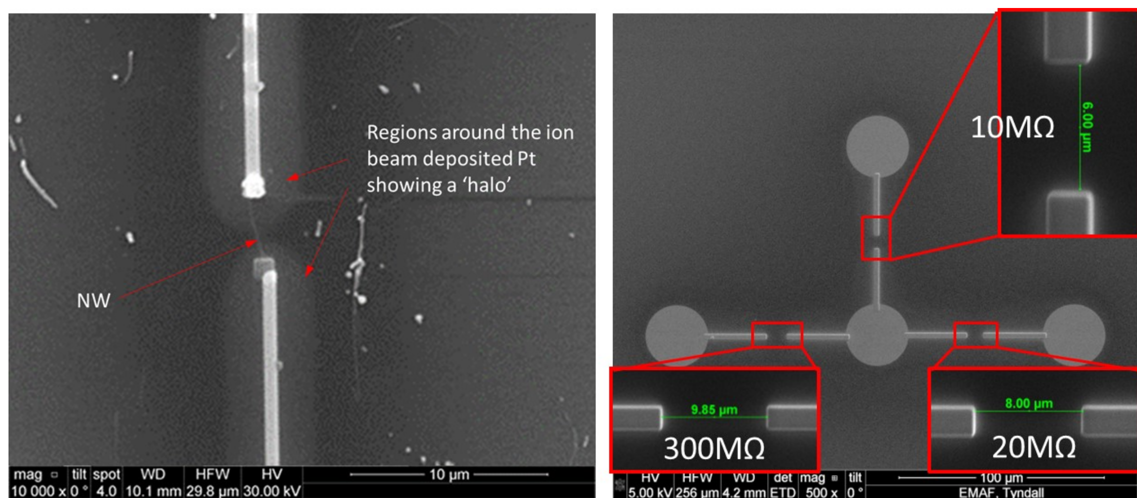


Figure 4-12: SEM image of a contacted NW illustrating the 'halo' effect (left). Three-armed structure with increasing gap length showing measurable resistance values for gaps up to 10µm.

4.1.5.b In-doped Sb NW-based devices

The contacting and characterization results obtained on sample #632 led to devise an alternative approach to contacting the next set of samples (#680). First, structures similar to Figure 12 (right) were used as pads and contacts for the NWs in order to avoid the need for predefined metal patterns prior to NWs transfering, this presents the advantage that all NWs can be selected for electrical testing not only those ideally located between predefined pads. The resistance values measured for gaps (6µm, 8µm and 10µm) between the drawn Pt tracks of the structure in Figure 12 (right) confirm the suspected shorting due to the 'halo' effect discussed in the previous section. The gap between the ion beam deposited Pt tracks must be at least 12µm long. The second modification concerns the region near the NW, for the previous samples, E-beam deposited Pt squares were applied on both ends of the NW and then covered by the ion beam deposited Pt tracks. In this modified approach, the E-beam sections either side of the NW

were stretched further away from the NW to meet the ion beam sections (Figure 13), this presents two advantages, the NW is less subjected to the Ga ion implantation and the shorting due the 'halo' effect seen in figure 12 is reduced.

In addition, once contacted the NWs were capped with TEOS in order to encapsulate the NW and prevent possible evaporation of material during the pulsing. The NW were tested in d.c. pre and post TEOS to confirm that this process doesn't significantly alter the NW properties. The TEOS capping is performed using an electron beam at 5 kV and with a beam current of 3.3 nA. For this study the TEOS capping was performed using a FEI Quanta 3D 300i FIB system available at the Tyndall Institute of Cork. Both the nanowire and any electron beam deposited Pt were capped using TEOS. This typically meant that an area of 12 μm by 2 μm was covered (40–60 nm in thickness) with TEOS. This was a much slower process so deposition times were or the order of 13–16 minutes. During this time, minor corrections to beam alignment had to be made. This arose due to charging of the SiO_2 layer on the substrate; which was more apparent over the course of the 15 minutes.

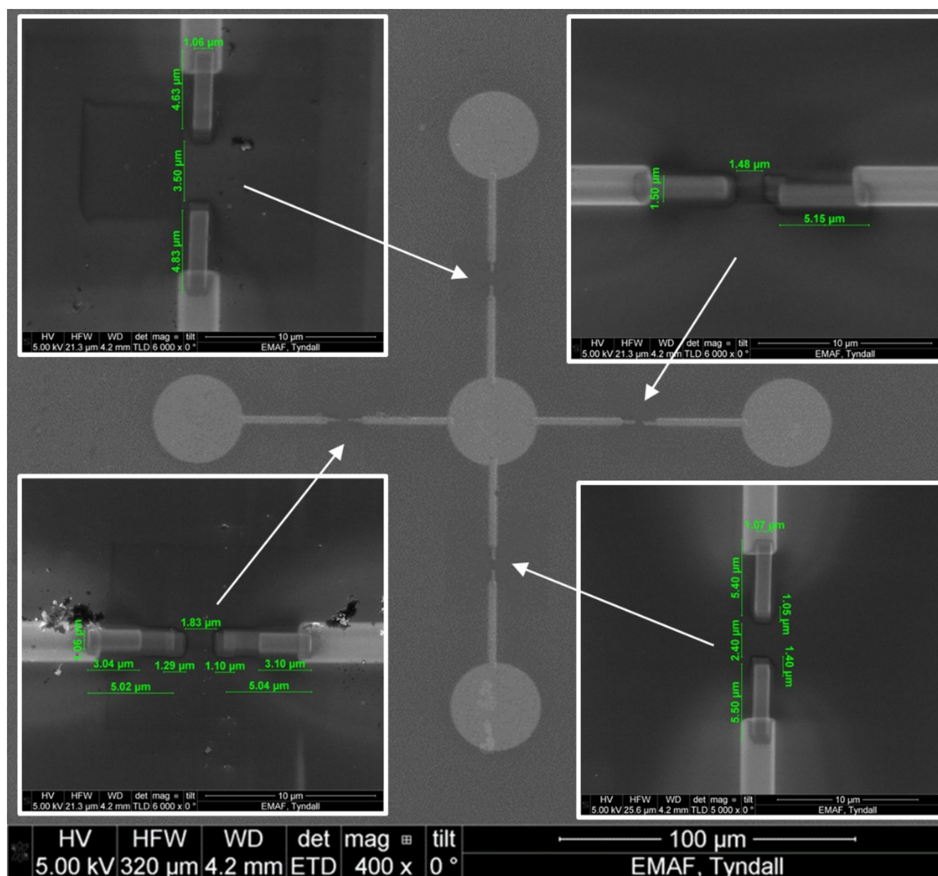


Figure 4-13: SEM image of a four-armed cross structure formed using ion beam deposited Pt. The zoomed in insets show the E-beam extensions with different separation.

Prior contacting NWs using this methodology, the cross structures were used to check the background current leakage and the resistance of Pt tracks. Figure 13 shows a Pt cross structure processed using ion beam deposition. Each one of the cross' four arms presented initially a 12µm long gap which was confirmed to be open (background current <50fA at 2V). Then E-beam extensions were attached to ion beam Pt tracks as can be seen in the zoomed in images of figure 13. Each arm presented a different Pt separation (1.48µm, 1.83µm 2.4 µm and 3.5 µm) and the resulting current for all four separations was consistently below 200 fA at 2V which is equivalent to 10 TΩ.

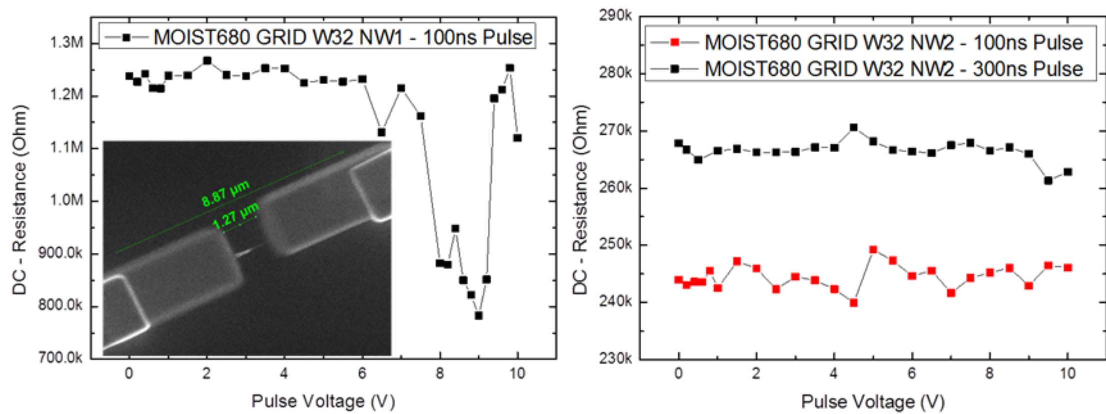


Figure 4-14: Resistance vs pulse voltage measured for two In-doped Sb NW-based devices: NW1 (left) and NW2 (right). The pulse width was 100ns and the rise and fall time was 10ns. NW2 was also subjected to 300ns pulses.

Several In-doped Sb NWs of sample #680 were contacted using this method and subjected to voltage pulses in order to RESET them. Figure 14 shows the resistance as function of pulse amplitude for two devices: #680 W32-NW1 and #680 W32-NW2. One of the NWs (NW1) exhibits a resistance decrease above 6 V which is reverted at higher pulse amplitude. The other NW (NW2) showed a stable resistance across the whole pulse voltage range for two successive series of pulse widths (100ns and 300ns). A change in the resistance can be observed for NW2 between the two pulsing experiments (Figure 14 right).

Table III shows the significant resistance change with time for both NWs monitored. This variation in resistance is comparable to the increase discussed in the previous section dealing with $In_3Sb_1Te_2$ NWs of sample #632. Therefore, this resistance instability is probably not originating from changes affecting the NW properties; it is assumed that the Pt contact, more specifically the electrical properties of the E-beam deposited Pt, which is directly in contact with the NW, might be changing with time. This is confirmed by resistance measurements over time carried out on bridge structures where ion beam deposited pads and tracks where shorted with a length of E-beam deposited Pt. These structures where fabricated initially to characterize the resistivity of the E-beam deposited Pt.

Day	1	2	5	6
#680 W32-NW1	846kΩ	1.07MΩ	1.5MΩ	959kΩ (TEOS)
#680 W32-NW2		133kΩ	196kΩ	290kΩ (TEOS)

Table 4-3: Resistance values monitored at different dates for NWs 1 and 2 of sample #680. The last measurement was taken after capping the NWs with TEOS.

Following these unsuccessful voltage pulsing experiments, it has modified the pulsing setup to include a voltage amplifier. This would enable to explore whether higher voltage amplitudes (i.e. higher currents) would cause a phase change in these NWs.

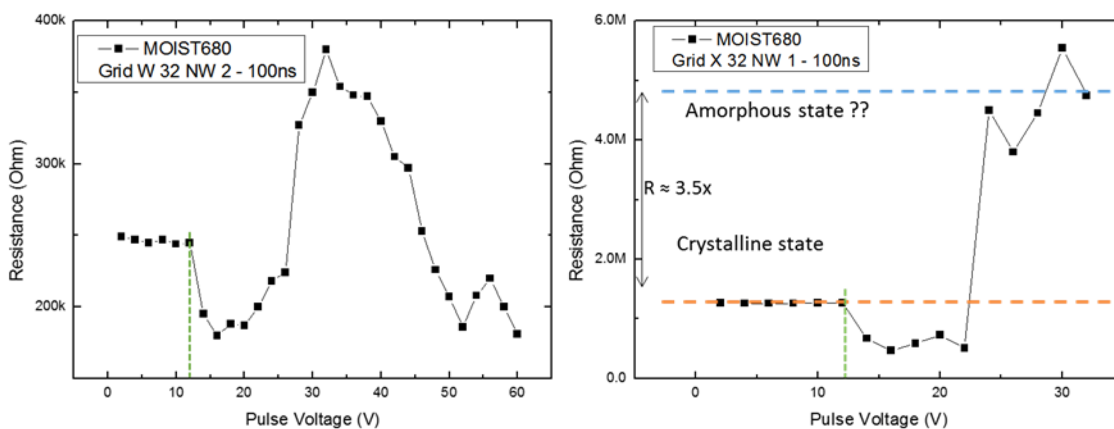


Figure 4-15: Resistance vs pulse voltage measured for two contacted In-doped Sb NWs from sample #680 using a modified setup including a 250MHz voltage amplifier. The pulse width was 100ns and the rise and fall time was 10ns.

Figure 15 shows the resistance as a function of pulse amplitude for two In-doped Sb NWs: #680 W32-NW2 was previously pulsed up to 10V (figure 14 left) and #680 X32-NW1 which hasn't been pulsed before. W32-NW2 shows the similar trend observed before but the resistance reduction occurred above 10V this time, the resistance increased again above 30V up to a value which is not orders of magnitude higher than the initial state. X32-NW1 shows a very similar behavior but the resistance increase above 20V was more substantial (x3.5), therefore the voltage amplitude wasn't incremented to much higher values for this NW.

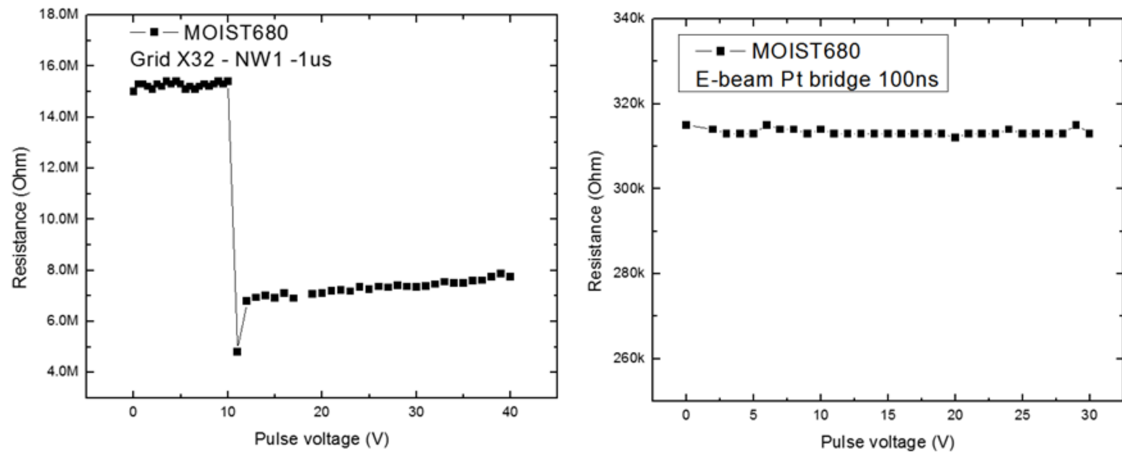


Figure 4-16: Resistance vs pulse voltage for X32-NW1 (left) which presented a possible phase switching behavior (figure 15). The pulse width was 1μs and the rise and fall time was 100ns. An E-beam Pt bridge was also subjected to 100ns voltage pulses to verify the resistance change not due to a change in the Pt tracks.

Before applying the SET pulses (1μs pulse width and 100ns rise and fall times) to X32-NW1 the d.c. resistance was measured again and was found much higher (~20 MΩ) than ~5 MΩ measured at the end of the RESET experiments (figure 15 right). The origin of this resistance drift with time could also be attributed to the issue with the E-beam Pt contacts discussed previously. The SET experiments were nevertheless carried out (figure 16 left), the resistance was 15 MΩ for voltage values below 10 V, at 11 V a sharp resistance drop occurred back to approximately the level at the end of the reset experiment of figure 15. This change in resistance is significant but it is unclear if it is related to a change in the crystalline phase of the NW. An E-beam Pt bridge was also pulsed (figure 16 right) showing no significant change upon pulse amplitude.

Ahn et al. used FIB deposited Pt to contact $In_3Sb_1Te_2$ NWs and very similar pulse conditions to RESET and SET these [43]. The geometry of the NWs reported in Ref. [43] is comparable to the NWs of this work, however their resistance much higher than the current NWs. The reset voltage was 9.6 V and the set voltage 1.6 V.

4.1.6 Summary

In this section, it has reported the results of the electrical characterization performed on $In_3Sb_1Te_2$ and In-doped Sb NWs contacted by FIB deposited Pt electrodes. Extensive effort was undertaken to optimize the contacting methodology. The FIB contacting recipe yielding the lowest Pt tracks resistance was found to cause shorting of the NWs. The contacting approach was then modified in order to reduce the shorting and limit the damage caused by ion

implantation into the underlying oxide and the NW. E-beam only deposited Pt sections were used to bridge between the NWs and the ion beam deposited Pt regions. While this solution eliminated the shorting effect, the E-beam deposited Pt material was found to present some resistance fluctuation with time. However, this material was found not to be affected by the applied pulses used to switch the NWs.

Most devices microfabricated by focused ion/electron beam induced Pt deposition showed an initial resistance reduction during the RESET experiments which were meant to amorphize the NWs and therefore increase their resistivity by orders of magnitude. This initial reduction could be due to the presence of an oxide at the NW/Pt interface, which breaks down at a certain field hence reducing the overall resistance of the structures. For some devices the required voltage to induce a significant change in the electrical properties was above 20 V and the magnitude of this resistivity increase was not indicative of a phase change transition which is expected to vary by orders of magnitude. This could be resulting from a modification of the NW/Pt interface that could dominate the overall resistance of the device. If the fall time of the RESET pulses is not fast enough to avoid a re-crystallization of the NWs, this could provide another explanation for the failure of the phase change memory switching.

EBL techniques could have been beneficial in order to overcome the described implementation issues, since they do not require ion beam exposure to break the metal precursor and the purity of the metals deposited in an EBL process is higher than the FIB deposited Pt which contains carbon. For these reasons, such alternative approach was employed to manufacturing other PCM cells, as will be described in the next part of the manuscript.

4.2 Device manufactured by EBL technique

This section concerning the two-terminal NW-based PCM device implemented using EBL and metals evaporation, and their preliminary electrical characterization.

4.2.1 Implementation

Macroscopic back-gate contacts and top contacts have been patterned on highly doped Si substrates with 100 nm thermal oxide on top by multistep optical lithography and wet etching processes, followed by sputter deposition of a Ti/Au (10 nm/100 nm) thin film and lift-off. An image of the macro pads array is reported in Figure 17. Nineteen fields containing six top contacts and three back-gate contacts (indicated by blue rectangles and red circles respectively in Figure 17) are the constituents of each fabricated array of pads. For the devices fabrication, NWs were removed from the growth substrate and dry-transferred onto this patterned substrate.

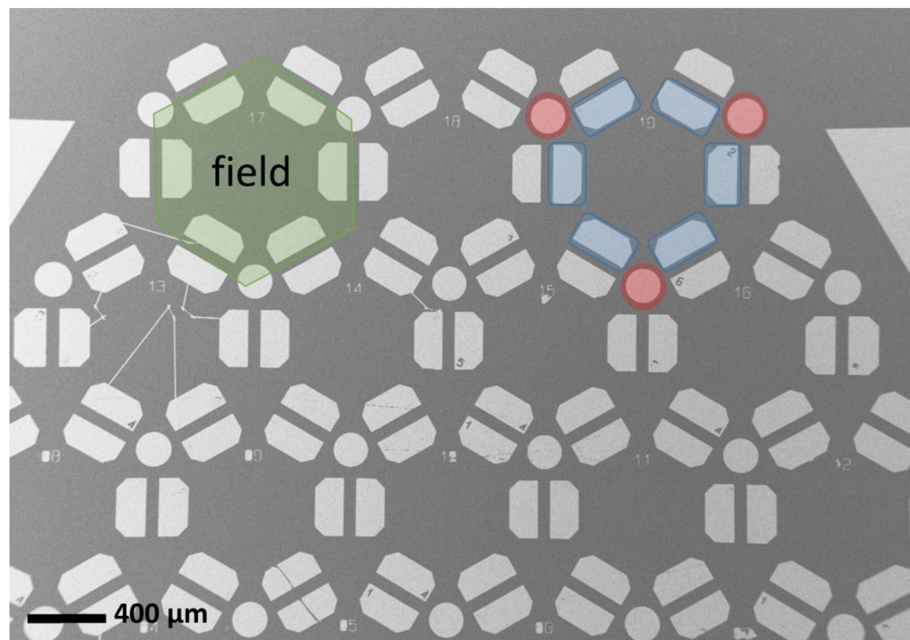


Figure 4-17: SEM image of a macro pads array, fabricated onto an insulating substrate, prepared for the NWs transferring.

Then suitable NWs for the device implementation were identified on the sample surface and their position respect to the pads array was registered and saved by SEM imaging. The selected NWs had to show the following features:

- isolated from other nanowires (without overlapping)
- length greater than 1.5 µm

- diameter of less than 40 nm
- minimum taper along the length
- regular surface morphology
- straight along the substrate (without bending)

The first two characteristics listed were mandatory for a successfully device implementation while others requirements were related to the scope of this work, the study of nano-sized PCM for low power application.

EBL technique makes possible the fabrication of high-resolution metallic patterns, easy reproducible on a large scale, and their alignment with to the structures on the sample's surface with a nanometric precision. The goal was to employ EBL to design and produce ad hoc metal connections between each pre-selected NW and a couple of top electrodes of the pre-patterned pads array. In this work have been realized metal connections featuring:

1. nano-contacts on the NW sides (inset Figure 18)
2. gap between the nano-contacs (L_{gap}) ranging from 0.5 μm and 2 μm
3. metal tracks connecting nano-contacts and macro-pads (Figure 18)
4. either Ti/Au and Ni/Au

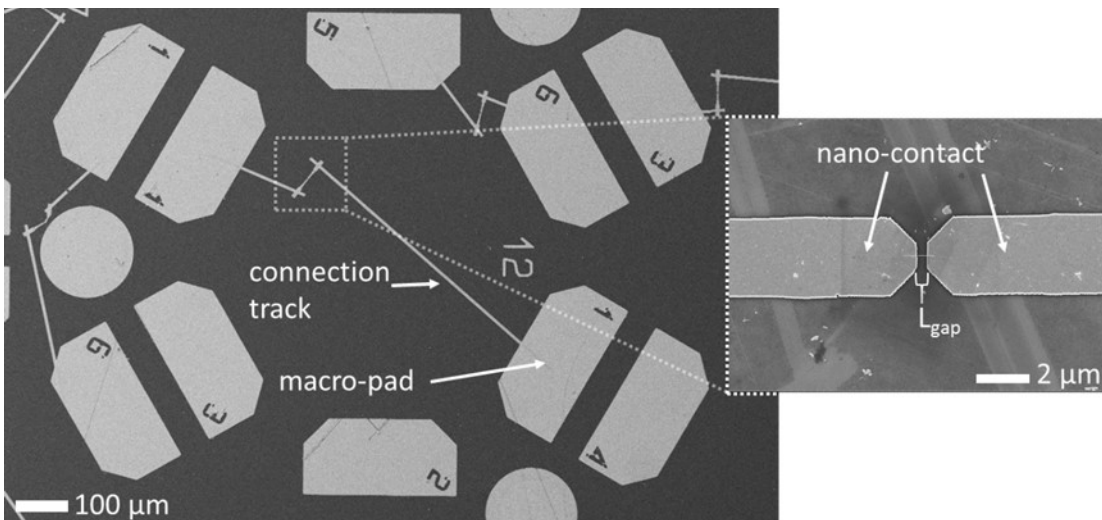


Figure 4-18: SEM image of the metal connections fabricated by EBL technique.

The first step of the devices manufacturing is to draw the mask of the metal connections and align it with the pre-patterned macro-pads array and the pre-selected NWs on the sample's surface. Then, AR-P 679.04 positive E-beam resist, formed by PMMA polymer dissolved in ethyl lactate (molecular mass of 950K and solids content of 4%) is spin-coated on the samples at 4000 rounds per minute (rpm) for 35 seconds. This operation produces a 270 nm thick resist layer on the surface, which is subsequently baked on a hotplate at 170 °C for 15 minutes, in

order to evaporate all solvents and improve the lithographic yield. After, the sample is loaded into the E-line and the designed mask is again aligned with the structures on the surface before the E-beam exposure of the resist. The parameters used for the exposure are:

- 10 kV accelerating voltage
- 30 µm beam aperture
- Working distance 7 mm
- 200 pA beam current
- Dose 0.110 pA/s

The exposed resist development is done by stirring the substrate in the AR 600-56 solution (main content MIBK) for 35 seconds. Later, substrate have to be rinsed immediately after development for 35 seconds with AR 600-60 stopper and are subsequently dried by nitrogen. Finally, thermal evaporation of the metals (Ti/Au: 5/90 nm or Ni/Au: 20/100 nm) and lift-off by stirring in hot acetone (40 °C) are performed. Notably, the described procedure allow fabricating of about fifth devices for each macro-pads array substrate in three days of work.

4.2.2 Electrical conductivity characterization

Table IV summarizes the different sets of samples electrically investigated after NW-based devices fabrication by EBL technique.

Name	**Au catalyst size**	**NWs type**	**Metallization**
#621 A	10 nm	$In_3Sb_1Te_2$	Ni/Au
#621 B	10 nm	$In_3Sb_1Te_2$	Ni/Au
#755	20 nm	In-doped Sb	Ni/Au
#714 A	10 nm	Ge/In_2Te_3	Ti/Au
#714 B	10 nm	Ge/In_2Te_3	Ti/Au
#714 C	20 nm	Ge-doped InTe	Ni/Au

Table 4-4: List of samples electrically characterized after NW-based devices fabrication by EBL.

In order to identify the best candidates, on which carry out a study of the phase-change memory performance (discussed in the next chapter), the electrical conductivity of each as-manufactured device have been investigated. In particular, the shape of the current–bias (I-V) characteristic and the resistance of the devices have been evaluated by two-probe measurements. In general, high contact resistance values and nonlinear I–V characteristics have been observed. This can be explained by the existence of back-to-back Schottky barriers arising from the metal–NW contacts [77]. For example, it has been proven that the metal (Pt) strip series resistance accounts for over 85% of the total resistance measured in SnO_2 nanowires by 2-probe measurements and the main contribution of the measured resistance originates in the metal/NW junctions. [78]. The contact resistance between electrodes and NW can be improved by flowing a current in the NW-based devices [79]. Because of the high interfacial resistance, Joule heating locally occurs at the metal/NW joining points, improving the materials intermixing ("forming" of the electrical contact) and thus decreasing the overall resistance. This effect was successfully exploited in some of the NW-based devices investigated in this work.

Only the devices on which the "forming" process had occurred successfully have been selected for the phase-change functional study, which will be discussed in the next chapter. This choice was made because, in PCMs the SET state (logic "1") must have resistance values should not be larger than few hundreds of kΩ, to ensure a fast and reliable reading [11]. Moreover, relatively low SET state resistances could also allow to programing the memory cell by voltages in the range provided by the typical cell selectors used in PCMs [80].

4.2.2.a $In_3Sb_1Te_2$ NW-based devices

About fifty $In_3Sb_1Te_2$ NWs of samples #621 A and #621 B were contacted. The recipe developed for contacting these NWs involved the use of Ni/Au metallization. All the as-fabricated NW-based devices exhibited non-linear I-V characteristic and high resistances, with values ranging from few hundred megaohms to few gigaohms.

After the electrical "forming" process of the metal/NW contacts, obtained by performing some d.c. sweeps on the as-fabricated devices, about half of them have been shown a linear I-V curve along with a drastic decrease of their resistance, whose values ranged between 30 and 100 kΩ . Whereas, the other half of the contacted NWs did not change appreciably their I-V characteristics.

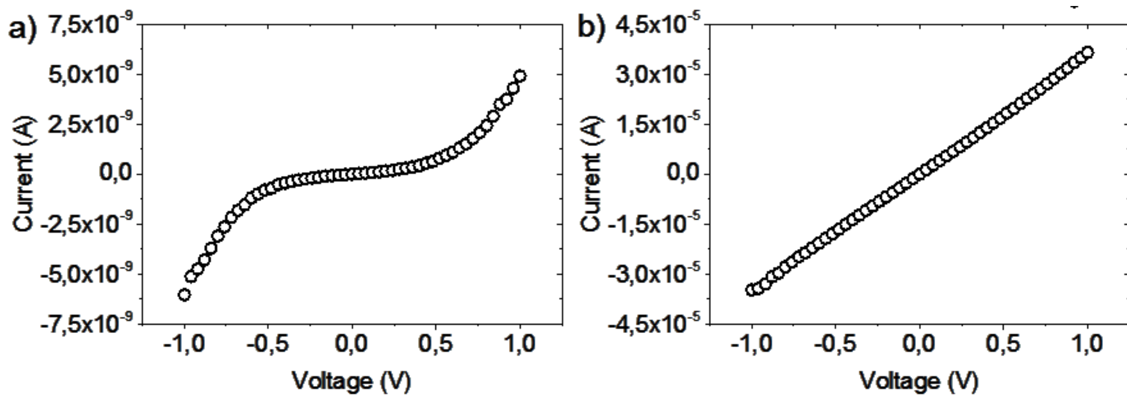


Figure 4-19: I-V curve of an $In_3Sb_1Te_2$ NW-based device before (a) and after (b) the electrical "forming" process of the metal/NW contacts.

Figure 19 (a) reports the I-V curve between -1 V and +1 V of one as-fabricated $In_3Sb_1Te_2$ NW-based device, where is visible a non-linear electrical behavior. Before the "forming" process, the device resistance, measured at 0.5 V, was 667 MΩ. After a d.c. sweep among -2 V and +2 V, the device has changed its electrical characteristic, showing a linear trend with a resistance of 30 kΩ (Figure 19 (b)).

4.2.2.b In-doped Sb NW-based devices

Most of the In-doped Sb NW-based devices fabricated on samples #755 (using Ni/Au electrodes) showed a non-linear I-V characteristic before the "forming" procedure, even if a linear behavior was also observed for some of the as-fabricated devices. In both cases, lower overall resistance values have been measured compared with those of the as-fabricated $In_3Sb_1Te_2$ NW devices. In particular, resistances of some hundreds of kiloohms have been observed. A stably drop of the resistance was obtained for all devices of this type (along with the I-V linearization, when possible), by applying the "forming" current. After the electrical "forming", the devices' resistance was about 20 kΩ, with very small variations (few kΩ) between the different devices.

4.2.2.c In-Ge-Te NW-based devices

Regarding the devices fabricated using the Ge/In_2Te_3 core/shell NWs and the Ge-doped InTe NWs, both types exhibited non-linear I-V characteristics and very high resistances (> 1 GΩ) also after the "forming" procedure adopted for the other devices (Figure 20).

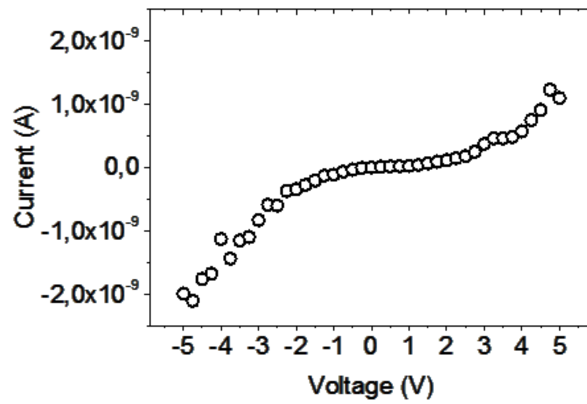


Figure 4-20: Typical I-V curve of a In-Ge-Te NW-based device after the electrical "forming" process of the metal/NW contacts.

For this reason, to improve the electrical conductivity of these In-Ge-Te NW-based devices, rapid thermal annealing (RTA) processes have also been performed in N_2/H_2 atmosphere (to avoid oxidation) from 150 °C to 400 °C, by step of 50 °C. Even the RTA processes did not change the electrical behavior of the devices.

Chapter 5 : Functional analysis

The results of the functional analysis performed on the most promising NW-based PCM devices, fabricated in this work, are reported in this chapter. In the first section, a short description of the electrical setup employed for the functional characterization of the devices is presented, along with the explanation of the advantages related to the use of the TLP technique for our scopes. Then, in the second part of the chapter, the electrical characterization of PCM devices formed by $In_3Sb_1Te_2$ chalcogenide NWs, with diameters as small as 20 nm, is reported. Finally, phase-change memory switching study of In doped Sb non-chalcogenide NW-based devices will be exposed.

5.1 Transmission line pulse technique

The phase-change properties of the $In_3Sb_1Te_2$ and In doped Sb NW-based devices were investigated by the TLP technique [65], using a HPPI ® system. In particular, the measurement set-up consisted of a 50 Ω high voltage pulse generator, a high speed digital oscilloscope, a Source Meter Unit (SMU) and a control computer. The differential voltage was measured

directly at the fabricated devices by the four-point Kelvin method. In order to measure the device resistance, direct current (d.c.) measurements in the pA ÷ mA range were performed after each pulse, using the switch configuration with the SMU. A more detailed description of this set-up is reported in the chapter 2.

It worth to notice that, contrarily to DC signals, nanosecond timescale signals require careful routing. Let us consider a typical voltage pulse of: 1 V, 100 ns width. Pulsing such short signals implies that the rising and falling edges thereof are ≈ 1/10 of the whole signal duration. As a result, pulse edges range in the 1 to 10 ns timescale. In this regime, the signal is transmitted or reflected whenever an impedance mismatch occurs. Signal reflection effects (Figure 1) :

1) diminishes the actual energy supplied to the DUT.

2) alters the shape of the pulse.

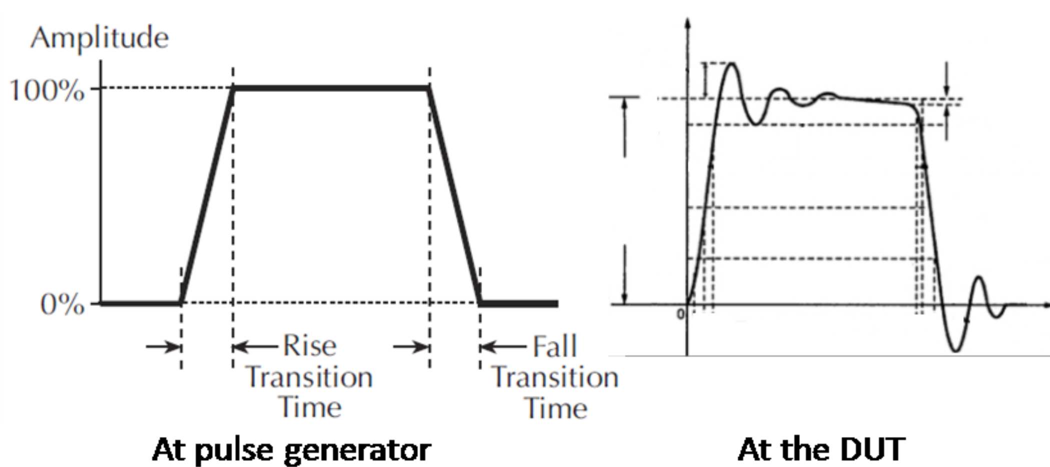


Figure 5-1:Schematic representation of the reflection effects at nanosecond timescale on the voltage pulse amplitude and shape at the DUT.

A TLP system allows to generate voltage pulses with a very fine control on their amplitude and shape at the DUT. In particular, it is possible to realize a very fast pulse falling time, which is crucial for the amorphization of phase change materials, because a rapid quenching is required to avoid recrystallization phenomena.

5.2 Low Power Phase Change Memory Switching of Ultra-Thin $In_3Sb_1Te_2$ Nanowires

In this section we report the results, published in Ref [81], on the electrical characterization of PCM devices formed by $In_3Sb_1Te_2$ chalcogenide NWs, with diameters as small as 20 nm. The NWs were self-assembled by metal organic chemical vapor deposition via the vapor-liquid-solid method, catalyzed by 10nm Au nanoparticles. Reversible and well reproducible memory switching of the NWs between low and high resistance states was demonstrated. The conduction mechanism of the high resistance state was investigated according to a trap-limited model for electrical transport in the amorphous phase. The size of the amorphized portion of the NW and the critical electric field for the transition to the low resistance state were evaluated. The $In_3Sb_1Te_2$ NW-based devices showed very low working parameters, such as RESET voltage (~3 V), current (~40 μA) and power (~130 μW). This results indicated that the studied $In_3Sb_1Te_2$ NWs are suitable candidates for the realization of ultra-scaled, high performance PCM devices.

In recent years, the interest for the development of a new class of memories, the Storage Class Memory (SCM), has greatly increased [82]. The SCM would fill the gap between ‘‘operation’’ memory (DRAM) and ‘‘storage’’ memory (Flash and/or hard disk drive). Possible SCM candidates should be based on non-volatile memory cells, much faster and with higher endurance than Flash devices, and have high density and reasonably low cost/bit [14]. Phase Change Memories (PCMs) are promising constituents for SCM, due to their fast switching, inherent scalability, high device endurance and relatively long data retention time [3]. Currently, the main limitations of PCMs are the somehow inadequate thermal stability, affecting the retention time, and the relatively high amorphization (RESET) currents. Typical technological implementations of PCM devices are generally based on a heater/chalcogenide thin film architecture and exploit alloys of the pseudo-binary line between Sb_2Te_3 and GeTe [9], such as $Ge_2Sb_2Te_5$. To overcome the current limitations of PCMs, the investigation of different phase change materials and the development of devices employing innovative nanostructures are required.

The use of phase-change NWs is a particularly appealing solution, allowing a tremendous downscaling of the cell size, and hence to reach higher memory densities. Moreover, compared to conventional PCMs, NWs have been shown to exhibit more efficient phase change transition processes and, in particular, a reduced RESET power. The self-heating approach is expected to be the most efficient for PCM applications [27] and does not require special heater-electrodes,

as the heat generation occurs directly within the phase-change material. However, it implies a risky technological implementation, due to the high aspect-ratio that is needed for the involved nanostructures. Self-assembled NWs normally present a sufficiently high aspect ratio, along with extremely small diameters, particularly suitable for the self-heating mechanism. Moreover, NWs grown by bottom-up techniques turn out to be typically defect-free structures, whereas the conventional top-down approach with multiple lithographic and etching steps generally leads to structural/chemical degradation of the phase-change materials, which is detrimental to the high scalability, low power consumption and non-volatility requirements. While the physical mechanisms of electrical resistance variations in NWs are still under debate [83]–[85], the reduction of the writing currents has been demonstrated in $Ge_2Sb_2Te_5$ and GeTe NW-based PCM cells [30], [67]. On the other hand, recrystallization studies have shown a diminution of activation energies and data retention times depending on the NW diameter [30]. One possibility to counteract this effect is given by the use of In-Sb-Te chalcogenide alloys, such as $In_3Sb_1Te_2$, which exhibit a higher crystallization temperature (>290 °C) with respect to Ge-Sb-Te alloys [37], [68], [69]. In-Sb-Te PCM cells based on thin films have been fabricated and characterized, demonstrating good resistance contrast, high endurance and multiple resistance levels [40], [41]. The phase change functioning of $In_3Sb_1Te_2$ NWs has also been reported in [43]. However, in these works much higher RESET voltage values than those employed in industrial implementations of PCMs were observed. Here we report on the low-power and low-programming voltage phase change properties of ultra-thin $In_3Sb_1Te_2$ NWs, grown by MOCVD coupled to the VLS mechanism [72].

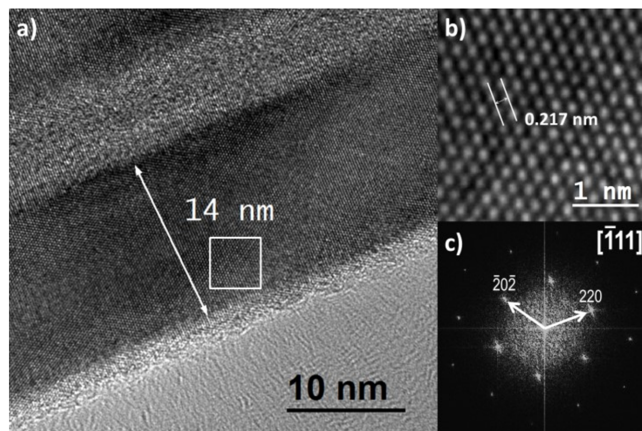


Figure 5-2: HRTEM image of a 14 nm thick $In_3Sb_1Te_2$ NW. (b) Enlargement of the white squared region showing the atomic arrangement of the rock salt phase in the [-111] projection and (c) its FFT. [81]

The growth of the $In_3Sb_1Te_2$ NWs is described in chapter 3 in detail. The NWs were self-assembled on 1 cm^2 Si(100) substrates, on which the catalyst Au nanoparticles for VLS with a diameter of 10 nm were deposited. The used metalorganic precursors were electronic

grade dimethylaminopropyldimethylindium ($C_7H_{18}InN$), antimonytrichloride ($SbCl_3$,) and bis(trimethylsilyl)telluride ($Te(SiMe_3)_2$). The optimization of the growth parameters, discussed in chapter 3, led to the synthesis of $In_3Sb_1Te_2$ NWs, with diameters down to 14 nm and lengths of a few microns.

HRTEM, performed in a field emission JEOL® 2200FS microscope, equipped with X-Ray microanalysis (EDX), showed that the NWs grow in the rock salt phase of $In_3Sb_1Te_2$. Notably, the NWs appear to be perfect crystals, as no extended defects were observed. Figure 2(a) shows a HRTEM image of a 14 nm thick $In_3Sb_1Te_2$ NW. The atomic arrangement is clearly visible in the higher magnification image of Figure 2(b). The lattice spacing of the atomic planes along the growth direction was measured to be 0.217 nm, which is compatible with the {220} planes of the $Fm\overline{3}m$ structure of the $In_3Sb_1Te_2$ [17]. This indication is further confirmed by the FFT reported in Figure 2(c): the NW is oriented along the [-111] zone axis, thus showing the six identical {220} reflections.

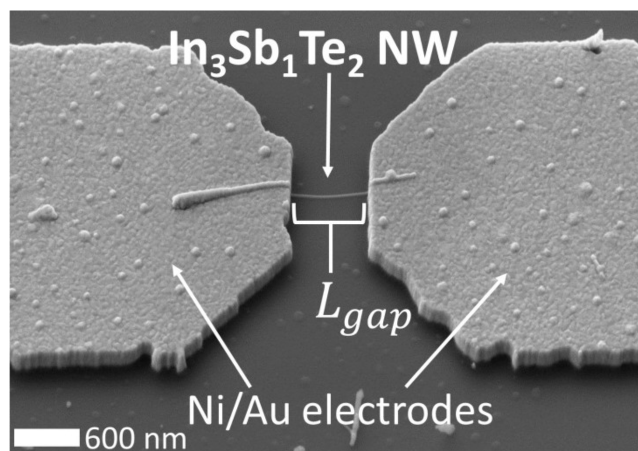


Figure 5-3: Tilted SEM image of the PCM device formed by a $In_3Sb_1Te_2$ NW, contacted by Ni/Au micro-electrodes fabricated on top of the NW by EBL. [81]

For the electrical characterization, NWs were dry-transferred onto insulating substrates with pre-patterned macro-pads and two-terminal devices were fabricated using EBL, the implementation procedures are reported in chapter 4. A thick layer of PMMA was spin-coated and baked at 180 °C, following which EBL of the connection tracks and nano-contacts, metallization (Ni/Au: 20/100 nm) and lift-off were performed (Figure 3). The electrical properties of the $In_3Sb_1Te_2$ NWs were investigated by the TLP technique, as explained in the previous paragraph. The inset in Figure 4 shows a representative RESET pulse with a voltage amplitude of 3 V, a duration of 100 ns and a falling time of 1 ns, directly measured at the device under test.

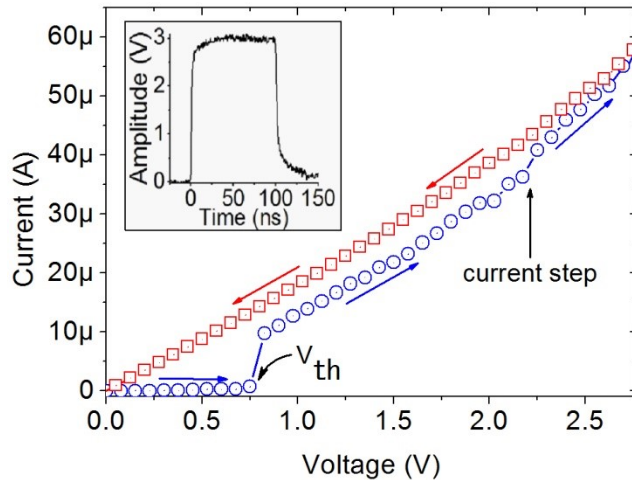


Figure 5-4: Programming curve of a 20 nm $In_3Sb_1Te_2$ NW device, composed by the I-V characteristics of the amorphous (blue circles) and crystalline (red squares) states. The threshold voltage (V_{th}) for the amorphous to crystalline transition and an additional step in the measured current at about 2.25 V are indicated. The inset shows a representative RESET pulse directly measured at the device. [81]

Figure 4 reports the electrical I-V characteristics of a device fabricated using an $In_3Sb_1Te_2$ NW with a diameter of 20 nm and a separation between the Ni/Au contacts (L_{gap}) of 700 nm. Below the threshold voltage (V_{th}), two different physical states of the device are present: amorphous (high resistance, RESET) and crystalline (low resistance, SET). Starting from the NW in a SET state (~ 50 kΩ), the RESET state (~12 MΩ) was enforced by applying a voltage pulse of 100 ns and amplitude of 3 V (corresponding to a current of 60 μA). The device was then brought to a low resistance state (~ 85 kΩ) during the I-V, once a V_{th} of ~ 780 mV was reached. The initial SET state (~ 50 kΩ) was restored increasing the voltage up to 2.75 V. This SET state was stable and the device resistance remained low as the voltage was swept back to zero. It is important to notice that the SET resistances measured here are about two orders of magnitude smaller than those previously published for In-Sb-Te NWs [43] and comparable to what reported for other phase change NWs, like $Ge_2Sb_2Te_5$ [30] and GeTe [67]. The remarkably lower resistance values with respect to the previously reported ones [43] might be related to a lower defect density of the studied NWs, or to a lower contribution of the metal/NW contact resistance. It should be noticed that in PCM devices the SET resistances should not be larger than hundreds of kΩ, to ensure a fast and reliable reading [11]. Low resistance values could also explain the lower voltage required for RESET (~ 3 V) compared to the ~ 9.4 V value reported in [43]. This is another crucial aspect, due to the limitations of the voltage range provided by the cell selectors used in PCMs [80]. Our RESET and threshold voltages are also considerably smaller than those reported for In-Sb-Te-based planar cells [40], [41].

The conduction mechanism of the high resistance state was investigated according to a trap-limited model for electrical transport in the amorphous phase. The size of the amorphized portion of the NW and the critical electric field for the transition to the low resistance state were evaluated. The transition from the high resistance amorphous state to the low resistance crystalline state, occurring at V_{th}, is expected to be controlled by the electric field present across the amorphous region. In fact, when a critical value of the field is reached, the resistance of the amorphous phase decreases. In turn, this drop in resistance allows an appreciable current to flow and causes the amorphous phase to reach a material-specific crystallization temperature, thus enabling the SET transition. We estimated the value of the critical electric field (E_{th}) by using the existing models. Since $E_{th}=V_{th}/u_a$, where u_a is the effective length of the amorphized part of the NW, the first step consists in evaluating this length. This can be done by analyzing the I-V curves of the NWs in the RESET (amorphous) state within the subthreshold range, i.e. for $V<V_{th}$. We used the model proposed in [86], for a conduction limited by the traps at a (constant) distance Δz from each other, where the current is expected to follow the equation:

$$I = 2qAN_{T,tot}\frac{\Delta z}{\tau_o}e^{-(E_C-E_F)/kT}\sinh\left(\frac{qV}{kT}\frac{\Delta z}{2u_a}\right) \quad (5.1).$$

In equation (5.1), q is the elementary charge, E_F is the Fermi level, E_C is the conduction band level, A is the cross section of the NW, $N_{T,tot}$ is the integral of the trap distribution in the gap above the Fermi level, τ_0 is the characteristic attempt-to-escape time for the trapped electron, k is the Boltzmann constant and T is the temperature. The data fitting by equation (5.1) of the measured subthreshold I-V characteristic of a NW in the RESET state is reported in Figure 5 (a). From the fit, the values of $u_a/\Delta z$ were calculated for several NWs in different RESET states. The plot of V_{th} as a function of the $u_a/\Delta z$ values is shown in Figure 5 (b). V_{th} increases linearly with u_a (Δz is constant in the model by [86]), indicating a constant value of E_{th}. From the slope of the linear fit to the data points, the value of E_{th} can be estimated, except for the value of Δz, i.e. $E_{th}\cdot\Delta z = 0.29 \pm 0.02$ V. For a value of $\Delta z = 5$ nm [86], Eth is about 60 V/µm. Such value of E_{th} is comparable to those measured for $Ge_2Sb_2Te_5$ in heater-based [87] and “line concept” [88] PCM cells and for GeTe and Sb_2Te_3 NW-based devices [67]. Figure 4(b) also suggests that only a small fraction of the NW length (a few tens of nm) is amorphized during the RESET operation. Nevertheless, the typical values of V_{th} in our devices are high enough to guarantee a sufficient wide read out window and bit stability against voltage fluctuations.

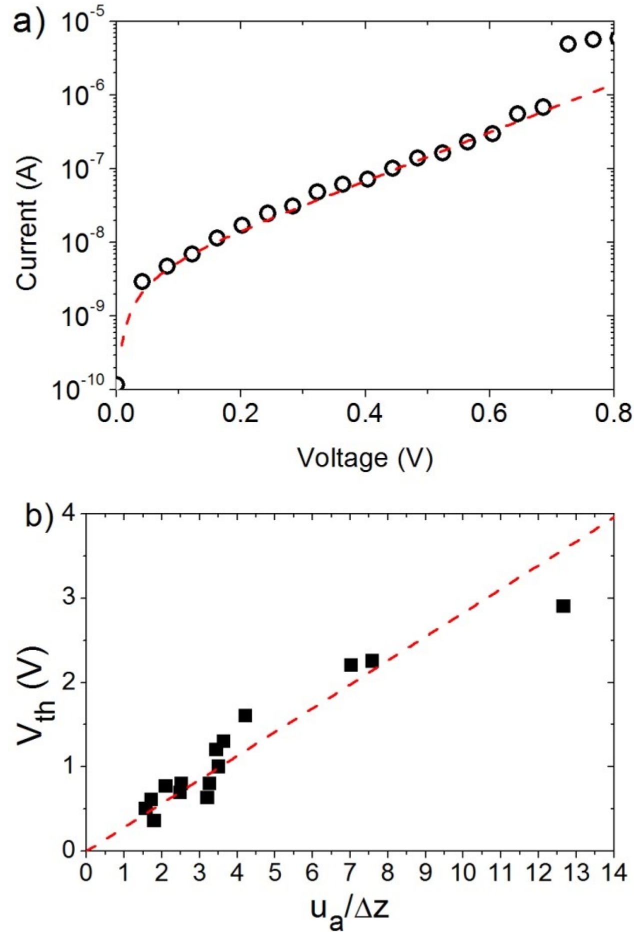


Figure 5-5: (a) Fitting by equation (1) (dashed red curve) of I-V data (black circles) for $V<V_{th}$ with V_{th}=0.69 V, measured on a NW with L_{gap}= 480 nm and diameter of 22 nm in the RESET state; the calculated value of $u_a/\Delta z$ is 2.5. (b) $u_a/\Delta z$ dependence of V_{th} (black squares) for several NWs in different RESET states. The dashed red line is the linear fit of the experimental data. [81]

Interestingly, the I-V curve in Figure 4 shows two current steps during the voltage sweep. The presence of current steps in the I-V curve of planar $In_3Sb_1Te_2$ PCM cells at voltages larger than the V_{th} has also been reported in [40] and attributed to successive structural transformations of the crystalline state. This is an appealing characteristic of the $In_3Sb_1Te_2$ alloy in the quest for the development of multilevel memory cell technology.

Reversible and well reproducible memory switching of the $In_3Sb_1Te_2$ NWs was proved for several devices. Figure 6 (a) shows a SET-RESET cycling test performed on a 22 nm NW device with L_{gap} = 480 nm. Both SET and RESET resistances were measured at 20 mV. For each cycle the amorphous state (blue circles in Figure 6 (a)) was obtained by a RESET voltage pulse of 100 ns and amplitude of 3.17 ± 0.06 V. The crystalline state (red squares in Figure 6 (a)) was obtained by a d.c. sweep from 0 to 2.5 V. The low resistance state obtained with a d.c. sweep represents the limiting case (“infinite” SET pulse duration) and gives the intrinsic SET state resistance of the device. Figure 6 (a) clearly shows two distinct memory states, with a

resistance gap of over two orders of magnitude. The cycling test proved that the memory window was well maintained up to 8 cycles, even without a passivation coating to avoid NW degradation. It worth to notice that, as observed in the work of Meister et al.[89], the RESET state resistance value may depend not only on the programming pulse characteristics (amplitude, duration, etc), but also on the history of the sample. This is due to the fact that the device resistance is also a function of the detailed crystalline and amorphous phase distribution that determines available conduction pathways. This phenomenon may explain the fluctuation of the RESET state resistance values in the cycling test shown in Fig. 6 (a).

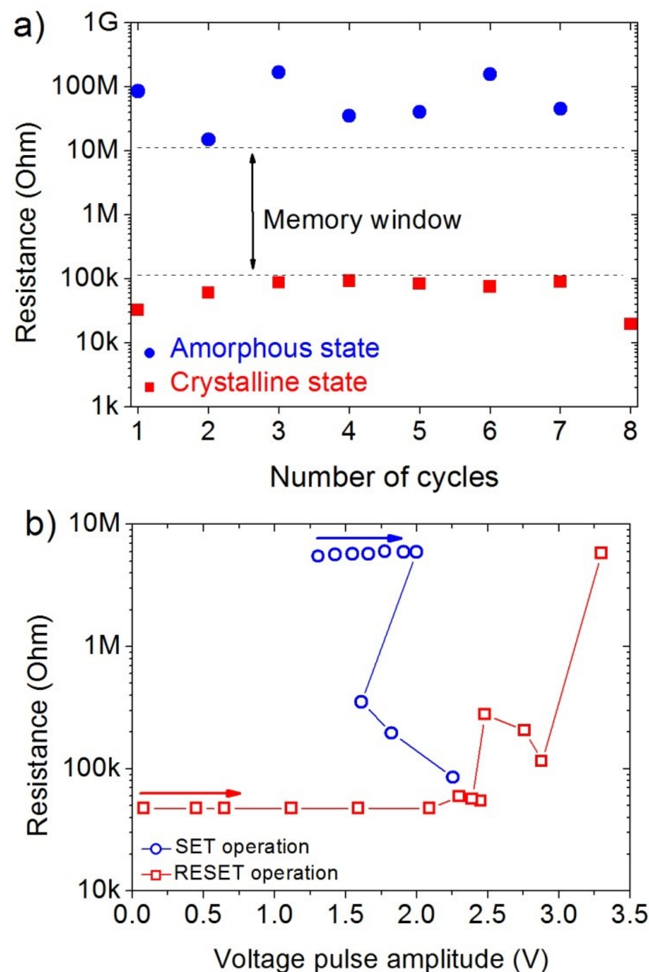


Figure 5-6: (a) SET-RESET cycling test of a 22 nm $In_3Sb_1Te_2$ NW device. The memory window defined by the resistance difference between the amorphous (blue circles) and crystalline (red squares) states is indicated. (b) Resistance of a 20 nm $In_3Sb_1Te_2$ NW device after writing pulses of 100 ns with increasing voltage amplitudes, obtained for initially high (blue circles) and initially low (red squares) resistance states. [81]

The average value (calculated over the switching cycles) of the RESET current, converted from the measured amplitude of the pulsed RESET voltage and the device SET state

resistance (measured in d.c.), was 41 ± 6 μA, equivalent to a current density of 13 ± 2 MA/cm^2; the corresponding RESET power was 130 ± 20 μW. These values of RESET current and power are considerably lower than those reported for NWs based on the Ge-Sb-Te system [30], [90]. Lower RESET power in chalcogenide NWs has only been obtained via defect engineering of their microstructure [85].

Fast SET operation was also proved by pulsed voltage. The resistance change of a 20 nm thick NW device, starting from the high resistance state and applying consecutive writing pulses of 100 ns with increasing voltage amplitudes, is shown in Figure 6 (b). A significant resistance decrease was observed above a value of 2.0 V, as a result of the electronic switch of the amorphous phase, followed by Joule-heating-induced recrystallization. The decrease of the measured voltage pulse amplitude in correspondence of the drop of the resistance, from about 8 MΩ to about 300 KΩ, is probably due to the Negative Differential Resistance (NDR) effect observed in the phase change switching phenomena, as shown in Ref [88]. The corresponding RESET programming curve, obtained starting from a low resistance state, is also reported. In this case, a large resistance increase was observed above 2.9 V, due to the amorphization in the NW. The non-monotonic behavior of the resistance around 2.9 V could be related to a competition between amorphization and crystallization processes [89]. The showed R–V pulses curves of Figure 6 (b) also clearly show two distinct memory states, with a resistance difference of almost two orders of magnitude.

In summary, we demonstrated the phase change behavior of ultra-thin $In_3Sb_1Te_2$ NWs with low programming voltage, current and power consumption. This makes them suitable building blocks for the realization of devices with better performances than the most recent heater-based PCMs with confined cell scheme [36], [91]. This study also establishes the possibility to verify the long-term data retention and multilevel properties of In-Sb-Te based nano-sized PCM cells.

5.3 In doped Sb nanowires for high speed electrical phase change memories

This section is dedicated to the study of the electrical phase-change memory behavior of In doped Sb NW-based devices.

The crystallization speed, which closely relates to the operation rate, is probably the most critical parameter in the discovery of new phase-change materials for PCM [5]. Until now, most studies still focus on GeTe-Sb_2Te_3 pseudo binary system, $Ge_2Sb_2Te_5$ (GST) especially [92]. Along the pseudo binary line, the crystallization speed monotonously increases with increasing Sb_2Te_3 content [93]. Therefore, Sb_2Te_3-based PCM cells will show fast operation speed. However, the low crystallization temperature of Sb_2Te_3 (<100 °C) makes the amorphous state unstable, which means that Sb_2Te_3 is not appropriate for PCM application.

As is well known, antimony is an extremely rapid phase-transition material with a growth-dominated crystallization mechanism. Besides, this kind of Te-free phase-change material is a environmental friendly material compared with other alloys containing Te. However, it has very high crystallization rates but poor archival life stability. Therefore, several new Sb-based phase-change materials, such as Ga-Sb, Ge-Sb and In-Sb, are being investigated [47]. These materials combine rapid crystallization and adequate amorphous phase stability. Of these materials, In-Sb has the lowest melting point; its eutectic point is about 490 °C ($In_{32}Sb_{68}$). Materials with a low melting point are advantageous due to their lower power consumption and therefore suitable for the realization of a high performance PCM. Moreover, In-Sb has a higher crystallization speed and a higher crystallization temperature than Sb-Te [48]. In particular, a crystallization temperature between 150 ° C - 192 ° C has been reported for Sb-rich In-Sb alloys [94][95]. Heretofore, In-Sb phase change alloys have been proposed for high data-rate optical recording, such as in Digital Versatile Discs (DVDs) technology.

In this work, In doped Sb material is proposed for the development of a high speed electrical PCM. NW-based devices have been investigated, being NWs a very attractive option for the realization of highly scaled PCM, as extensively argued in this manuscript.

The NWs were grown via MOCVD, exploiting the VLS growth method, using 20 nm Au nanoparticles as catalysts. The description of the NWs synthesis and of the growth conditions, that have allowed to obtain the In doped Sb NWs, are discussed in the chapter 3 (section 3.3.4.b NWs grown with 20 nm Au nanoparticles).

NWs with length up to 6 μm and having diameters down to ~ 25 nm have been obtained. The structural and analytical characterization of In doped Sb NWs (See the paragraph 3.3.4.b NWs grown with 20 nm Au nanoparticles) revealed that defect-free, single crystal In doped Sb NWs, with In content ranging between 5 and 15%, have been successfully synthesized.

NWs were mechanically transferred onto a silicon oxide substrate with pre-patterned macro-contacts. Then, two-terminal devices were fabricated by EBL technique. Figure 7 displays a SEM image of one PCM device formed by an In doped Sb NW, contacted by Ni/Au micro-electrodes fabricated on top of the NW.

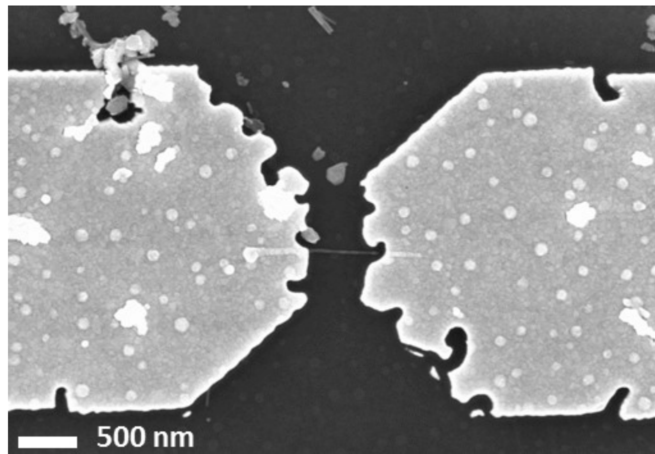


Figure 5-7: SEM image of the PCM device formed by a In doped Sb NW, contacted by Ni/Au micro-electrodes fabricated on top of the NW by EBL.

The details of the devices implementation procedures are reported in chapter 4 of this manuscript (section 4.2.1 Implementation). The electrical phase-change properties of the NWs were investigated by the TLP technique, which has been explained in the first paragraph of this chapter.

To demonstrate memory switching behavior, the current–voltage characteristics of a device based on an In doped Sb NW, with a diameter of 25 nm and a L_{gap} of 650 nm between the Ni/Au electrodes, were measured. Figure 8 (a) reports the programming curve of this device, composed by the I-V characteristics of its RESET (blue circles) and SET (red squares) states. Below the V_{th}, two different physical states of the NW are present: amorphous (high resistance) and crystalline (low resistance). Starting from the device in the SET state with R of ~ 20 kΩ, the RESET state (R ~550 KΩ) was enforced by applying a voltage pulse of 25 ns and amplitude of

2.8 V, corresponding to a RESET current of ~ 140 µA. The device was then brought to the SET state during the I-V, once a V_{th} of ~ 250 mV was reached (Figure 8 (a)).

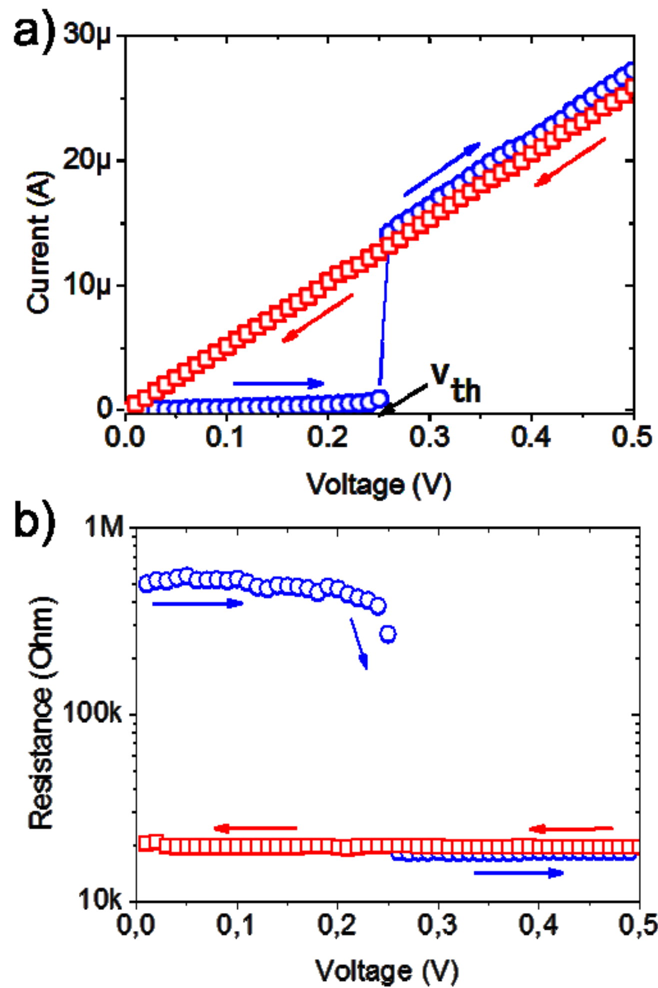


Figure 5-8: Programming curve, composed by the I-V (a) and by the R-V (b) characteristics of the amorphous (blue circles) and crystalline (red squares) states, of a 25 nm In doped Sb NW device. The threshold voltage (V_{th}) for the amorphous to crystalline transition is indicated in (a).

The obtained low resistance state was stable and the device resistance remained low as the voltage was swept back to zero, thus the non-volatility nature of the memory cell is proven. As explained in the first chapter, this threshold memory switching is a critical phenomenon arising from electronic switching at high fields followed by amorphous to crystalline phase-change from Joule heating. The R–I curve (Figure 8(b)) clearly shows two distinct memory states at low bias, with resistance varying over one order of magnitude, ensuring a reliable and adjustable logical partition.

Figure 9 presents the SET-RESET cycling test of a 25 nm In doped Sb NW memory device switched between high- and low-resistance states repeatedly. The voltage pulses for cycling are 2.8 V, 25 ns pulse width for RESET (amorphization or transition into high

resistance) state and 1.5 V, 25 ns for SET (recrystallization or transition into low resistance) state. The reported SET-REST states cycle demonstrates that reversibly and stably memory switch occurs in In doped Sb NWs. Moreover, the memory cell can readily achieve complete SET and RESET operation at 25 ns pulse width, well satisfying the desired performance of high-speed operation. In addition, The average RESET current (calculated over the switching cycles) obtained for a 25 nm NW, converted from the RESET voltage and the SET state resistance (measured in d.c.), was ~ 140 μA, equivalent to a current density of ~ 30 MA/cm^2; the corresponding RESET power was 400 μW. It is worth mentioning that these values of RESET current and power are comparable with those reported for 30 nm $Ge_2Sb_2Te_5$ NWs [30], while they are four times higher than ones measured for $In_3Sb_1Te_2$ NWs of comparable size in this work.

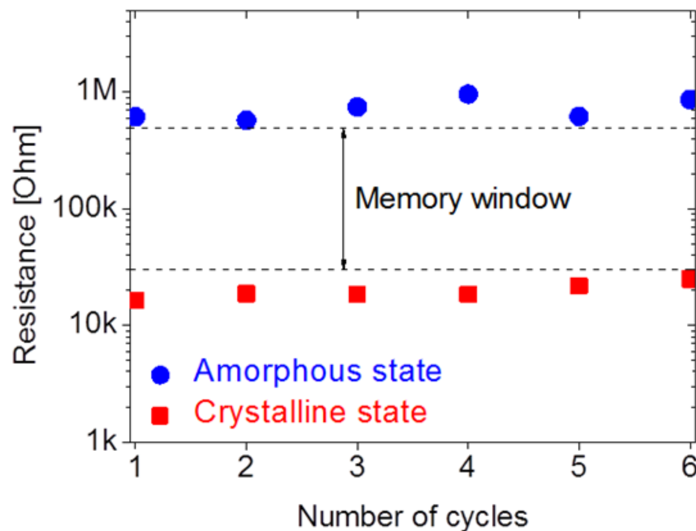


Figure 5-9: SET-RESET cycling test of a 25 nm In doped Sb NW device. The memory window defined by the resistance difference between the amorphous (blue circles) and crystalline (red squares) states is indicated.

In summary, the functional analysis of the In doped Sb NW-based PCM devices gave very promising results, showing ultrafast memory switching reversibly induced by 25 ns current pulses for both crystallization and amorphization processes. In addition, these devices showed a resistance difference between the SET and RESET states higher than one order of magnitude and a relatively low power consumption of ~ 400 μW.

Conclusions

The successful development of PCM technology has been one of the most significant novelties in the field of semiconductor memories of the last years. On one hand PCM device scaling is an essential step in order to make possible denser and low power applications, on the other hand material engineering may represent a breakthrough in terms of reliability and performance enhancement. A smart combination of scaling and material engineering may result into wider application spectrum for PCM.

This work was meant to shed more light on the electrical and functional properties of extremely scaled PCM cells based on emerging phase-change materials. To do so, phase-change nanowires and In-based phase-change alloys have been exploited.

As reported in Chapter 3, the joint use of metalorganic chemical vapor deposition and vapor-liquid-solid self-assembly made it possible to efficiently accomplish a 'bottom-up' growth of different In-based nanowires. In particular, $In_3Sb_1Te_2$, In-doped Sb_4Te_1, In-doped Sb, Ge-doped InTe, and core/shell Ge/In_2Te_3 nanowires have been synthesized, with diameters down to 15 nm. In the same chapter, the chemical, morphological and structural properties of the various grown NWs have been discussed.

The microfabrication of nanowire-based PCM cells is described in Chapter 4, along with a preliminary electrical characterization, which allowed to evaluate the results of the manufacturing processes and select the devices with suitable features for advanced PCM applications. In this regard, technological issues in the implementation of nanowire-based devices were also highlighted.

In Chapter 5, electrical and functional analysis of $In_3Sb_1Te_2$ and In-doped Sb nanowire-based PCM cells was documented. In the same section, the figures of merit of these devices were determined and compared to those of other extremely scaled PCM structures.

In this Thesis, it was proven that ultra-thin In-based NWs display a phase-change behavior with low programming voltage, current, and power consumption. The obtained results support the conclusion that such NWs are potential building blocks for the realization of ultra-scaled, low power PCMs. This work also established the possibility to evaluate the effective features of the up-and-coming In-based class of phase-change materials, such as the thermal stability of the amorphous phase and the crystallization speed, in one-dimensional nanostructures.

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List of publications

- S. Selmo, R. Cecchini, S. Cecchi, C. Wiemer, M. Fanciulli, E. Rotunno, L. Lazzarini, M. Rigato, D. Pogany, A. Lugstein, and M. Longo, “ Low power phase change memory switching of ultra-thin $In_3Sb_1Te_2$ nanowires”, *Appl. Phys. Lett.* 109, 213103 (2016), DOI: 10.1063/1.4968510.
- S. Selmo, S. Cecchi, R. Cecchini, C. Wiemer, M. Fanciulli, E. Rotunno, L. Lazzarini, and M. Longo, “ MOCVD growth and structural characterization of In-Sb-Te nanowires”, *Phys. Status Solidi A* 213(2), 335–338 (2016), DOI: 10.1002/pssa.201532381.
- J.-L. Battaglia, A. Saci, I. De, R. Cecchini, S. Selmo, M. Fanciulli, S. Cecchi and M. Longo, "Thermal resistance measurement of In_3SbTe_2 nanowires", *Phys. Status Solidi A*, (2016), DOI: 10.1002/pssa.201600500.

List of conferences

- 2016 MRS Fall Meeting, Nov 16, Boston, Massachusetts, “Structural and Electrical properties of In doped Sb nanowires for high speed phase change memories”, E. Rotunno, S. Selmo, R. Cecchini, C. Wiemer, M. Longo, L. Lazzarini, Oral presentation, NM1.17.03.
- CIMTEC 2016, Jun 16, Perugia; Italy, “$In_3Sb_1Te_2$ Phase-change nanowires for low power memory”, S. Selmo, R. Cecchini, C. Wiemer, M. Fanciulli, E. Rotunno, L. Lazzarini, A. Lugstein, M. Longo, Poster, K:HP13.
- 2016 MRS Spring Meeting, Mar 16, Phoenix, Arizona, “Au-catalyzed ordered Synthesis and characterization of In-Ge-Te nanowires by MOCVD”, R. Cecchini, S. Selmo, C. Wiemer, M. Fanciulli, E. Rotunno, L. Lazzarini, L. Caccamo, A. Waag, B. Sheehan, S, Monaghan, K. Cherkaoui, P. Hurley, M. Longo, Oral presentation, MD4.7.02.
- E-MRS 2015, May 15, Lille, France, "MOCVD growth and structural characterization of In-Sb-Te nanowires", S. Cecchi, S. Selmo, R. Cecchini, M. Fanciulli, E. Rotunno, L. Lazzarini, C. Wiemer, M. Longo, Oral presentation, AA.I 2.
- E-MRS 2015, May 15, Lille, France, "Matrix of Gold Nano-Droplets for Site-Controlled Growth of Chalcogenide Nanowires", S. Selmo, R. Fallica, R. Cecchini, S. Cecchi, C. Wiemer, M. Longo, Poster, AA.PI 47.

Acknowledgements

This work was performed within the SYNAPSE project (“synthesis and functionality of chalcogenide nanostructures for Phase change memories”), which has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement no. 310339.

I would like to thank the MDM Laboratory, Unit of Agrate Brianza of the CNR Institute for Microelectronics and Microsystems, where the main part of my work was carried out, for hosting my PhD.

After three years spent at the MDM lab, there is a long series of people that I would like to acknowledge for sharing this beautiful experience and contributing, in many different ways, to this PhD thesis.

Special thanks are well deserved by Dr. Massimo Longo and Prof. Marco Fanciulli, who actually made it possible, offering the opportunity to work in the active environment of MDM lab and their scientific supervision as the tutors of my research activity.

Many thanks are due to all the people who directly collaborated to the realization of this work:

Dr. **Raimondo Cecchini** and Dr. **Stefano Cecchi** (MDM Lab) for growing the NWs and for collaborating to their morphology characterization and average compositional analysis, and also for the very useful discussion on all the PCM-related topics.

Dr. **Claudia Wiemer** (MDM Lab) for the XRD measurements, used to evaluate the average crystal structure and growth orientation of the grown nanostructures, and for fruitful discussions on the experimental results.

Dr. **Enzo Rotunno** and Dr. **Laura Lazzarini** (IMEM-CNR, Parma, Italy) for the remarkable HR-TEM characterization of single nanowires.

I am sincerely grateful to Prof. Paul Hurley (Tyndall National Institute, Cork (IE)) and Prof. Alois Lugstein (Institute of Solid State Electronics, TU Wien, Vienna (AT)) and to all their teammates (the list is too long!) for hosting and supporting me during my two internships over there.

Then, thanks to all those people who, in large or small measure, helped me with the research activity during the PhD: Roberto, Davide, Toni, Sebastian, Masiar, Anton, Markus, Matteo, Johannes, Markus, Karim, Brendan, Mario, Simone, Stefano, Tommaso, Sabina and Grazia.

At the very end, I would like to thank all the person who joined in this adventure, sharing happy as well as difficult moments: all my colleagues in MDM, my dearest friends and my family.