Smart integration of silicon nanowire arrays in all-silicon thermoelectric micro-nanogenerators

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Smart integration of silicon nanowire arrays in all-silicon thermoelectric micro-nanogenerators

Luis Fonseca[1,5]**, Jose-Domingo Santos**[2]**, Alberto Roncaglia**[3]**,
Dario Narducci**[4]**, Carlos Calaza**[1]**, Marc Salleras**[1]**, Inci Donmez**[1]**,
Albert Tarancon**[2]**, Alex Morata**[2]**, Gerard Gadea**[2]**, Luca Belsito**[3] **and
Laura Zulian**[4]

[1] IMB-CNM (CSIC), Campus UAB, E-08193 Bellaterra, Spain
[2] IREC, Jardí de les Dones de Negre 1, E-08930 Sant Adrià de Besòs, Spain
[3] CNR-IMM, V.Piero Gobetti, 101, I-40129 Bologna, Italy
[4] Dept. Materials Science, University of Milano Bicocca, v. R. Cozzi 55, I-20125 Milan, Italy

E-mail: luis.fonseca@imb-cnm.csic.es

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Abstract

Micro and nanotechnologies are called to play a key role in the fabrication of small and low cost sensors with excellent performance enabling new continuous monitoring scenarios and distributed intelligence paradigms (*Internet of Things*, *Trillion Sensors*). Harvesting devices providing energy autonomy to those large numbers of microsensors will be essential. In those scenarios where waste heat sources are present, thermoelectricity will be the obvious choice. However, miniaturization of state of the art thermoelectric modules is not easy with the current technologies used for their fabrication. Micro and nanotechnologies offer an interesting alternative considering that silicon in nanowire form is a material with a promising thermoelectric figure of merit. This paper presents two approaches for the integration of large numbers of silicon nanowires in a cost-effective and practical way using only micromachining and thin-film processes compatible with silicon technologies. Both approaches lead to automated physical and electrical integration of medium-high density stacked arrays of crystalline or polycrystalline silicon nanowires with arbitrary length (tens to hundreds microns) and diameters below 100 nm.

Keywords: silicon nanowires, silicon technologies, thermoelectricity, top-down approach, bottom-up approach

(Some figures may appear in colour only in the online journal)

Introduction

In order to fulfill new paradigms such as *Internet of Things* or *Trillion Sensors* large volume fabrication of miniaturized

devices needs to be addressed. In order to provide those devices with energy autonomy, solutions other than primary batteries are advisable, i.e. energy harvesting approaches. In those application scenarios where residual heat is present thermoelectricity may be exploited as a source of energy autonomy. Miniaturization and large volume fabrication are significant characteristics of silicon technologies and, indeed, many sensors and auxiliary electronic and communication devices are fabricated with such technologies. On the other hand, the assembly technology used in standard thermoelectric modules is not prone to automation and

[5] Author to whom any correspondence should be addressed.

miniaturization and usually needs materials with complex internal structure involving scarce elements.

Up to ten years ago silicon was considered a material of poor interest for thermoelectric purposes. Although silicon is an abundant inexpensive material and a fantastic technology is available for its processing, its thermoelectric figure of merit *ZT* is too low compared to that of standard thermoelectric materials to make it interesting in the field of thermoelectric generation. This opinion abruptly changed with the discovery that thermal conductivity in silicon nanowires (Si NWs) decreases significantly when the wire diameter is brought to nanometer scale. In two seminal papers appeared in 2008 [1, 2], two collaborations independently showed that Si thermal conductivity decreases by a factor of 20 when moving from bulk silicon to nanowires (for which $\kappa \approx$ 6 W m^{-1} K^{-1} at 300 K), provided that the surface roughness is such to enable specular reflection of electrons while incoherently scattering phonons. This brought *ZT* of single crystalline silicon NWs to a region, around 0.6, for which applications are of interest. Although the detailed mechanism of selective scattering of phonons over electrons was not completely clear in 2008, it was however evident that two critical sizes ruled κ, namely the NW diameter and the NW surface roughness σ. Actually, in any nanostructure (either 1D or 2D) phonon mean free path Λ is limited by scattering at outer surfaces, provided that phonon wavelength λ is small compared to σ. This interplay between λ and σ was actually well known in nanolayers: no damping of κ had been observed in multilayers obtained by MBE, where sharp interfaces cause phonons to be coherently scattered (reflected) with no reduction of their Λ, while a dramatic reduction of the thermal conductivity was reported to occur in ultrathin films with ruggedized outer surfaces [3].

The enhanced properties of silicon NWs have been proved by painstakingly placing a single nanowire (grown elsewhere and sonicated) in a suspended ad hoc thermal test microstructure and securing its mechanical and electrical bonds by means of FIB-assisted processes such as in [1]. It is obvious that fabricating a useful thermoelectric device will demand much more *populated arrays* of Si NWs and they need to be integrated in a way that their connections to the thermally active parts of the generator are achieved in an *automated* way. Monolithic silicon top-down approaches have been already assayed to achieve this goal with silicon technologies. For instance, a planar micro thermo-electric generator (TEG) can be obtained by fabricating a suspended silicon platform and defining a low density flat Si NWs array in a silicon-on-insulator (SOI) wafer with a nano-thick *device* layer [2]. The resulting devices are fragile and require the use of time-consuming nanopatterning techniques such as e-beam or FIB. A second approach is using state of the art submicron CMOS technologies to obtain more robust structures and higher density arrays of Si NWs. In this case the microgenerator is of vertical architecture, which adapts better to naturally occurring thermal gradients, but the 'height' of the vertically defined nanowires is limited to the order of one micron, which is not large enough to develop significant temperature differences across them [4].
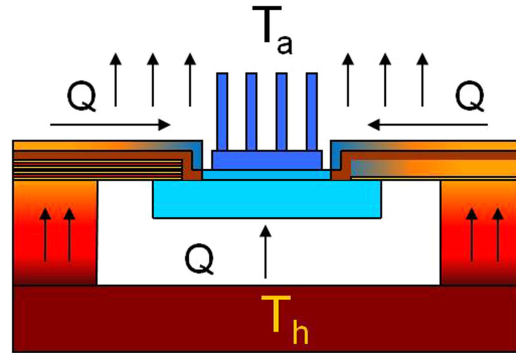

Figure 1. Lateral micro-TEG based on Si NWs integrated in a micromachined device.

In this work, two alternative approaches for the automatic integration of a large number of several tens of microns long Si NWs into lateral thermoelectric devices are introduced. The focus is put on integration feasibility, device architecture and compatible processing sequence definition, in order to bring the previously reported good thermoelectric features of single Si NWs a step forward towards useful devices. Both single-crystalline and polycrystalline silicon NWs are considered. Actually, grain boundaries are known to have additional beneficial effects on the reduction of NW thermal conductivity [5]. This evidence is in good agreement with recent analyses by Yang and Dames [6]. The reduction of κ in nanostructures is the result of the selective suppression of phonon modes. Nano-objects of appropriate size and spacing inhibit heat conduction by phonons with λ smaller than the scatterer size and Λ comparable or larger than their spacing. Thus, nano-grains by at least one order of magnitude smaller than the diameter of the NWs will suppress phonon modes with wavelengths larger than surface roughness σ, which are not affected by the incoherent scattering at the nanostructure outer walls. As a result, thermal conductivities of 3 -4 W m^{-1} K^{-1} were measured in poly-Si NWs with diameters around 100 nm, namely κ values by a factor 2 smaller than in single-crystalline Si NWs of similar size [6]. Consistently, a much less evident effect was reported in poly-Si nanolayers as in that case the grain size was comparable to the nanolayer thickness [7]. On the other hand, the presence of grain boundaries affects negatively the NW power factor (electric conductivity is reduced). In spite of this trade-off, values of $ZT \approx 0.1$ were obtained at 300 K [8], which justifies further investigation of poly-Si NWs and the effort of devising an approach for their mass integration.

Integration of Si NWs into silicon planar architectures

For both single crystalline and polycrystalline Si NWs, the architectural approach considered in this work is planar in order to make their integration consistent with typical silicon technologies. Transposing natural vertical thermal gradients into a lateral architecture requires the definition of a thermally isolated platform to properly re-steer heat flow. The typical resulting

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(b)
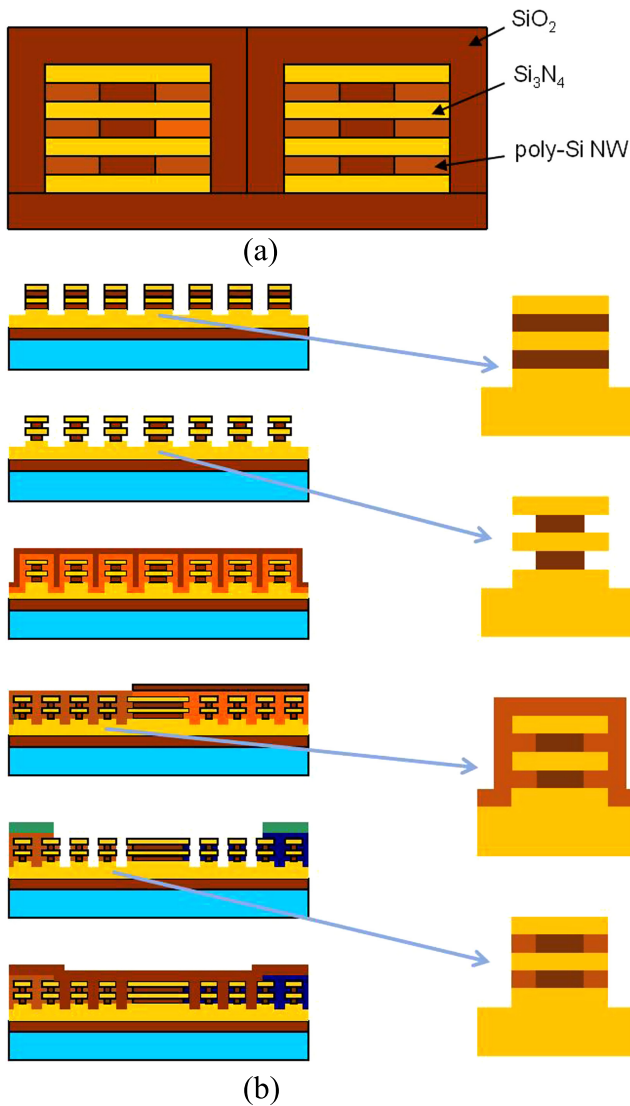
Figure 2. Top-down fabricated polycrystalline Si NWs multilayered arrays for micro-TEGs. (a) Schematic cross-section of the stacked NWs arrays. (b) Critical sequence of main steps leading to n and p poly-Si NWs embedded in a Si_3N_4/SiO_2 structured multilayer.

geometry is depicted in figure 1 where a lateral temperature difference is obtained from a vertical gradient using a structure consisting of a suspended platform (usually in contact with a heater exchanger) connected via Si NWs with the surrounding silicon bulk rim (usually in contact with the heat source). Such suspended platforms can be routinely obtained by standard silicon micromachining. In this way, the use of silicon device-making technologies together with the use of monolithically integrated Si NWs as thermoelectric material pave the way to all-silicon thermoelectric micro-nanogenerators.

Top-down integration of poly-Si NWs arrays

The first approach considered in this work provides a way to integrate medium-high densities of stacked top-down
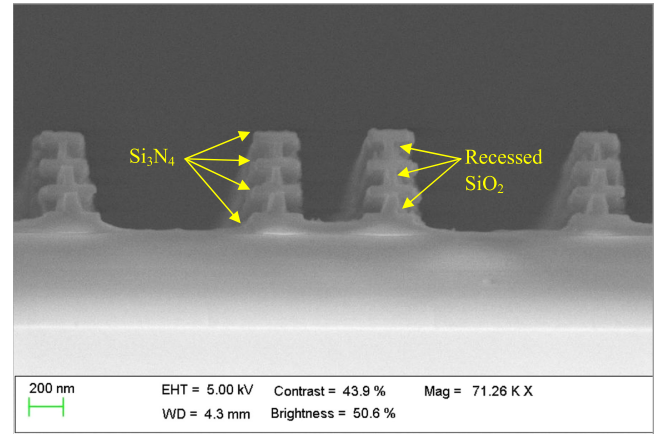

a
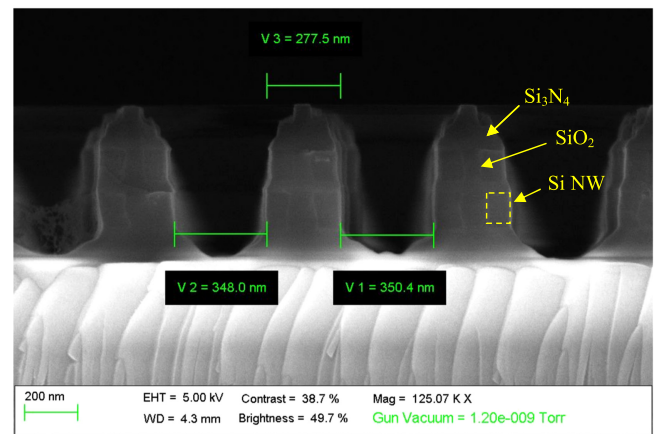
b

Figure 3. (a) Si_3N_4/SiO_2 nanotemplates and (b) high-density multilayered embedded poly-Si NWs.

polysilicon nanowires. It makes use of multilayered strips of very thin silicon oxide and silicon nitride films vertically patterned [9]. A selective silicon oxide wet etch is performed to produce lateral nano-recesses in the oxide layers of the stacked structure. A conformal polysilicon deposition and dry etch-back follows, leaving behind polysilicon filled nano-recesses that give rise to arrays of as-long-as-designed poly-Si NWs. This process sequence is schematically shown in figure 2 and SEM images of pre- and post-filled nano-recesses are shown in figure 3.

The NW section is roughly square, with a typical dimension of 70–100 nm. Linear densities of a few thousands of NWs per mm may be achieved without stressing much the finesse of the lithography method (figure 3). N and p doped regions are locally defined after the polysilicon deposition so that the typical two legs of the thermogenerator are easily obtained.

The p–n thermopile is fabricated by alternating thermo-elements composed by stacked nanowires with opposite doping type, side by side, and connecting them in series with Al interconnections, both in the hot and cold junctions. The n and p regions are obtained following thin film lithography and doping techniques common for silicon technologies: once the polysilicon is deposited, n-doping is achieved with a $POCl_3$

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b
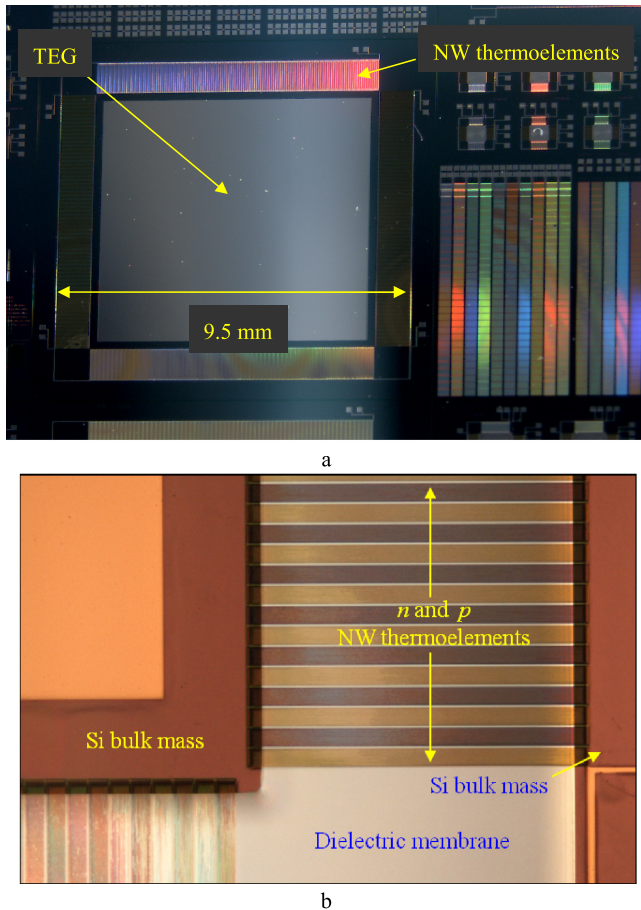
Figure 4. (a) Lateral micro-TEG with thermoelements built with top-down defined poly-Si NWs. (b) Zoom up of the TEG lower right corner where the adjacent n and p regions are shown.

thermal process in certain areas of NWs while protecting the adjacent ones with a SiO$_2$ layer (as in the fourth diagram of figure 2(b)); the process is repeated for the p areas using a spin-on-dielectric method for Boron doping. By alternating such p and n-type multilayered nanowire arrays, a thermocouple chain is manufactured on the final micro-TEG device, around a central area of roughly 8 × 8 mm^2 (figure 4(a)). In this area, a thermal radiator can be mounted in order to enhance the thermal exchange with the surrounding environment and consequently improve the performance of thermoelectric conversion. The micro-TEG is formed by 264 n regions and 264 p regions connected in series. Every one of those regions features 78 nanowire strips, containing six nanowires each (as in figure 3(b)). The length of the nanowires is 950 μm (a rather extreme technological case). Using smaller devices as test structures, an electrical resistivity of 2 and 4 mΩ cm, and a Seebeck coefficient of 160 and 140 μV K^{-1} have been determined for n and p-type nanowires, respectively. A Seebeck voltage of 500 mV has been obtained in preliminary measurements when letting rest one of the TEG structures of figure 4(a) onto a hotplate at 50 °C without any thermal radiator. This evidence points to the fact that such large number of Si NWs has been functionally integrated.

Bottom-up integration of Si NWs arrays

The second approach shares with the previous one the technology used to produce the areas enabling a thermal contrast in the device (microplatforms), but makes use of bottom-up techniques to obtain the massive parallel integration of nano-objects. Since no fine lithography approach is needed at all for defining the nanowires themselves or their nanotemplates, higher Si NWs densities can be obtained at a minimum technological cost.

In this bottom-up approach, gold nanoparticles have to be selectively deposited onto the active area of the device structure: the vertical walls of the suspended platform and rim. These gold nanoparticles act as catalyst for the growth of the Si NWs by means of the chemical-vapor-deposition vapor–liquid–solid (CVD-VLS) method. The gold nanoparticles favor the decomposition of the molecules used as silicon precursors to elemental silicon. The silicon atoms are then incorporated in the gold seeds until the saturation is reached. At this point, the silicon precipitates and the epitaxial growth of the Si NWs take place till they reach the opposing wall, connecting rim and platform.

Although, neither the galvanic displacement method used for the gold seeds nor the CVD-VLS technique for NW growing are new [10–13], only recently they have been used for thermoelectric purposes [14]. Precisely, a thorough revision of the deposition conditions for both processes has been carried out in order to optimize the final Si NW array characteristics (Si NW alignment, diameter, and areal density) [15].

As mentioned above, the first step of the bottom-up approach consists on the selective gold deposition onto active areas by means of the microemulsion galvanic displacement. In this procedure, the substrate/device structure is immersed in a microemulsion prepared by mixing an aqueous solution (consisting of deionized water, NaAuCl$_4$ and HF) and an organic phase (consisting of n-heptane and AOT-surfactant). A redox reaction causes the gold precipitation onto the bare silicon surfaces. This reaction is inhibited onto those surfaces appropriately covered with silicon oxide, thus allowing selective catalyst deposition on the areas of interest.

After the substrate annealing, a gold seed array is obtained (figure 5), whose mean diameter and surface density will later determine the properties of the resulting Si NW array. This way, the modification of the galvanic displacement conditions allows the control of both array parameters. The effect of varying the aqueous/organic phase proportion and the substrate dipping time were investigated. The results have showed that is possible to control the gold nanoparticles diameter in a wide range between 10 and 100 nm, and the areal density in a range between 1 and 100 nanoparticles μm^{-2} [15].

Specifically, the microemulsion used for galvanic displacement seeding in the present work was obtained by mixing by sonication two phases prepared separately: (i) 1 ml of aqueous phase consisting of 0.2 M HF and 0.01 M NaAuCl$_4$ diluted in deionized water; (ii) 8 ml of organic phase consisting of 0.33 M sodium bis(2-ethylhexyl) sulfosuccinate (AOT, a surfactant) diluted in n-heptane. The dipping time was 30 s in all
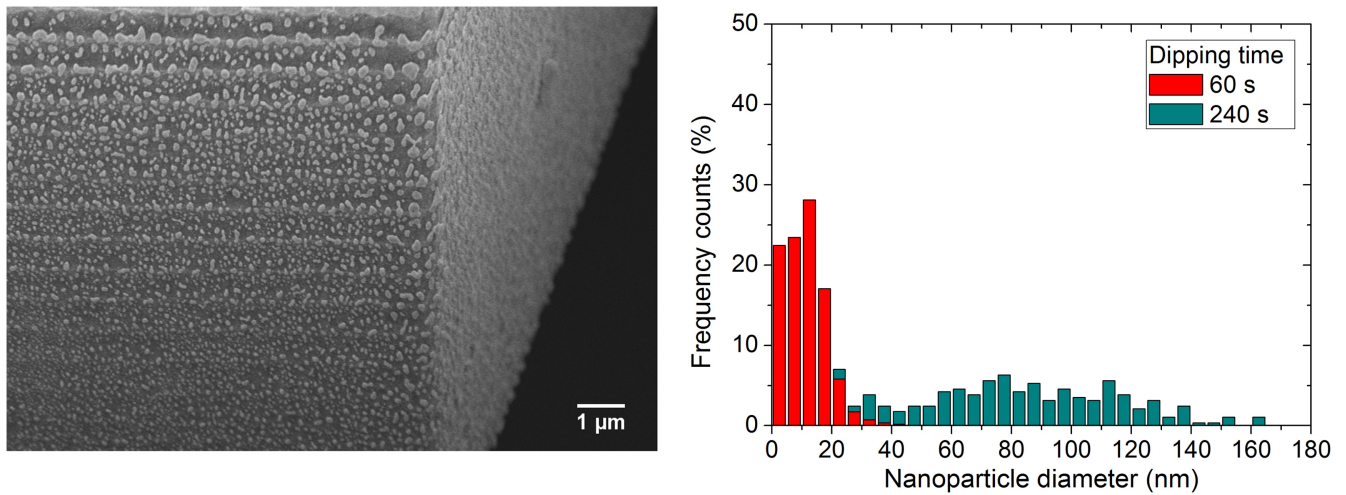
Figure 5. Gold nanoparticles successfully deposited in the active part of the device structure: 15 μm deep silicon trenches (left). Different gold seed size distribution obtained in a device structure by adjusting the galvanic displacement conditions (right).
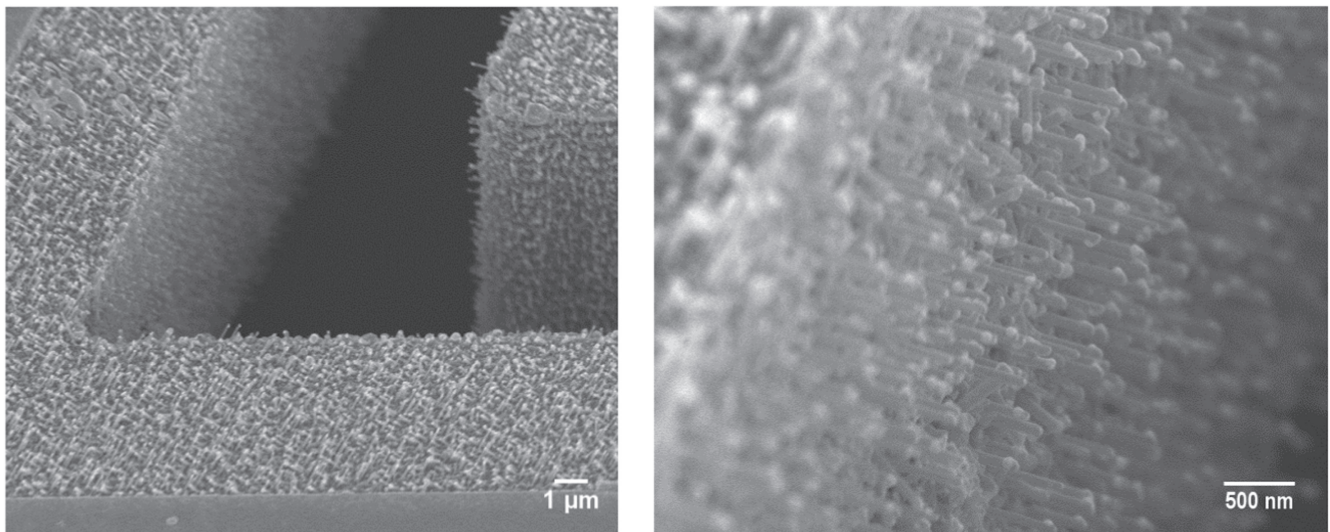
Figure 6. Vertical distribution of proto-Si NWs (less than 1 μm of length) obtained in trenches after a very short CVD-VLS growth (left). Zoom up at the trench mid-section (right).

cases. Magnetic stirring was used in order to improve micro-emulsion penetration into the microtrenches.

Secondly, the Si NW growth conditions should be fine-tuned to achieve the optimum thermoelectric array. The proposed CVD process uses silane (SiH_4) as NW growth precursor, which allows lower deposition temperatures more compatible with MEMS technology, instead of the commonly used silicon tetrachloride. Precisely, CVD parameters like the deposition temperature or the silane partial pressure are decisive for obtaining an array of well aligned and parallel Si NWs. Additionally, these parameters also influence on the mean diameter of the resulting Si NWs, and consequently, they should be tuned for a given gold nanoparticles size. Specifically, for a $\langle 111 \rangle$ silicon surface, it has been demonstrated that a deposition temperature of 650 °C and a pressure of 2.5 Torr favors obtaining Si NWs with a diameter distribution around 50–70 nm [15]. Thus, it is possible to reach a trade-off between the growth of mechanically stable Si NWs

and the desired effect of phonon scattering (expected for diameters lower than 100 nm) [1]. The first stages of the NW array growth inside the device trench can be observed in figure 6, where its high density and homogeneity can be appreciated.

Figure 7 shows the final result after the Si NW array bridges both trench walls. The quasi-epitaxial nanowire-bulk connection obtained by means of the bottom-up approach provides a mechanically robust junction with a very low thermal and electrical contact resistance.

Since the growth of the NWs by CVD-VLS requires a $\langle 111 \rangle$ surface and temperatures above 650 °C, the only precautions to be taken at device level are the choice of the appropriate starting silicon orientation ($\langle 110 \rangle$), the topographical alignment of the perimeter of the platform with the position of vertically occurring $\langle 111 \rangle$ planes, and the use of metals that can withstand the temperature of the CVD process (e.g. W). For technological simplicity the starting substrates
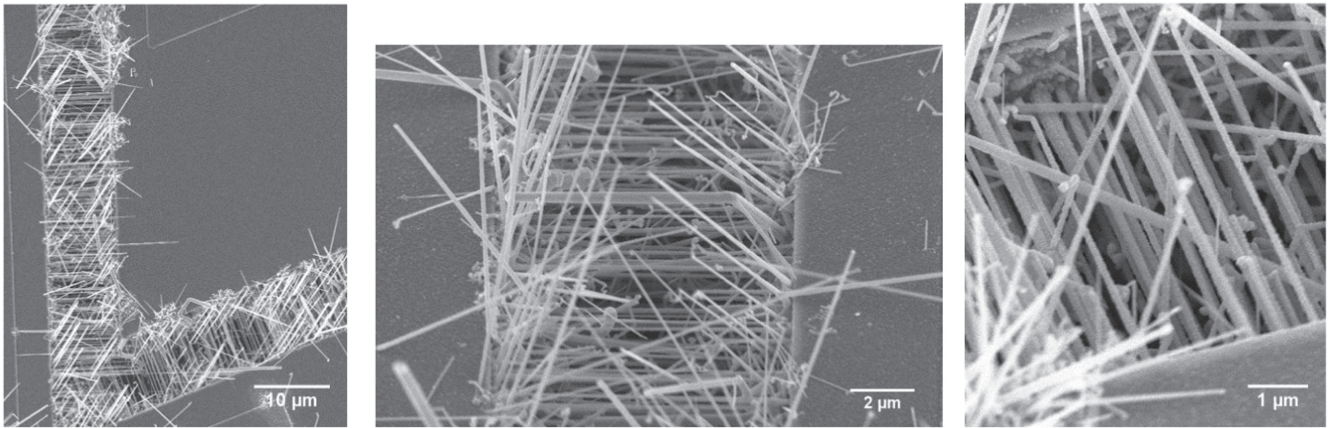
Figure 7. Top view of the Si NW array obtained by means of bottom-up approach, connecting rim and suspended platform. Different magnifications are presented from left to right.

chosen are SOI wafers, with a $\langle 110 \rangle$ silicon *device* layer of several microns on top of a $500\,\mu m$ $\langle 100 \rangle$ standard *handle* wafer with a one micron silicon oxide layer in between. The *handle* wafer is the one locally removed under the device layer for defining the suspended platforms. The thickness of the silicon *device* layer together with the perimeter of the platform and the areal density of gold seeds determine the number of Si NWs that will be obtained in the device. The architecture proposed for the thermoelectric generator is uni-leg, which means that only one type (p-type) of semiconductor is used, while the second thermoelectric leg is made of metal (figure 8). A p-type Si NW array is achieved by simply introducing diborane (B_2H_6) during the CVD growth process, while the doping level is controlled by means of the diborane partial pressure [16].

The resulting TEG performance is 'halved' but the technology is kept simple. This uni-leg approach is common in planar thin film thermopiles used as infrared sensors. Figure 8(b) shows how the uni-leg configuration is materialized in our planar approach: the suspended platform and surrounding rim configure one single uni-leg thermocouple (corresponding to the dotted circle of figure 8(a)) of the final thermopile, where the Si NWs distributed across the perimeter of the platform and connecting it to the rim are the p-leg and the metal track going from the platform to rim through the silicon supporting bridge is the metal leg. Microplatforms such the ones described have been fabricated and Si NWs have been successfully integrated in large numbers as can be seen in figure 9.

Although both top-down and bottom-up approaches use a similar planar architecture, it must be stressed that the suspended platform in the case of the top-down approach configures a *whole thermopile* (with several p–n thermocouples) while for the bottom-up approach the suspended platform configures a *single uni-leg thermocouple* and several of them need to be fabricated in parallel and connected to produce a uni-leg thermopile. Consequently, the suspended platform in the top-down approach is large (ca $1\,cm^2$) but small for the bottom-up approach (ca $1\,mm^2$).

With appropriate Si NWs doping, resistances as low as $60\,\Omega$ have been measured for the NWs ensemble in devices like the ones of figure 9; this resistance corresponds to a great extent to the metal collectors, pointing to a good electric contact of the NWs with the silicon areas they are grown from. Preliminary characterization shows that one of those bottom-up thermocouples produces about 90 nW when placed onto a $250\,°C$ hot plate. The lack of a heat exchanger limits the effective ΔT perceived by the Si NWs and the corresponding harvested power. If that same temperature is forced locally in the suspended platform by means of the built-in heater shown in figure 9(a), the power obtained reaches $10\,\mu W$, which clearly points to the need of a heat exchanger that maximizes the temperature across the nanowires while in operation.

Optimal density of Si NWs arrays

It becomes clear that both approaches offer an important control capability of the NW array properties. This trait is of special interest to maximize the device performance, since it is well known the need of finding an optimal trade-off between the electrical resistance and thermal resistance of the TEG [17].

For a thermoelectric device, it can be shown that the maximum power in load matching conditions P_{out} is described by the following formula:

$$P_{out} = \frac{(N_{TE}S\Delta T)^2}{4N_{TE}R_{TE}} \qquad (1)$$

in which S is the Seebeck coefficient of the individual nanostructured thermoelement, R_{TE} its electrical resistance, ΔT the temperature difference which builds up across the thermoelements when the device is operating, and N_{TE} the number of thermoelements connected in series in the generator. Equation (1) is derived from the electrical power transferred to an output load in matching conditions from a linear network with output resistance R_{out} and equivalent Thévenin voltage source V_{eq}, equal to $P_{out} = V_{eq}^2/(4R_{eq})$. For

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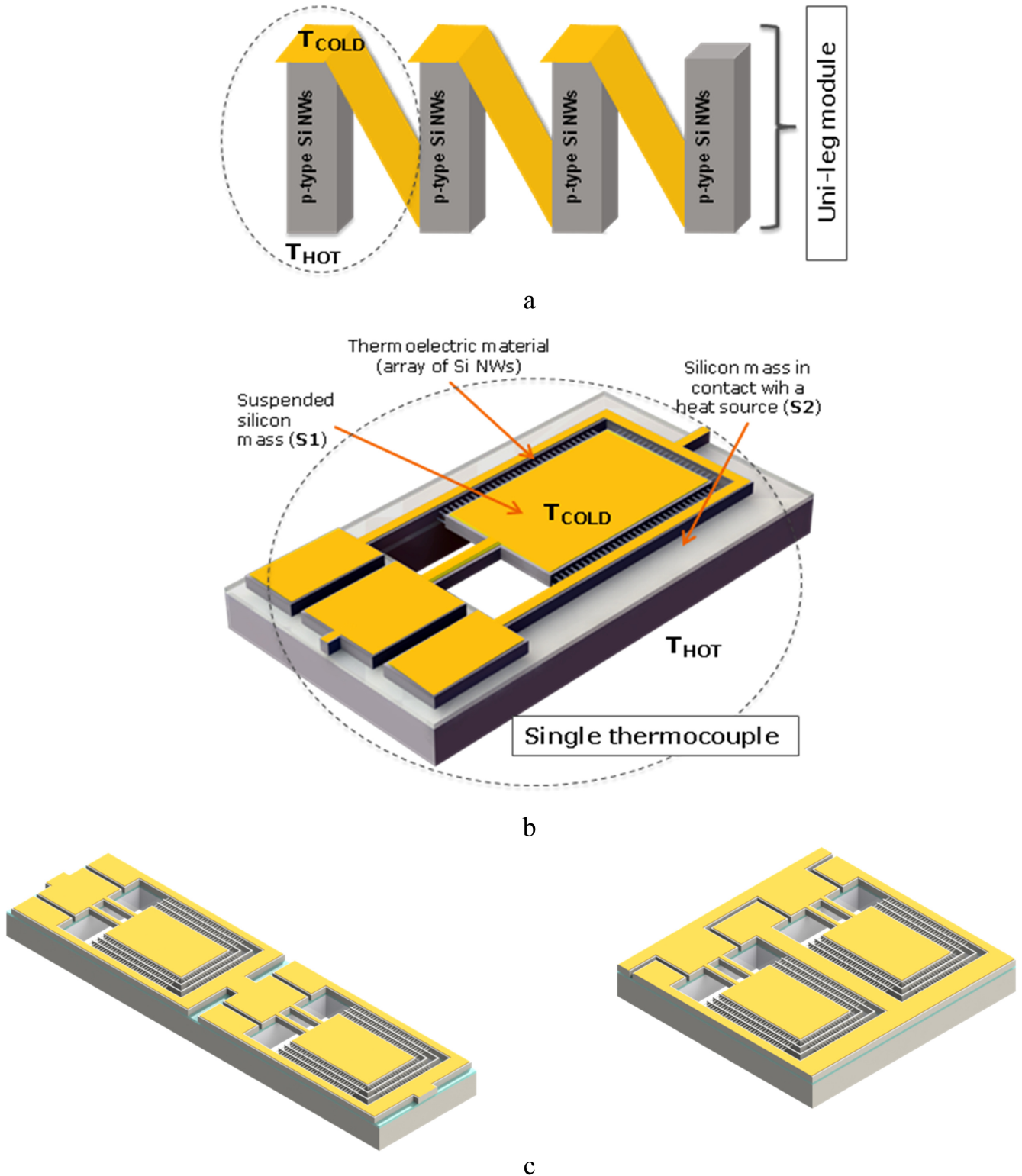
Figure 8. (a) Sketch of a uni-leg approach: only one polarity semiconductor is used, the second leg is made of metal. (b) Schematics of the unitary thermocouple formed by the metal track and the bridging Si NWs array in a suspended platform planar configuration; it corresponds to the physical implementation of the dotted circle in figure 8(a). (c) In-chip arrangements of several termocouples with appropriate series or parallel connections are needed to define the final micro-TEG with appropriate *V* and *I* characteristics.

the particular case of a thermoelectric generator, the identities $V_{\text{eq}} = N_{\text{TE}}S\Delta T$ and $R_{\text{eq}} = N_{\text{TE}}R_{\text{TE}}$ hold.

Specifically, the Si NW areal density becomes the key parameter in this optimization process once the generator structure properties (parasitic thermal and electrical resistance) and the thermoelectric material properties (thermal conductivity, κ_{SiNW}, electrical resistivity, ρ_{SiNW}, and Seebeck coefficient, S_{SiNW}) are set.
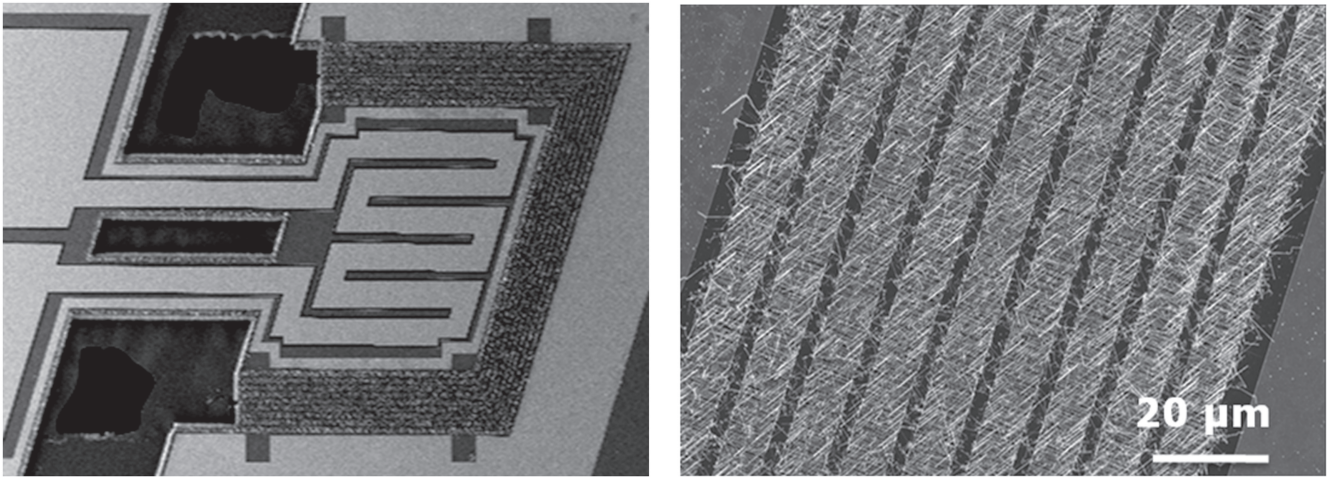
Figure 9. Lateral high density crystalline Si NWs arrays bridging the suspended microplatform and the surrounding device rim. A multi-trench strategy using intermediate narrow Si spacers has been adopted here to obtain 'effective' longer NWs after a single 10 μm NW CVD-VLS process (left). Zoom up of a section of the bridging area with nine consecutive filled trenches (right) [14].

Table 1. Si NW parameters used for the bottom-up micro-TEG performance modeling. Electrical properties correspond to a boron doping level of 10^{18} cm^{-3}. Thermal conductivity corresponds to a Si NW mean diameter in the order of 50 nm.

Length (μm)	ρ_{SiNW} (mΩ cm)	S_{SiNW} (μV K^{-1})	k_{SiNW} (W m^{-1} K^{-1})
10	48	970	10

Bottom-up approach

In order to theoretically determine the influence of NW array density (among other parameters) on device performance, an analytical device model has been developed that includes the main features of the proposed uni-leg bottom-up micro-TEG design and the typical thermoelectric Si NW properties (summarized in table 1) [1, 16, 18].

Being the NWs assembled in a parallel configuration, the progressive increase of the Si NW array density leads to a reduction of its effective resistance ($R_{SiNW\ array}$), thus improving the device internal resistance and its maximum short-circuit electrical current (I_{SC}). However, this effect is limited by the generator parasitic electrical resistance, and counterbalanced by the greater thermal conductance of the Si NW array ($K_{SiNW\ array}$) that causes a thermal gradient drop. As a result, the initial I_{SC} improvement curves down at very high array densities, associated to a worsening of the maximum open-circuit voltage (V_{OC}). Both effects are appreciated in figure 10, in which a temperature gradient of 100 K is considered.

Thus, the model confirms the existence of a proper NW μm^{-2} value that enhances the device performance. Specifically, it has been found that for typical Si NW thermal conductivities, the optimum array density is in the range of 0.1–10 NW μm^{-2}. Moreover, results in figure 11 show that for low enough κ_{SiNW}, maximum power values of the order of 100–200 μW could be achieved with a temperature gradient of 100 K. Similarly, changes in the Si NW doping level

require an array density adjustment in order to maximize the device performance. Again, optimum areal densities are found in the range of 0.1–10 NW μm^{-2}, confirming the feasibility of a fully optimized micro-TEG. The power values have been calculated using equation (1) with $N_{TE} = 1$ (single thermocouple with thermal and electrical parallel arrangement of NWs).

Top-down approach

For the top-down approach, similar considerations can be formulated about the nanowire density for a fixed length of the thermoelements that are composed by nanowires connected thermally in parallel and electrically in series. It can be shown that the thermal behavior of the top-down TEG structure can be approximately described by an analytical model [19]. Figure 12 (left) reports the power generated by the top-down TEG versus the number of nanowire levels (NWL) used in the stacked array, calculated using such analytical model with physical parameters measured on heavily doped polycrystalline silicon nanowires in previous works [5, 20]. As can be seen, also in this case an optimum NWL (and consequently an optimum nanowire density) exists. However, such optimized value is different when the length of the thermoelement is varied, as shown in figure 12 (right).

As far as the series connection of the thermocouples is concerned, a reference geometry like the one shown in figure 13 can be considered for the top-down device. Assuming than all the available space in the device around the radiator area is utilized to accommodate the largest possible number of thermoelements, the temperature difference ΔT will be, to a first-level approximation, independent of the type of arrangement chosen for the thermoelements because this will weakly affect the thermal resistance of the generator. Moreover, by indicating with W the width of the thermoelement (figure 13), it can be noted that, in order to increase the number of thermocouples connected in series, their width will
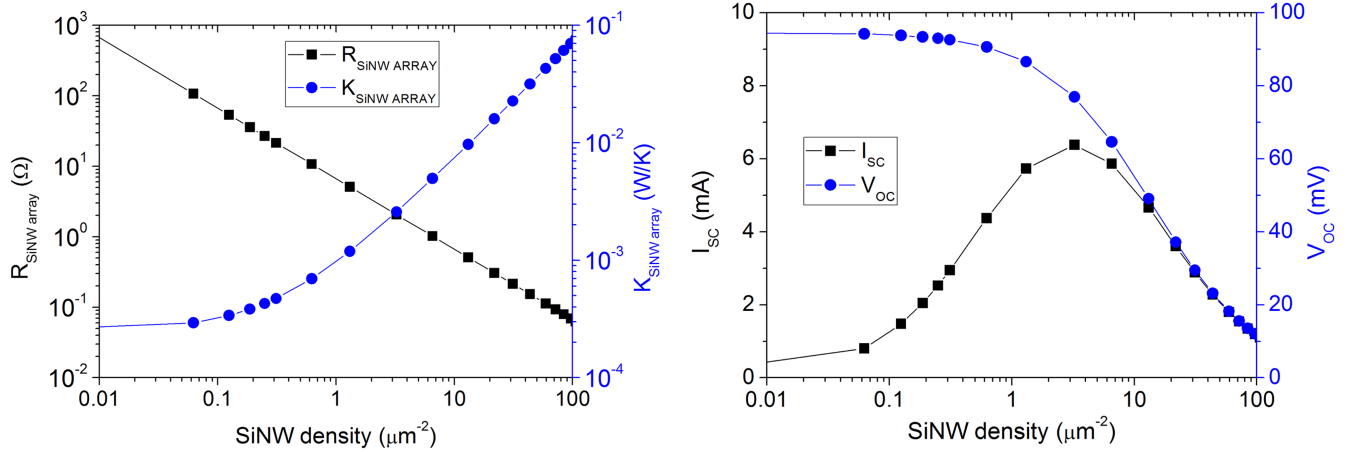
Figure 10. Evolution of the modeled Si NW array electrical and thermal properties as the array density is increased (left). Evolution of the modeled short-circuit current and open-circuit voltage as the array density is increased (right). Table 1 parameters are used.
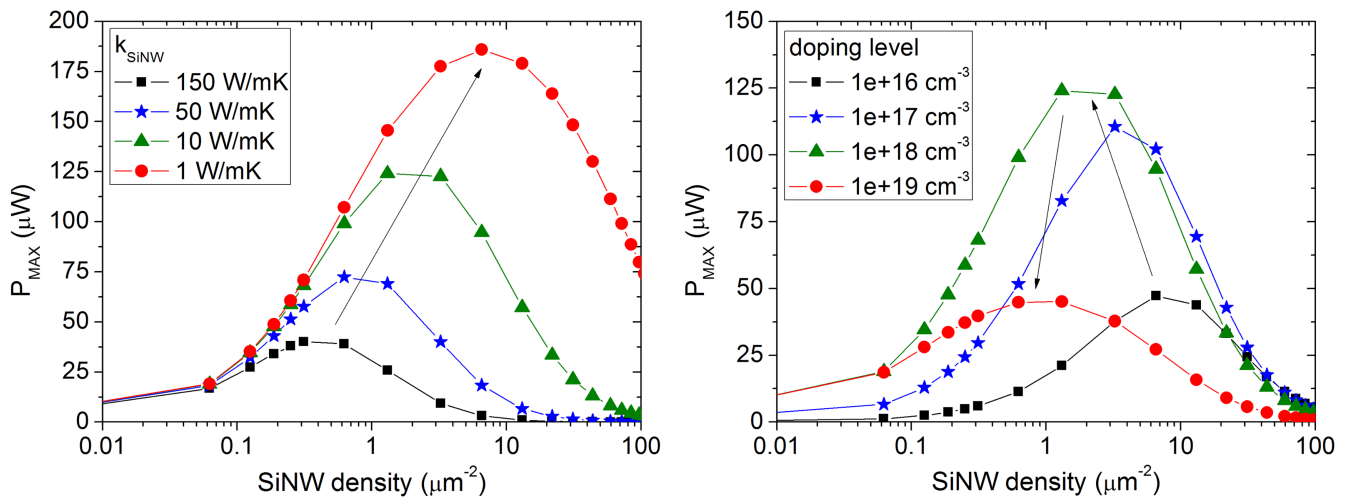
Figure 11. Maximum power dependence on the array density for different Si NW thermal conductivity values (left) and for different Si NW doping levels (right). A doping level of 10^{18} cm^{-3} and a κ_{SiNW} of 10 W m^{-1} K^{-1} are respectively considered.
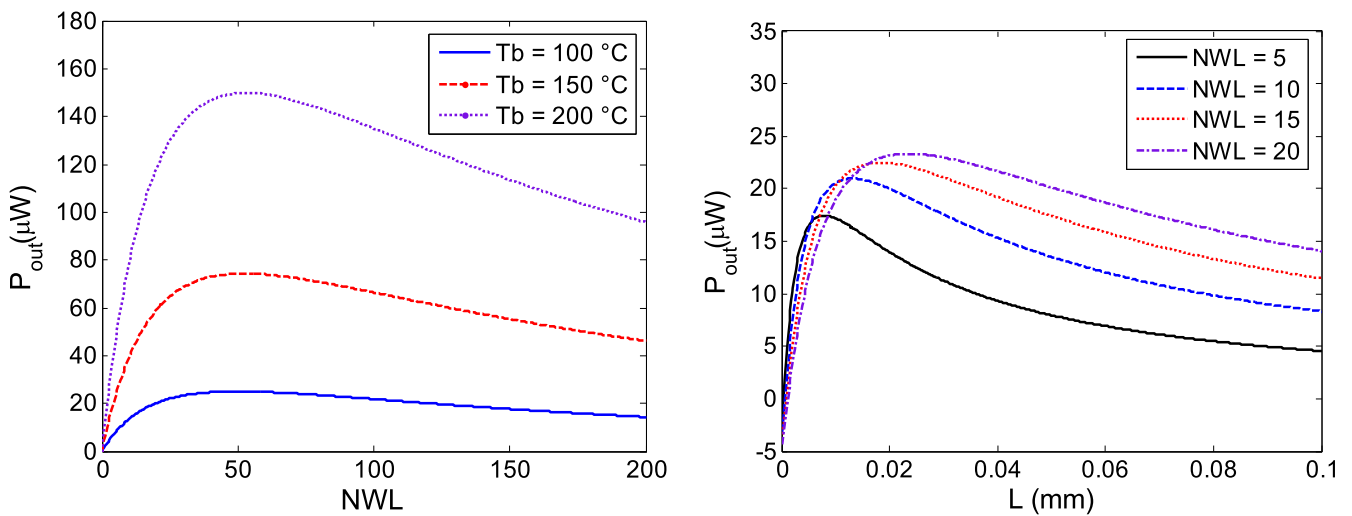
Figure 12. Calculated output power dependence on NWL ($L = 50$ μm) for different hot body temperatures (left) and on L (Tb = 100 °C) for different NWLs (right). The lateral distance between vertical NW stacks is set to 200 nm.
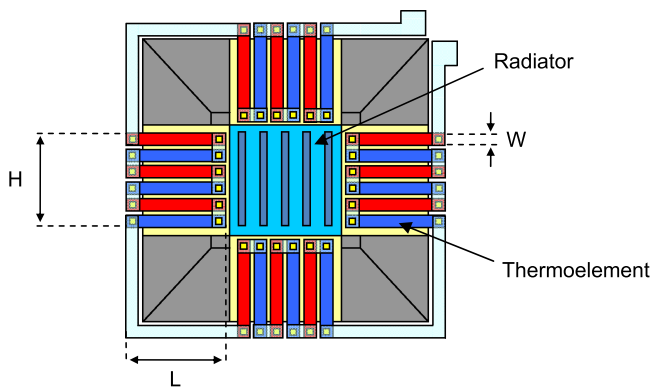
Figure 13. Top-view of top-down thermoelectric generator.

have to be decreased since for space limitations the maximum number of thermoelements in the device will be equal to 4 H/W. As a consequence, both N_{TE} and R_{TE} will be proportional to $1/W$, and, as per equation (1), P_{out} will turn out to be independent of W or, equivalently, of N_{TE}. Therefore, to a first approximation, the same maximum converted power is expected for equal devices which only differ in the number of series-connected thermocouples. This will not hold for the output voltage that, on the contrary, will be proportional to N_{TE}.

Conclusions

Two approaches for obtaining stacked Si-based NWs arrays of medium-high density have been presented. Both approaches make use of silicon technologies and compatible materials and processes. Specifically, such technologies are used to produce 3D architectures with suspended silicon membranes that offer areas of thermal contrast where to integrate nano-objects of thermoelectric relevance. Single crystalline and polycrystalline silicon nanowires of arbitrary length and with effective diameters below 100 nm have been successfully obtained so that phonon scattering phenomena will lead to high enough ZT values. Tens or hundreds of thousands of NWs readily connected can be obtained. In the first case considered, the top-down approach typical of silicon technology has been extended to define polysilicon stacked nanowires arrays from thin multilayers exploiting a smart sequential combination of thin film deposition and etch steps using only standard silicon materials. In the second case, a bottom-up approach has been used to obtain dense bundles of laterally oriented crystalline silicon nanowires across vertical silicon scaffolds, achieving parallel integration of large number of nanowires at a minimum technological cost. NWs densities attainable with both methods have been shown to be in line with the optimum range needed for maximizing TEG power output for typical NWs doping levels and expected thermal conductivities. Preliminary electrical parameters of the nanowires ensembles have been measured on-chip demonstrating that both approaches have led to successful integration. Next steps will involve the performance

characterization of both types of Si-based NWs arrangements into TEG devices. In both cases, the ultimate goal is the monolithic integration of all-silicon thermoelectric micro-nanogenerators that can be fabricated cost-effectively in large volumes with minimal material and technological complexity (avoiding for instance time-consuming nanolithography processes). Such micro-nanogenerators could be used as power sources for the deployment of autonomous microsensors where waste heat sources are present.

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