Ministero dello Sviluppo Economico

Ricevuta di presentazione

per

Brevetto per invenzione industriale

Domanda numero: 102016000109345

Data di presentazione: 28/10/2016

DATI IDENTIFICATIVI DEL DEPOSITO

Ruolo	Mandatario
Data di compilazione	28/10/2016
Titolo	Generatore termoelettrico integrato e relativo metodo di fabbricazione
Carattere domanda	Ordinaria
Esenzione	NO
Accessibilità al pubblico	NO
Numero rivendicazioni	9
Autorità depositaria	

RICHIEDENTE/I

Natura giuridica	Persona giuridica
Denominazione	Consorzio Delta Ti Research
Partita IVA	07407580963
Nazione sede legale	Italia
Tipo Società	consorzio con attivita' esterna

DOMICILIO ELETTIVO

Cognome/R.sociale	Società Italiana Brevetti S.p.A.
Indirizzo	via Carducci 8
CAP	20123
Comune	Milano
Telefono	02 - 806331
Fax	02 - 80633200
Indirizzo Email	milano@pec.sib.it
Indirizzo PEC	

Riferimento depositante	BI2713M

MANDATARI/RAPPRESENTANTI

Cognome	Nome
Bardini	Marco Luigi
Borrini	Stefano
Brazzini	Silvia
Concone	Emanuele Enrico Maria
De Benedetti	Jacopo
De Benedetti	Fabrizio
Di Giovine	Paolo
Germinario	Claudio
Manfrin	Marta
Montelatici	Linda Anna
Moscone	Francesca
Papa	Elisabetta
Pietri	Simona
Pizzoli	Antonio Mario
Predazzi	Valentina
Romano	Giuseppe
Soldatini	Andrea
Spina	Alessandro
Barbaro	Gaetano

INVENTORI

Cognome	Nome	Nazione residenza
IULIANELLA	Enrico	Italia
NARDUCCI	Dario	Italia
SPAZIANI	Fabio	Italia

MASCOLO	Danilo	Italia
BUOSCIOLO	Antonietta	Italia
LATESSA	Giuseppe	Italia
GISON	Italo	Italia

CLASSIFICAZIONI

Sezione	Classe	Sottoclasse	Gruppo	Sottogruppo
H	01	L		

NUMERO DOMANDE COLLEGATE

DOCUMENTAZIONE ALLEGATA

Tipo documento	Riserva	Documento
Disegni	NO	BI2713M-di.pdf.p7m hash: f7cce1d8333e3b15953a33e43c2776e8
Descrizione in inglese	NO	BI2713M-spe.pdf.p7m hash: 69ce914ba1f6cd0f4ceb01d93a38961d
Riassunto in Inglese	NO	BI2713M-abs.pdf.p7m hash: 86b1c81b55821c1a40a6b56c1b25cc43
Rivendicazioni in inglese	NO	BI2713M-clm.pdf.p7m hash: 6ce6835b5f7ade8aaf9fb6e8eb81efec
Descrizione in italiano*	SI	hash:
Riassunto	SI	hash:
Rivendicazioni	SI	hash:

RIFERIMENTO AL DEPOSITO DELL'INCARICO

Riferimento al deposito dell'incarico	802014000000662

INTEGRATED THERMOELECTRIC GENERATOR AND RELATED METHOD OF FABRICATION

TECHNICAL FIELD

This disclosure relates in general to solid state thermoelectric devices, in particular to
5 thermoelectric generators (TEGs) amenable to be fabricated with CMOS or BiCMOS technologies, and a related method of fabrication.

BACKGROUND OF THE INVENTION

Thermoelectric generators (TEGs) are earnestly investigated as low enthalpy waste heat exploitation devices of outstanding robustness, reliability and virtually unlimited service
10 life, besides being made of environmental friendly materials.

As power consumption of increasingly popular electronic devices is constantly minimized, TEGs begin to be considered as supplementary power source in conjunction or even in substitution of batteries or other energy storage devices like super-capacitors.

There is an increasing number of publications concerning thin film technology TEGs
15 exploiting well established processing techniques developed in the Microelectronics and Micro-Electro-Mechanical-Systems (MEMSs), like planar processing, micromachining implant and post implant treatments, flip-chip and bonding techniques and alike.

The doctorate thesis “Silicon-Micromachined Thermoelectric Generators for Power Generation from hot gas streams” by Israel Boniche, University of Florida, 2010, and
20 “Monolithic integration of VLS silicon nanowires into planar thermoelectric generators” by Diana Davila Pineda, Autonomous University of Barcelona, 2011, offer an extensive introductory review of state-of-the-art practices in the field of thermoelectric devices for solid state heat pumps and power generators.

The review encompasses also two families of TEGs manufactured with silicon-
25 compatible micro- and nano-technologies: in devices of a first family heat flow is parallel and in the other family orthogonally to the substrate. The architectures of these integrated TEGs generally comprise a number of elementary cells having n-p doped legs, arranged in such a way that the elementary cells are thermally in parallel and electrically in series.

30 Typically, integrated TEG devices in which heat flows parallel to the substrate may have conductive legs of thermoelectrically active materials deposited over a very high

thermal resistance material or a membrane, suspended several hundreds of micrometers above the substrate, or the legs of active materials themselves are free-standing [membrane-less].

Other relevant examples are reported in :

5 ▪ Huesgen, T.; Wois, P.; Kockmann, N. Design and fabrication of MEMS thermoelectric generators with high temperature efficiency. Sens. Actuators A 2008, 145–146, 423–429.

▪ Xie, J.; Lee, C.; Feng, H. Design, fabrication and characterization of CMOS MEMS-based thermoelectric power generators. J. Micromech. Syst. 2010, 19, 317–324.

10 ▪ Wang, Z.; Leonov, V.; Fiorini, P.; van Hoof, C. Realization of a wearable miniaturized thermoelectric generator for human body applications. Sens. Actuators A 2009, 156, 95–102.

▪ Wang, Z.; Fiorini, P.; Leonov, V.; van Hoof, C. Characterization and optimization of polycrystalline Si70%Ge30% for surface micromachined thermopiles

15 in human body applications. J. Micromech. Microeng. 2009, doi: 10.1088/0960-1317/19/9/094011.

▪ Su, J.; Leonov, V.; Goedbloed, M.; van Andel, Y.; de Nooijer, M.C.; Elfrink, R.; Wang, Z.; Vullers, R.J. A batch process micromachined thermoelectric energy harvester: Fabrication and characterization. J. Micromech. Microeng. 2010, doi:

20 10.1088/0960-1317/20/10/104005.

▪ Yang, S.M.; Lee, T.; Jeng, C.A. Development of a thermoelectric energy harvester with thermal isolation cavity by standard CMOS process. Sens. Actuators A 2009, 153, 244–250.

▪ Kao, P.-H.; Shih, P.-J.; Dai, C.-L.; Liu, M.-C. Fabrication and characterization

25 of CMOS-MEMS thermoelectric micro generators. Sensors 2010, 10, 1315–1325.

▪ Wang, Z.; van Andel, Y.; Jambunathan, M.; Leonov, V.; Elfrink, R.; Vullers, J.M. Characterization of a bulk-micromachined membraneless in-plane thermopile. J. Electron. Mater. 2011, 40, 499–503.13.

▪ Patent US 7,875,791 B1 “Method for manufacturing a thermopile on a

30 membrane and a membrane-less thermopile, the thermopile thus obtained and a thermoelectric generator comprising such thermopiles” Vladimir Leonov, Paolo Fiorini,

Chris Van Hoof (2011)

- Miniaturized thermopile on a membrane are also described by A. Jacquot, W.L. Liu, G. Chen, J.P. Flrial, A. Dauscher, B. Lenoir, in “Fabrication and Modeling of an in-plane thermoelectric micro-generator”, Proceedings ICT'02. 21st International Conference on Thermoelectrics, p. 561-564 (2002).

Other examples of parallel heat flow TEG structures rely on the ability of growing or defining populations of conductors (nanowires). The articles: “A. I. Hochbaum, R. K. Chen, R. D. Delgado, W. J. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. D. Yang, Nature 451, 163-U5 (2008)” and “A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. Goddard III, and J. R. Heath, Nature 451, 168-171 (2008)”; “F. Suriano, M. Ferri, F. Moscatelli, F. Mancarella, L. Belsito, S. Solmi, A. Roncaglia, S. Frabboni, G.C. Gazzadi, and D. Narducci, ‘Influence of Grain Size on the Thermoelectric Properties of Polycrystalline Silicon Nanowires’, Journal of Electronic Materials, 44 (2015) 371 (USA)” and “N. Neophytou, X. Zianni, M. Ferri, A. Roncaglia, G. F. Cerofolini, and D. Narducci, ‘Nanograin effects on the thermoelectric properties of poly-Si nanowires’, Journal of Electronic Materials, 42 (2013) 2393 (USA)”; WO2009/125317; EP1,083,610; WO2011/007241; WO2011/073142; offer a review of practices following such an approach.

US 7,875,791 B1 (by Leonov et al.) discloses thermopiles that may be supported by a membrane layer or that may be self-supporting. Despite the apparent easy manufacturability of these devices, heat is forced to move in a complicated structure with significant thermal losses. In addition, in some cases adhesive are needed in order to assure thermal contact to a heat source at the top or the bottom surface of the initial substrate. This results in poor thermal coupling at system level, lossy thermal paths and mechanical fragilities, all features that penalize performance of the thermopile.

A second family of TEG devices is often referred to as “out-of-plane” heat flux TEGs. They are characterized by the fact that heat flows orthogonally to the substrate. In these devices the thermoelectrically active materials are usually laid on or are part of high aspect-ratio supporting structures standing onto the substrate. Despite a more sophisticated and apparently expensive fabrication process, this configuration minimizes thermal losses, simplifies thermal coupling at system level enhancing overall

performance.

The “out-of-plane” heat flux TEGs are amenable to miniaturization and integration in microelectronic and optoelectronic devices, among other applications. Examples are reported by M. Strasser et al. in “Miniaturized Thermoelectric Generators Based on Poly-Si and Poly-SiGe Surface Micromachining”, (presented in The 11th International Conference on Solid-State Sensors and Actuators, Munich, Germany, June 10-14, 2001) and “Micromachined CMOS Thermoelectric Generators as On-Chip Power Supply” (presented in The 12th International Conference on Solid-State Sensors and Actuators and Microsystems, Boston, USA, June 8-12, 2003). Out-of-plane or orthogonal heat flux thin film structures are useful for innumerable applications, for example for micro power generation or for temperature management in complex integrated systems, for energy recovery or harvesting.

US2014/0246066 (Chen et al.), upon the teaching of which the preamble of claim 1 is drafted, discloses a thermoelectric energy harvester, shown in figure 1, having a plurality of P-type and N-type thermoelectric elements connected in series. The thermoelectric energy harvester may be formed with separated thermoelectric elements 610A, 610B realized on two different substrates 630 and 640 that may be mounted together.

Electric power yield from a given heat flow and electric power yield versus the footprint area of out-of-plane or orthogonal heat flux devices of the prior art, based on a common semiconductor or any material compatible with ICs fabrication processes, has to be enhanced. There is a need of more efficient and compact TEG that could be realized by means of a process fully compatible with standard CMOS or BiCMOS technologies.

SUMMARY

As in known devices, the generator of this disclosure has hill-top junction metal contacts and valley-bottom junction metal contacts joining juxtaposed ends of segments alternately p-doped and n-doped defined over inclined opposite flanks of hills and valleys of a dielectric material, useful for converting in electricity part of the heat flowing in a direction orthogonal to the planar generator, and a planar electrically non conductive cover layer laying onto the hill-top junction metal contacts and suspended above the valleys, that are void spaces delimited at the top by the non conductive cover

layer.

The present applicant has found an integrated thermoelectric generator of out-of-plane heat flux configuration that can be fabricated with a process fully compatible with standard front-end CMOS or BiCMOS technologies. According to this disclosure,
5 portions of the planar electrically non conductive cover layer above over the valleys have sufficiently large through holes to let isotropic etching solutions or etching plasma pass therethrough, across the thickness of the electrically non conductive cover layer (9), so as to realize void cavities by etching a sacrificial layer. The generator further comprises a top capping layer (11) deposited onto a free surface of said planar
10 electrically non conductive cover layer (9) so as to occlude the through holes (10) of the electrically non conductive cover layer (9).

A method of fabricating an integrated thermoelectric generator of out-of-plane heat flux configuration is also disclosed.

The claims as filed are integral part of this specification and are herein incorporated by
15 reference.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 depicts a prior thermoelectric energy harvester.

Figures 2 to 11 illustrate in succession the steps of a process of fabrication of a cell of an integrated thermoelectric generator according to this disclosure.

20 DETAILED DESCRIPTION

Figures from 2 to 11 illustrate the fabrication steps of a single cell of a thermoelectric generator of this disclosure. The depicted structure may be replicated identically over a silicon wafer to realize an integrated thermoelectric generator with a fabrication process fully compatible with CMOS and BiCMOS technologies.

25 With reference to figures from 2 to 11, a bottom substrate 1, that may be a silicon wafer, is used for fabricating thereon the integrated TEG of out-of-plane (orthogonal) heat flux type. Commercially available silicon wafers of any size may be used.

A dielectric base layer 2 of substantially uniform thickness (Fig. 2), that for example may be made of silicon dioxide, is grown or deposited by thermal oxidation or PECVD
30 deposition on the bottom substrate 1. By means of well established techniques, the dielectric base layer 2 is shaped in order to have an uneven thickness to define hills, in

correspondence of thicker portions, spaced by valleys 3, in correspondence of thinner portions of the dielectric layer 2.

The dielectric base layer 2 has a minimum thickness in correspondence of the valleys 3 sufficient to provide a necessary bottom electrical insulation without introducing a
5 significant thermal resistance. The height of the spaced hills generally may be comprised between 0,1 and 50 μm. The typical inclined flanks of hills define valleys 3 therebetween, the substantially planar bottom of which generally may have a width comprised between 0,1 and 100 μm, most preferably between 0.2 and 50 μm, similarly to the width of the top of the hills. The hills may be defined through a succession of
10 masking and etching steps in order to slant the walls of the progressively etched valleys 3 toward a substantially flat bottom by an angle of inclination from the base plane that preferably is comprised between 45 and 85 degrees.

Thin film segments 4 and 5 of thermoelectric (TE) materials are deposited over the hills and valleys 3 defined by the dielectric base layer 2. According to an embodiment, the
15 thin film segments 4 and 5 are made of p-doped and n-doped polycrystalline semiconductor material such as, for example, doped Si or SiGe. The segments 4 and 5, deposited in form of a thin film of substantially uniform thickness over the bottom dielectric 2 and the spaced hills, constitute the two legs of thermoelectric material that electrically connect a junction at the valley bottom to the two adjacent junctions on top
20 of the hills. In order to have a thermoelectric effect, the thin film segments may be deposited side to side to form junctions of different thermoelectric materials, as shown in figure 4, or, according to an alternative not shown in the enclosed figures, there may be a gap filled with metal between adjacent segments 4 and 5.

The hills material should have a low thermal conductivity, significantly lower than the
25 thermal conductivity of the material of the p-type and n-type segments of conductive material supported thereon, in order to further penalize by-pass paths of heat conduction flow alternative to the paths of productive heat conduction along the polycrystalline doped semiconductor thin film segments or legs defined over opposite slanted surfaces of the truncated rectangular pyramid shaped hills or of hills with a trapezoidal cross
30 section along one axis and straight sides or flanks orthogonal to it.

Examples of suitable materials of lower thermal conductivity than the thermal

conductivity of a thermoelectrically active polycrystalline semiconductor and their respective heat conduction coefficients are reported in the following table.

Material	Thickness[nm]	Thermal Conductivity [W m^{-1} K^{-1}]
Thermal SiO2	> 250	~ 1.2
SiO2 (PECVD@300C)	30 -50	0.82 ± 0.02
SiO2 (PECVD@300C)	90 -180	1.00 ± 0.10
SiO2 (PECVD@300C)	>200	~ 1.2 (Bulk)
SiNx (PECVD@300C)	20 -40	0.55 ± 0.05
SiNx (PECVD@300C)	60 -120	0.65 ± 0.05
SiNx (APCVD@900C)	180	~1.45

The deposited doped polycrystalline silicon layer of the segments 4 and 5 may have thickness, generally comprised between 10 and 1000 nm, but may even be as thick as
5 one or more micrometers, depending on contemplated applications, scaling of the elementary cell structure, properties of the polycrystalline semiconductor material used and design choices of the integrated TEG. The cold and hot junctions, respectively at valley bottoms and at hill-tops or vice versa, are both constituted by metal contacts of low aspect ratio, respectively 6 and 7, electrically connecting the ends of adjacent p-
10 doped segments 5 and of n-doped segments 4. The metal contacts 6 and 7 may be made, for example, of an Aluminum-Silicon alloy.

Differently from what is commonly hold true in the art, it is not mandatory to have adjacent p-doped segments 5 and of n-doped segments 4 separated by a gap filled with metal for avoiding formation of p-n junctions. The present applicant noticed that the
15 metal contacts 6 and 7, that must be realized for acting as hot and cold electrodes of the thermoelectric generator, are large enough to short-circuit the p-n junctions covering the whole depletion region, thus the junctions do not hinder current flow through the generator. Defining thermoelectric segments side by side may be convenient because the performances of the generator are not worsened, though the fabrication process is

relevantly simplified because it is not necessary an additional masking step for defining the gaps (to be filled with metal) between the segments 4 and 5.

The deposited metal layer of the junction metal contacts 6 and 7 that extend over and in electrical contact with the end portions of the two segments 4 and 5 of polycrystalline
5 semiconductor, may have a thickness ranging from about 0.1 to about 5 μm.

In order to increase thermal isolation among hill-top metal contacts 6, that will constitute either the hot or cold electrodes of the thermal generator, and valley-bottom metal contacts 7, that will constitute either the cold or hot electrodes, it is highly beneficial to seal the void valleys under vacuum. In order to close the void valleys 3
10 between the hills with a capping layer 11 (figure 11) using a fabrication process fully compatible with a front-end CMOS or BiCMOS fabrication technology, the steps illustrated in figures from 6 to 11 are performed.

A layer 8 of sacrificial material (figure 6), adapted to be isotropically etched with wet etching solutions or with an etching plasma, is deposited onto the structure of figure 5
15 so as to fill the valleys 3 and to bury the metal contacts 6 and 7 and the segments 4 and 5. This sacrificial material may be Silicon dioxide or a Carbon Based Material, deposited for example at a low temperature. The sacrificial layer 8 is then planarized (figure 7) so as to uncover an upper surface of the hill-top metal contacts 6, for example with a Chemical Mechanical Polishing (CMP) technique or with an etch back technique
20 or with a combination of the two.

An electrically non-conductive cover layer 9 is deposited (figure 8) onto the planarized free surface of the sacrificial layer 8 and onto the upper surfaces of the hill-top metal contacts 6. For example, the cover layer 9 may be made of Silicon nitride or Silicon dioxide deposited using a conventional low temperature PECVD technique. Then
25 portions of the electrically non conductive cover layer 9 are pierced in correspondence of the valleys so as to define holes 10 (figure 9) through its thickness, for example with standard photolithographic and dry etch steps. The holes 10 are sufficiently large to let isotropic etching solutions or etching plasma pass therethrough and are placed and shaped so as to efficiently remove the sacrificial layer 8 (figure 10) with either a wet
30 etching process, for example by flowing Hydrofluoric Acid vapor, or a dry etch process, for example using Oxygen plasma. When the whole sacrificial layer has been removed,

portions of the cover layer 9 are suspended above the void spaces in correspondence of the valleys 3.

Finally, a top capping layer 11 is deposited (figure 11), for example with a sputtering process, over the nonconductive layer 9 so as to occlude the through holes 10 of the non
5 conductive cover layer 9. Numerous materials may be used for this last step: preferably, a metal like Aluminum can be used for realizing a top capping layer 11 with both good electrical and thermal coupling.

Preferably, the bottom substrate 1 and the top capping layer 11, that will be placed in contact either with a hot or with a cold heat source, respectively, are subjected to a
10 thinning process, after device manufacturing, aiming to reduce heat losses between the substrate 1 or layer 11 and the junctions of thermoelectric segments 4 and 5. According to an embodiment, the thicknesses of the bottom substrate 1 and of the top capping layer 11 range respectively between 0.5 to 2.0 microns and 0.1 to 2 microns.

The void spaces in correspondence of the valleys 3 are permanently sealed during
15 packaging or back-end operations by occluding side gaps between the bottom substrate 1 and the non conductive cover layer 9, and are evacuated upon packaging.

The cell shown in figure 11 can be identically replicated numerous times over a silicon wafer and the corresponding hot and cold electrodes 6 and 7 can be electrically and thermally connected together to form hot and cold electrodes of a multi-cell
20 thermoelectric generator.

The thermoelectric generator of this disclosure has the following advantages:

- it can be fabricated with a CMOS or BiCMOS fully compatible process without using any bonding technique, such as flip chip or wafer to wafer technique;
- there is no risk of misalignment nor is necessary to use resins, as in bonding
25 techniques, that would increase thermal losses and thus would reduce the overall efficiency of the thermoelectric generator;
- vacuum inside the cavities allows to minimize heat losses.

CLAIMS

1. An integrated thermoelectric generator of out-of-plane heat flux configuration, said generator comprising:

a bottom substrate (1);

5 a dielectric layer (2) deposited onto a face of said bottom substrate (1) with uneven thickness, in order to define hills and valleys of dielectric material;

juxtaposed segments (4, 5), alternately p-doped and n-doped, of defined thin film lines of segments of a polycrystalline semiconductor, extending over inclined opposite flanks of said hills, useful for converting in electricity part of the heat flowing 10 in a direction orthogonal to the planar generator,

hill-top junction metal contacts (6) and valley-bottom junction metal contacts (7) joining juxtaposed ends of said segments (4, 5) alternately p-doped and n-doped,

a planar electrically non conductive cover layer (9) laying onto said hill-top junction metal contacts and suspended above said valleys, all valleys among said hills 15 (3) being void spaces delimited at the top by the non conductive cover layer (9),

characterized in that

portions of said planar electrically non conductive cover layer (9) suspended over each valley of said valleys have sufficiently large through holes (10) to let isotropic etching solutions or etching plasma pass therethrough, across the thickness of the 20 electrically non conductive cover layer (9);

said generator further comprises a top capping layer (11) deposited onto a free surface of said planar electrically non conductive cover layer (9) so as to occlude the through holes (10) of the electrically non conductive cover layer (9).

2. The thermoelectric generator of claim 1, wherein said void spaces are 25 permanently sealed during packaging or back-end operations by occluding side gaps between the bottom substrate (1) and said electrically non conductive cover layer (9).

3. The thermoelectric generator of claim 1 or 2, wherein said void spaces are evacuated upon packaging.

4. The thermoelectric generator of one of claims from 1 to 3, wherein said p-doped 30 and n-doped segments (4, 5) are joined together in an alternated fashion to form p-n junctions, each of said hill-top junction metal contacts (6) and valley-bottom junction

metal contacts (7) being disposed to short-circuit a respective one of said p-n junctions.

5. The thermoelectric generator of one of claims from 1 to 4, wherein said topmost capping layer (11) is a metal layer.

6. The thermoelectric generator of claim 1, wherein said n-doped and p-doped thin film segments (4, 5) are made of polycrystalline silicon.

7. The thermoelectric generator of claim 1, wherein said hills (3) are regularly spaced and have a truncated rectangular pyramid shape or a trapezoidal cross section along one axis and straight sides or flanks orthogonal to it.

8. A method of fabricating an integrated thermoelectric generator of out-of-plane heat flux configuration, comprising the following steps:

depositing a dielectric layer (2) with uneven thickness onto a face of a bottom substrate (1) in order to define hills and valleys of dielectric material,

depositing juxtaposed segments (4, 5), alternately p-doped and n-doped, of defined thin film lines of segments of a polycrystalline semiconductor extending over inclined opposite flanks of said hills,

depositing hill-top junction metal contacts (6) and valley-bottom junction metal contacts (7) joining juxtaposed ends of said segments (4, 5) alternately p-doped and n-doped,

depositing a layer of sacrificial material (8) in order to fill said valleys and to cover said juxtaposed segments (4, 5), leaving uncovered only upper surfaces of said hill-top junction metal contacts (6),

depositing a planar electrically non conductive cover layer (9) laying onto said hill-top junction metal contacts,

characterized in that the method is fully compatible with a front-end CMOS or BiCMOS fabrication technology, and further comprises the steps of:

realizing sufficiently large through holes (10) to let isotropic etching solutions or etching plasma pass therethrough, across the thickness of the electrically non conductive cover layer (9);

removing said sacrificial material (8) by injecting an isotropic etching solution or an etching plasma throughout said holes (10), in order to make the planar electrically non conductive cover layer (9) lay onto said hill-top junction metal contacts and be

suspended above said valleys, all valleys among said hills (3) being void spaces delimited at the top by the electrically non conductive cover layer (9);

depositing a top capping layer (11) onto a free surface of said planar electrically non conductive cover layer (9) so as to occlude the through holes (10) of the electrically
5 non conductive cover layer (9).

9. The method of claim 8, further comprising the steps of:

evacuating said void spaces upon packaging;

sealing permanently said void spaces during packaging or back-end operations by occluding side gaps between the bottom substrate (1) and said electrically non
10 conductive cover layer (9).

ABSTRACT

An integrated thermoelectric generator of out-of-plane heat flux configuration can be fabricated with a process fully compatible with standard front-end CMOS or BiCMOS
5 technologies, if portions of the planar electrically non conductive cover layer suspended over the valleys have sufficiently large through holes to let isotropic etching solutions or etching plasma pass therethrough, across the thickness of the non conductive cover layer (9), so as to realize void cavities. The generator further comprises a top capping layer (11) deposited onto a free surface of said planar electrically non conductive cover
10 layer (9) so as to occlude the through holes (10) of the non conductive cover layer (9).
A method of fabricating an integrated thermoelectric generator of out-of-plane heat flux configuration is also disclosed.

15 [Fig. 11]

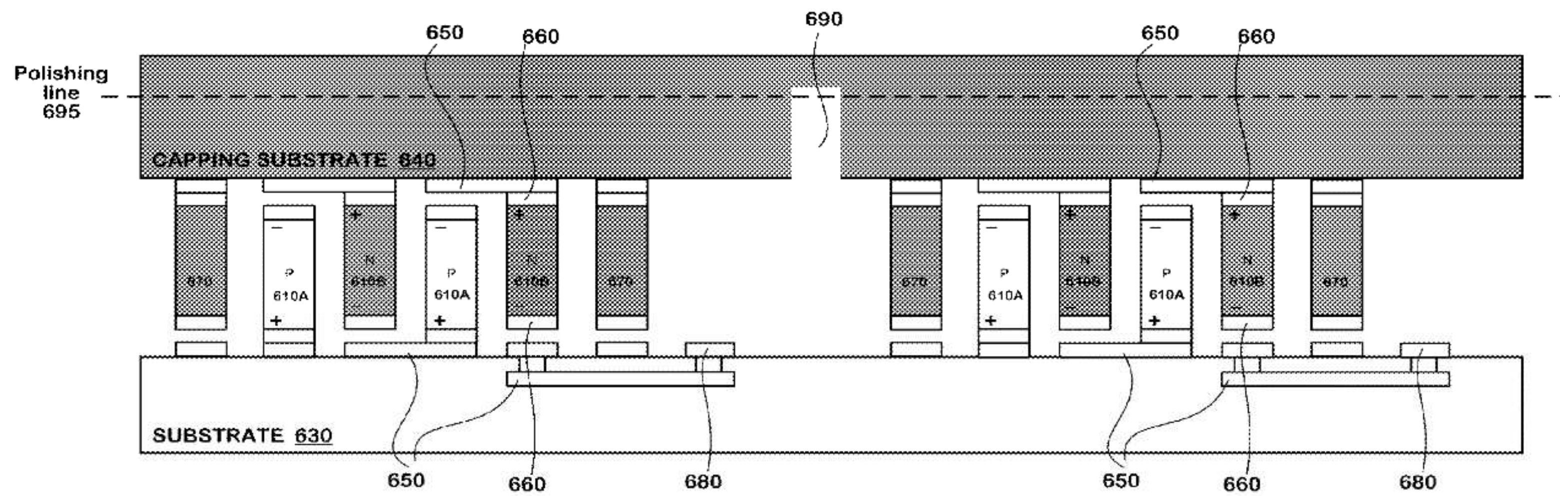

FIG. 1

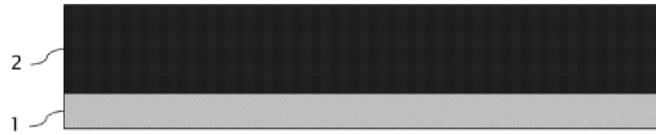

FIG. 2

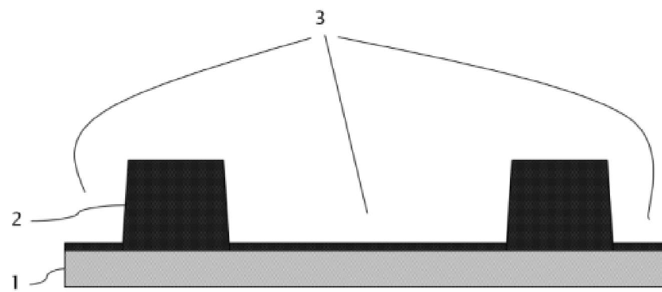

FIG. 3

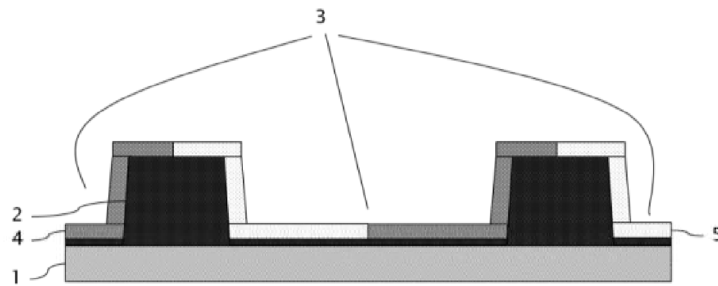

FIG. 4

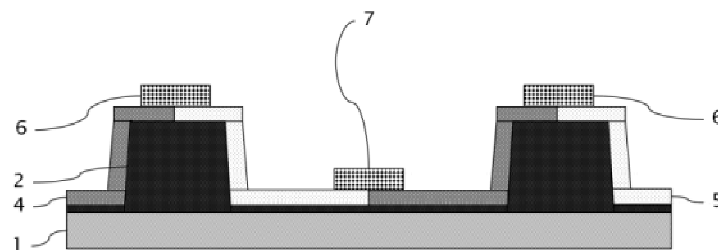

FIG. 5

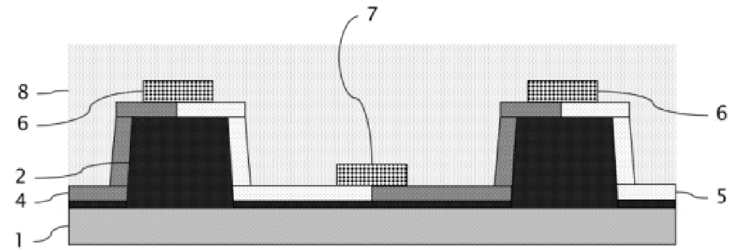

FIG. 6

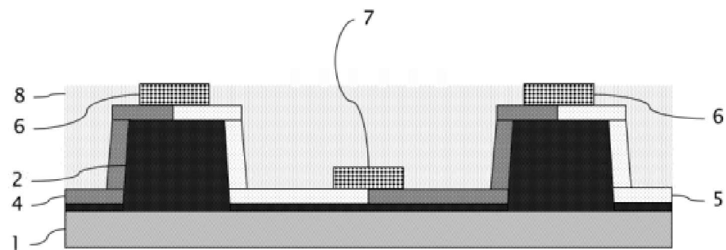

FIG. 7

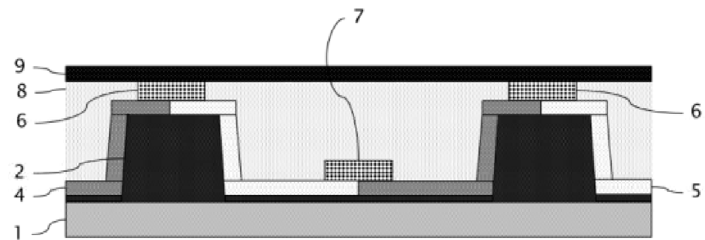

FIG. 8

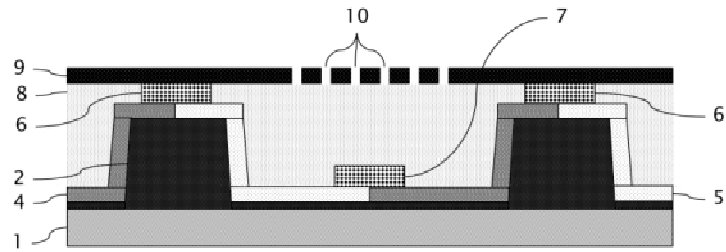

FIG. 9

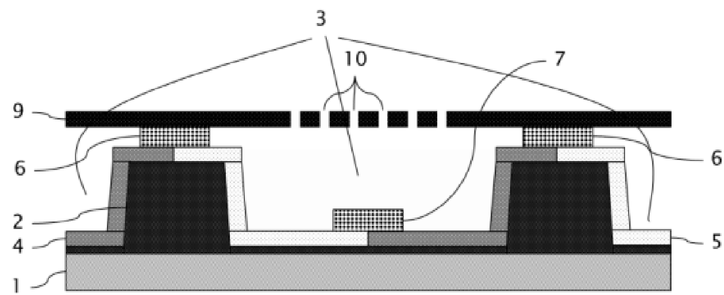

FIG. 10

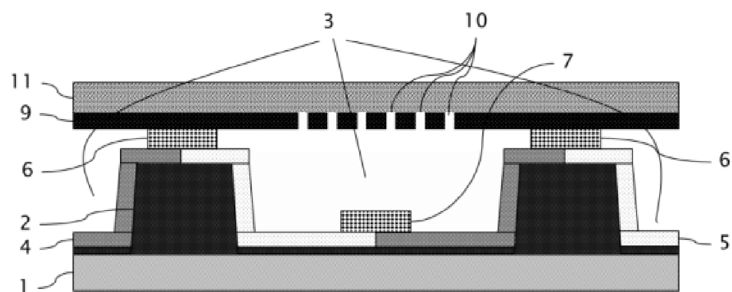

FIG. 11