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# Design and Development of an Integrated Readout System for the Triple-GEM Detector

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# Preface

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# Introduction

## 1.1 Background and Motivations

In the wide world of particle detectors, gaseous ionization chambers are largely used due to their ability to make energy measurements and to discriminate various types of radiation. In last years a particular topology has emerged, named GEM (Gas Electron Multiplier) [1], developed at Gas Detector Development Group at CERN (European Organization for Nuclear Research) in 1997.
This detector has several advantages with respect to multi-wire proportional chambers, employed for similar applications. First of all, the manufacturing costs are much lower and, in principle, wide area GEM detectors are suitable for mass production. Instead, typical multi-wire chambers are very difficult to be assembled and more expensive, compared to GEMs. In addition, GEM detectors feature the capability to suppress positive ions, one of the most effective limiting factor in counting rate performance for this class of detectors.
On the other side this enhancement in the counting rate requires fast front-end electronics, enabling integrated circuit solutions.
Among the several advantages concerning GEM detectors design features, one of the key factors is that they can be easily built in different shapes and volumes. Standard fabrication techniques (such as lithography) has strongly increased the possible applications, reducing costs, and possibly improving the interfacing with CMOS integrated circuits.
Taking into account these aspects, several high-energy physics experiments exploit these detectors, especially for beam monitoring. One of the earlier employments was the COMPASS experiment at CERN [2], aiming at the study of hadronic structure and spectroscopy with high intensity muon and hadron beams, where GEMs were used as trackers.
Furthermore, they have been employed as neutron detectors with a Charge-Coupled Device (CCD) front-end system [3], within a radiographic system [4], as an X-Ray polarimeter [5] for astrophysics measurements, in ultra-fast soft X-Ray plasma diagnostics [6] and as a new-type photo-multiplier [7]. In addition to physics experiments, this detector has the great potentiality to be included in biomedical instrumentation, especially for diagnostics and monitoring [8].
The research in GEM detectors is pushing towards two mutual research branches.
The first regards the detector physical/structure optimization, especially in the materials choice, in order to increase the signal gain, resolution and the count rate.
This brings to new architectures, including new gas mixtures and shape choices. A recent evolution has been named the Triple-GEM, realized at LNF (Laboratori Nazionali

di Frascati) in Italy [9][10]. It consists in cascading three GEM foils in order to boost the detector signal gain. Furthermore, a particular mixture of gases ($Ar/CO_2/CF_4$ 45/15/40) improves time resolution.
The second research branch is devoted to improve the front-end performance, using dedicated CMOS integrated solutions, suitable to sustain overall count rate (about $10^6$ counts-per-second [10]), while reducing power consumption, and increasing system portability. In particular, the front-end here proposed allows to reduce power with respect to several circuits present in literature [11], enabling the possibility to include and optimize several input channels in the same silicon area (chip).
In the Triple-GEM readout system, an existent front-end has been adapted from other applications; this is the case of the CARIOCA [12], originally developed for Charge-Coupled Devices (CCDs) and included in a primary version of the Triple-GEM. But the limited count-rate and the relatively high power consumption has made the necessity of a dedicated readout system very real.
As a solution, the development of an ASIC (Application Specific Integrated Circuit) can afford several advantages with respect to other common solutions, i.e. PCBs [13]. In fact, the ultimate aim is the inclusion of a digital-based data elaboration in the front-end, greatly increasing performance and at the same time reducing the overall readout system complexity. Indeed, this fact can limit the inclusion of off-chip devices like FPGAs or standard micro-controllers.
Then, silicon implementation allows very dedicated circuital/system-level choices, optimizing overall readout performance while facing several project design issues, like large detector input parasitic capacitance and relatively low sensitivity.

## 1.2 The GEM Detector

The detector for which the ASIC has been designed is the Gas Electron Multiplier (GEM), and belongs to the wide family of proportional counters. Provided that a more detailed description of the detector itself is not the main goal of this work, here a general overview of the device will be given.
A typical GEM is made by a 50 µm thick kapton foil, with a copper clad on each side, perforated with a high-surface density of bi-conical channels. This foil is immersed in a particular mixture of gases. In figure 1.1 a SEM image of the foil is shown.
It can be realized in various geometrical configurations and also in great sizes. It's been introduced for particle detection recently [1], and this is one of the more active object of innovation in this field. Due to this, the development of a more dedicated front-end system is interesting, and in last years some configurations have emerged and will be explained in the next chapter.
The GEM can be used for different families of particle detection, such as neutrons, muons, electrons or gamma rays, with very few modifications to the basic structure (e.g. adding a conversion cathode for uncharge particles).

### 1.2.1 Basic principles of functioning

The main process of signal generation inside the detector is the same of a typical gas ionization chamber. In fact, a charged particle entering the active volume, if energy

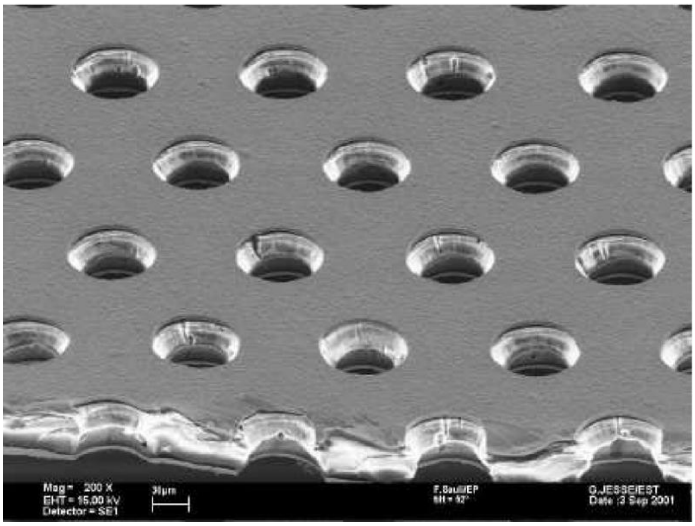


Figure 1.1: SEM image of the GEM foil (from CERN GDD Group)

constraints are respected, ionizes an atom of the gas and creates an electron-ion pair. In presence of an electric field, this two carriers will tend to move towards the anode and cathode respectively. If the intensity of this electric field is high enough to overcome a specific threshold, the kinetic energy of the electrons will increase up to ionize an other atom, creating other active carriers. Thus, a greater signal will be produced at the anode, although keeping the proportionality between deposited energy and the amount of charge at the anode. This fact enables the possibility to make a spectroscopic analysis of the incident particles.
The great innovation of the GEM is that the high electric field necessary to multiply the carriers is generated in the foil channels (typically with a 70 µm diameter) by applying a bias voltage between each of the two copper clads. Therefore, a lower bias can be applied in order to obtain the same electric field intensity of conventional proportional detectors (approximately 10 MV/m). Into channels, as a consequence, an electric field similar to that shown in figure 1.2 will establish.
It's in this region that the multiplication process takes place. In a typical configuration, each foil has a multiplication factor in the order of 20. In order to achieve further signal amplification, more GEM foils can be added to the chamber (three foils, as shown in figure 1.3, reach a 8000 multiplication factor).
Other key advantages in employing GEM detectors are the possibility to get information about the position of particle interaction as a consequence of this structure, and to make time-of-flight measures thanks to its very little characteristic time of detection. The enhanced adaptivity of the GEM is the key of its success in particle detection employment; it can be tuned for several applications changing its geometrical configuration or the materials of its components.
A typical complete configuration is shown in figure 1.4.

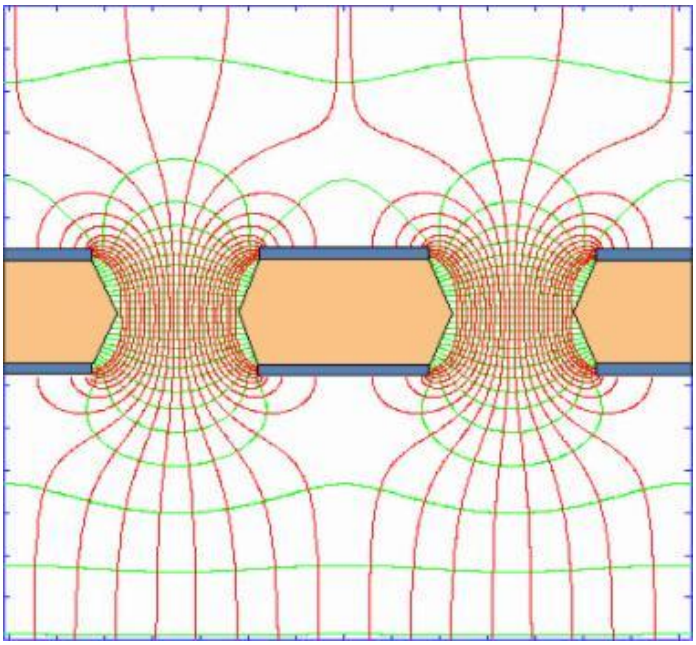

Figure 1.2: Electric field lines in a GEM (from CERN GDD Group)

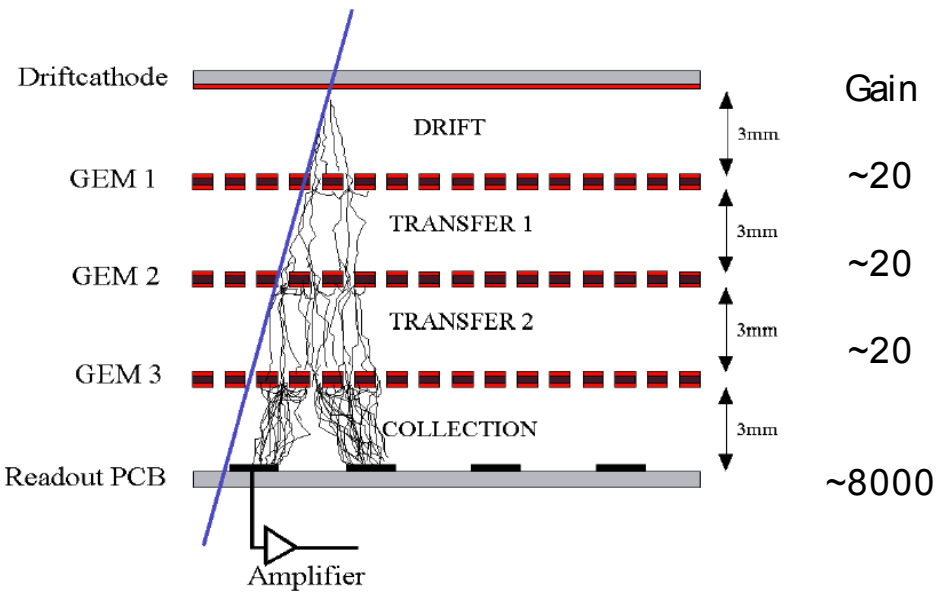


Figure 1.3: Structure and gain of a GEM (courtesy of F. Murtas)

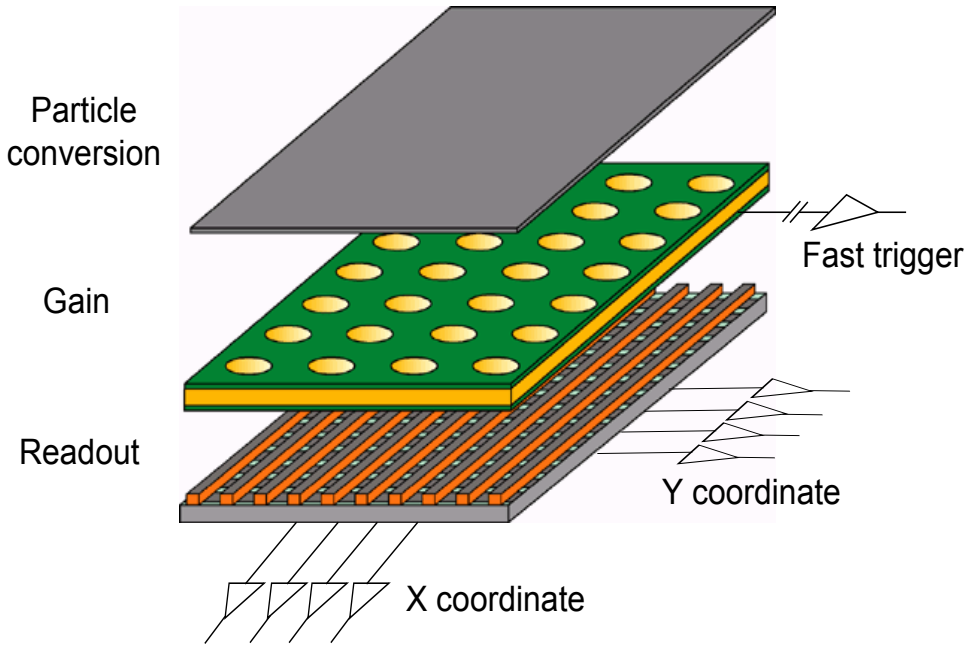


Figure 1.4: GEM typical configuration (courtesy of F. Murtas)

### 1.2.2 Recent Developments: BANDGEM

New high count rate detectors are needed for future spallation neutron sources where large areas (several $m^2$) and high efficiency ($> 50\%$) detectors are envisaged.
In this framework, GEM is one of the explored detector technologies since they feature good spatial resolution ($< 0.5$ cm) and timing properties, have excellent rate capability ($MHz/mm^2$) and can cover large areas (some $m^2$) at low cost.
Thus, the BANDGEM (Boron Array Neutron Detector) approach (Figure 1.5), a 3D geometry for the neutron converter cathode, was developed expecting to provide an efficiency $> 20\%$ in the wavelength range of interest for Small-Angle-Neutron-Scattering instruments.
A system of thin lamellas (250 µm) of dielectric material coated with 1 µm layer of $^{10}B_4C$ has been built and positioned in the first detector gap, orthogonally to the cathode.
By tilting the lamellas system with respect to the beam, there is a significant increase of effective thickness of the borated material crossed by the neutrons. As a consequence, both interaction probability and detection efficiency are increased.
This detector is aiming to replace $^3$He tubes for neutron detection. In fact, although their performance (in particular the high energy resolution and the high efficiency in charge collection), the availability of $^3$He has become prohibitive, with extremely high costs, together with the bulky structure of the detector itself.

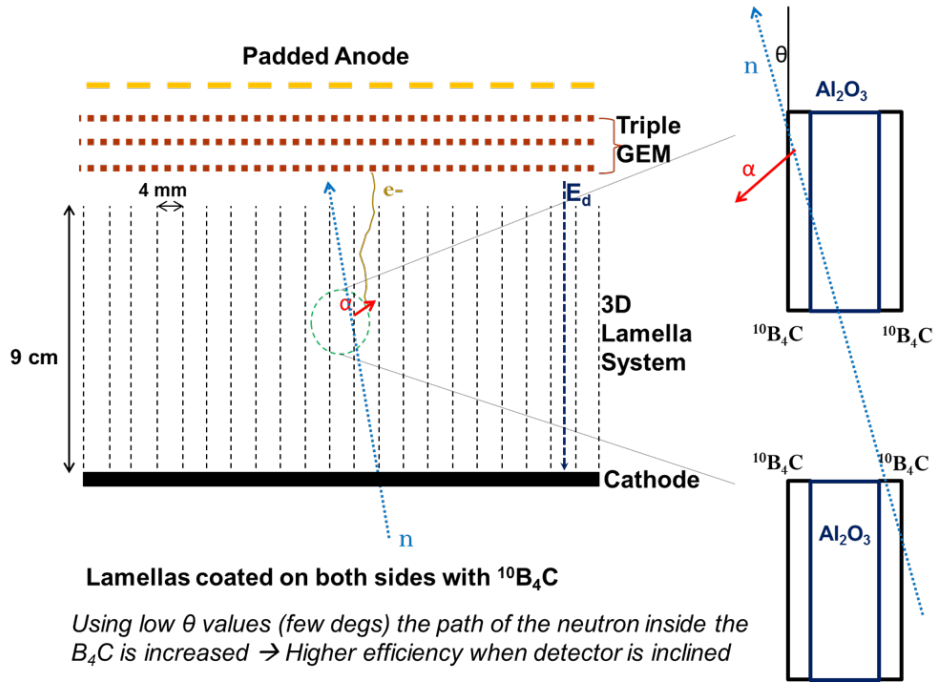


Figure 1.5: The BANDGEM configuration (courtesy of G. Croci)

## 1.3 The State-of-the-Art on Readout Electronics

One of the most commonly used ASIC for GEM detector readout is the CARIOCA (CERN And RIO Current-mode Amplifier), which is an octal amplifier shaper discriminator with baseline restoration, dedicated to Multi Wire Proportional Chambers (MWPC), and later re-adapted for GEM detectors [12]. It is developed in 250 nm CMOS technology, that operates at 2.5 V. The CARIOCA amplifier is developed in the current-mode approach, that is attractive for fast circuits. The chip has to amplify, shape and discriminate the current signal induced on the wire chamber electrodes. Another recent development is the GASTONE64 chip [14]. The GASTONE64 (GEM Amplifier Shaper Tracking ON Events) is a low-noise low-power mixed-signal ASIC designed to host 64 channels to readout a cylindrical GEM detector. Each channel is made of a charge sensitive preamplifier, a shaper, a discriminator and a monostable. Digital output data are transmitted via serial interface at 100 Mbit/s data rate. The chip has been designed in 350 nm CMOS process.

# Part II

# GEMMA Prototype

# 2
# Front-End

The block scheme of the GEMMA front-end channel is presented in figure 2.1. It consists of three main blocks, that is the charge sensitive preamplifier, the charge-time conversion block and the calibration/control block. The front-end in figure 2.1 has been designed specifically for negative charged particles. Its ultimate aim is to measure the arrival time (Event-Detection-Signal, EDS) and the amount of charge generated by the GEM detector (Charge-Time-Signal, CTS).

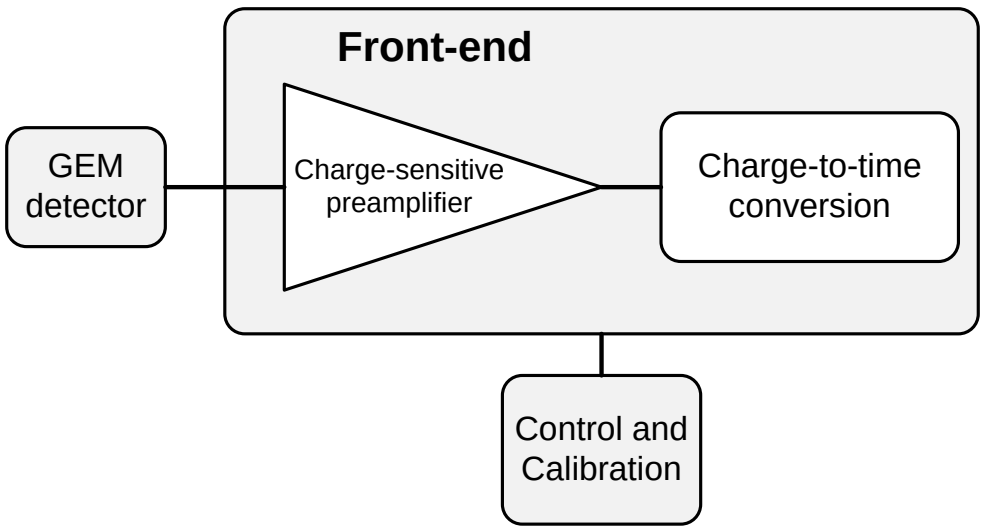


Figure 2.1: GEM detector front-end, block scheme

## 2.1 GEM Detector signal modeling

The input charge time-duration enters into a 30 ns up to 100 ns range [12]. The input pulse shaping is reported in figure 2.2, and it has been considered to feature different rise and fall time, respectively as 1/3 and 2/3 of the total time duration [10]. The input charge can assume values from 30 fC, corresponding to a MIP (Minimum Ionization Particle), up to 1 pC.

## 2.2 GEMMA Signals

With reference to figure 2.3, EDS is available when an input charge higher than 30 fC is detected by the front-end. This signal is generated by a comparator, named for clearance *EDS-Comp*. This signal has to be generated within a 30 ns time interval after

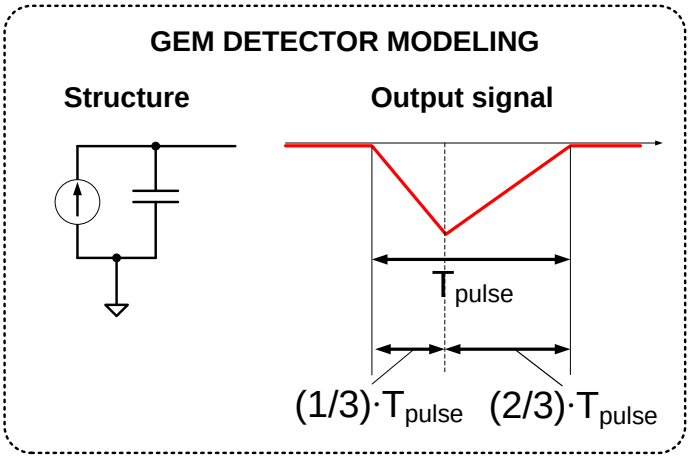


Figure 2.2: GEM detector modeling

the 0 time in figure 2.3.

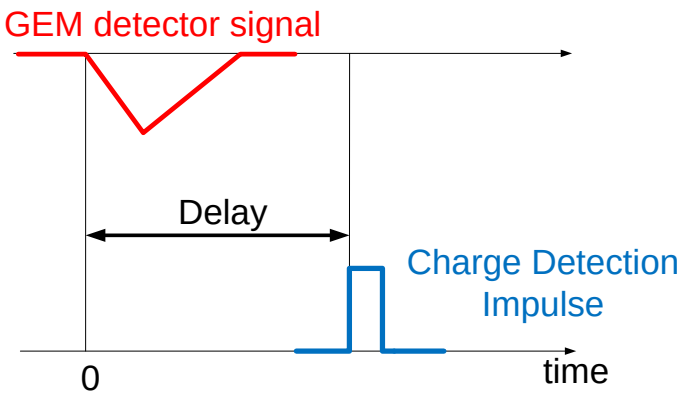


Figure 2.3: Event detection impulse (EDS) diagram

Contemporaneously with the EDS impulse, the preamplifier starts to integrate the GEM signal, and the CTS measure starts, as the output of another comparator named *CTS-Comp*. After 100 ns, a negative constant-slope ramp starts and the output of the CTS-Comp remains high until the preamplifier output voltage crosses the ramp. The produced pulse, shown in figure 2.4, contains information about the amount of charge at the front-end input, because its time duration is directly proportional to the input detector charge.

## 2.3 Detection Chain

The signal coming from GEM detector goes through the Charge-Sensitive Preamplifier (CSP), composed by a passive feedback net $C_F$-$R_F$, the reset switch SWfb, and the single-ended Opamp, shown in figure 2.5. $R_F$ (set very high, about 1 MΩ maintains

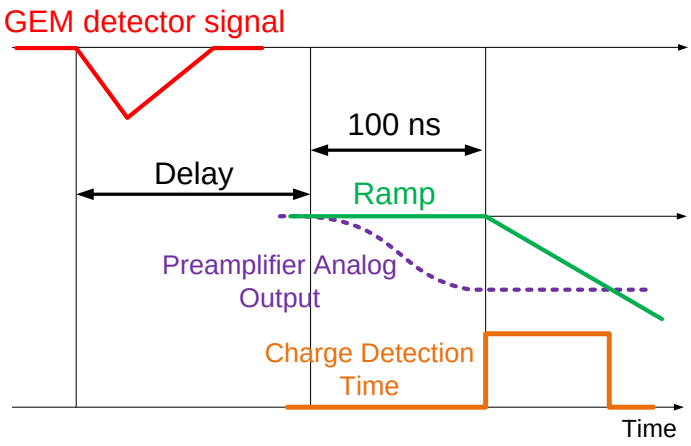


Figure 2.4: CTS diagram

the Opamp input/output operating point. By closing SWfb it is possible to discharge the $C_F$ capacitor and restore the common-mode voltage at the opamp input/output node. Such reset operation is required every time a EDS pulse occurs, and once the CTS signal is available.

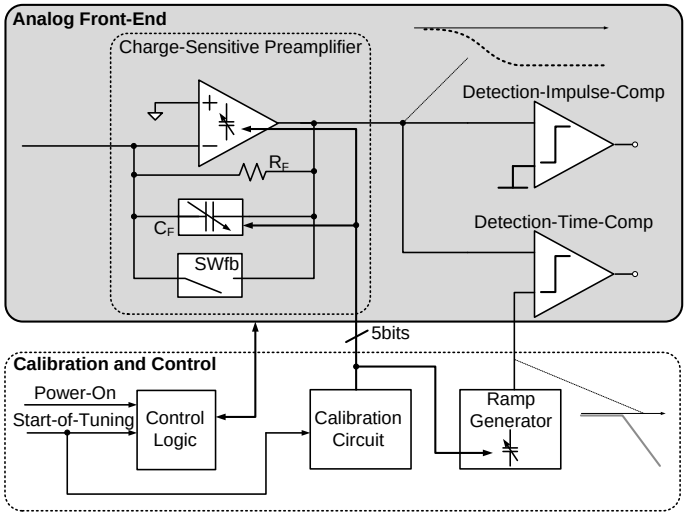


Figure 2.5: GEMMA Front-end complete scheme

Basically the front-end here presented is able to perform a charge vs. time conversion. The ramp signal for voltage vs. time conversion is generated by a proper Ramp-Generator circuit, whose implementation is based on a constant current charging a capacitor during a fixed time. A very precise external current has to be provided, while variable capacitors are tuned by the calibration circuit (explained in detail in

section 2.5) in order to guarantee a very precise ramp signal, within a $\pm$ 5% tolerance.

## 2.4 Front-end Design: Charge Sensitive Preamplifier

### 2.4.1 Operational Amplifier

Due to the virtual ground principle at the Operational Amplifier input, GEM detector parasitic capacitance does not affect significantly the charge-to-voltage conversion, implemented by the CSP. For this reason system-level analysis has demonstrated at least 60 dB of DC-gain are needed for Operational Amplifier in figure 2.5.
Moreover, taking into account a possible DC-gain drop, due to PVT and aging, 70 dB DC-gain has been required. Since rising time should be about 1/3 of the input signal total time duration (100 ns), output slew-rate for the Operational Amplifier is about 16.6 V/µs. At the same time for Equivalent-Noise-Charge (ENC) performance, Input-Referred-Noise (evaluated as spot noise on the middle of preamplifier bandwidth) should be lower than 10 nV/$\sqrt{Hz}$. Unity gain bandwidth requirements are then fixed by rise/fall time. A resume of the most important Op-Amp requirements is reported in table 2.1. Notice that for stability reasons at least a 60° Phase Margin is required.

| **Parameter** | Value |
|---|---|
| DC-gain ($A_0$) | $>$ 70 dB |
| Unity-Gain-Bandwidth (UGB) | $>$ 120 MHz |
| Input-Referred-Noise (IRN) | $<$ 10 nV/$\sqrt{Hz}$ |
| Phase Margin | $>$ 60° |
| External Slew-Rate | $>$ 16.6 V/µs |

Table 2.1: Operational Amplifier requirements

The charge-sensitive preamplifier should be designed with a very high open loop gain in order to obtain a very low input impedance. The solution adopted in this work is a 3-stage Op-Amp with Nested Miller Feed-Forward compensation technique [15]. In particular, 70 dB DC-gain and 120 MHz minimum unity gain bandwidth requirements make the Op-Amp design very challenging. Single Miller compensation is here not sufficient, because three gain stages are needed to perform the minimum required DC-gain of 70 dB. Feed-Forward compensation appears the most reasonable solution, in order to guarantee stability (at the cost of smaller power increasing due to the feed-forward path, see figure 2.6).

## 2.5 Front-end Design: Calibration Circuit

### 2.5.1 Calibration circuit general description

The CMOS integration process, due to its nature, brings to a statistical variation of all parameters involved in a circuit [16]. These parameters are related to transistors, resistors, capacitors, and also the silicon wafer. These variations are particularly relevant, and the designer has to take them into consideration because they affect the

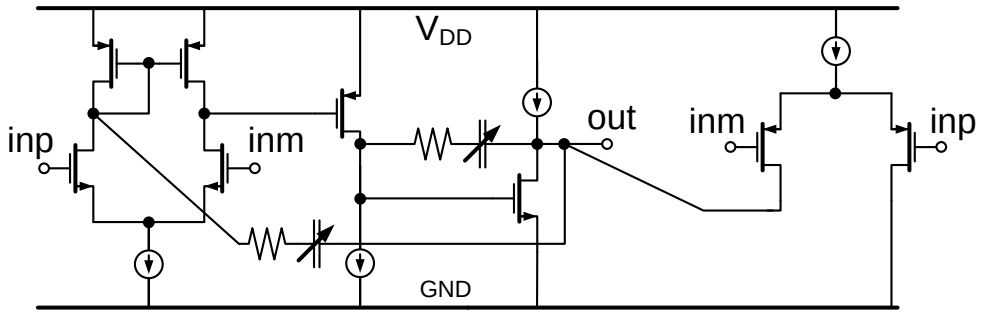


Figure 2.6: Operational Amplifier schematic

global performance.
In detail, this project bases its functioning on capacitors, included in the preamplifier as feedback capacitor and Miller compensation capacitors.
It has been demonstrated that the capacitors mean standard variation due to the integration process can reach 40% w.r.t. the nominal value [17]. This fact can affect seriously the front-end performance.
In this design indeed, the requested precision of capacitance values is 5%. This fact is due to three critical points. The first two regard the preamplifier feedback capacitor ($C_F$) value, included into the integration constant, and responsible of the loop gain, and so of the Op-Amp phase margin. The third, linked to the Miller compensation capacitor values, is responsible of the preamplifier Op-Amp stability.
The solution to this issue consists in designing an automatic calibration circuit, which tunes the capacitors value directly on-chip and automatically, including only a precise current reference (given as a chip input) and a stable clock signal.
The calibration algorithm is made by three main steps: sensing, calibration and convergence.

**Sensing**

The sensing procedure is started at the algorithm beginning. It consists in evaluating the effective capacitance implemented value. Namely, the sensing is made by generating a linear descending ramp into a determined time interval, established in multiples of the clock signal cycles. Indeed, assuming

$$\mathrm{I} = \frac{\Delta \mathrm{Q}}{\Delta \mathrm{t}} = \mathrm{cost.} \tag{2.1}$$

hence

$$\Delta \mathrm{Q} = \mathrm{C} \cdot \Delta \mathrm{V} \Longrightarrow \frac{\Delta \mathrm{V}}{\Delta \mathrm{t}} = \frac{\mathrm{I}}{\mathrm{C}} \tag{2.2}$$

So, a fixed constant current charging a capacitor in a determined interval of time will produce a precise bias voltage. The produced ramp is shown in figure 2.7.
The sensing procedure will be made in the SET phase. Reference bias values, time duration and clock frequency have been chosen according to a MATLAB® simulation.

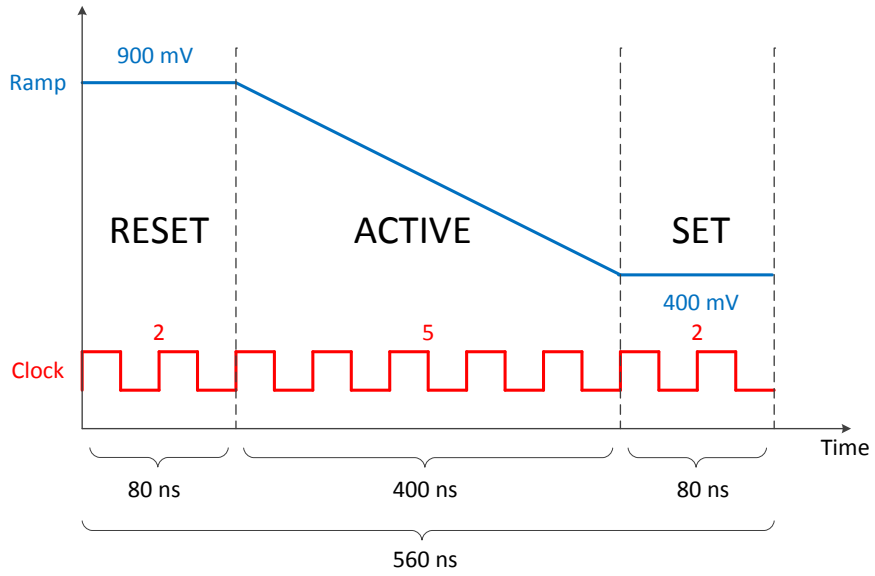


Figure 2.7: The calibration ramp in nominal conditions

In equation 2.2, once fixed the starting bias level, the nominal capacitor value and the charging current (respectively 900 mV, 1.8 pF and 2.25 µA), it is possible to calculate the clock frequency or the arriving bias voltage. In fact the ramp duration has to be a multiple of clock signal, because all the analysis is made digitally. Here a 5 times the clock period ramp time has been chosen. With a 12.5 MHz clock, the ramp lasts 400 µs and reaches a 400 mV bias.

**Calibration**

The basic concept behind its logic is the checking of resulting ramp bias and to make the capacitance value to change accordingly. So, a binary-weighted digital programmable capacitor array has been implemented, which allows to select a specific value with a digital word. The calibration precision so will depend on the number of implemented capacitors, acting as bits.
Let be $C_{nom}$ the nominal value of the capacitance, $N$ the number of array bits, $\Delta C$ the maximum relative variation of the capacitance value due to integration technology. Therefore, the possible combinations of the capacitance value are $2^N$. The minimum value $C_{min}$ and the maximum $C_{max}$ will be

$$\mathrm{C_{min}} = \mathrm{C_{nom}} \cdot (1 - \Delta \mathrm{C}) \tag{2.3}$$

$$\mathrm{C_{max}} = \mathrm{C_{nom}} \cdot (1 + \Delta \mathrm{C}) \tag{2.4}$$

Hence, the difference between two consecutive values and so the maximum error $\epsilon$ with respect to the nominal value is simply

$$\epsilon = \frac{\mathrm{C_{max}} - \mathrm{C_{min}}}{2^{\mathrm{N}}} = \frac{2 \cdot \Delta \mathrm{C}}{2^{\mathrm{N}}} = \frac{\Delta \mathrm{C}}{2^{\mathrm{N}-1}} \tag{2.5}$$

Once the capacitance value maximum variation is known, fixing the number of bits corresponds to fix the maximum error.
After that, following the calculations made in equations 2.3 to 2.5 and the maximum variation of the capacitance fixed ($\Delta C$ in equation 2.5), the MATLAB® program calculates the offset capacitor of the array as $C_{min}$ and makes a relation between the bit code and the value of capacitance in the array. Choosing the bit code corresponding to nominal capacitance, named $N_{init}$, the program calculates also the two thresholds for the comparators, respectively $V_{th_H}$ and $V_{th_L}$ as follows:

$$V_{th_L} = V_{reset} - \frac{T_{charge} \cdot I_{ref}}{C(N_{init})} \tag{2.6}$$

$$V_{th_H} = V_{reset} - \frac{T_{charge} \cdot I_{ref}}{C(N_{init} + 1)} \tag{2.7}$$

**Convergence**

The setting of array bits changes until the bias variation in a determined number of clock cycles is into the desired window, as shown in figure 2.8.

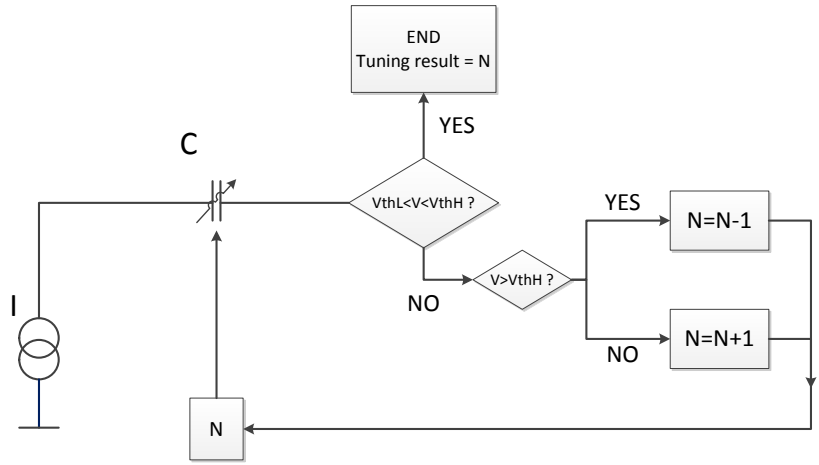


Figure 2.8: Algorithm of the tuning process

In figure 2.9 the digital word vs. capacitance relation is shown in the nominal case, and in the case of 20% positive and negative variation due to the integration process. In figure 2.10 the MATLAB® simulation results are shown, including a simulated convergence in the case of -20% capacitance variation (the second plot).

**Schematic choice**

The tuning machine, as shown in figure 2.11, is composed by two main blocks: the analog ramp generator and the digital controller.
Inside the first block, a constant current charges a digital programmed array of N capacitors put in feedback of an operational amplifier. So, by opportune clock phases generated by the digital part, a series of switches generate a ramp signal. This

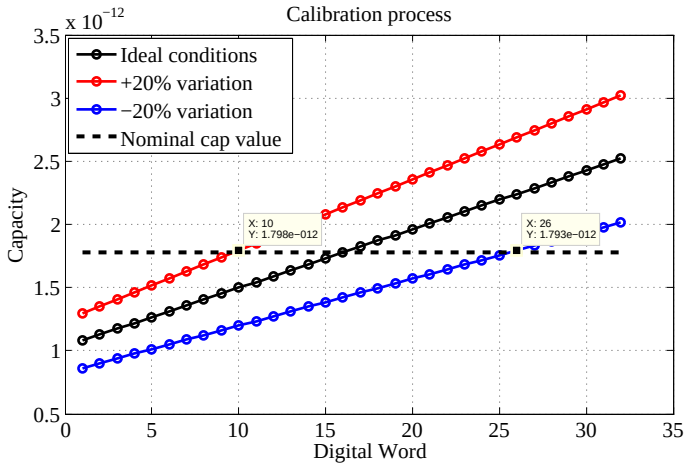


Figure 2.9: The capacitor values related to the digital words

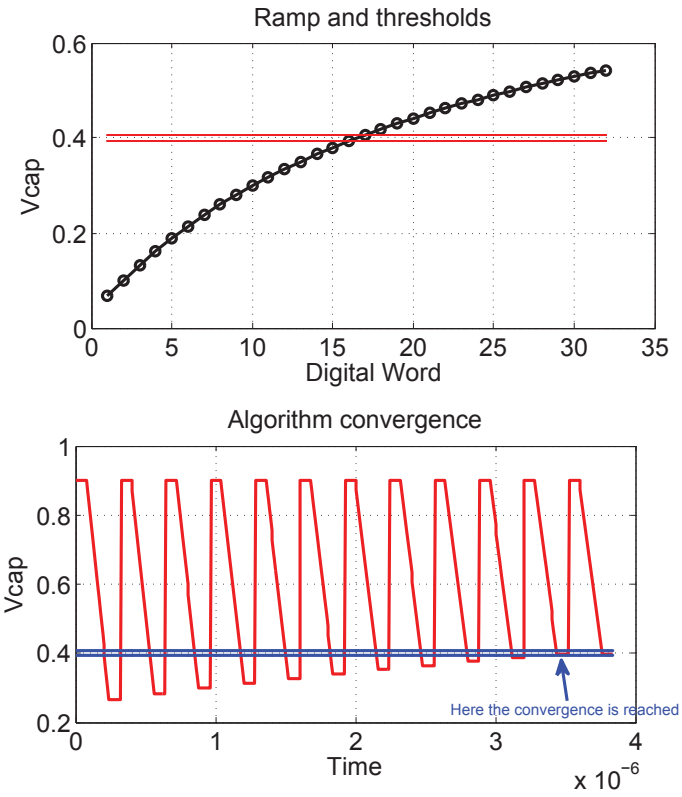


Figure 2.10: Matlab simulation results

configuration has been preferred to a simple charged capacitor as shown in figure 2.12.

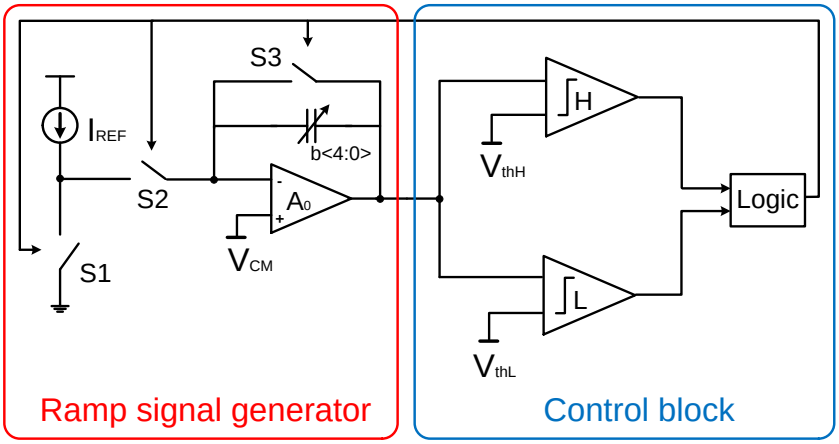


Figure 2.11: Low-level diagram of the tuning machine

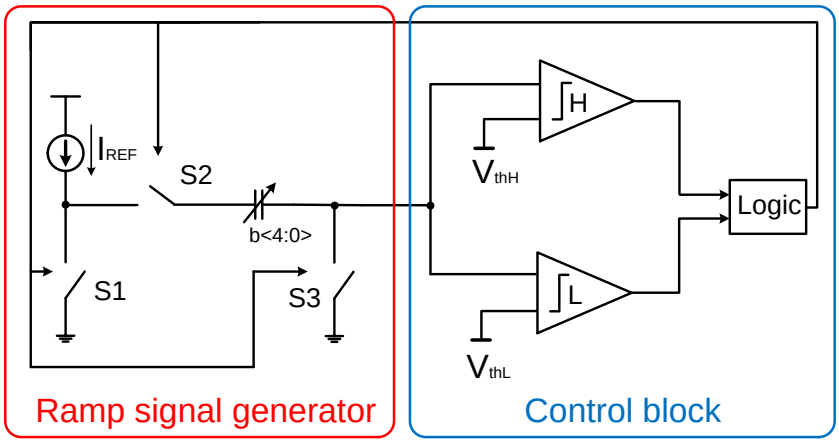


Figure 2.12: Alternative low-level diagram of the tuning machine

In fact, in this last configuration, the Op-Amp allows to drive a load capacitance, and guarantees an uncoupling with respect to the rest of the circuit. Moreover, the ramp in first (and used) configuration is descending, while in the second is raising.

### 2.5.2 Calibration Analog Section

In this chapter the analog components of the calibration circuit will be described. Although the whole tuning machine is a perfect example of a mixed-signal circuit, because the digital and analog worlds are strictly working together, the description of each one will be separated.

#### Operational Amplifier

The operational amplifier implemented here has not a real amplifying behavior, but is fundamental to maintain the ramp linear. In fact, the virtual ground principle

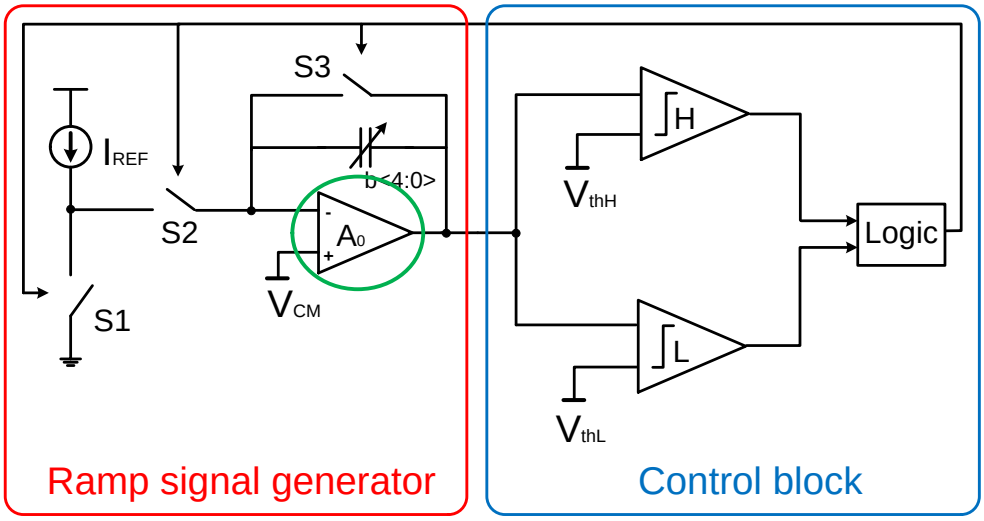


Figure 2.13: Operational Amplifier

states that if an Op-Amp has a very high open-loop gain, and it has a feedback, the difference between its input terminals is negligible. So, the input current is maintained constant. Moreover, the use of an Op-Amp allows to drive an output load, in this specific case represented by the two comparators inputs. The Op-Amp schematic is shown in figure 2.14.

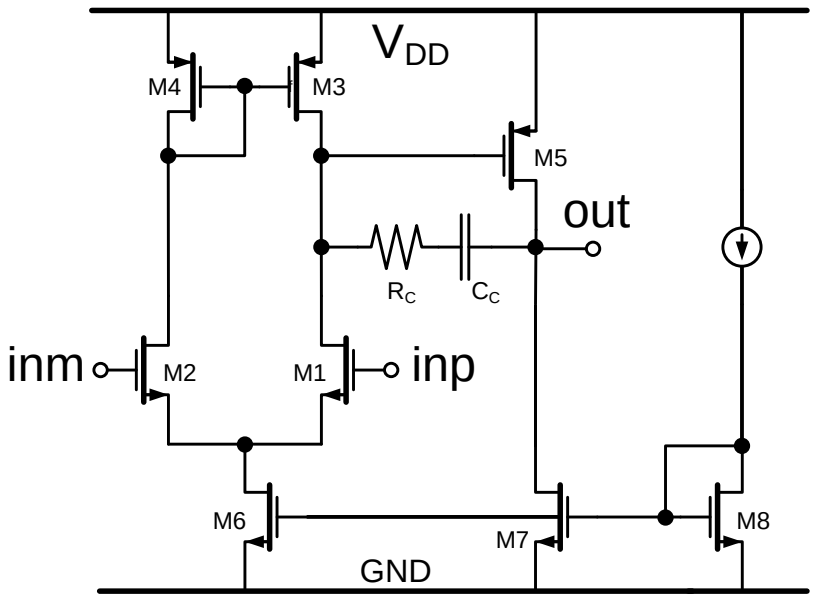


Figure 2.14: Op-Amp schematic

It's a two-stage Class-A Miller compensated amplifier, with no particular low-noise architectures; the noise in this application is not relevant. The design parameters of the Op-Amp have been chosen according to the following procedure.

**First stage** First, the input current has to be determined. This CMOS technology has a 500 mV threshold voltage. The relation between input current and the parameters of input stage transistors is

$$g_m = 2 \cdot \frac{I_D}{V_{ov}} \tag{2.8}$$

As already anticipated, this Op-Amp has no restrictive requirements on noise. Therefore, the attention has been focused on power consumption, choosing the input stage current to be 12.5 µA for each side. In order to guarantee the saturation region, overdrive voltage has been imposed to be 100 mV, and then a 0.25 mS $g_m$ value results. The shaping ratio (W/L) can be found in this way:

$$\frac{W}{L} = \frac{I_d}{k_{n/p} \cdot (V_{ov})^2} \tag{2.9}$$

With a 14 µA/V$^2$ electrons mobility $k_n$ (NMOS), the shape ratio will be 87.5. So a choice including a 35 µm W and a 400 nm L for the input stage transistors has been made. Moreover, for the active charge, the $g_m$ results 0.2 mS, with a 125 mV overdrive voltage. So with a 8 µA/V$^2$ holes mobility (PMOS), the shaping ratio will result 100. Therefore the active charge has been designed with the same W (35 µm) but a lower L (350 nm).

**Second stage** The parameters needed in order to design properly the second stage are the desired Unity Gain Bandwidth (UGB) frequency, the Op-Amp phase margin (PM) and the load capacitance $C_L$ on the output. Assuming that this Op-Amp will not work at very high frequency, the UGB has been fixed to 65 MHz. In order to guarantee a very strong stability, because the amplifier has to operate in an open loop configuration, a 80 degree phase margin has been chosen. As regards the load capacitance, considering that the only load will be 2 gates (the comparator inputs), a 200 fF value has been taken into account. The second pole frequency can be calculated with this formula:

$$f_{II} = \frac{g_m}{2\pi \cdot C_L} \tag{2.10}$$

But the second pole frequency can be obtained with another formula:

$$f_{II} = \frac{f_{UGB}}{\tan\left(\frac{\pi}{2} - PM\right)} \tag{2.11}$$

Therefore, the second pole frequency should lie at 369 MHz, while the second stage $g_m$ will be 0.46 mS. According to equations 2.8 and 2.9, choosing a 25 µA current, the overdrive voltage will be 105 mV, and consequently the shaping ratio will assume a value of 285.7. So, with a 350 nm L, the W can be chosen to be 100 µm.

**Current mirrors** With a 10 µA external current chosen, the first and second stage mirrors has been designed with a 25 µm W, due to the fact that each stage requires 25 µA and the reference mirror transistor has a 10 µm W.

**Miller compensation** The Miller capacitance has been calculated with equation 2.12, ad it has been found to be approximately 500 fF, and the zero compensating resistance, calculated with equation 2.13, will be designed to be 3.5 kΩ.

$$C_C = \frac{g_{m_I}}{2\pi \cdot f_{UGB}} \tag{2.12}$$

$$R_C = \frac{1}{g_{m_{II}}} \tag{2.13}$$

**Slew Rate** With the chosen configuration, the slew rate can be calculated with the two following formulas:

$$SR^+ = \frac{I_I}{C_C} \tag{2.14}$$

$$SR_- = \frac{I_{II}}{C_L + C_C} \tag{2.15}$$

The two formulas are due to a positive or negative excursion of the input signal, respectively $SR^+$ $SR^-$. So, the results are 50 V/µs for the $SR^+$, and 36 V/µs for the $SR^-$. The fact that they are different is not important for the Op-Amp functioning, because it has not to work at very high frequency.
The transistors dimensions are summarized in table 2.2.

| Transistor | W | L | Transistor | W | L |
|---|---|---|---|---|---|
| M1 | 35 µm | 0.4 µm | M5 | 100 µm | 0.35 µm |
| M2 | 35 µm | 0.4 µm | M6 | 25 µm | 2 µm |
| M3 | 35 µm | 0.4 µm | M7 | 25 µm | 2 µm |
| M4 | 35 µm | 0.4 µm | M8 | 10 µm | 2 µm |

Table 2.2: List of transistors dimensions

**Cadence® Spectre® Simulations** For the Op-Amp, two simulations in nominal conditions have been run.
The first one deals with the frequency response in terms of magnitude and phase. In figure 2.15 the results are shown.
The DC-gain results 68 dB, close to the 70 dB chosen for the design, while the UGB is 65 MHz with a 78° phase margin. So, for the frequency response, the Op-Amp respects the requirements.
As regards stability and rise-time, the step response simulation is a good test. In figure 2.16 the results are shown.

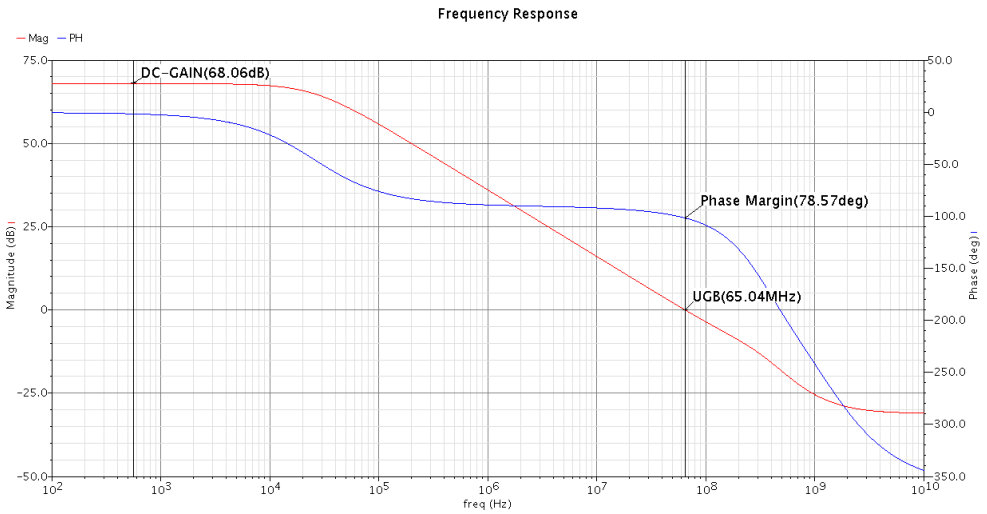


Figure 2.15: Op-Amp frequency response

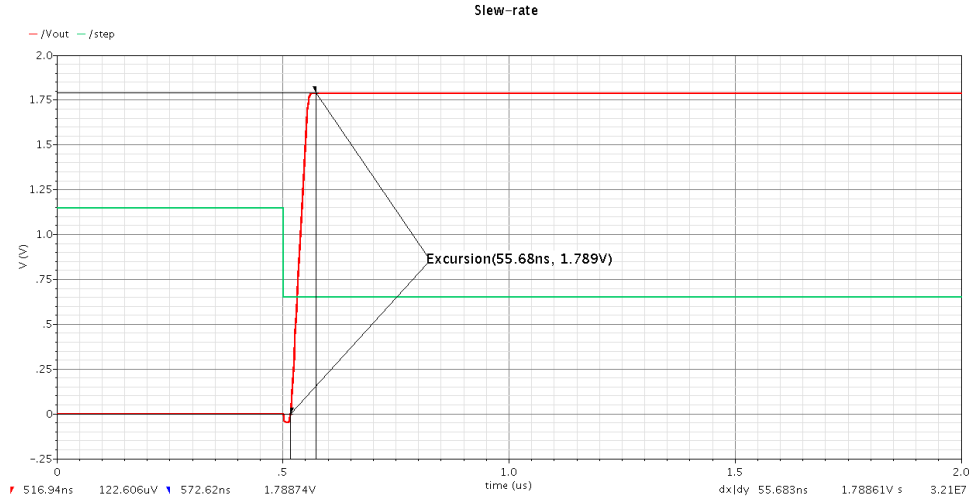


Figure 2.16: Op-Amp step response

The input step is 500 mV, as the ramp bias difference. The result is a 37.5 V/ µs slew-rate, suitable for the application.
This operational amplifier consumes a 600.2 µA current, as shown in figure 2.17.

### Comparators

**Delay and Offset** The two comparators, one for the high threshold and one for the low one, have an identical basic structure. This fact reduces the possibility of non-uniformity of their response with respect to each other, particularly the synchronism

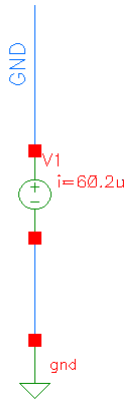


Figure 2.17: Op-Amp power consumption

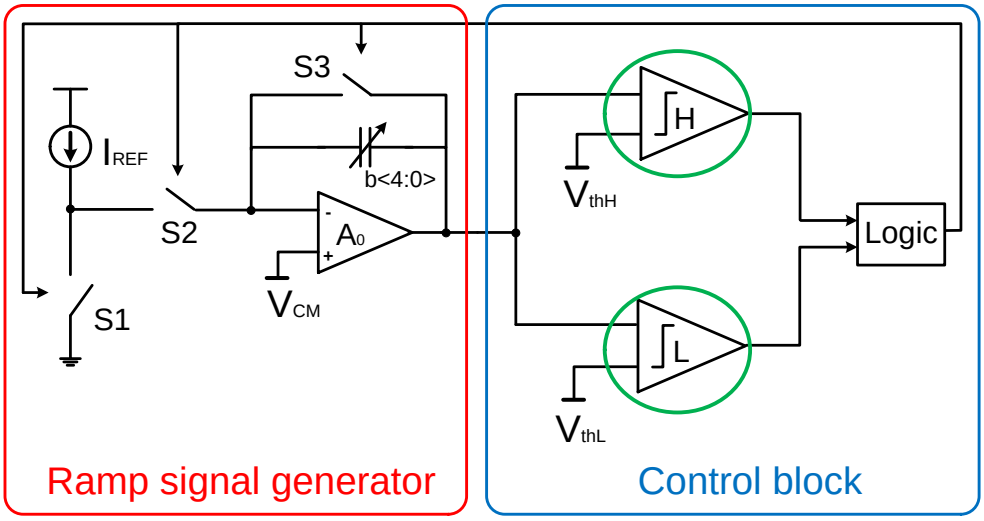


Figure 2.18: Comparators

and offset. Indeed the most important parameters are slew rate and offset. Offset is defined by the minimum voltage difference between the two input terminals that makes the comparator switch.
If the situation were ideal, and then no differences between the two sides of the input stage (each one referred to an input transistor) exist, the offset will be zero. Therefore, the obvious design rule is to make the two sides perfectly identical. Although this fact, local variation of the $V_{th}$ (threshold voltage of the input differential pair) can render the circuit asymmetrical, bringing to unideal behavior. So, in order to reach the equilibrium, an offset has to exist.
However, a relation exists between the standard deviation of a CMOS transistor parameter (such as $V_{th}$) and its area, and is shown in equation 2.16, where $k$ is a

technology dependent constant.

$$\sigma = \frac{\mathrm{k}}{\sqrt{\mathrm{W} \cdot \mathrm{L}}} \tag{2.16}$$

So, making the area of input pair bigger, [16], will reduce the variation of $V_{th}$.
On the other side, increasing in particular the L (channel width), the transistor become slower, with the consequence that the comparator reacts to an impulse in a longer time interval.
Due to this trade-off, a compromise has to be made. So, the input pair has been designed with a 40 µm W and a 0.35 µm L, therefore with a 114 $nm^2$ area, assuming $k$ to be 3 mV·µm, a 0.8 mV $\sigma$ results. If the 99% of possible cases have to be considered, the $3\sigma$ value results 2.4 mV.
The second stage has been designed to guarantee a sufficiently high slew-rate, in order to let the output signal to switch rapidly. Since the two comparators will be connected with digital circuits, their outputs enter a gate; so, a load output capacitance has been assumed to be 200 fF. With a 6.6 µA current, a 33 V/µs slew-rate is reached, according to equation 2.14 (Miller compensation is not needed).
In order to allow the comparators to have a large output swing, the second stage transistor must have a little overdrive voltage. Following the equation 2.9, and choosing for simplicity that the shaping ratio of the two transistor are identical, the two overdrive voltages are 180 mV for the NMOS and 240 mV for the PMOS, with a 10 µm W and a 0.35 µm L. In order to regenerate and rectify the logic signal, a buffer (two inverters) has been added, but this fact have slightly worsened the timing performance.

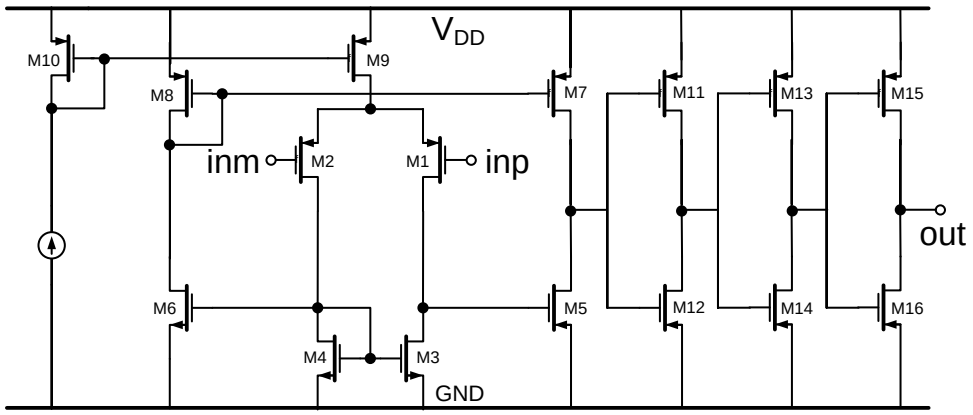


Figure 2.19: High threshold comparator schematic

As regards the two global schematics, shown in figures 2.19 and 2.20, the only difference is represented by a different number of inverters at the end, because the high threshold comparator has to switch high when the input is lower than its reference, while the low threshold one has to switch high when the input is greater than its

reference.

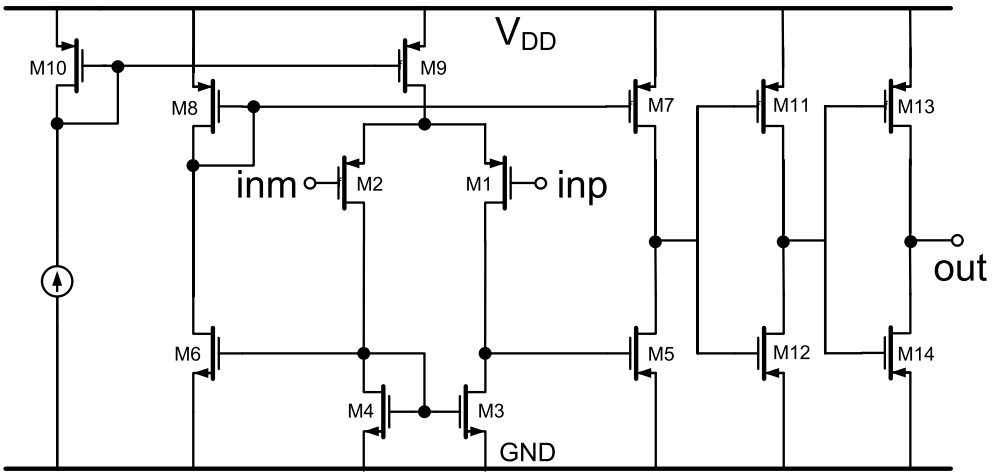


Figure 2.20: Low threshold comparator schematic

In table 2.3 the transistors dimensions for the common block are listed.

| Transistor | W | L | Transistor | W | L |
|---|---|---|---|---|---|
| M1 | 40 µm | 0.35 µm | M5 | 10 µm | 0.35 µm |
| M2 | 40 µm | 0.35 µm | M6 | 10 µm | 0.35 µm |
| M3 | 20 µm | 0.35 µm | M7 | 10 µm | 0.35 µm |
| M4 | 20 µm | 0.35 µm | M8 | 10 µm | 0.35 µm |

Table 2.3: List of transistors dimensions

**Cadence® Spectre® Simulations** In nominal conditions and with an ideal ramp and an ideal reference voltage, the two comparators behave like in figure 2.21.
But, in order to run a more significant test, a Monte Carlo simulation has been set, where all the parameters of technology are varied according to a gaussian distribution. The results are shown in figure 2.22.
The switching of comparators is considered correct if they assume the right value before the middle of SET region. So, the main data to extract from this type of simulation regard the percentage of iterations in which the two comparators behave as expected. In this case the 92% of tests have given a positive result.
The two comparators power consumption (in current) is presented in figure 2.23.

**Voltage references**

The two voltage references, in detail one for the Op-Amp, and one for each comparator, has been calculated within the MATLAB simulations, and are respectively 394 mV (low) and 406 mV (high). The calibration circuit needs another reference for the non-inverting Op-Amp terminal (900 mV). They are all realized with resistive dividers, in

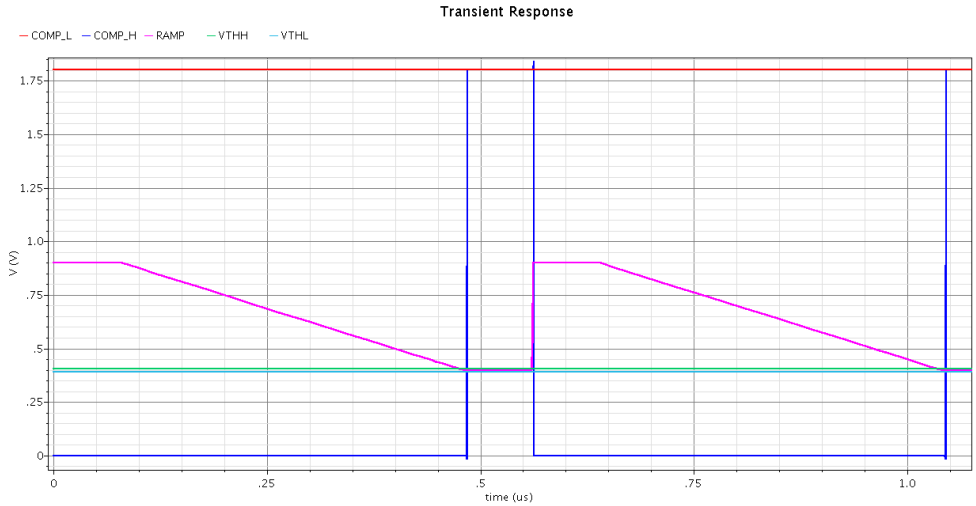


Figure 2.21: Comparators response in nominal conditions

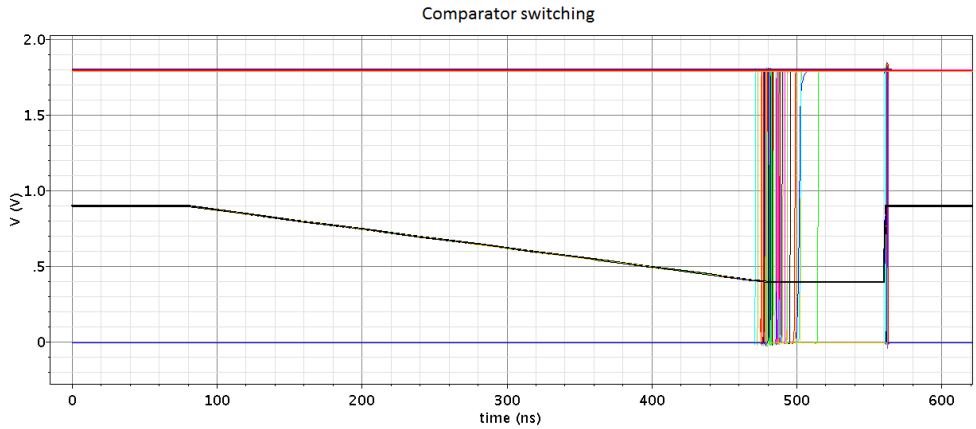


Figure 2.22: Comparators response with a Monte Carlo simulation

order to avoid that a local variation of each resistance due to the integration process affects the reference voltage. In dividers, the output voltage depends only by the ratio of resistances, and CMOS integration processes guarantee very precise ratio values [16]. In each output node of the dividers a 2 pF capacitor has been put toward ground, as shown in figure 2.24, in order to minimize resistor's thermal noise.
In detail, in order to minimize power consumption, the current flowing into the dividers has to be reduced as much as possible, compatibly with the resistor dimensions. Indeed, the greater is the current, the smaller are the two resistors. In addition to this fact, increasing the resistor values will increase their thermal noise, following the equation 2.17. This trade-off has been overcome choosing a 10 µA bias current, and consequently the $R_1$ and $R_2$ values listed in table 2.4, calculated with the equations

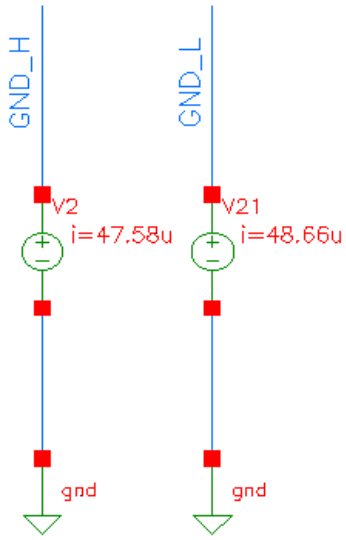


Figure 2.23: Comparators power consumption

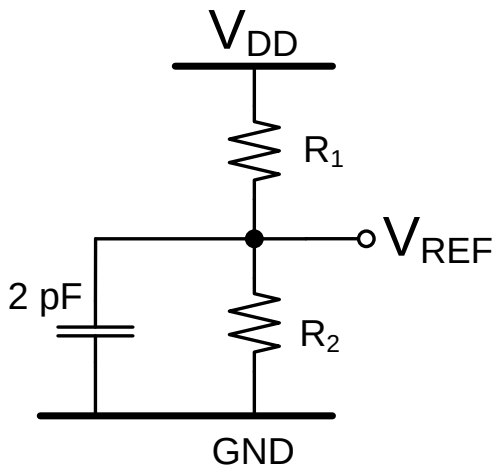


Figure 2.24: Voltage references architecture

2.18, 2.19 and 2.20.

$$\frac{v_n^2}{\Delta f} = 4 \cdot K_B T R \tag{2.17}$$

$$\frac{V_O}{V_I} = \frac{R_2}{R_1 + R_2} \tag{2.18}$$

$$R_2 = \frac{V_O}{I} \tag{2.19}$$

$$R_1 = \frac{V_I - V_O}{I} \tag{2.20}$$

| REFERENCE | $R_1$ | $R_2$ |
|---|---|---|
| $V_{CM}$ | 90 KΩ | 90 KΩ |
| $V_{TH_H}$ | 40.6 KΩ | 139.4 KΩ |
| $V_{TH_L}$ | 39.4 KΩ | 140.6 KΩ |

Table 2.4: Resistive dividers values

**Capacitor array**

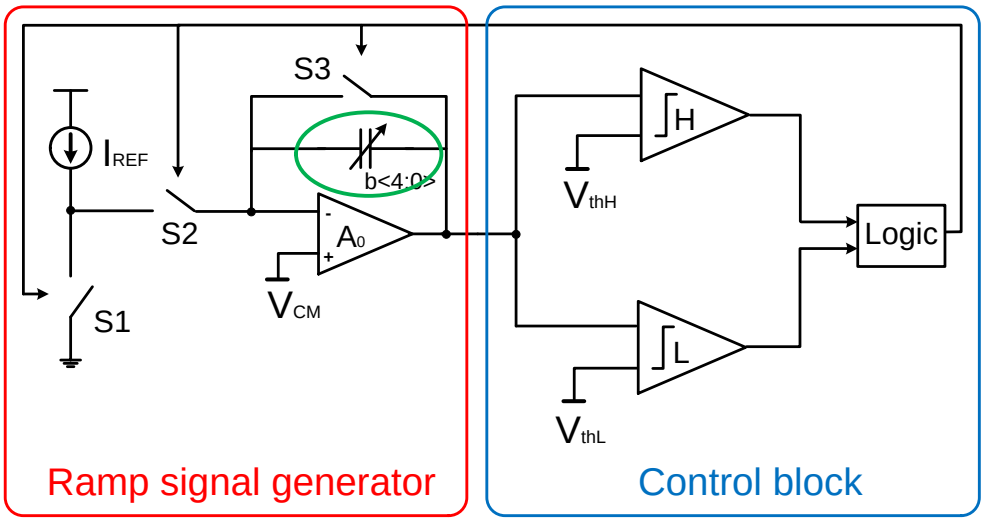


Figure 2.25: Capacitor array

The design of this specific block is not particularly complicated; the designer has to pay attention to the role of the switches.
In fact, this array has four switches for each capacitor, except for the offset one, which work in pairs. The first pair is connected to the two terminals of one capacitor, as shown in figure 2.26, and when closed they allow the current to charge the capacitor. When they are opened, the capacitor is isolated from the circuit. In this case, the charge accumulated in the capacitor remains there, and when the two terminals are connected again, this charge could affect the whole array behavior. A second pair, therefore, is included in the block named “cap array switch", shown in figure 2.27. This pair acts on reverse logic with respect to the other: they are preceded by an inverter, and when closed they allow the capacitor to discharge toward the ground, avoiding undesired discharging phenomenons.
As regards the capacitors, the choice has been made on metallic ones, because they have a larger area with the capacitance value being equal. Hence, as the spread is

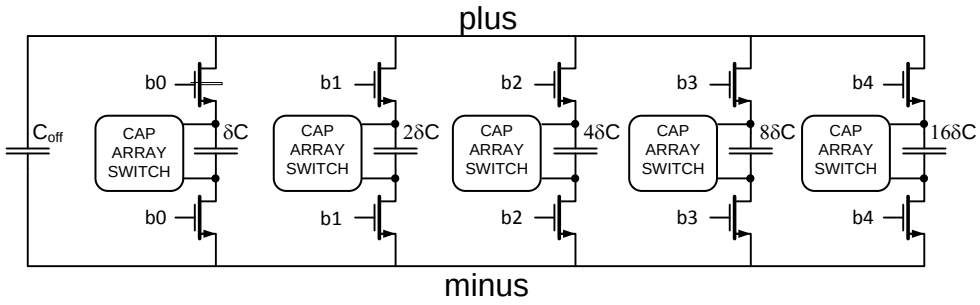


Figure 2.26: Schematic of the capacitor array

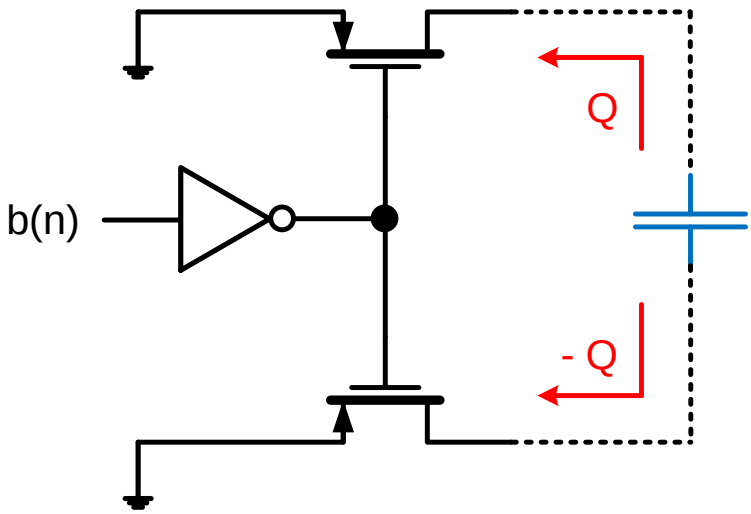


Figure 2.27: Schematic of the “cap array switch" block

proportional to the capacitance area, they are less sensitive to integration process variation. So six capacitors have been included in the array. The offset one, corresponding to $C_{min}$ in equation 2.3, and five capacitors with $2^m \cdot \epsilon$ values, with $0 \leq m \leq 4$ and $\epsilon$ calculated with equation 2.5. MATLAB simulation has calculated $\epsilon$ (in figure 2.26 $\delta C$) to be 46 fF and $C_{off}$ to be 1.08 pF.

### 2.5.3 Calibration Digital Section

The designer has two possibilities to realize a digital circuit.
The first, the more immediate, consists in combining opportunely the digital components included for the specific used technology, such as logic port or elementary blocks, so that the circuit produces the desired outputs. But this procedure brings to several issues. The first is the complex structure which can reach a digital circuit, (this is the case), when the task are multiple and require a high number of logic ports. The second is due to the delays, which are very hard to manage.

Therefore, the choice has been focused on the automatic digital synthesis tool included in the Cadence® software package, named RTL® Encounter® . This tool converts a VHDL code into a schematic optimizing the logic ports number and their delay, in order to guarantee a more synchronized response. In addition to this fact, this tool realizes the layout of the structure, and test its matching with the schematic. The tool functioning can be summarized with the block scheme in figure 2.28.

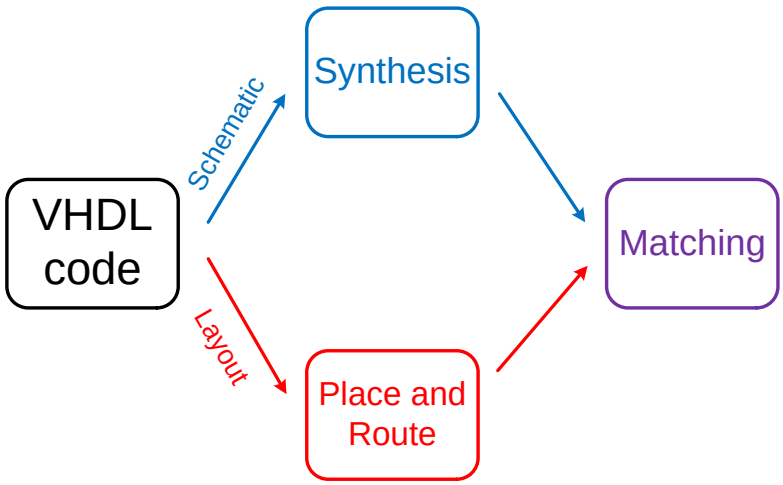


Figure 2.28: Automatic digital synthesis tool structure

Dealing with this specific design, in figure 2.29 all the blocks and their connections are shown.

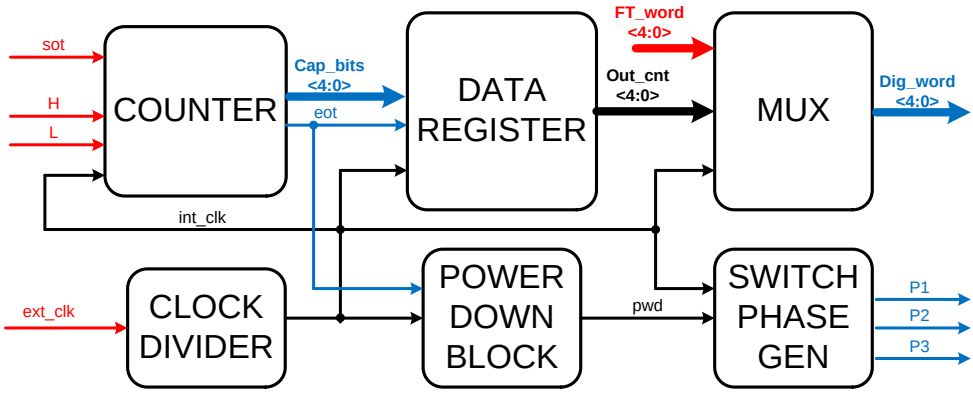


Figure 2.29: The Digital Part block scheme

### Clock divider

The clock used by the front-end channel, generated by an internal oscillating circuit, has a 25 MHz frequency. For the tuning process, a clock with half the main frequency

has been chosen (12.5 MHz), because it's a *una tantum* process, made by default at the power-on of the whole ASIC, and only when the working conditions (e.g. temperature variations) change. So a fast clock is not needed and, in addition to this, a slower clock will interfere with the nearest signals less.
Due to this fact, a clock divider block has been implemented, made by only a flip-flop block and an inverter. Every time the main clock switches high, the flip-flop output is inverted and put into the same flip-flop input. In this way the duty cycle is doubled, and the resulting flip-flop output will be a clock with a half frequency.

**Switch phase generator**

In chapter 2.5.1, the ramp has been described. In order to generate a such impulse, three switches are needed, as shown in figure 2.11. This specific block generates the three phases. The first switch is closed in the RESET phase, when the charging current, not needed, has to be dispersed. The second switch is closed in the ACTIVE phase, in order to allow the capacitor charging, while the third switch has to be closed in the RESET phase, shorting the inverting input and the output of the Op-Amp. So, in figure 2.30, the three phases are shown. Note that the first and the second switch are PMOS, while the third is NMOS.

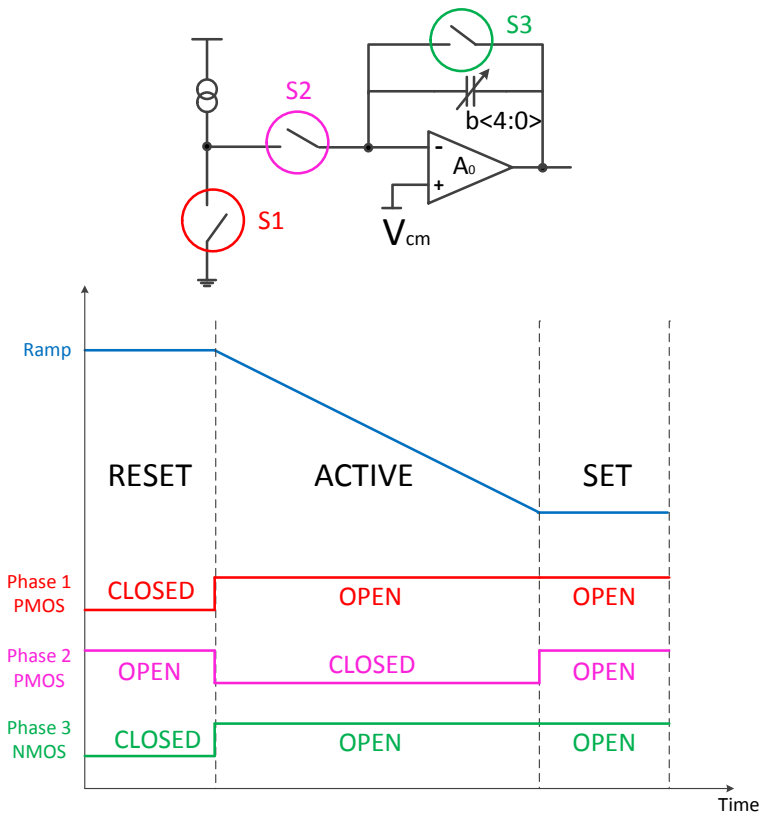


Figure 2.30: Switch phases

**Counter**

The counter is the main block of the digital part. In detail, its role is to choose the digital word needed to tune the capacitor array value as close as possible to the nominal value, such as into the predicted error (see equation 2.5). Its behavior can be described with an algorithm corresponding to figure 2.8.
Specifically, the counting starts, if the EN (enable) input pin is high, with the default value (15d $\rightarrow$ 01111b). With this digital word, the capacitor array will have the correct value if no variations with respect to the capacitance value occur, and then the two comparators output will be both high. If, otherwise, one comparator does not switch, the counter increments or decrements the digital word according to comparators response.
For example: if the capacitor array value is too low, the ramp will end below the two thresholds. In the SET phase of the ramp, shown in figure 2.7, the low comparator output will be zero, and the counter will increment the digital word by one, and the process will be repeated. When both the comparator will be high in the SET phase, the counter will make the EOT (end of tuning) pin high.

**Power-down block**

This block has the unique function to power-on or power-down the entire tuning process. When its SOT (start of tuning) input pin, its block makes the counter and phase generator EN pin high, in order to start the process. When the counter makes EOT high, this block makes the two EN pin low, stopping the ramp generation.

**Tuning data register**

When the tuning process is running or it has been disabled, the default digital word has to be put into all tunable capacitor of the ASIC (01111b). Only when the EOT pin in high, the register outputs the counter word. In other cases, the default word reaches the MUX.

**MUX**

This block selects, according to its FT_EN input pin, which digital word between the register one and an external word named FT<4:0> (force tune), selected by the user, reaches the tunable capacitors of the ASIC. The force-tune word can be put into the capacitor arrays when the user has the necessity to impose the capacitors value or in case of tuning failure. Putting the FT_EN high, the FT word reaches all the capacitor arrays, otherwise the register word do this.

**Pins' list and description**

In figure 2.31 all input and output pins of the tuning block are shown. Here is also a list of them and their functionalities.

**INPUT PINS**

- SOT: start of tuning. This pin, when high, makes the tuning process start.
- RES: reset. This pin has the priority over every other pin.

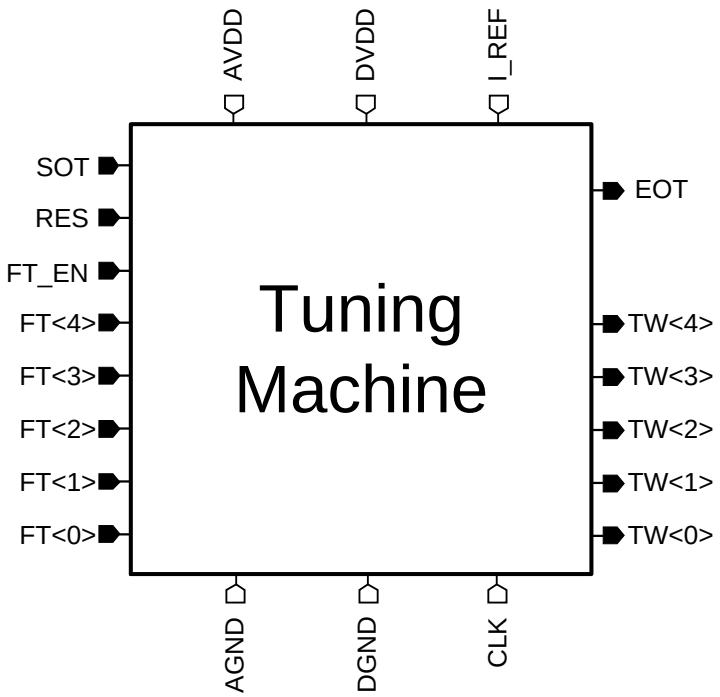


Figure 2.31: High-level diagram of the tuning machine

- FT_EN: force tune enable. This pin, when high, enables the introduction of a 5-bit word directly to the output.
- FT<4:0>: These pins are to be set as the desired force tune word. They are active only when FT_EN is high.

**OUTPUT PINS**

- EOT: end of tuning. When this pin is high, the tuning process has ended with success.
- TW<4:0>: This pin compose the word to be put into every capacitor of the chip.

The other pins, set in white in figure 2.31, are the bias connections, shared with those of the whole chip. In detail, AVDD and DVDD have to be set at 1.8 V, while I_REF requires a 9 µA bias current. In addition to this, the digital part works synchronously with a 12.5 MHz clock signal, generated into the chip. Note that setting or resetting pins synchronously is not necessary.

**Settings details**

Before the first start, typically when the ASIC is powered on, the RES pin has to be set high in order to initialize the digital part. When the user wants to make the tuning process start, he has to make the SOT pin high.

The process then starts and, at the end, the EOT pin becomes high.
Note that the entire process, apart from the setting of all input pins, is managed automatically inside the chip.
Every time the user wants to remake the tuning, he has to reset and set the SOT pin.
In order to guarantee the correct functioning of the machine, every set or reset has to last at least 2 clock times.
In every moment, setting high the RES pin will reset all the blocks, and the tuning process will be aborted.

# 3
# Layout

After having tested the circuit performance with the simulations described in part 4, the designer has to implement the real architecture of the project with the layout process. Indeed, the layout corresponds exactly to the real circuit. With this procedure the designer creates all the metal connections, the transistors, the capacitors etc. and he places them in determined positions of the available silicon area.
This process will be implemented in silicon by the foundry, following the indications and including the layers present in the layout view.
The technology used for the design includes the basic components, the same used for the circuit topology, and all the available layers, such as metals, polysilicon, oxides, contact, vias and so on.

## 3.1 Design rules and guidelines

Every technology, depending on the scaling level and the integration process, has a series of rules which the designer has to respect when layouting a circuit.
These rules regards with the minimum or maximum realizable dimensions of components, layer compatibility and distance, metal wire distance and minimum width, the number of vias required to connect two different metals and other less relevant requests.
In order to check the abidance of the layout, the Cadence® Virtuoso® software provides a tool named DRC (Design Rules Check), while the correspondence with the relative schematic is checked by the LVS (Layout Versus Schematic) tool.
In addition to this, attention has to be paid for the working condition of components, depending on their geometry, position and connections. Indeed, in the simple schematic design, connections are ideal and the geometrical variety of single devices doesn't affect their behavior.
For the layout instead, identical components placed in different positions behave differently, and even the surrounding structures can cause malfunctioning.
For instance, when layouting a transistor, one of the main point to consider is the use of fingers. In fact, a single component included in the circuit can assume a longed shape, if its W and L are pretty different. This causes excessive strains, with consequent variation in the behavior of each part.
The transistor is then divided in single small unities, called fingers, connected in parallel so that the global structure is analogous to the original one.
The main advantages are obviously the more homogeneous working conditions and a more compact structure. One possible drawback is the fact that the two side fingers can work in a unexpected way due to the asymmetrical conditions in which they are implemented. In order to prevent this fact, two dummy fingers have to be added in

the two sides. These fingers are always off, and their use is limited to homogenize the transistor working conditions.
An example in shown in figure 3.1.

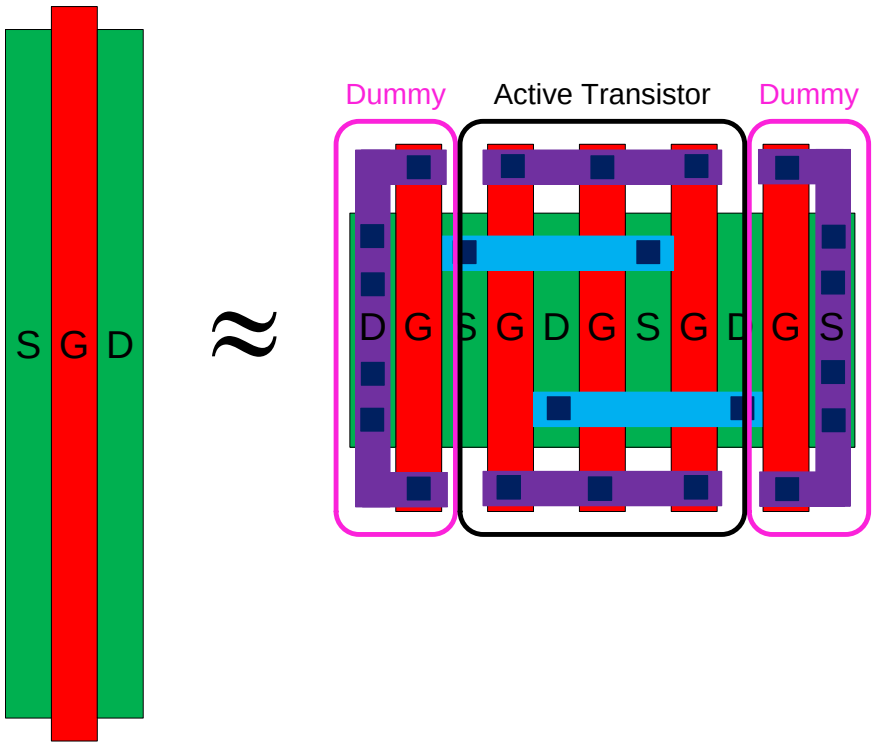


Figure 3.1: Transistor layout: without and with fingers and dummies

## 3.2 Calibration circuit opamp layout

The figure 3.2 presents the layout of the opamp block.
The block marked as 1 is the first stage input pair, the number 2 embodies the first stage active charge, the number 3 is the second stage, the number 4 includes all the current mirrors, while the numbers 5 and 6 are respectively the Miller resistance and capacitance. In addition to these blocks, some resistance shorted toward ground are been included, in order to dissipate electrostatic energy.
Every indicated block is surrounded by a vias' ring, in order to create ground contacts. Note that the NMOS transistors are included directly in the bulk (p-type), while the PMOS are embedded into a n-well together with a vias' ring (for the $V_{DD}$ contacts). In this design the finger structure described is clearly visible.

### 3.2.1 Calibration circuit comparators

The two comparators layout is presented in figure 3.3.
The common part is composed by the parts marked as 1 (the mirrors) and 2 (the two

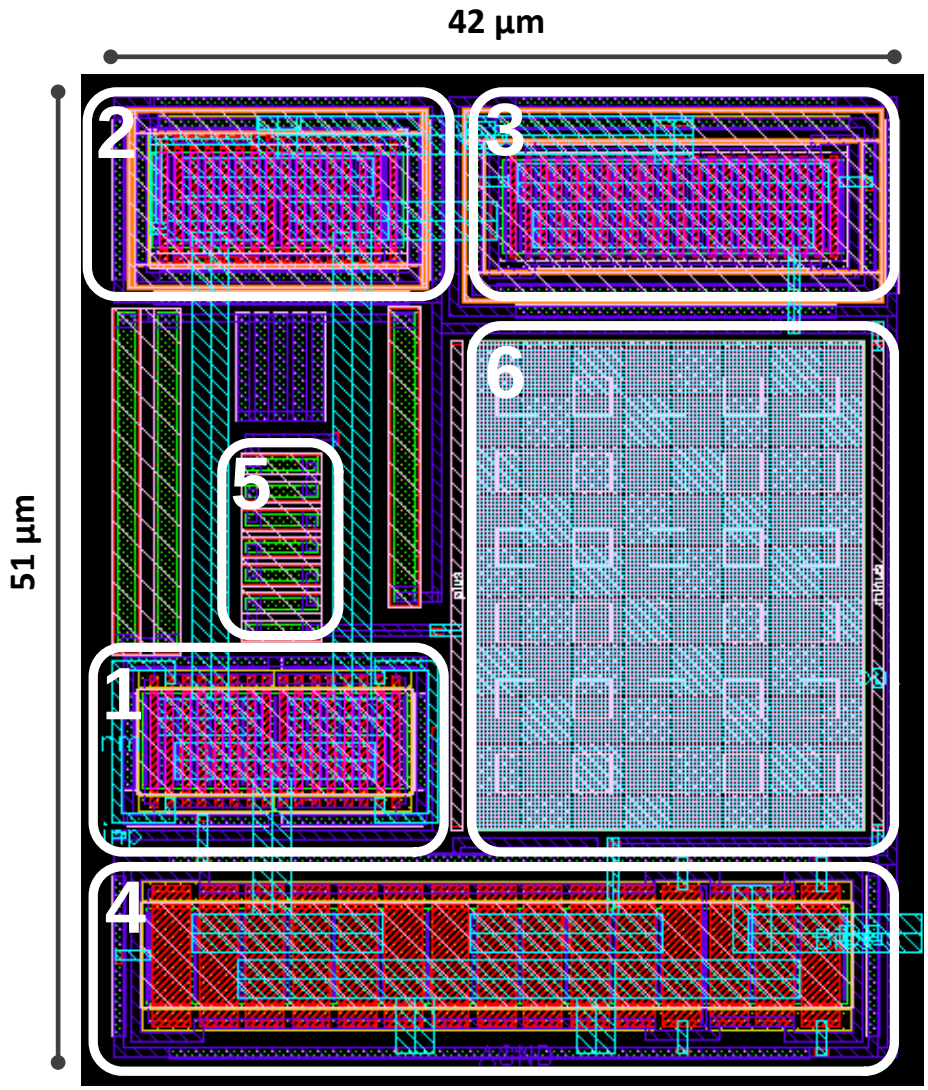


Figure 3.2: Calibration circuit opamp layout

stages), while the buffers and the inverter blocks are marked respectively as 3 and 4. The similarity of the two layouts increments the probability of matched response.

### 3.2.2 Capacitors array

Figure 3.4 reports the capacitors array layout.
The part 1 include the first couples of switches (see the section 2.5.2), while the part 2 shows the second couples. In part 3 there is the offset capacitor, in part 4 the first four bit capacitors (b0 to b4) and in part 5 the b5 one. In order to improve matching, every capacitor, except the offset one, has been composed by multiples of the b4 capacitor.

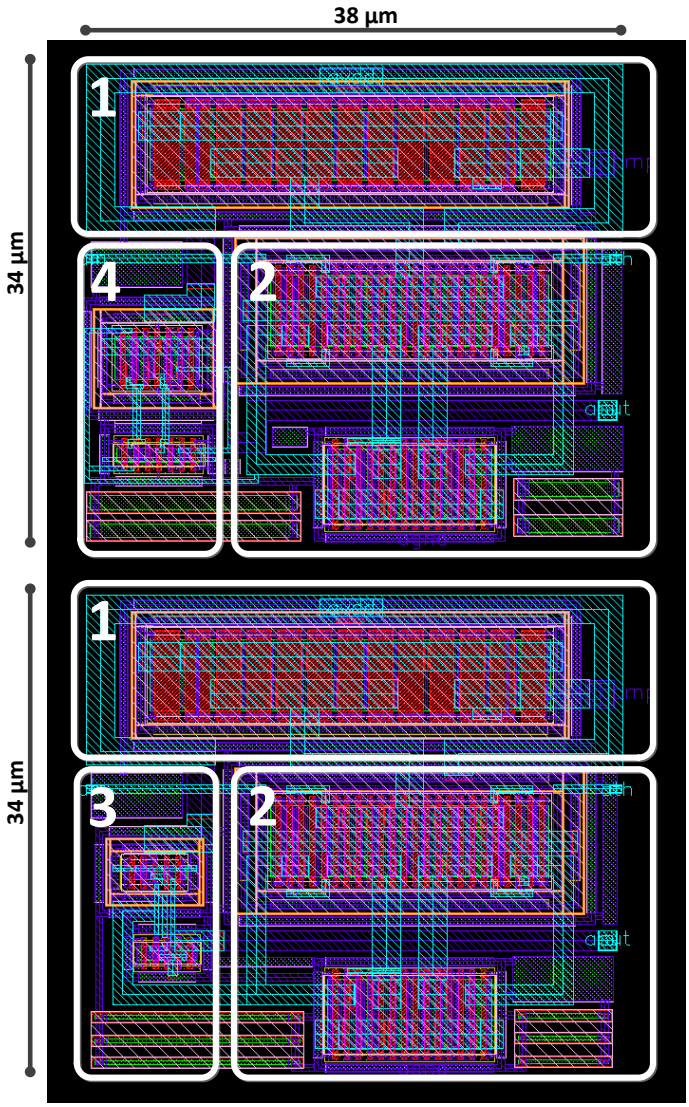


Figure 3.3: Calibration circuit comparators layout: the high one is on top while the low one is on the bottom

### 3.2.3 The whole analog calibration circuit

The entire analog calibration circuit layout is presented in figure 3.5.
The blocks marked as 1 are the three noise filtering capacitors (each one consists of two capacitor in parallel), connected to the three resistive dividers, marked as 7, used as voltage references. The capacitors array is the block 2, the two comparators (high and low) are respectively blocks 3 and 4, the Op-Amp is block 5, the switches are block 6 and the current references are block 8.

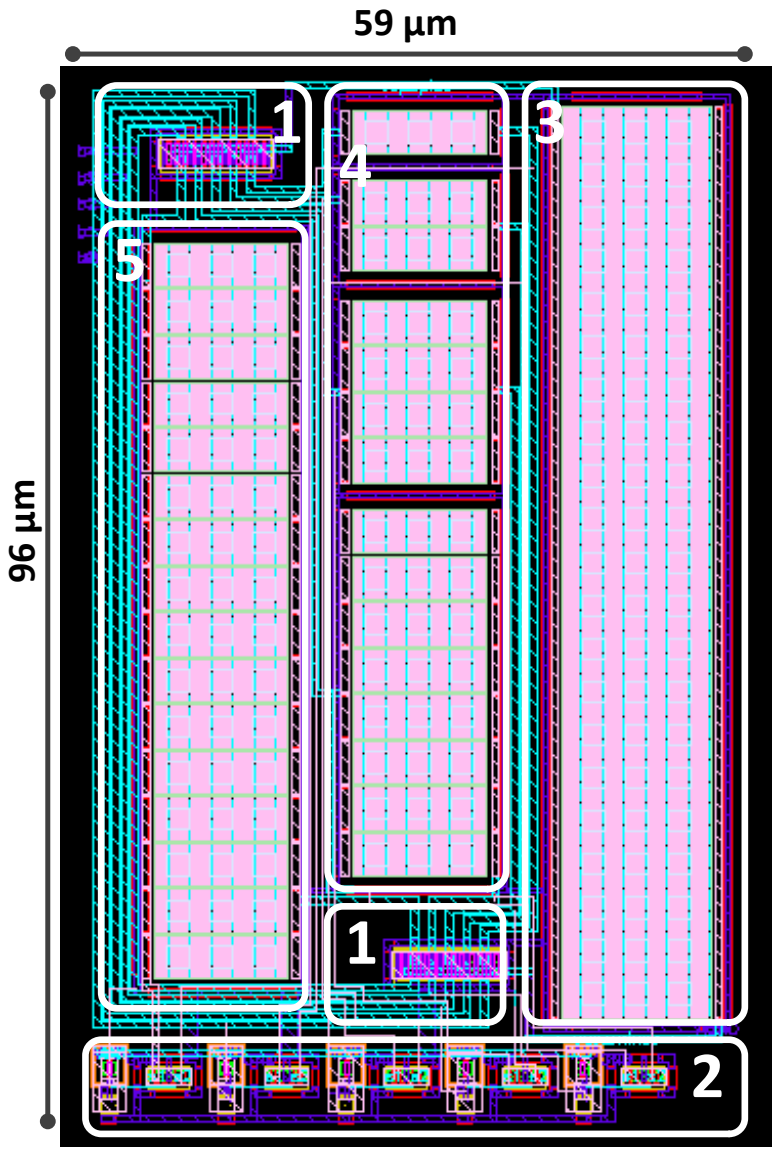


Figure 3.4: Capacitors array layout

## 3.3 Digital Layout

The digital section layout is an automatic process. Indeed, since the structure of a digital circuit includes basic blocks, the layout is a combination of these elementary units, in order to obtain the desired circuit. Therefore, the layout process can be automatized. Once the desired geometry and dimensions of the layout have been chosen, in addition to the pins positions, the synthesis produces a layout like the one shown in figure 3.6. This figure is the digital section of the calibration circuit.

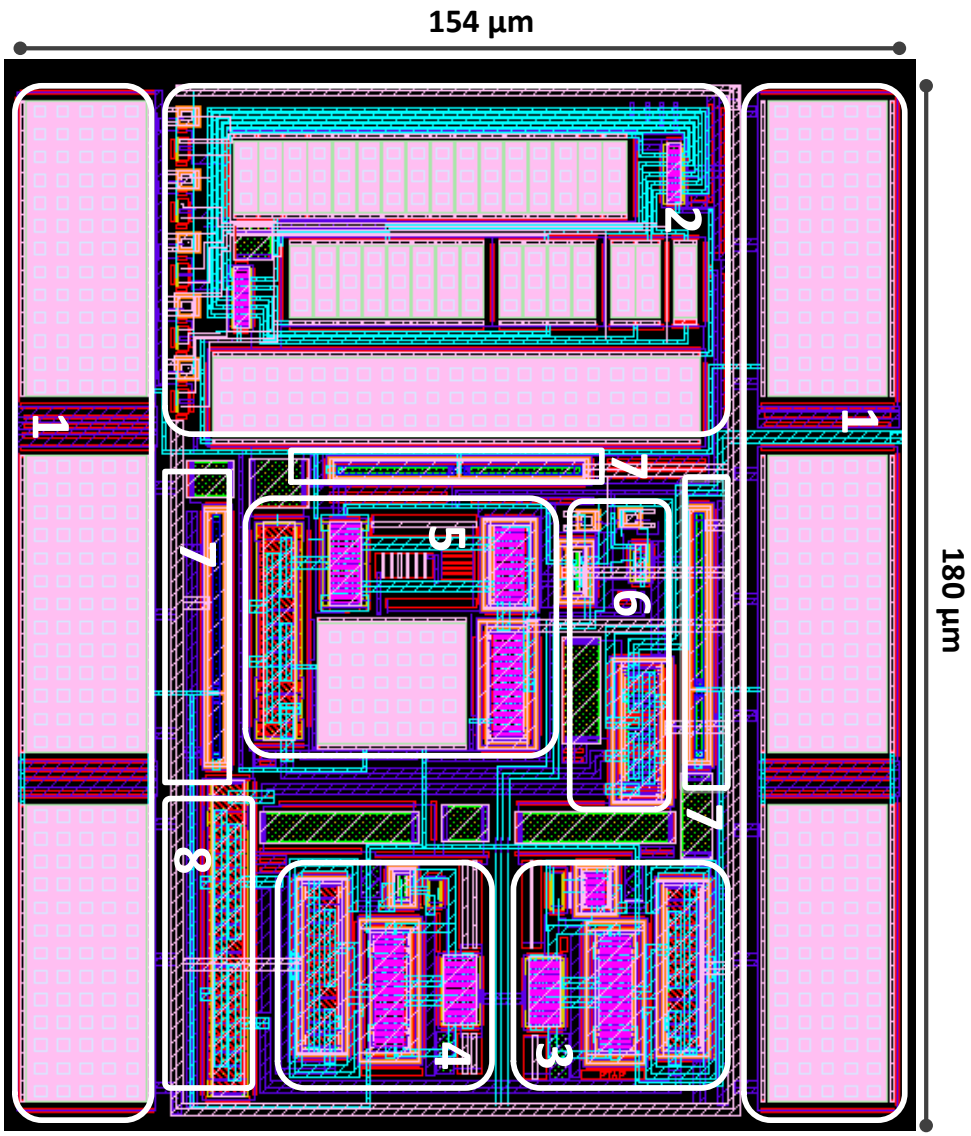


Figure 3.5: Analog section of the calibration circuit layout

## 3.4 The ASIC layout

The figure 3.7 is the complete layout of the chip.
It is important to notice the presence of the pad ring, that is the ensemble of all the input and output pins, with which the chip is connected to the outside. Its layout has to respect the dimensional constraint imposed by the inner circuit, and if needed, spacer layers, named fillers must be added between pads. Furthermore, the pad ring itself needs a power supply and a ground pin.

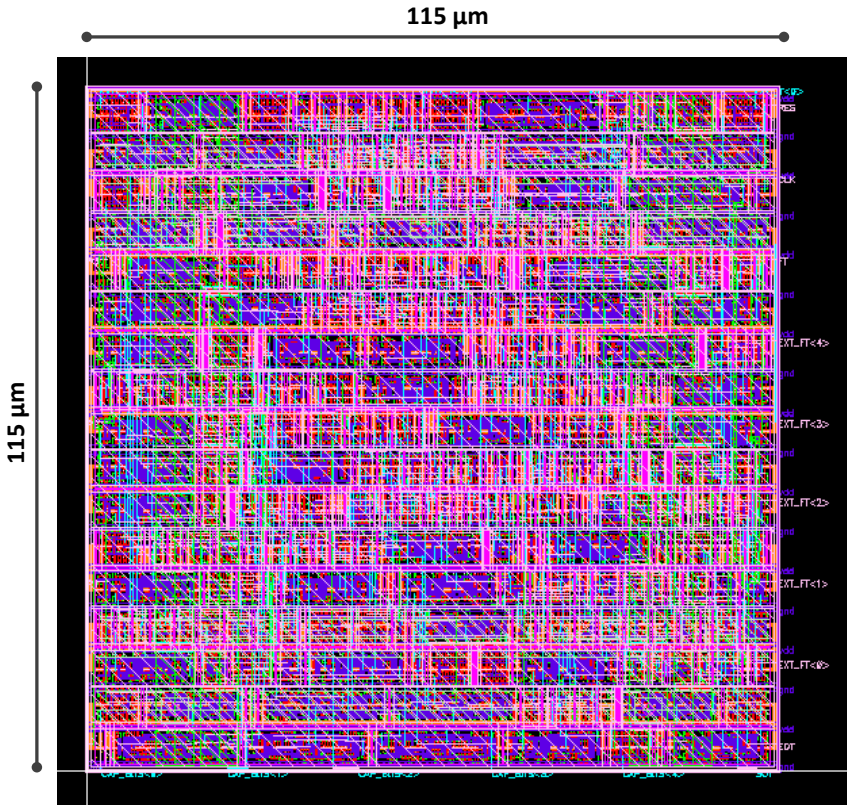


Figure 3.6: Calibration circuit digital block layout

The eight channels are clearly noticeable, while the pad ring, $I^2C$ system, the analog MUX and the tuning machine are marked respectively as 1, 2, 3 and 4. The dimensions are 1.854 x 2.523 mm, with a 4.678 $\mathrm{mm}^2$ area.

### 3.4.1 Pins structure and position

The ASIC pin structure is presented in figure 3.8. On the left side odd channel pins are placed, while on the right side the even ones. Channels 1, 2, 5 and 6 are implemented with a calibration structure, instead of channels 3, 4, 7, 8 in which calibration is not included. For channels, the sequence of pin is:

- INC: calibration input signal (1-2,5-6)
- CEN: calibration enable (1-2,5-6)
- gnd: ground reference
- SEN: detector input signal
- DET: event detection output
- TOT: time over threshold output

On the top side $I^2C$ , quartz crystal, analog supply and the channel global reset pins are placed:

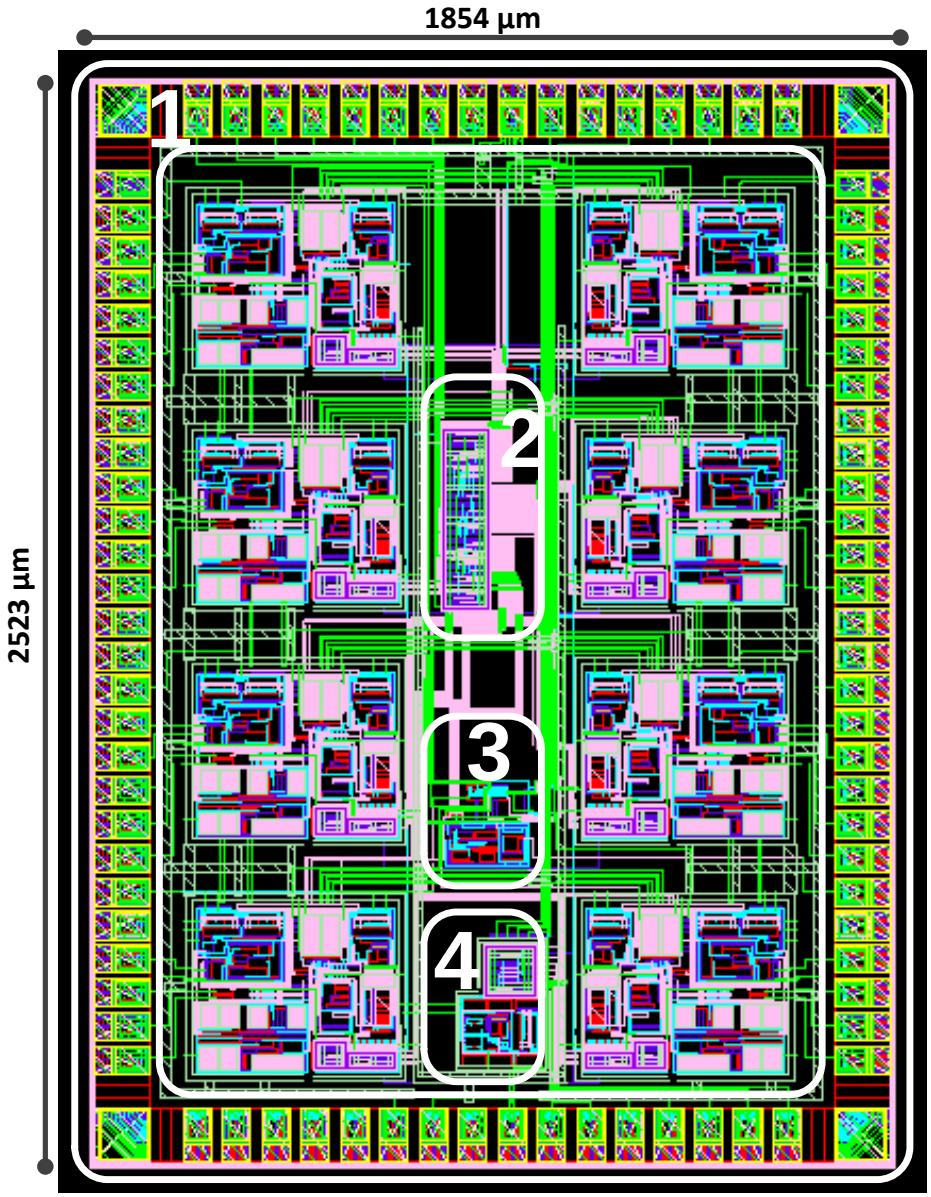


Figure 3.7: ASIC complete layout

- CLK_I2C: $I^2C$ main clock input
- RES_I2C: $I^2C$ reset
- SCL: $I^2C$ clock line
- SDA: $I^2C$ data line
- SLVADD<0:3>: $I^2C$ slave address pins
- AVDD: analog power supply
- gnd_a: analog ground reference
- XTAL<0:1>: quartz crystal pins
- RES_CH: channels global reset

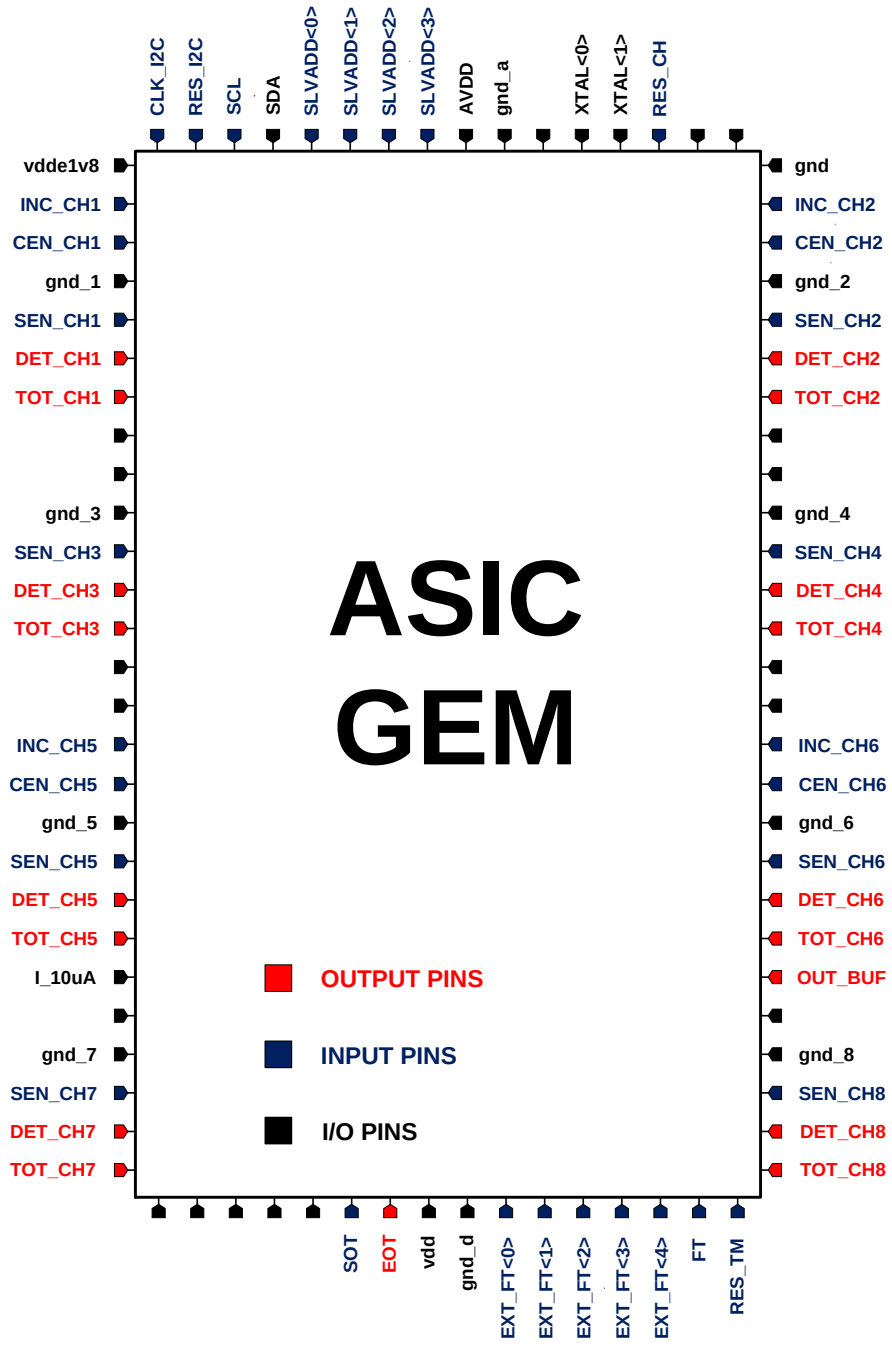


Figure 3.8: ASIC pin structure

On the bottom side calibration circuit pins and digital supply are placed:

- SOT: start of tuning
- EOT: end of tuning
- vdd: digital power supply
- gnd_d: digital ground reference
- EXT_FT<0:4>: force-tune word
- FT: force-tune enable
- RES_TM: calibration circuit reset

More four pins are needed:

- vdde1v8: pads power supply (left)
- gnd: pads ground reference (right)
- I_10uA: current reference (left)
- OUT_BUF: analog MUX output (right)

# 4
# Performance

## 4.1 Channel PVT Simulations

As already described in chapter 1, this type of ASIC can work into a non-ideal environment. One example is the immersion into radiation which could affect the desired behavior of the circuit.
In order to simulate these possible variation of conditions, the calibration circuit has been submitted to 81 different corners, in which the power supply voltage, the temperature, the transistors, resistors and capacitors processes (the possible silicon, dielectrics or metals mobility variations) vary. Specifically, in table 4.1 are listed all the settable conditions.

| Parameter | Possible Conditions |
|---|---|
| Supply Voltage (V) | 1.7; 1.8; 1.9 |
| Temperature (°C) | -40; 27; 120 |
| Transistor Process | Typical-Typical (TT); Slow-Slow (SS); Fast-Fast(FF); N-Slow P-Fast (SF); N-Fast P-Slow (FS) |
| Resistors and Capacitors Process | TYP; MIN value; MAX value |

Table 4.1: PVT possible conditions

In order to run the most significant combination of these conditions, an Ocean code has been written, which prints the digital word produced for each corner. Ocean is a programming language which allows to run simulations in sequence, varying the design parameters as desired. The results are listed in table 4.2. In the first column the corner parameters are listed, while in the second column, the digital words, converted into decimal, are shown.
A brief description of the simulation made for the analog channel is presented. They have been run in nominal conditions and spreading CMOS process, temperature and supply voltage, by Ocean tool. Front-end performance have been evaluated for several corners (combining all possible variations as in table 4.1).
As regards, the Event-Detection-Signal delay, the simulations evaluate delay between input charge arrival time and the charge-detection-impulse starting point. The instant in which the charge arrives is defined as the zero-point in figure 2.3. The EDS delay definition is also reported in the same figure.
Note that in figure 4.1 the delay in nominal conditions is plotted vs. input charge (27 °C, 1.8 V, tt, RC typ). Maximum delay occurs when the minimum input charge of 30 fC is simulated. In this case the front-end needs about 30 ns to detect the input charge. Note that the minimum duration of the input charge pulse is about 30 ns, so

| CORNER V; T; P | DIG. WORD | CORNER V; T; P | DIG. WORD | CORNER V; T; P | DIG. WORD |
|---|---|---|---|---|---|
| 1.7; -40; tt | 17 | 1.8; -40; tt | 15 | 1.9; -40; tt | 13 |
| 1.7; 27; tt | 17 | 1.8; 27; tt | 15 | 1.9; 27; tt | 14 |
| 1.7; 120; tt | 18 | 1.8; 120; tt | 16 | 1.9; 120; tt | 14 |
| 1.7; -40; ff_min | 26 | 1.8; -40; ff_min | 23 | 1.9; -40; ff_min | 21 |
| 1.7; 27; ff_min | 26 | 1.8; 27; ff_min | 24 | 1.9; 27; ff_min | 22 |
| 1.7; 120; ff_min | 27 | 1.8; 120; ff_min | 25 | 1.9; 120; ff_min | 22 |
| 1.7; -40; ff_max | 10 | 1.8; -40; ff_max | 8 | 1.9; -40; ff_max | 7 |
| 1.7; 27; ff_max | 10 | 1.8; 27; ff_max | 9 | 1.9; 27; ff_max | 7 |
| 1.7; 120; ff_max | 11 | 1.8; 120; ff_max | 9 | 1.9; 120; ff_max | 7 |
| 1.7; -40; ss_min | 25 | 1.8; -40; ss_min | 23 | 1.9; -40; ss_min | 21 |
| 1.7; 27; ss_min | 26 | 1.8; 27; ss_min | 23 | 1.9; 27; ss_min | 21 |
| 1.7; 120; ss_min | 26 | 1.8; 120; ss_min | 24 | 1.9; 120; ss_min | 22 |
| 1.7; -40; ss_max | 9 | 1.8; -40; ss_max | 8 | 1.9; -40; ss_max | 6 |
| 1.7; 27; ss_max | 10 | 1.8; 27; ss_max | 8 | 1.9; 27; ss_max | 7 |
| 1.7; 120; ss_max | 10 | 1.8; 120; ss_max | 8 | 1.9; 120; ss_max | 7 |
| 1.7; -40; sf_max | 10 | 1.8; -40; sf_max | 8 | 1.9; -40; sf_max | 7 |
| 1.7; 27; sf_max | 10 | 1.8; 27; sf_max | 9 | 1.9; 27; sf_max | 7 |
| 1.7; 120; sf_max | 11 | 1.8; 120; sf_max | 9 | 1.9; 120; sf_max | 7 |
| 1.7; -40; sf_min | 26 | 1.8; -40; sf_min | 23 | 1.9; -40; sf_min | 21 |
| 1.7; 27; sf_min | 26 | 1.8; 27; sf_min | 24 | 1.9; 27; sf_min | 22 |
| 1.7; 120; sf_min | 27 | 1.8; 120; sf_min | 25 | 1.9; 120; sf_min | 22 |
| 1.7; -40; fs_max | 9 | 1.8; -40; fs_max | 8 | 1.9; -40; fs_max | 6 |
| 1.7; 27; fs_max | 10 | 1.8; 27; fs_max | 8 | 1.9; 27; fs_max | 7 |
| 1.7; 120; fs_max | 10 | 1.8; 120; fs_max | 8 | 1.9; 120; fs_max | 7 |
| 1.7; -40; fs_min | 25 | 1.8; -40; fs_min | 23 | 1.9; -40; fs_min | 21 |
| 1.7; 27; fs_min | 25 | 1.8; 27; fs_min | 23 | 1.9; 27; fs_min | 21 |
| 1.7; 120; fs_min | 26 | 1.8; 120; fs_min | 24 | 1.9; 120; fs_min | 22 |

Table 4.2: PVT 81 corners with the corresponding resulting word

that delay performance results acceptable for the specific GEM detector front-end. EDS delay has been also evaluated under PVT spread.
Figure 4.2 presents the simulation results, highlighting what happens for minimum and maximum input charge. Note that in case of 30 fC input charge (which is the worst case for EDS delay), the delay remains around 30 ns or lower.
As concerns the Charge-Time-Signal, the voltage signal at the CSP output (that is the result of charge vs. voltage conversion), is then converted in time domain by CTS-Comp. In this way the front-end performs charge-to-time conversion. CTS impulse accuracy is very important in GEM detectors front-end [12]. So, linearity simulations have been run.

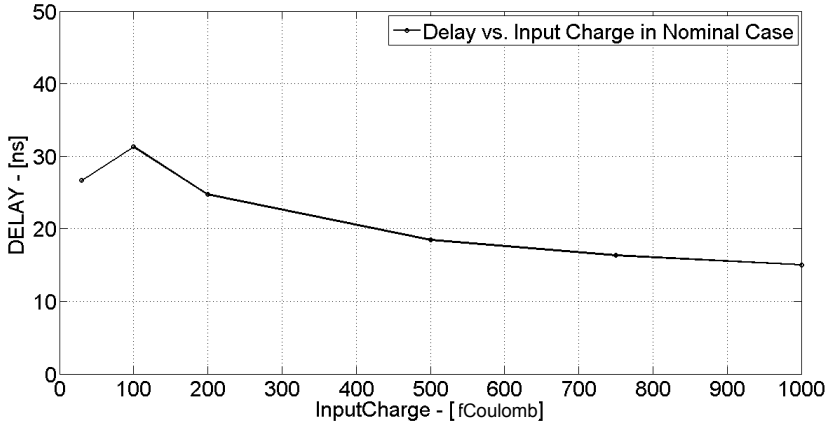


Figure 4.1: EDS delay vs. input charge in nominal case (from 30 fC to 1 pC)

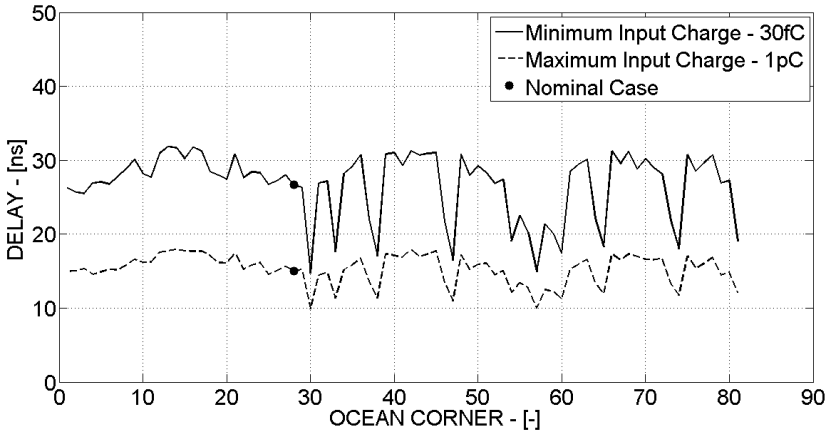


Figure 4.2: EDS delay vs. simulation corner (for 30 fC and 1 pC input charge)

### 4.1.1 Linearity

Figure 4.3 reports the CTS duration time vs. the input charge. Note that nominal case is highlighted (black-bold line). The maximum duration is about 100 ns, corresponding to the maximum input charge of 1 pC. Also the CTS pulse has been tested for several corners. Linearity performance are then plotted in figure 4.4, defined (for each input charge) as the deviation between nominal duration and effective CTS impulse duration. The linearity is expressed in percent values.
Note that the maximum deviation with respect to the nominal case is $\pm 5\%$, corresponding to 5 ns, over 100 ns of maximum CTS impulse duration. Note that EDS and CTS Ocean simulations demonstrate that the front-end performance does not change significantly under PVT variations. This is possible due to the specific design choice in charge-sensitive-preamplifier (the DC-gain does not reduce under 63 dB), and due

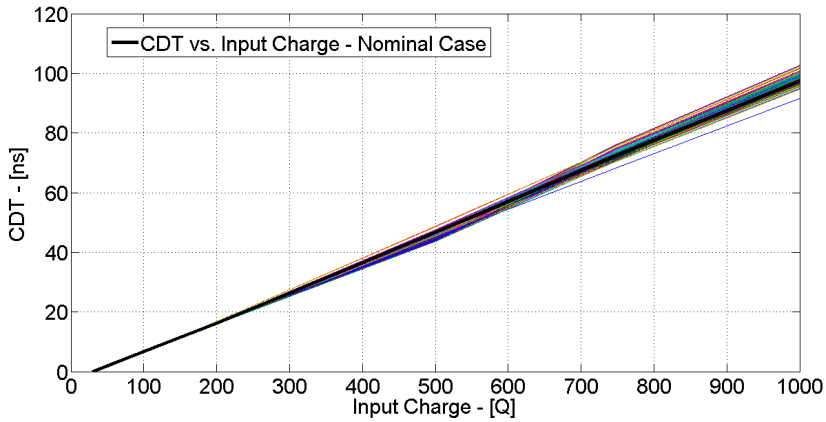


Figure 4.3: CTS duration vs. input charge vs. simulation corner

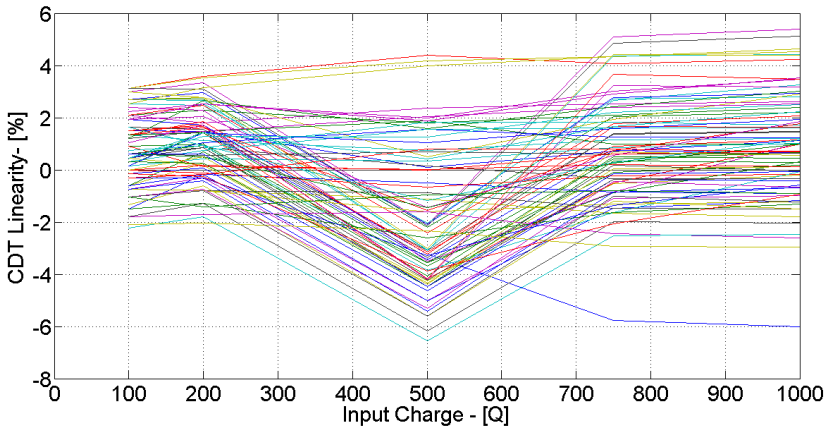


Figure 4.4: CTS linearity error vs. input charge vs. simulation corner

to the proper calibration circuit, which allows to achieve very precise ramp signal and to compensate technological spread in charge sensitive preamplifier Op-Amp. All that has been obtained, while reducing power, and technology $L_{MIN}$ with respect to the state-of-the-art [12].

### 4.1.2 Noise simulation

In this type of devices, the parameter which embodies the noise characteristics of the front-end channel is the Equivalent Noise Charge (ENC). This value represents the input charge corresponding to an output equal to the RMS noise only. It can be expressed in Coulombs or in electrons ($e^-$), with the obvious conversion. The considered noise comes from the preamplifier Op-Amp. In this simulation, the Input-Referred-Noise (IRN) has been calculated. Indeed, with a simple calculus, the ENC can be extracted.

One of the parameter needed is the sensitivity ($K_{CV}$), established at the beginning of the project to be 0.5 mV/fC. This fact because of the limited swing consequent to the reduced power supply. This choice avoids malfunctioning of the Op-Amp, due to the transistor working out of the saturation region, or even their switch-off.
The second parameter is the maximum bandwidth of the signal. This value corresponds to the inverse of the maximum integration time, namely 80 ns. So the bandwidth considered is 12.5 MHz.
The third parameter is, obviously, the IRN. In figure 4.5 the IRN plot is shown.

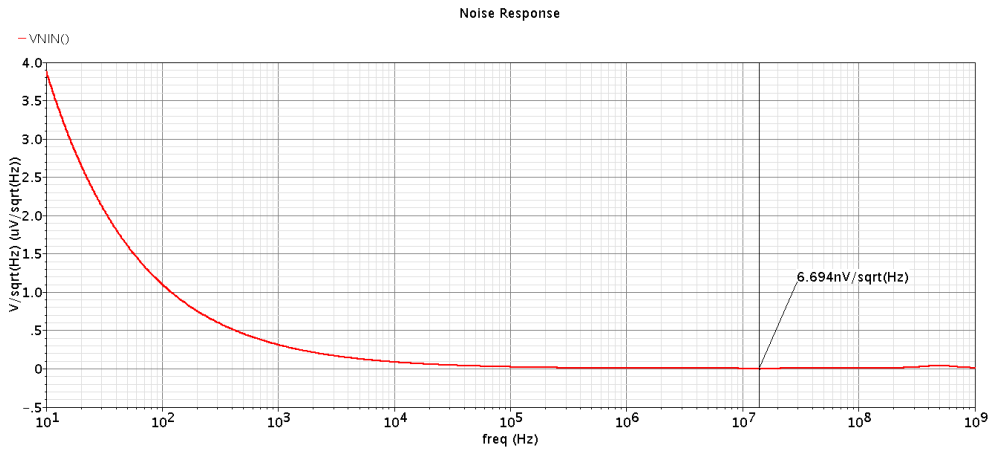


Figure 4.5: Preamplifier opamp IRN

Its minimum value is 6.69 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, agreeing with the initial requirements.
The output RMS noise value can be found with the equation 4.1:

$$v_{n_{RMS}} = \sqrt{2} \cdot IRN \cdot \sqrt{BW} = \sqrt{2} \cdot 6.69 \frac{nV}{\sqrt{Hz}} \cdot \sqrt{12.5MHz} = 33.5\ \mu V_{RMS} \tag{4.1}$$

Dividing the resulting RMS noise for the charge-voltage conversion, as shown in equation 4.2, the ENC can be calculated:

$$ENC = \frac{v_{n_{RMS}}}{K_{CV}} = \frac{33.5 \mu V_{RMS}}{0.5 \frac{mV}{fC}} = 6.7 \cdot 10^{-17} C \simeq 418\ e^- \tag{4.2}$$

As regards the Signal-to-Noise ratio (SNR), the output signal corresponding to the minimum input charge ($Q_{min} = 30fC$) is

$$V_{OUT} = K_{CV} \cdot Q_{min} = 15\ mV \tag{4.3}$$

Hence, the SNR will result

$$SNR = 20 \cdot \log_{10} \frac{V_{OUT}}{V_{n_{RMS}}} = 53\ dB \tag{4.4}$$

## 4.2 Measurements

### 4.2.1 Main Signals

In figures 4.6 and 4.7 the main GEMMA signals are shown. The plots are referred to the minimum (4.6) and the maximum (4.7) input charge. The signals are related to the CSP output, the EDS and CTS signals. It is noticeable the difference in CTS duration, which reflects the different input charge amount. The maximum dead time of the system is estimated to be 350 ns.

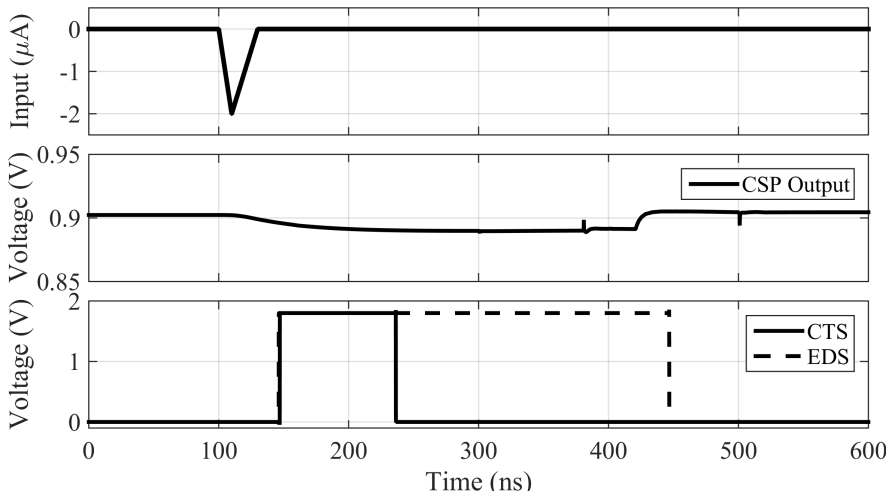


Figure 4.6: GEMMA Signals for 30 fC Charge

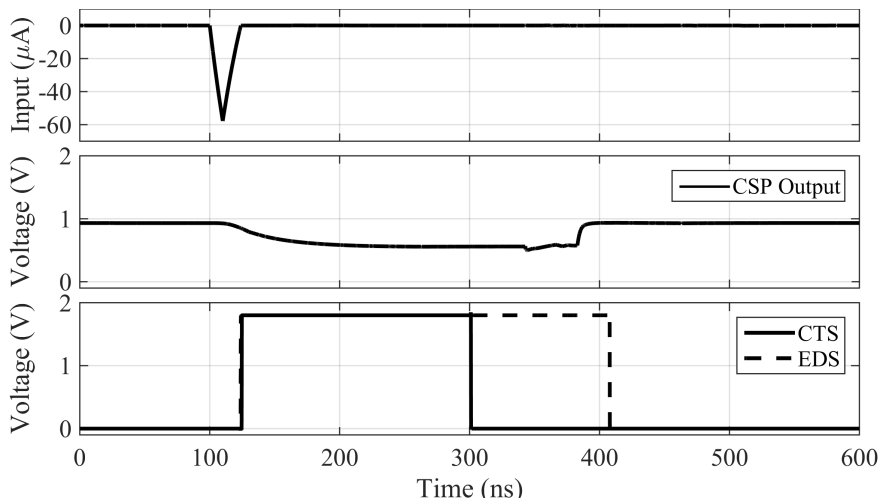


Figure 4.7: GEMMA Signals for 1 pC Charge

### 4.2.2 Linearity

In order to verify the system linearity, in figures 4.8 and 4.9 two plots are shown. Figure 4.8 clarifies the EDS signal delay with respect to the charge arrival instant, for the entire charge range and for different pad capacitances. The maximum delay condition occurs in case of minimum charge and maximum pad capacitance, as expected. The delay value is 38 ns. As regards the proportionality between input charge and CTS signal duration, figure 4.9 shows that a linear behavior is performed. A slight saturation occurs at maximum input charge, but the direct proportionality is maintained for all the pad capacitance values.

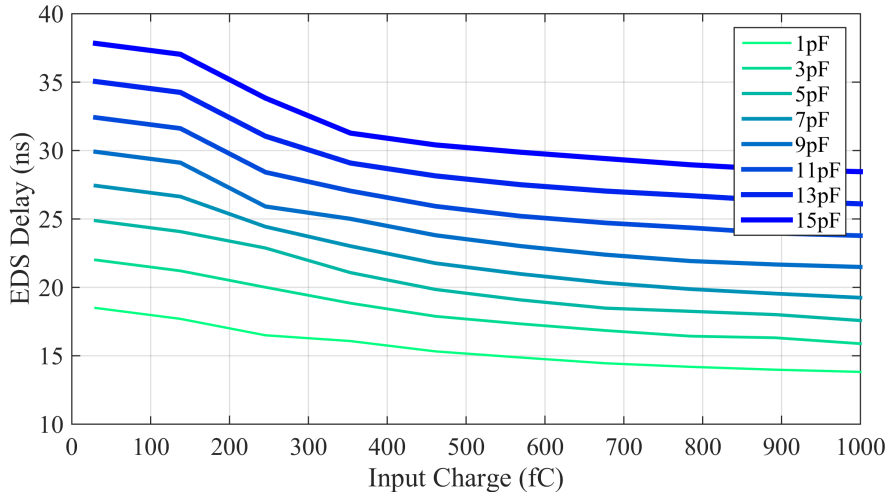


Figure 4.8: EDS Delay vs. Input Charge

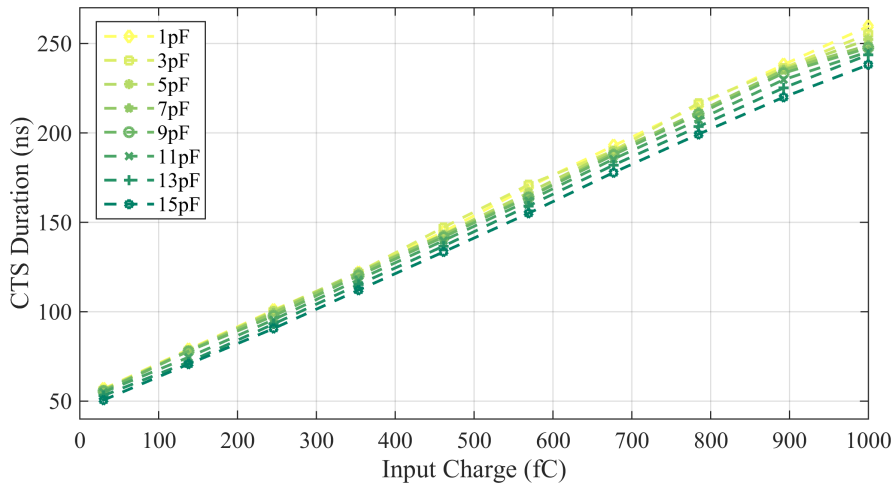


Figure 4.9: CTS Duration vs. Input Charge

### 4.2.3 Noise

In figure 4.10 the ENC is plotted for the entire range of pad capacitances. Ideally at 0 pF, the ENC is 417.5 $e^-$. The dependence from pad capacitance has been verified to be 208.7 $e^-$/pF. This fact allows to have, in the worst case, 0.28 $mV_{RMS}$ noise at the CSP output. So, with minimum charge hitting a 15 pF pad, a 15 mV signal is generated at the CSP output, with a consequent 34 dB SNR.

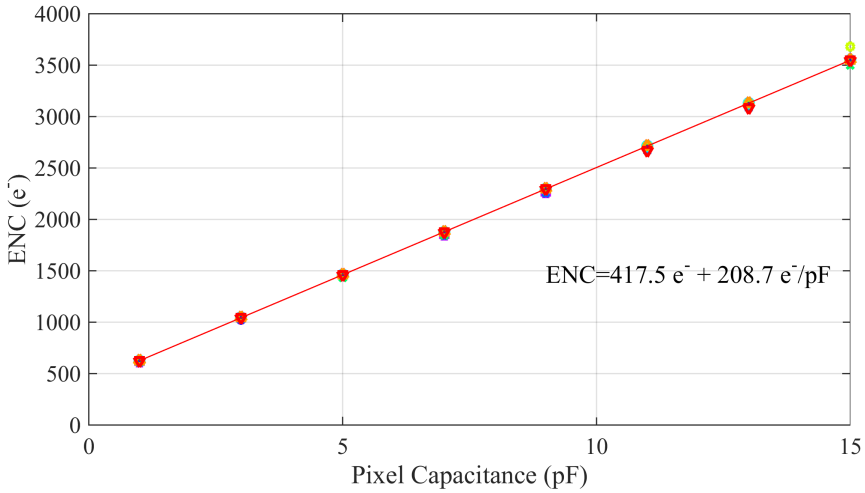


Figure 4.10: ENC vs. Pad Capacitance

# Part III

# GEMINI Prototype

# 5
# Front-End

## 5.1 Changing target

The GEMINI chip has different starting point considerations with respect to the GEMMA.
Indeed the portability constraint has been set to the most important feature. Therefore, the channel number has been increased to 16, in order to manage a doubled number of pixels with a single chip. This brings to reduce the overall system dimensions, moving towards a more compact solutions. On the other hand, the channel complexity has to be reduced for area and power consumption issues.
In addition to this, the portability issue leads to a wider range of input parasitic capacitor.
Not a secondary fact is represented by the detector output pads, manufactured in different size factors as shown in figure 5.1, which are a primary issue in the readout design. Their parasitic capacitance is directly involved in performance in terms of noise and efficiency.
As an example, 2.5 cm x 2.5 cm pads feature a 40 pF parasitic capacitance. So, while the GEMMA chip is able to sustain up to 15 pF, the GEMINI goes up to 40 pF, in order to comply with bigger pixel dimensions, specifically 2.5 cm x 2.5 cm.

## 5.2 GEMINI Channel Design

In figure 5.2 the GEMINI readout scheme is depicted. The SoC is made of 16 channels where, with the inclusion of a Charge-Sensitive Preamplifier (CSP), the signal from the detector is converted from charge to voltage domain. Then, the discriminator compares the CSP output voltage level with a channel-specific threshold, set by an R-2R Resistive DAC, generating the event detection output signal. The output is then converted into LVDS standard through a dedicated driver.

### 5.2.1 Charge-Sensitive Preamplifier

#### Operational Amplifier

The CSP composes of a Class-A Miller Op-Amp with $C_F$ capacitor connected in feedback, in parallel with a switch. Notice that, with respect to GEMMA, the $R_F$ feedback resistor is not included. In fact, the Op-Amp dc operating point is set with the complete discharge of $C_F$ capacitor. However, the reset switch has its own off-resistance, although it has a very high value ($\simeq 1\,G\Omega$).
The CSP sensitivity, $K_{QV}$, and the efficiency in charge collection from the detector, $\eta_Q$, are indicated in Eq. (5.1), depending from the Op-Amp Open-Loop DC Gain, $A$, $C_F$ and $C_D$, the detector parasitic capacitance. The ENC dominant contribution can be

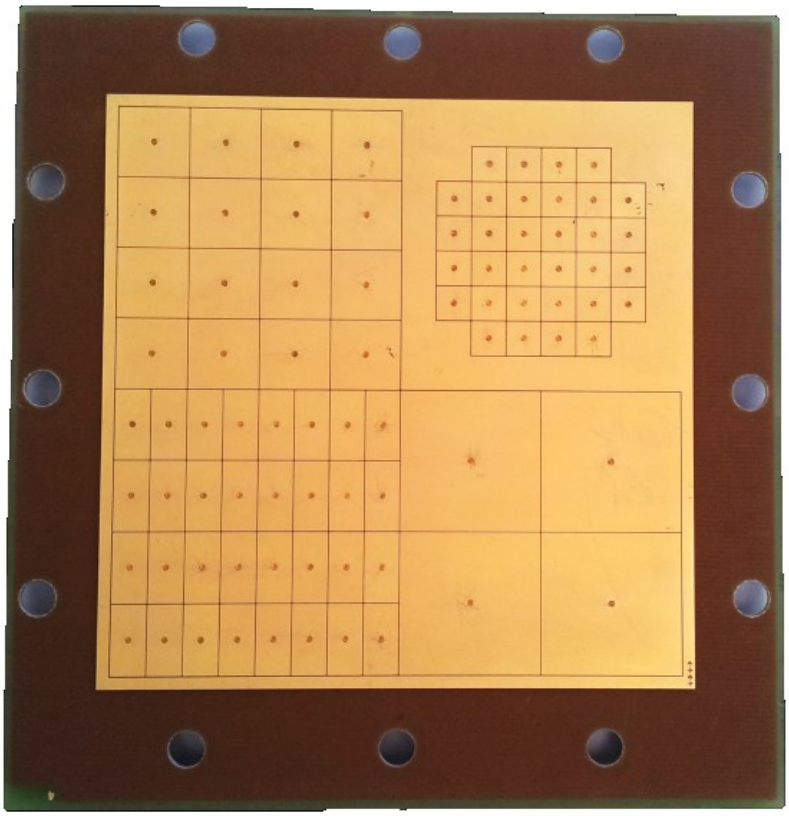

Figure 5.1: GEM Output Pads

calculated as in Eq. (5.2), starting from the input in-band integrated noise, $v_{ni_{OPAMP}}$.

$$K_{QV} \simeq \frac{1}{C_F}; \quad \eta_Q = \frac{1}{1 + \frac{C_D}{C_F(A+1)}} \tag{5.1}$$

$$ENC \simeq v_{ni_{OPAMP}}(C_D + C_F) \tag{5.2}$$

Note that $C_F$ is the only parameter to set the sensitivity, as well as $C_D$ plays a critical role on ENC. On the other hand, the efficiency can be maximized increasing the Op-Amp DC-Gain. So the Op-Amp design is a key-point. The sensitivity imposed by specifications sets directly $C_F$ to 1 pF. Imposing the ENC to be 2 fC with a 40 pF $C_D$ in order to comply with the minimum detectable charge, the Op-Amp has been designed to obtain 65 dB DC-Gain and 50 $\mu V_{RMS}$ input in-band integrated noise. The efficiency so is 98%.
At the same time for Equivalent-Noise-Charge (ENC) performance, Input-Referred-Noise (evaluated as spot noise on the middle of the preamplifier bandwidth) should be lower than $5\,nV/\sqrt{Hz}$ to match minimum threshold requirements. Unity gain

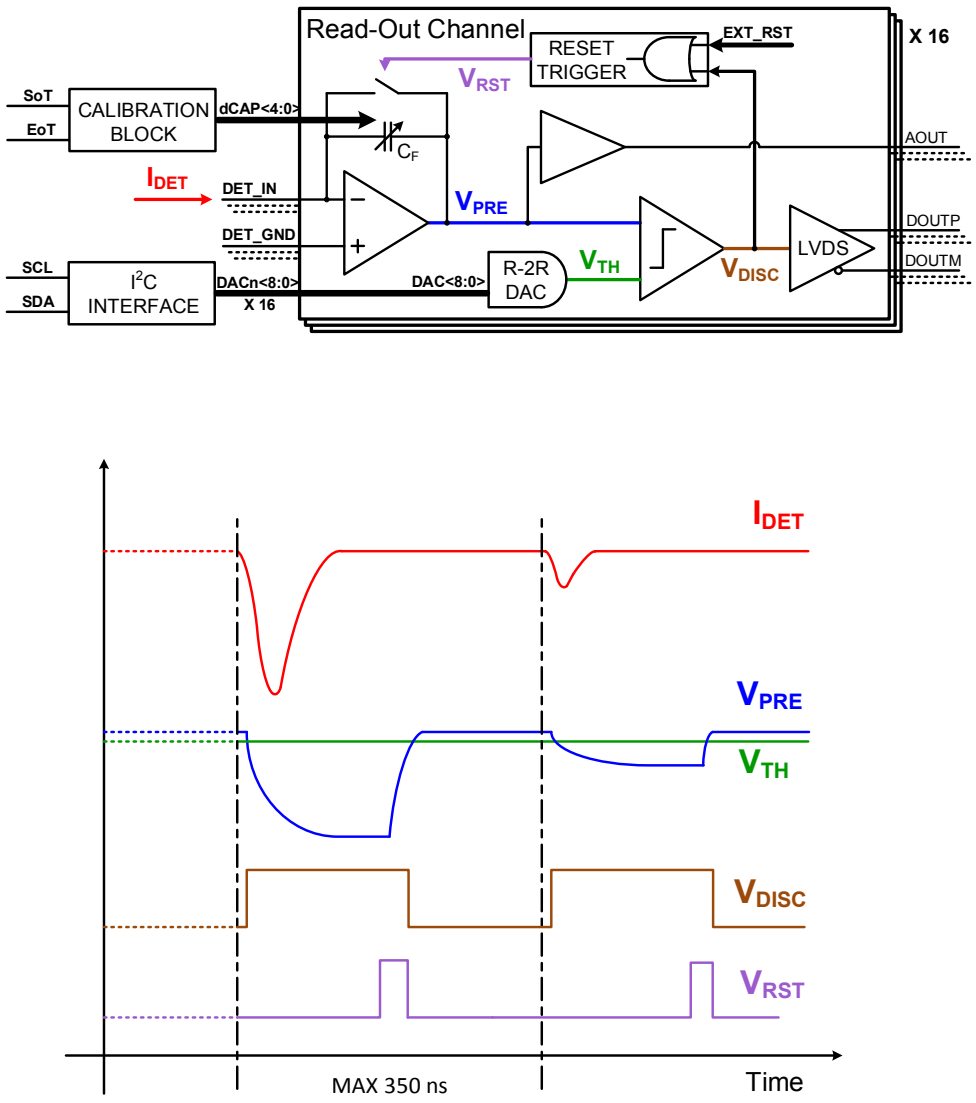


Figure 5.2: The GEMINI SoC Block Scheme

bandwidth is then fixed by rise/fall time requirements. A resume of the most important Op-Amp specifications is reported in table 5.1. Note that for stability reasons at least a 60° Phase Margin is required. In Figure 5.3 the Op-Amp schematic is shown, while in table 5.2 the transistor dimensions are listed.

### 5.2.2 Discriminator

As regards the discriminator (DISC), the main target is to reduce the input stage offset, in order to achieve the sensitivity and the detection jitter required (3 fC and 9 ns respectively). This means that the maximum tolerated offset is 3 mV after the CSP

| **Parameter** | Value |
|---|---|
| DC-gain ($A_0$) | $= 65\,\mathrm{dB}$ |
| Unity-Gain-Bandwidth (UGB) | $> 100\,\mathrm{MHz}$ |
| Input-Referred-Noise (IRN) | $< 5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ |
| Phase Margin | $> 60°$ |

Table 5.1: GEMINI Operational Amplifier requirements

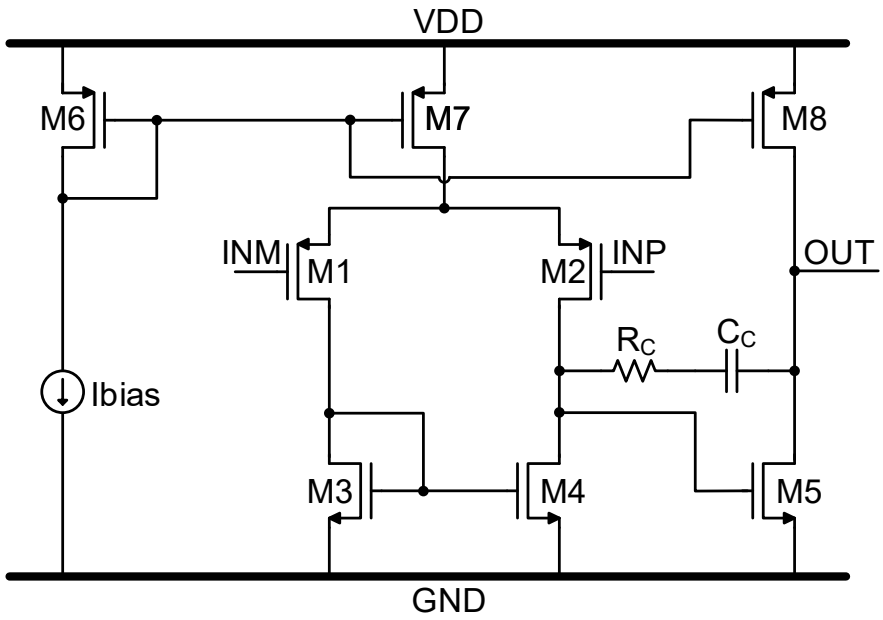


Figure 5.3: GEMINI Operational Amplifier schematic

| Transistor | W | L | Transistor | W | L |
|---|---|---|---|---|---|
| M1 | 200 µm | 0.3 µm | M5 | 200 µm | 0.4 µm |
| M2 | 200 µm | 0.3 µm | M6 | 40 µm | 2.55 µm |
| M3 | 60 µm | 0.4 µm | M7 | 160 µm | 2.55 µm |
| M4 | 60 µm | 0.4 µm | M8 | 280 µm | 2.55 µm |

Table 5.2: List of GEMINI CSP Op-Amp transistors dimensions

conversion. Designing the discriminator with a mirrored structure and exploiting the inter-digitated layout technique allows to limit the offset within specs. At the same time, since the detector charge polarity is intrinsically negative (the signal is generated by electrons), the CSP output signal embeds a decreasing behavior. For this reason, a PMOS discriminator input stage has been preferred to NMOS. In figure 5.4 the schematic of the comparator is drawn, while in table 5.3 the transistor dimensions are listed.

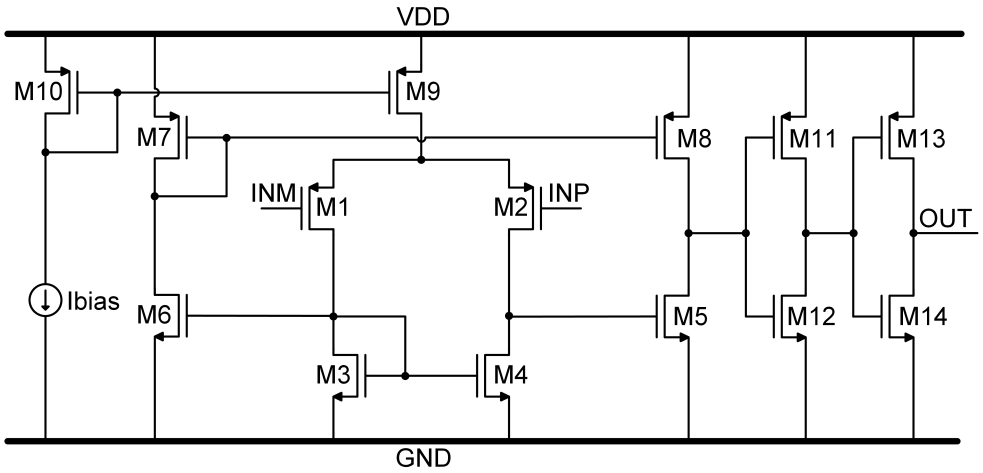


Figure 5.4: GEMINI Discriminator schematic

| Transistor | W | L | Transistor | W | L |
|---|---|---|---|---|---|
| M1 | 200 µm | 0.5 µm | M5 | 100 µm | 0.3 µm |
| M2 | 200 µm | 0.5 µm | M6 | 100 µm | 0.3 µm |
| M3 | 160 µm | 0.5 µm | M7 | 100 µm | 0.3 µm |
| M4 | 160 µm | 0.5 µm | M8 | 100 µm | 1 µm |

Table 5.3: List of GEMINI Discriminator transistors dimensions

### 5.2.3 Threshold DAC

Dealing with the threshold, the 9-bit R-2R Resistive DAC has a 1.2 mV LSB and 500 mV full-scale. The LSB has been set according to the minimum threshold required to make the channel to trigger after a 2 fC charge has been integrated. The R-2R Architecture has been chosen in order to avoid large area occupation while maintaining a high resolution. More complicated structures have been investigated, but for sake of simplicity and compactness, this architecture demonstrates to fit better the task. The resistor R value has been chosen in order to comply with the area/power trade-off, and it corresponds to 20 kΩ. In order to keep the output signal stable, a buffer has been placed before the DAC output. Notice that this DAC has to operate statically, so the buffer has been designed with a very low bandwidth, to avoid high frequency noise, and to guarantee a better output voltage stability in time. For design issues, the Op-Amp employed to realize the buffer is the same of the CSP, but with a reference current lowered by a factor of 2. In Figure 5.5, the DAC schematic is shown. The input digital words, independent for each channel, are stored into dedicated registers managed by the $I^2C$ interface.

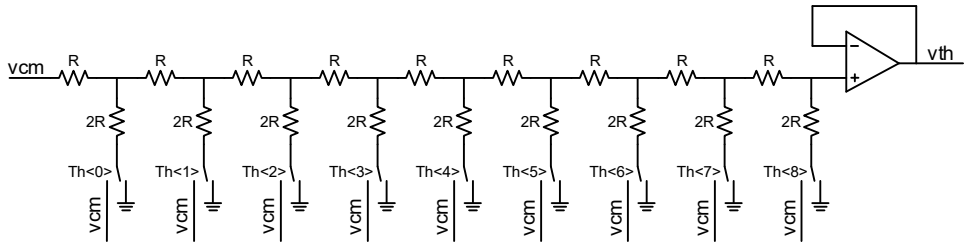


Figure 5.5: GEMINI DAC schematic

### 5.2.4 Reset Trigger

The event-driven reset signal is generated starting from the DISC output. In fact, with the simple use of a passive RC net and an OR logic gate, the reset pulse delay can be set. In detail, the RC time constant is applied to the DISC output signal and sent to one OR input. When the voltage is high enough the OR switches high, closing the CSP feedback switch. The other OR input can be used as a general channel reset. In this case, a 150 ns time constant has been set.

### 5.2.5 LVDS Driver

The DISC output signal, containing the arrival time information of the input charge, needs to be transmitted through very long cables. In fact, for some applications [18] the control room is up to 30 m far from the detector location. With this distance, the length of the cables can compromise the pulse quality. A long cable can affect either the pulse amplitude for resistive attenuation or the edges sharpness, due to capacitive/inductive effects. In this case, the information to take care of is represented by the rising edge of the pulse timing, but also the amplitude has not to be attenuated below the receiver threshold voltage, in order to be always detected.
For this reason, the LVDS standard [19] has been chosen for the EDS output pulse. This standard is common for these systems, due to several reasons. With its differential structure, there is tight electric and magnetic field coupling between the two wires, reducing the generation of electromagnetic noise. This reduction is due to the equal and opposite current in the two wires. LVDS receiver is also unaffected by common mode noise because it senses the differential voltage.
Moreover, the fact that LVDS transmitter consumes a constant current also places much less demand on the power supply decoupling and thus produces less interference in the power and ground lines of the transmitting circuit. This reduces or eliminates phenomena such as ground bounce, typically seen in terminated single-ended transmission lines.
The drawbacks are essentially two. The first is overall power consumption. This standard sets that with a 100 Ω differential load, a 400 mV pulse amplitude should be maintained. This means that the driver has to drive a 4 mA current, more than the entire channel consumption in this case. The second is the output pads number, doubled. This 16 channel prototype has 32 output pads only for output signals. It is

straightforward that this type of solution is limiting the number of channels due to the number of I/O pads.
In this chip, an auto-biased LVDS driver has been designed, as in Figure 5.6. The current flow is always constant, due to the presence of current drivers (PMOS on top and NMOS on bottom) enabled alternatively with the output signal level.

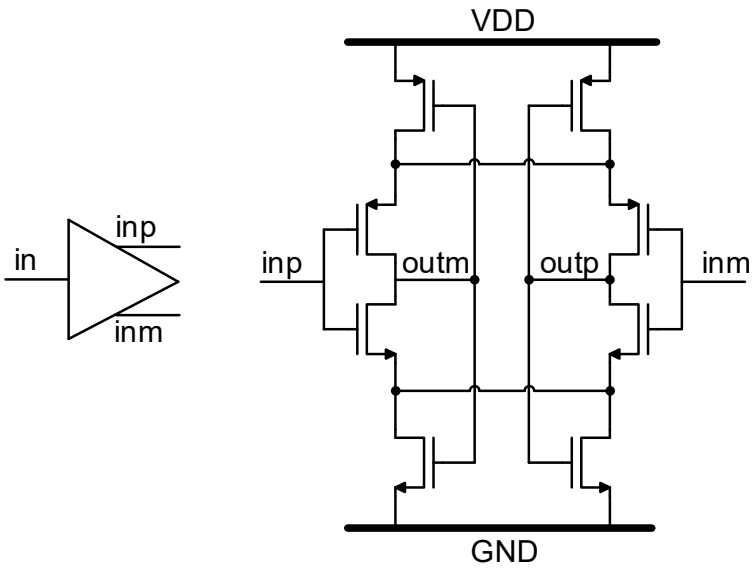


Figure 5.6: GEMINI LVDS Driver schematic

### 5.2.6 Calibration Circuit

The calibration circuit implemented into GEMINI is very similar to the one included in GEMMA. The capacitor to be tuned has a 1 pF nominal value. With the 12.5 MHz clock frequency, the main parameters are those listed in table 5.4. The Op-Amp is the same employed for DAC, with reduced current reference by the same factor.

| Parameter | Value |
|---|---|
| Current | 1.25 µA |
| Accuracy | 5% |
| Number of bits | 5 |
| Nominal End Level | 500 mV |
| High threshold | 504 mV |
| Low threshold | 496 mV |

Table 5.4: List of GEMINI Calibration Block Parameters

# 6
# Layout

## 6.1 Calibration circuit layout

The figure 3.2 presents the calibration circuit block layout.
It is composed by the analog part on left side, and the digital part on right side. Notice the symmetry of comparators layout, in order to achieve the better matching as possible between the two threshold settings.

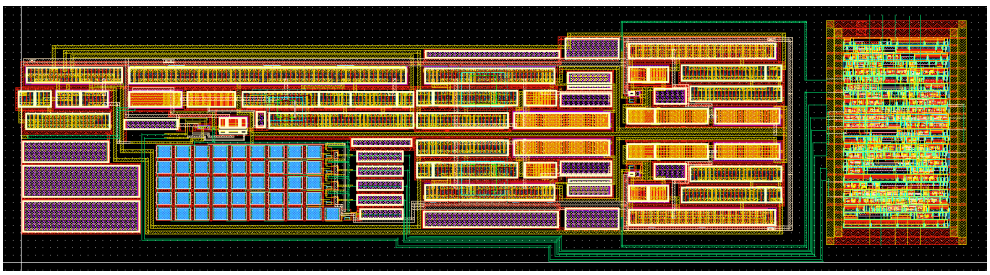

Figure 6.1: Calibration circuit layout

## 6.2 Channel Layout

### 6.2.1 Charge-Sensitive Preamplifier

The CSP layout is presented in figure 6.2. On the left side, the Op-Amp has been placed, with an horizontal (left $\rightarrow$ right) signal propagation.
All the stages exploit inter-digitated technique, for mismatch minimization.
On the right side, the feedback capacitor array is clearly visible, where all single array capacitors has been built with the same unit capacitor, always for matching purposes.

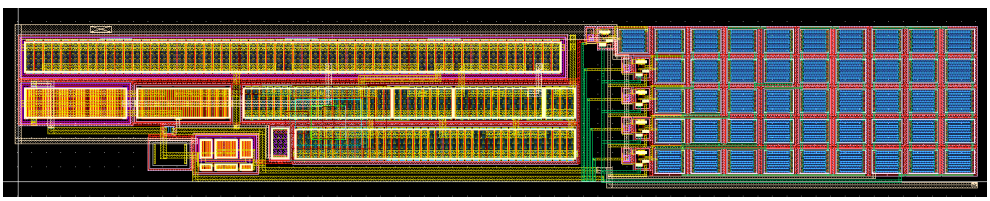

Figure 6.2: Preamplifier layout

### 6.2.2 Discriminator

Figure 6.3 reports the discriminator layout. On the bottom side, the core transistors has been placed, again with inter-digitated structure.
The signal propagation is always left $\rightarrow$ right. The mirrored structure is perfectly symmetrical with respect to the two inputs, in order to limit the offset.

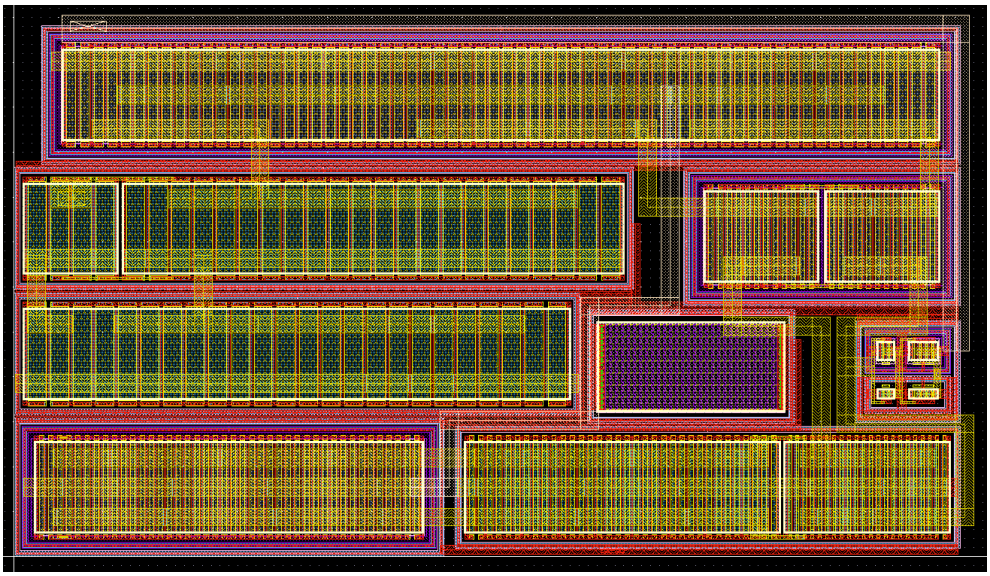

Figure 6.3: Capacitors array layout

### 6.2.3 Threshold DAC

The R-2R Threshold DAC layout is presented in figure 6.4.
The buffer has been placed on the left side, to reduce the common mode signal path length, since this is a chip input, placed on the left side of the core. On the right side there is the DAC, with resistor on top and switches on bottom.
Notice that the threshold 9-bit word is expected to come from the right side, avoiding any coupling with the input detector signal.

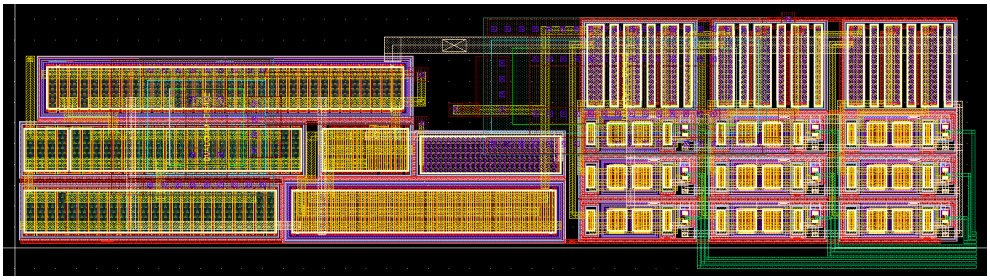

Figure 6.4: R-2R Threshold DAC layout

### 6.2.4 Whole channel and core

In Figure 6.5 there is the complete layout of the detecting channel.
Going from left to right, the CSP has been placed, followed by the analog buffer (the Op-Amp layout is the same as CSP Op-Amp), the Discriminator and at the end the DAC.
The layout has been forced to be horizontal, in order to realize a compact 16 channel structure, and to distribute the signal from left to right side of the chip, as clearly noticeable in figure 6.6.
The 16 channels are placed in the middle of the core, with the $I^2C$ system above and the calibration block below. The LVDS drivers are placed next to their output pads, on the chip right side. The whole chip occupies a 6.72 $\mathrm{mm}^2$ area.

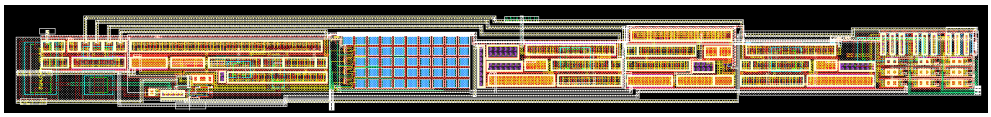

Figure 6.5: Detecting channel layout

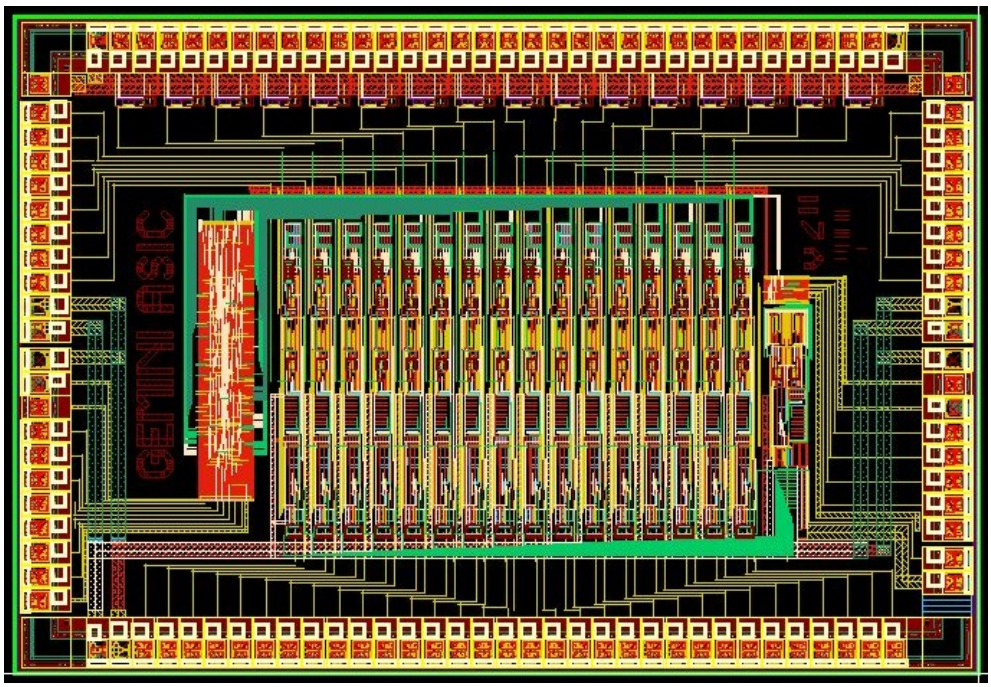


Figure 6.6: GEMINI ASIC complete layout

# 7
# Performance

After parasitic extraction, transient noise and Monte-Carlo post-layout simulations have been run, including temperature variation between −40 °C and 120 °C, as well as supply voltage 10% maximum spread.
The input pixel capacitance has been set to 40 pF. This worst-case scenario represents an optimum testbench also for radiation hardness. Although measurements during irradiation are a must, these results can prove for an overall robustness.

## 7.1 Transient Noise Monte Carlo CSP Simulation

Figure 7.1 shows the transient noise simulation related to the CSP output signal generated from the minimum input charge (30 fC). This simulation demonstrates that, also with the 40 pF pixel capacitance, the CSP design is valid in terms of noise, since setting the threshold for the minimum detectable charge specification (3 fC) will not generate false-positive events.

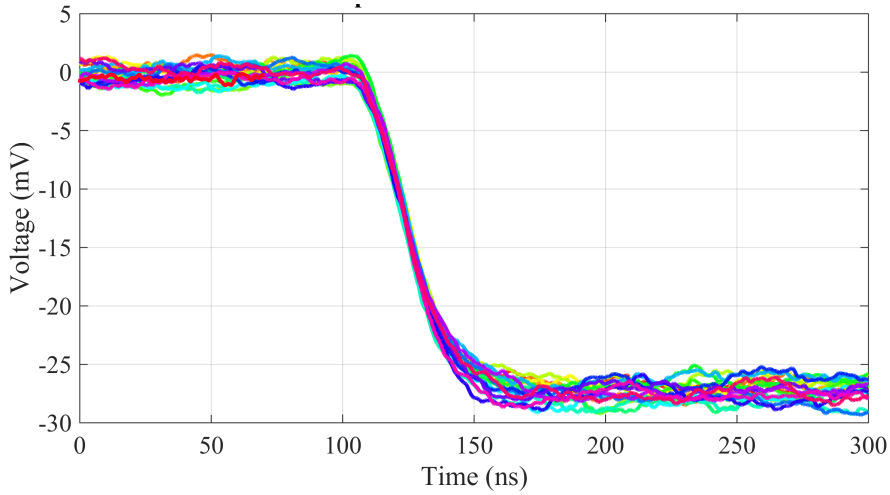


Figure 7.1: Post-Layout Transient Noise CSP Simulation

Figures 7.2 and 7.3 show the Monte-Carlo results. Together with the input signal, the channel analog and the digital outputs are shown. Note the effect of event-triggered reset on output signals. This evident spread in reset time (25 ns) is justified by reset time constant variation (passive RC net) due to CMOS process. This variation is not critical, since the output signal does not contain any information in the time duration. On the contrary, the trailing edge is very precise through corners, with a 7.7 ns maximum spread.

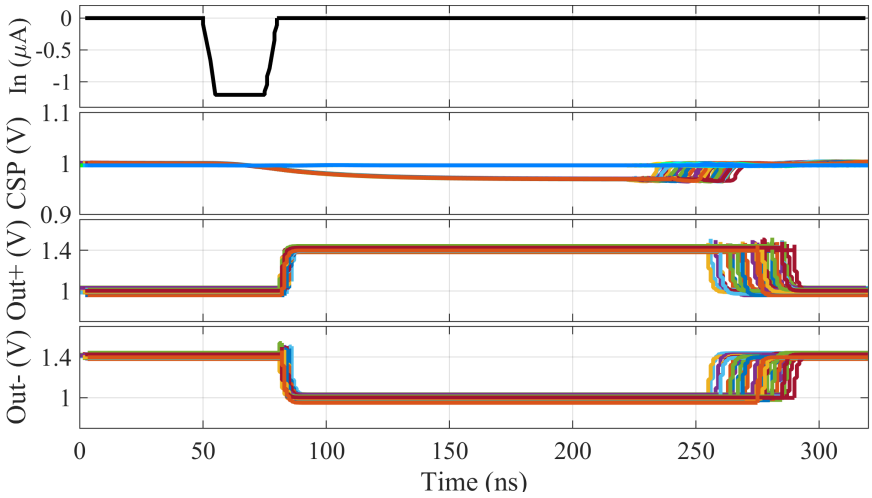


Figure 7.2: Post-Layout Monte-Carlo Simulation Results (Min Q)

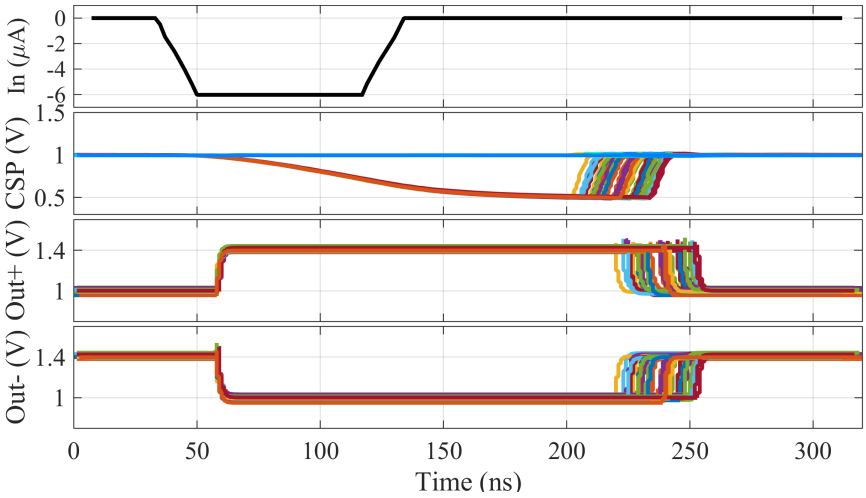


Figure 7.3: Post-Layout Monte-Carlo Simulation Results (Max Q)

## 7.2 Measurements

### 7.2.1 Test Equipment

In order to characterize the prototype, a board has been designed. It is shown in figure 7.4, together with the testing apparatus. A proper software for $I^2C$ control has been written, allowing to set the device through a GUI interface, with the use of a C232HM cable from FTDI. Figure 7.5 is the first prototype of GEMINI cards, designed appositely to be plugged on the rear side of the GEM anode.

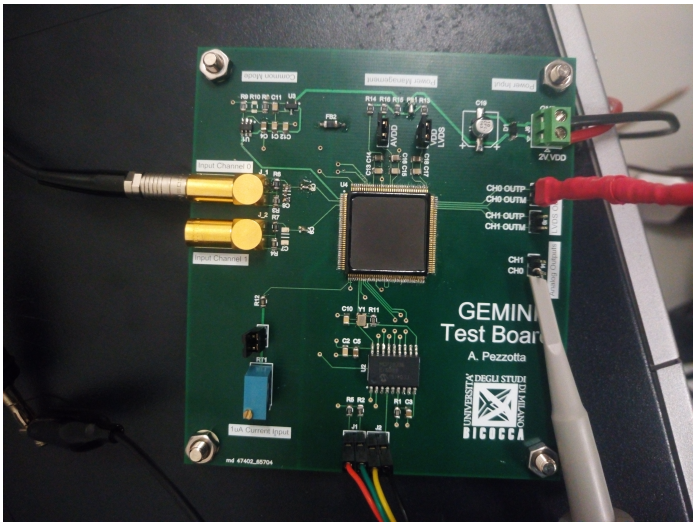


Figure 7.4: GEMINI Test Board

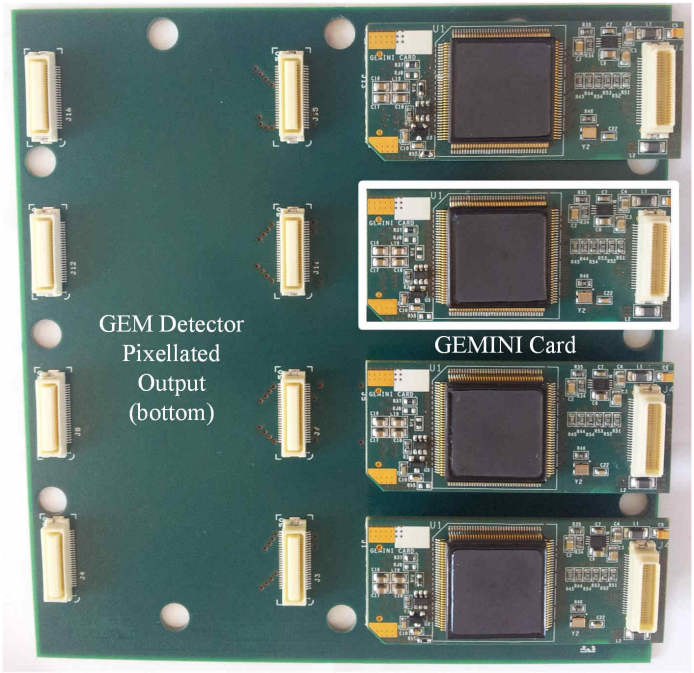


Figure 7.5: GEMINI System

### 7.2.2 Main Signals

Figures 7.6 and 7.7 show the GEMINI main signals. Together with the input signal, the analog and digital outputs are shown for minimum and maximum charge cases in figure 7.6 and 7.7 respectively. Notice that LVDS pulse duration is fixed (Sect. 5.2.4), and is 180 ns. The variation with respect to the design value (150 ns) is linked to the specific CMOS R-C process variation of the sample.

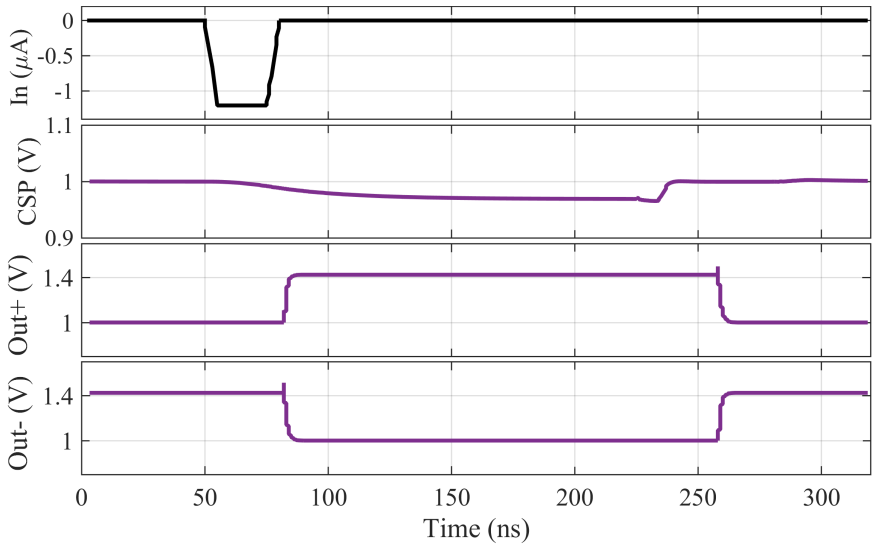


Figure 7.6: GEMINI Signals for 30 fC Charge

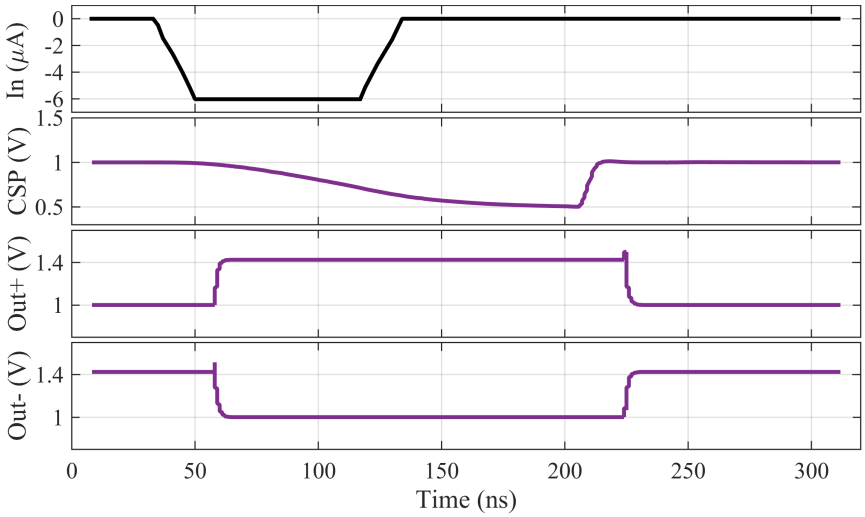


Figure 7.7: GEMINI Signals for 500 fC Charge

### 7.2.3 Triggering Delay and Jitter

To clarify the timing performance of GEMINI, in Figure 7.8 the detection delay is plotted versus the input charge, with different pixel capacitance values. The global effect of delay reduction is evident while decreasing the pixel capacitance value, but also is the delay spread over the entire charge range.
In fact, in Figure 7.9 the detection jitter is depicted versus the pixel capacitance, showing a maximum value of 7.7 ns.

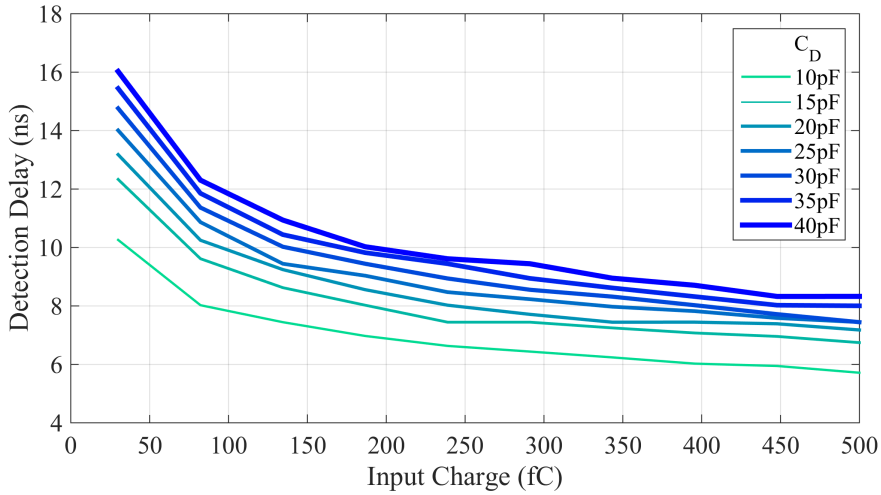


Figure 7.8: Detection Delay vs. Input Charge

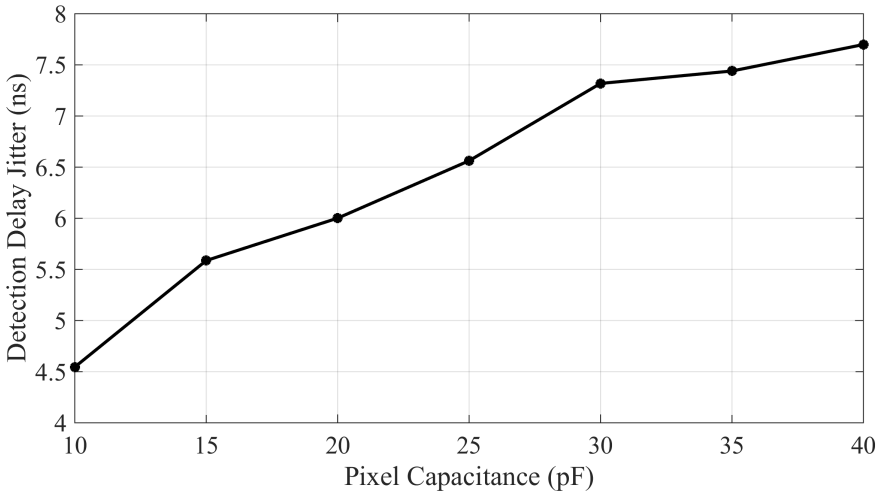


Figure 7.9: Detection Jitter vs. Pixel Capacitance

## 7.3 Noise

As regards noise performance, the ENC dependence from the pixel capacitance is plotted in Figure 7.10. The results confirm Eq. (4.2), with a linear dependence from the input pixel capacitance. The maximum ENC value, obtained with maximum pad capacitance (40 pF), is 1.48 fC, making GEMINI to trigger a 2 fC charge with a 2.6 dB SNR. Notice that no more efforts are needed to reduce noise in this case. In fact this would have brought to an increase in power consumption, with no evident advantages in terms of performance.

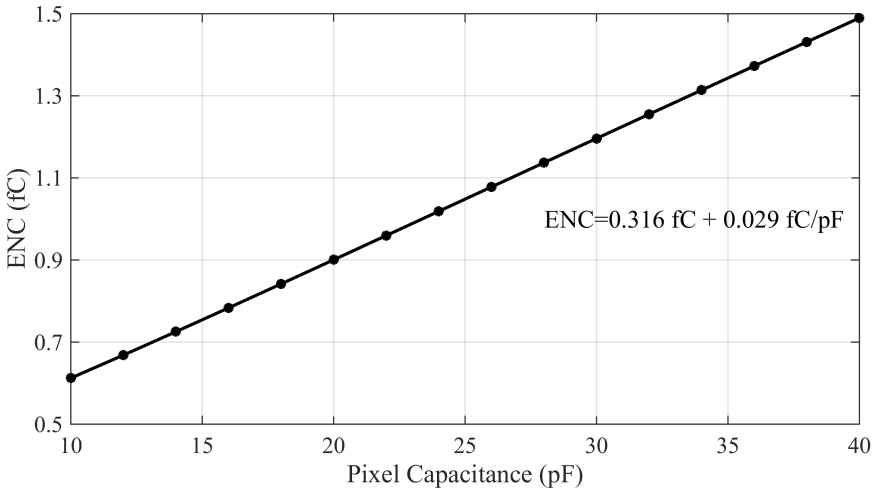


Figure 7.10: ENC vs. Pixel Capacitance

# Part IV

# Papers

# 8
# GEMMA Related Papers

The papers dedicated to GEMMA are listed in the next pages.
The first has been presented at IEEE ICECS 2012 Conference in Sevilla, Spain. It deals with a general overview of the ASIC.
The second, presented at IEEE ICICDT 2013 Conference in Pavia, Italy, is dedicated to the GEMMA Preamplifier, while the third, presented at IEEE IWASI 2013 Conference in Bari, Italy, goes in a deeper detail about the calibration system.

# 8.1 IEEE ICECS 2012

## A CMOS 0.13µm Low Power Front-End for GEM detectors

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***Abstract*— A low power front-end for GEM (Gas Electron Multiplier) detectors has been developed in 0.13µm CMOS node. The front-end sensitivity is 0.5mV/fC which remains almost unchanged up to a 15 pF detector parasitic capacitance. The input dynamic charge range varies from 30fC to 1pC including only a single (negative) polarity charge. The front-end provides as output signal two different time-domain square-wave signals.**

**The first one indicates the charge detection event and the second one the amount of charge (providing a time-domain impulse, whose duty-cycle is proportional to the effective charge read by the front-end). Proper automatic calibration circuits are then implemented in order to optimize the front-end performance in case of CMOS process and temperature variations. The power consumption is 3.8mW, against 12mW in the existing market solutions[9]. A feed-forward opamp architecture has been exploited in analog part of read-out channel, in order to improve speed and time-response slope.**

### I. INTRODUCTION

In several fields such as biology, biomedical, high energy physics experiments, dedicated electronic read-out interfaces are required[1]-[4]. In particular deep CMOS and BiCMOS technologies have been exploited for entire read-out channel implementation. This trend is justified by the intrinsic portability a of a fully-integrated mixed-signal circuits, strengthened by low-power operation in the most scaled CMOS technologies. CMOS scaling-down leads to lower standard supply voltage, and as a consequence lower power. Moreover, a significant performance increasing has been observed in CMOS digital circuits in terms of speed and complexity. On the other side analog design becomes more critical and radiation effects should be taken into account, by exploiting proper layout techniques.

In this paper a complete read-out front-end for Gas Electron Multiplier detectors is presented. The system is a fully-integrated mixed-signal System-on-Chip, in 0.13µm CMOS node, able to detect from 30fC up to 1pC, managing a very large GEM sensor parasitic capacitance (about 15pF connected to the read-out input pad).

It is composed by the analog charge-sensitive-preamplifier (responsible of charge conversion into voltage domain), and by an additional calibration circuit able to optimize on-chip (and automatically) the front-end performance. The output signal is available as two different time-domain impulses. The charge Detection-Impulse (Charge-DI) indicates the charge detection event, while the charge Detection-Time (DT) provides a time-domain impulse, whose duty cycle is proportional to the effective charge read by the preamplifier.

The preamplifier is the interface block between off-chip GEM sensor and CMOS front-end. For this reason it should exhibit low-noise and fast time-response. The selected 0.13µm CMOS technological node improves noise performance, while the charge-sensitive-preamplifier design becomes more challenging [5]. In deep sub-1µm CMOS technologies, MOS transistors feature larger transconductance $g_m$ (at the cost of lower output resistance $r_{ds}$), and that improves speed and reduces noise power[6]-[8]. In this scenario, the charge-sensitive preamplifier of the GEM front-end becomes more and more challenging, because transistor intrinsic gain globally decreases (defined as $g_m \cdot r_{ds}$ product). Transistor intrinsic gain is pretty poor in CMOS 0.13µm node, comparing with similar works implemented in 0.35µm and 0.25µm technologies[9][10], and cascode stages are not feasible due to the low-voltage supply. For this reason analog preamplifiers should distribute horizontally the gain leading to critical stability and power consumption issues.

The paper is organized as follows. Section II illustrates the most important characteristics of the entire front-end. Section III presents the preamplifier basic schematic and the adopted design choices in order to guarantee stability while saving power. In Section IV simulation results are presented in nominal conditions and spreading CMOS process, supply voltage and temperature (PVT simulations). At the end of the paper conclusions will be drawn.

### II. SYSTEM OVERVIEW AND REQUIREMENTS

The basic scheme of the front-end channel is presented in Fig. 1. The analog Preamplifier converts the input charge signal into voltage domain, while two Comparators (DI-Comp and DT_Comp) are used for charge detection and duty-cycle vs. charge impulse. The front-end in Fig. 1 has been designed specifically for negative charged particles. The ultimate aim is to measure the arrival time (Charge-Detection-Impulse) and the amount of charge generated by the GEM sensor (Charge-Detection-Time). The entire system in Fig. 1 is composed by the GEM sensor, the Analog Front-End and the Calibration and Control circuit.

#### *A. GEM Sensor*

The input charge time-duration must enter into a 30ns up to 100ns range[9]. The input pulse shaping is reported in Fig. 2, and features different rise and fall time, respectively as 1/3 and 2/3 of the total time duration. The input charge can assume values from 30fC up to 1pC with a 15pF sensor parasitic. In order to allow a 30fC minimum threshold, the Equivalent Noise Charge should not exceed 5fC. In Fig. 2 a complete time-diagram of the most important front-end signals is available. The input charge is the signal to be detected/converted into voltage domain. Charge-Detection-Impulse is available when an input charge higher than 30fC is detected by the front-end. Charge-Detection-Time duration is directly proportional to the input detector charge. Such signal is generated by DT-Comp in Fig. 1, where preamplifier output voltage is compared with a negative constant-slope ramp.

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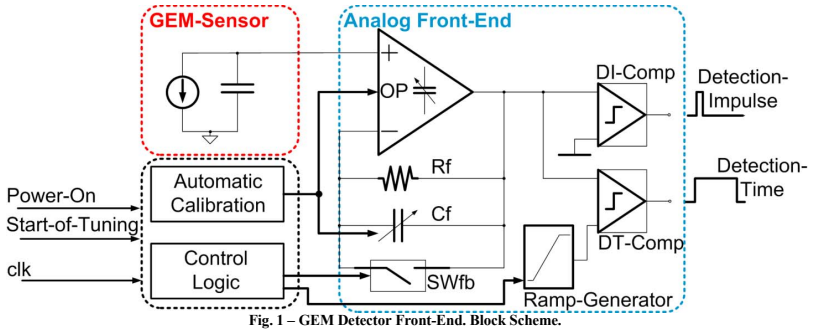


**Fig. 1 – GEM Detector Front-End. Block Scheme.**

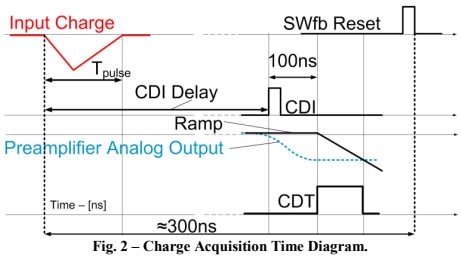


**Fig. 2 – Charge Acquisition Time Diagram.**

*B. Analog Front-End*

Signal coming from GEM sensor goes through the charge-sensitive preamplifier, composed by passive feedback net Cf-Rf, the reset switch SWfb, and the single-ended Opamp. Rf (set vey high, about 1MΩ) maintains input/output opamp operating point. By closing SWfb it is possible to set common-mode voltage at the opamp input/output node. Such operation is required every time a Charge-Detection-Impulse occurs, and once the Charge-Detection-Time signal is available. After being integrated, the signal enters into two different comparators. *Detection-Impulse-Comp* detects the arrival time of pulses. *Detection-Time-Comp* has a dynamic threshold which is a down-going ramp. The intersection between the ramp with the preamplifier output voltage represents the charge-detection-time, and it is proportional to the amount of charge coming from the GEM sensor. Basically the front-end here presented is able to perform a charge vs. time conversion. Ramp signal for voltage vs. time conversion is generated by a proper Ramp-Generator circuit, whose implementation is very simple, since it is based on a constant current charging a capacitor during a constant time. A very precise external current is provided, while variable capacitors are tuned by the calibration circuit in order to guarantee a very precise ramp signal (+/-5%).

*C. Automatic Calibration and Control Logic*

Calibration circuit is used for process and temperature spread compensation. In CMOS technology capacitors and transistor small-signal parameters suffer form technological spread, leading to a 10/20% variation with respect to the nominal value[7]. For this reason a proper calibration circuit is used to align preamplifier gain and ramp slope, making the front-end robust in front of process/temperature spread.

This task is entirely implemented on-chip, and the calibration circuit is able to start automatically the tuning procedure at the power-on signal. A small control logic is then needed in order to manage the calibration algorithm start, and the analog front-end calibration.

## III. Read-Out Front-End Design

*A. Opamp*

The GEM sensor parasitic capacitance can attenuate the charge-to-voltage conversion. In order to avoid voltage signal degradation system-level analysis has demonstrated that at least 60dB of dc-gain are needed for Operational Amplifier. In this way, due to the virtual ground principle, the charge-sensitive preamplifier features very low input impedance.

Moreover, taking into account possible dc-gain drop, due to PVT and aging, 70dB dc-gain has been required. Since rising time should be about 1/3 of the total time duration (100ns), output slew-rate for the Operational Amplifier (OP in Fig. 1) is about 16.6V/µs. At the same time for Equivalent-Noise-Charge performance, Input-Referred-Noise (evaluated as spot noise on the middle of the preamplifier bandwidth) should be lower than 5nV/√Hz. Unity gain bandwidth requirements are then fixed by rise/fall time requirements. A resume of the most important Opamp requirements is reported in Tab. I. Note that for stability reasons at least 60° of Phase Margin are required.

| Parameter | Value |
|---|---|
| dc-gain ($A_0$) | >70dB |
| Unity-gain-bandwidth (ugbw) | >120MHz |
| Input-Referred-Noise (IRN) | <5nV/√Hz |
| Phase Margin | >60° |
| External Slew-Rate | >16.6V/µs |

**Tab. I – Operational Amplifier Requirements**

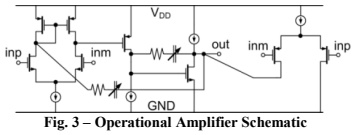


**Fig. 3 – Operational Amplifier Schematic**

The solution adopted in this work is a three-stage operational amplifier with two Miller compensations capacitors and a feed-forward compensation[11].

In particular 70dB dc-gain and minimum unity gain bandwidth requirements, make the Opamp design very challenging. Miller compensation is here not sufficient, because three gain stages are needed to perform the minimum

required dc-gain of 70dB. Feed-forward compensation appears the most reasonable solution, in order to guarantee stability (at the cost of smaller power increasing due to the feed-forward path, see Fig. 3)[12].

*B. Charge-Sensitive-Preamplifier Stability.*

One of the most critical points in charge-sensitive-amplifiers is loop gain stability. Loop-gain stability has been evaluated in two different conditions: during the charge vs. voltage conversion step (when SWfb is open and Rf-Cf feedback net is on), and in the reset mode, when SWfb is closed and Rf-Cf is bypassed.

*Charge vs. voltage conversion.*

On charge vs. voltage conversion, loop gain should be calculated as illustrated in Fig. 4. SWfb is open, so that its resistance can be neglected, while Rf-Cf net and $C_P$+$C_{OP}$ capacitors create a pole-zero couple that guarantees 85° loop phase margin, leading to a completely stable circuit (see Fig. 5, where Opamp and Loop-Gain magnitude and Phase are plotted). $C_{OP}$ is the parasitic capacitor due to the Opamp input stage. Since A(s) is the open-loop operational amplifier transfer function, then loop-gain transfer function is given by:

eq. 1 $$G_{loop}(s) = \frac{v_t'}{v_t} = -A(s) \cdot \frac{1 + s \cdot Cf \cdot Rf}{1 + s \cdot (Cf + C_P + C_{OP}) \cdot Rf}$$

*Reset Mode.*

The most critical situation for stability occurs when SWfb is closed and the Opamp equivalent load capacitors is $C_P$+$C_{OP}$. Such situation is illustrated in Fig. 6, where Rf-Cf are bypassed by SWfb. Magnitude and phase are then plotted in Fig. 7. Note that loop-gain phase margin is worst than Fig. 5 case. This is because the Rf-Cf net is here bypassed so that an additional pole (without any zero) is present in loop-gain transfer function due to $C_P$+$C_{OP}$. $C_P$ capacitance is quite large (15pF), leading to 45° loop phase margin. Miller capacitors (in Fig. 3) have been tuned by the output digital word of the Calibration Circuit, so that the Opamp results quite robust in front of PVT variations. Ocean simulations (whose spread parameters are shown in Tab. II) have demonstrated a minimum loop-gain phase margin of 38°.

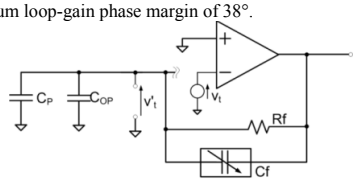


**Fig. 4 – Circuit for Loop-Gain on charge vs. voltage conversion.**

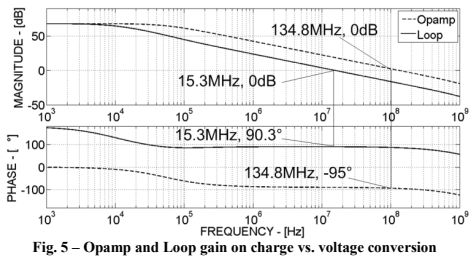


**Fig. 5 – Opamp and Loop gain on charge vs. voltage conversion**

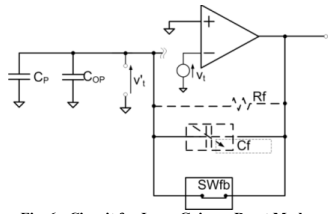


**Fig. 6 - Circuit for Loop-Gain on Reset Mode.**

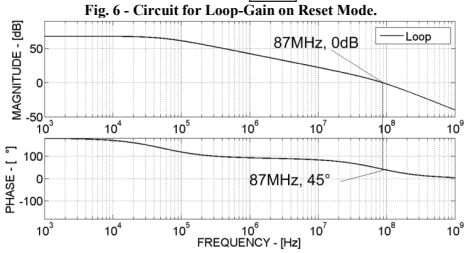


**Fig. 7 – Opamp and Loop-Gain on Reset mode.**

| Parameter | Value |
|---|---|
| Temperature | -40°C, 27°C, 120°C |
| $V_{DD}$ Voltage | 1.62V, 1.8V, 1.98V |
| Process | typical-typical, slow-slow, fast-fast, slow-fast, fast-slow |
| RC Process | RC MAX, RC MIN |

**Tab. II – Charge-Sensitive preamplifer Ocean Corners.**

## IV. SIMULATIONS RESULTS

In order to validate the design, spice simulations have been ran in nominal conditions and spreading CMOS process, temperature and supply voltage, by Ocean tool. Front-end performance have been evaluated for several corners (combining all possible variations as in Tab. II).

*Charge-Detection-Impulse Delay (Fig. 8).*

These simulations evaluate the delay between the input charge arrival time and the charge-detection-impulse starting point. The CDI delay definition is also reported in Fig. 2. Note that in Fig. 8 the delay in nominal conditions is plotted vs. input charge (27°C, 1.8V-supply-voltage, typical-typical process, RC nominal). Maximum delay occurs when the minimum input charge of 30fC is simulated. In this case the front-end needs about 30ns to detect the input charge. Note that the minimum duration of the input charge pulse is about 33ns, so that delay performance results acceptable for the specific GEM detector front-end.

CDI delay has been also evaluated under PVT spread. Fig. 9 presents the simulation results, highlighting what happens for minimum and maximum input charge. Note that in case of 30fC input charge (which is the worst case for CDI delay), the delay remains around 33ns or lower.

*Charge-Detection-Time Linearity( Fig. 10).*

The voltage signal at the charge-sensitive preamplifier output (that is the result of the charge vs. voltage conversion), is then converted in time domain by CDT-Comp. In this way the front-end performs the charge-to-time conversion. CDT impulse accuracy is very important in GEM detectors front-end[9]. Fig. 10 reports the CDT duration time vs. the input charge. Note that nominal case is highlighted (black-bold line). The maximum duration is about 100ns, corresponding to

the maximum input charge of 1pC. CDT impulse has been tested for several corners. Linearity performance are then plotted in Fig. 11, defined (for each input charge) as the deviation between nominal duration and effective CDT impulse duration. The linearity is expressed in percent values. Note that the maximum deviation with respect to the nominal case is ±5%, corresponding to 5ns, over 100ns of maximum CDT impulse duration. Note that CDI and CDT Ocean simulations demonstrate the front-end performance does not change significantly under PVT variations. This is possible due to the specific design choice in charge-sensitive-preamplifier (the dc-gain does not reduce under 63dB), and due to the proper calibration circuit, which allows to achieve very precise ramp signal and to compensate technological spread in charge sensitive preamplifier amplifier. The reliability is here a key point, since radiation tolerance can be improved[9].

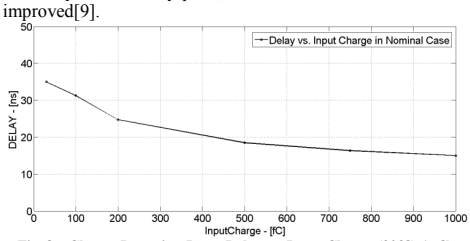


**Fig. 8 – Charge-Detection-Input Delay vs. Input Charge (30fC÷1pC)**

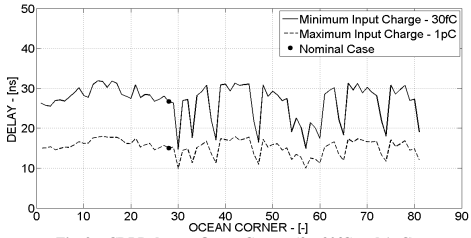


**Fig. 9 – CDI Delay vs. Ocean Corner (for 30fC and 1pC)**

## V. CONCLUSIONS

A complete read-out front-end channel for GEM detectors has been presented. The front-end performs charge-to-voltage and charge-to-time conversion, that is directly proportional to the amount of charge effectively read by the front-end. The read-out channel consumes 3.8mW of power consumption from a single 1.8V supply voltage. The system has been designed in 0.13µm CMOS technology and it is favourable compared with the state of the art, as reported in Tab. III.

| Parameter | This Work | CARIOCA[9] | [1] | [10] |
|---|---|---|---|---|
| CMOS Technology | **0.13µm** | 0.25µm | 90nm | 0.35µm |
| Supply Voltage | **1.8V** | 2.5V | 1.2V | 3.3V |
| Power Consumption | **3.8mW** | 12mW | 5mW | 9mW |
| Sensor Parasitic Cap. | **15pF** | 120pF | 5.6pF | 10pF |
| Max. Input Frequency | **4MHz** | 800kHz | - | - |
| Equivalent Noise Charge | **397e-** | 450e- | 350e- | 196e- |

**Tab. III – Performance Resume.**

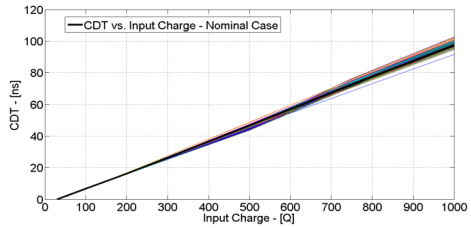


**Fig. 10 – Charge-Detection-Time Duration vs. Input Charge vs. Ocean Corner**

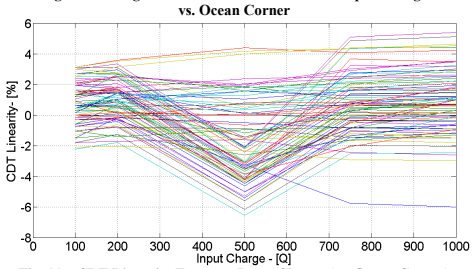


**Fig. 11 – CDT Linearity Error vs. Input Charge (vs. Ocean Corner)**

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## 8.2 IEEE ICICDT 2013

# A Low-Power CMOS 0.13 μm Charge-Sensitive Preamplifier for GEM Detectors

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***Abstract*—In this paper a Charge-Sensitive Preamplifier (CSP) for GEM (Gas Electron Multiplier) detectors readout is presented. The CSP is responsible for signal acquisition and the conversion of the input charge into a voltage signal. The design has been realized in 0.13 μm CMOS technology. It has been demonstrated through a detailed analysis that this is the best CMOS technology to be used in this case, as regards power consumption, intrinsic gain, noise and radiation hardness. The aim is to reduce the power consumption while maintaining other performance at the state-of-the-art. The preamplifier is composed by a three-stage nested Miller Operational Amplifier, with a feed-forward compensation. The system is able to manage a 15 pF detector capacitance. The global power consumption is 1.1 mW and the Equivalent Noise Charge is 418 e⁻.**

***Keywords*—GEM detector; front-end; readout; preamplifier; CMOS; charge-sensitive; trends**

### I. Introduction

The use of ASICs in physics experiments [1] [15] has become larger and larger, because of the advantages brought by integrated circuits with respect to PCBs, especially in terms of costs, portability and performance. Nowadays, many different CMOS technologies are available in the market and the designer has to take into consideration advantages and limits of each one in order to make the most convenient choice for the specific experiment. Several papers available in literature detail the most relevant effects of the CMOS scaling-down on analog circuits [1] - [6].

Considering the most recent CMOS technologies, in deep sub-1 μm CMOS technologies the power and noise performance are significantly improved due to the mostly-digital approach of several CMOS processes. Deep integration scale leads to lower digital power consumption (since it is proportional to $V_{DD}^2$). Standard supply voltage behavior vs. CMOS technology node is illustrated in fig. 1, with the correspondent threshold voltage and oxide thickness. Notice that from CMOS 90 nm and down, the $V_{DD}/V_{TH}$ ratio decreases, and guaranteeing the analog circuits operating point is more problematic. Moreover, in the most scaled CMOS processes, the transistors are specifically designed for digital applications, and as a consequence they are quite fast and feature larger transconductance, $g_m$ [4].

On the other hand, MOS transistors output resistance $r_{ds}$ experiences a significant reduction, due to the scaling-down [6], leading to transistors intrinsic gain (defined as $g_m \cdot r_{ds}$) decrease. For analog circuits, like Charge-Sensitive Preamplifiers, this scenario is not favorable for several reasons. Among them, the Operational Amplifier (Opamp) used in CSPs needs to have large dc-gain in order to manage large GEM detectors parasitic capacitances (15 pF in this case). In order to mitigate this effect, a possible approach is to distribute horizontally the gain. In addition, since the count rate required in GEM detectors is at least a few MHz, large bandwidth Opamp would be designed cascading more stages, increasing circuital complexity. Each stage introduces one pole, so that stability becomes critical.

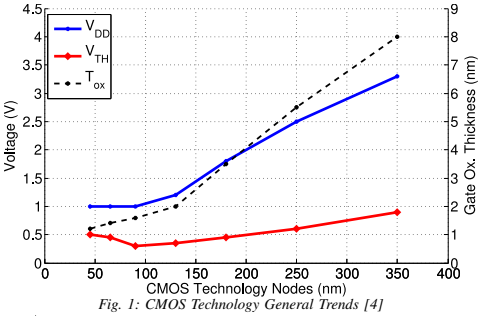


*Fig. 1: CMOS Technology General Trends [4]*

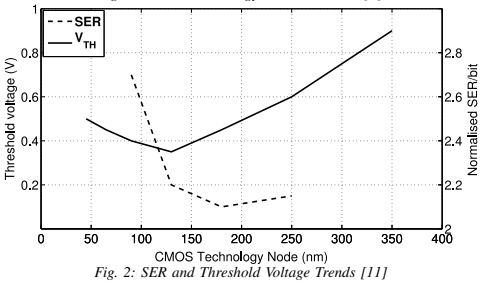


*Fig. 2: SER and Threshold Voltage Trends [11]*

In addition to power, noise performance and operating point issues, in the analog circuits for high-energy physics experiments radiation effects should be taken into account. It has been demonstrated that the behavior of a chip can be strongly influenced even by the natural radioactivity [8]. In general, the larger is the area of an integrated device, the higher will be the probability to interact with the radiation, causing leakage currents, structure modification (i.e. when a heavy particle strikes the transistor), short-channel effects [9] or mainly soft errors [11]. At the same time a general increase of the error rate is noticeable with the CMOS scaling-down. In fig. 2 the trend of the SER (Soft Error Rate) due to neutron interaction damage is plotted with the threshold voltage as a function of the CMOS node. The Soft Error Rate is defined as the rate at which a device generates or encounters a wrong data [11]. This trend is related to the extra charge injected by radiations into active devices. In fact the scaling-down implies a reduced number of carriers into the MOS conduction channel, so the amount brought by radiation can have a greater effect on corrupting the information. Therefore a detailed simulation as a function of PVT (process-voltage-temperature) conditions can clarify

the behavior of a specific technology. Particularly in GEM detectors, the radiation hardness has to be considered [8], since integrated circuits have to be able to work in strong electromagnetic fields.

In this paper a complete design of a Charge-Sensitive Preamplifier for GEM detectors, in CMOS 0.13 μm, is presented. Considering all the technological issues related with high-energy physics experiments, the main aspect of this design is a global power reduction while maintaining performance at the state-of-the-art, including the choice of the CMOS technology that can fit better. Even though in GEM detectors front-end design, deep scaling-down approach is definitively advantageous for power consumption reduction and for signal acquisition rate, but radiation hardness, operating point and stability aspects should be taken into account. For this reason, a complete model of the operational amplifier, used for Charge-Sensitive Preamplifier design, has been implemented in Matlab. The Matlab model simulation results here presented allow to check the most important features of the CSP, vs. technological CMOS node. In this way it is possible to demonstrate that the selected CMOS 0.13 μm process allows a significant power consumption reduction, with respect to the state-of-the-art, while maintaining operating point, stability and robustness in front of radiations [4], making the designer to prefer it with respect to more scaled nodes.

The paper has been organized as follows. In Section II the Matlab model main simulation results will be shown and described. Section III details the most relevant design aspects of the Charge-Sensitive Preamplifier, while Section IV shows the simulation results, in nominal case and with respect to PVT variations. At the end of the paper conclusions will be drawn.

## II. Charge-Sensitive Preamplifier Matlab model

The design approach here developed is to design a Matlab model of the Charge-Sensitive Preamplifier and to simulate it spreading the most important physical and electrical parameters of several CMOS technologies. By evaluating the definitive Matlab performance vs. technology node it will be possible to fix the better power-noise-operating point trade-off, and as a consequence to select the most efficient CMOS technology node. The entire system architecture of the analog front-end for GEM detectors is available in fig. 3, and already described in [12]. The analysis is focused on the Charge-Sensitive Preamplifier. This block is responsible for signal acquisition and converting the charge coming from the detector into a voltage signal.

### A. GEM Front-End Requirements

A very common approach to design the CSP is to use an operational amplifier, with the R-C feedback net [15]. Since $C_D$ (the detector parasitic capacitance) is quite large, about 15 pF, stability is critical in this design. For a complete validation of the CSP Matlab model, the overall system specifications are needed [12]. Furthermore, in table I, the operational amplifier specifications directly involved in the analysis are listed. The input signal bandwidth is about 12.5 MHz, so the minimum required unity gain bandwidth for the operational amplifier is 120 MHz, obtained from system-level considerations. At least 70 dB of dc-gain are needed, in order to reject signal degradation due to the large parasitic capacitance $C_D$. Due to the intrinsic pulse shaping of the GEM detector input signal, modeled as in fig. 3, stability analysis requires at least 70° of phase margin, in order to avoid signal degradation and unwanted ripples during charge-to-voltage conversion.

| Parameter | Value |
|---|---|
| Power Supply | 1.8 V |
| Opamp dc-gain ($A_0$) | 70 dB |
| Charge-Voltage conversion Factor ($K_{CV}$) | 0.5 mV/fC |
| Input Signal Bandwidth (BW) | 12.5 MHz |
| Opamp Unity-Gain Bandwidth ($f_{UGBW}$) | >120 MHz |
| IRN | $< 9$ nV/$\sqrt{\text{Hz}}$ |
| Opamp Phase Margin (PM) | >70° |
| Detector Input Parasitic Cap. ($C_D$) | 15 pF |
| Feedback Resistance ($R_F$) | 1 MΩ |

*TABLE 1: Preamplifier Main Requirements*

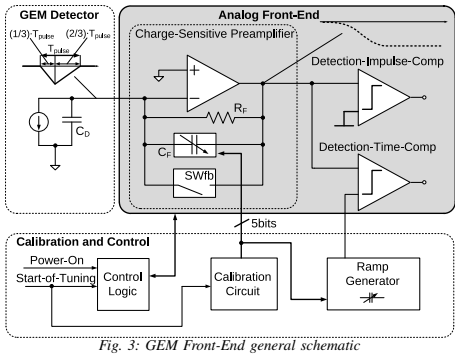


*Fig. 3: GEM Front-End general schematic*

### B. CSP Power Consumption vs. Technology Node

In order to understand the CMOS scaling-down effects on power consumption, the Matlab script aims to identify which parameters included into the power calculus are influenced. In the script, for simplicity, a two-stage Miller-compensated Operational Amplifier has been included, and for each stage an estimation of the current budget has been made. The global power (PW) has been calculated as in (1), where the input transistor current $I_{in}$ and the output current $I_{out}$ can be expressed as in (2) and (3), respectively. The overdrive voltage ($V_{ov}$) for this analysis has been set and maintained at 100 mV, in order to guarantee the transistors to operate into the saturation region.

$$\mathrm{PW} = \mathrm{V_{DD}} \cdot (\mathrm{I_{in}} + \mathrm{I_{out}}) \tag{1}$$

$$\mathrm{I_{in}} = \frac{1}{2} \cdot \mathrm{g_{mIN}} \cdot \mathrm{V_{ov}} = \frac{1}{2} \cdot \left(\frac{8}{3} \cdot \mathrm{K_B} \cdot \mathrm{T} \cdot \frac{1}{\mathrm{IRN}^2}\right) \cdot \mathrm{V_{ov}} \tag{2}$$

$$\mathrm{I_{out}} = \frac{1}{2} \cdot \mathrm{g_{mOUT}} \cdot \mathrm{V_{ov}} = \pi \cdot \mathrm{C_L} \cdot \frac{\mathrm{f_{UGBW}}}{\left(\tan\frac{\pi}{2} - \mathrm{PM}\right)} \cdot \mathrm{V_{ov}} \tag{3}$$

$K_B$ is the Boltzmann constant, while T is the temperature, assumed to be 300 K. $C_L$ is the load capacitance, represented by the sum of the detector input capacitance $C_D$ and the Miller capacitance $C_C$. Analyzing the power trend, depicted in fig. 4, the power consumption tends to be constant increasing the scaling-down and, starting from 0.13 μm, power reduction appears not appreciable. This effect is related to the $V_{DD}$ flat-zone shown in fig. 1 at lower nodes. As a consequence, and taking into account the aspects linked to radiation hardness, the 0.13 μm CMOS technology node has been adopted, since it shows a $V_{DD}/V_{TH}$ ratio approximately close to 3 (fig. 1). This feature allows to relax operating-point specifications and guarantees better output dynamics with respect to lower CMOS nodes, and at the same time a low-power design.

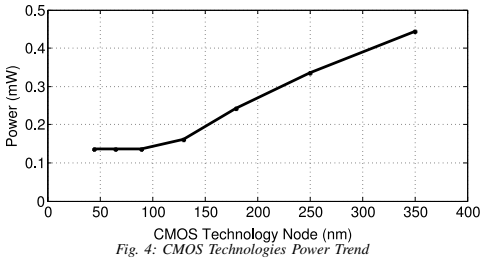

*Fig. 4: CMOS Technologies Power Trend*

## III. Charge-Sensitive Preamplifier Design

### A. Operational Amplifier structure

The structure of the operational amplifier is shown in fig. 5.

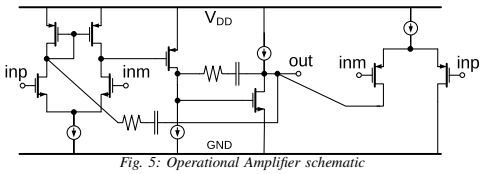

*Fig. 5: Operational Amplifier schematic*

Specifications impose to guarantee a high dc-gain (70 dB) and to avoid an excessive degradation of it varying PVT conditions. Despite what comes out from the Matlab script, the $V_{DD}/V_{TH}$ ratio is still limited and the difficulty to implement cascode stages is tangible. Therefore three stages have been implemented. But a higher number of stages implies a higher number of poles in the transfer function, so guaranteeing stability for this structure is challenging. The solutions here adopted are a Nested Miller compensation (NMC) with a feed-forward compensation (FFC). In order to understand the reasons, a detailed analysis is following.

A three-stage Operational Amplifier with only the NMC has a transfer function with the form (4). Miller zeros have been neglected (assumed to be compensated with the inclusion of Miller resistors).

$$H(s) = \frac{A_0}{(1 + s\,\tau_1)\,(1 + s\,\tau_2)\,(1 + s\,\tau_3)} \tag{4}$$

The dependence of the Unity-Gain-Bandwidth (UGBW) frequency from the load capacitance $C_L$ is shown in (5). $C_{m1}$ and $C_{m2}$ are the two Miller capacitances, while $g_{m1}$, $g_{m2}$ and $g_{m3}$ are relative to the first, second and third stage respectively. Assuming to have a separate-pole approach, the three time constants $\tau_1$, $\tau_2$ and $\tau_3$ in (4) can be set in order to guarantee (5) to be verified.

$$\omega_{\mathrm{UGBW}} = \frac{g_{m1}}{C_{m1}} = \frac{1}{2}\frac{g_{m2}}{C_{m2}} = \frac{1}{4}\frac{g_{m3}}{C_L} \tag{5}$$

The simple NMC shows a 51° phase margin (PM) as shown in (6).

$$PM_{\mathrm{noFF}} = 90^\circ - \arctan\left(\frac{1}{2}\right) - \arctan\left(\frac{1}{4}\right) = 51^\circ \tag{6}$$

With a 15 pF detector input capacitance, this solution is not sustainable due to the loop-gain excessive reduction. But, including the FFC, the second pole will be compensated with a corresponding zero, and the phase margin will modify like in (7).

$$PM_{\mathrm{FF}} = 90^\circ - \arctan\left(\frac{1}{4}\right) = 76^\circ \tag{7}$$

This improvement can guarantee better performance in terms of stability, with a low cost in terms of power. In fact, the addition of the feed-forward stage does not compromise the overall consumption, due to the presence of three gain stages, which consume most of the whole power needed.

## IV. Simulation Results

### A. Nominal case and Post-Layout Simulations

#### 1) Operational Amplifier Frequency Response

The nominal Operational Amplifier open-loop frequency response, in terms of magnitude and phase, is plotted (dashed) in fig. 6. It is clearly noticeable the effect of the FFC on the second pole, and the consequent large phase margin. The results are in agreement with the specifications.

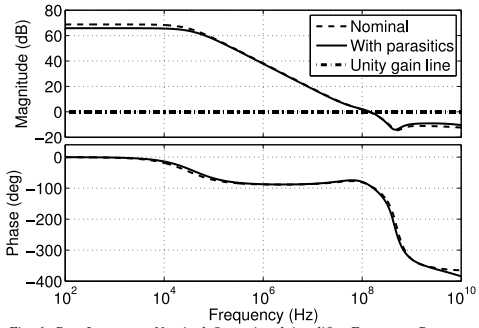

*Fig. 6: Post Layout vs. Nominal Operational Amplifier Frequency Response*

Moreover, nominal-conditions post-layout simulations have been run in order to check performance with the inclusion of parasitic components, generated with the parasitics extraction from the layout. The results are depicted also in fig. 6. In detail, the phase margin remains quite equal with respect to the nominal simulation. As regards particularly the loop-gain, parasitics are not compromising because of the presence of the detector input capacitance (15 pF), much greater than possible parasitics in that node.

#### 2) Operational Amplifier Input-Referred Noise

In fig. 7 the Input-Referred-Noise is plotted. The IRN value extracted is 6.69 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, lower than the requirements.

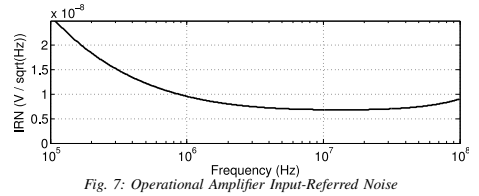

*Fig. 7: Operational Amplifier Input-Referred Noise*

But in this type of devices, the parameter which embodies the noise performance is the ENC (Equivalent-Noise-Charge), namely the input charge necessary to get at the output a signal equal to noise. Its calculus will be based on this intrinsic definition, neglecting the

standard calculus depending on the signal shaping, not present in this design. Starting from the charge-voltage conversion factor ($K_{CV}$) indicated in table I, together with the maximum signal bandwidth (BW) and extracting the IRN value from fig. 7 the ENC can be expressed as in (8).

$$ENC = \frac{v_{nRMS}}{K_{CV}} = \frac{\sqrt{2} \cdot IRN \cdot \sqrt{BW}}{K_{CV}} = 418\ e^{-} \qquad (8)$$

### B. PVT Ocean Simulations

As described in the introduction, the necessity to verify the behavior of this particular technology with respect to the PVT variations is fundamental in order to achieve significant results. In addition to this, PVT simulations can emulate the effects of radiations on circuits, making easier the checking of the overall performance. In this sense the Operational Amplifier performance have been investigated. 81 overall corners have been set, combining values in Table II.

| Parameter | Values |
|---|---|
| Process | typ-typ; slow-slow; fast-fast; slow-fast; fast-slow |
| Voltage (V) | 1.62; 1.8; 1.98 |
| Temp. (°C) | -40; 27; 120 |
| R-C value | RC Min; RC Max |

*TABLE II: PVT parameters*

#### 1) Operational Amplifier Frequency Response

The PVT simulation results of the Operational Amplifier frequency response are depicted in fig. 8. Over these 81 corners, the phase margin assumes values from a minimum of 82° to a maximum of 90°. These results confirm the stability, and its good according to specifications even in worst-case conditions. The effect of the feedforward compensation is maintained quite over all the corners, demonstrating the robustness of this solution. As a summary, in Table III the overall features of the preamplifier are shown.

| Parameter | THIS WORK | [14] | [7] |
|---|---|---|---|
| CMOS Technology | 0.13 µm | 65 nm | 90 nm |
| Power Supply | 1.8 V | 1.8 V | 1.2 V |
| Power Consumption | 1.1 mW | 5 mW | 5 mW |
| Input Parasitic Cap. | 15 pF | 500 fF | 5.6 pF |
| ENC | 418 $e^-$ | 37 $e^-$ | 350 $e^-$ |
| Input Signal Bandwidth | 12 MHz | 10 MHz | - |

*TABLE III: General Performance*

The effort in reducing power comes out in the parallel with similar application designs present in literature [7] [14]. Considering the significant difference in the input capacitance, the results are encouraging. Therefore, the preamplifier performance are in agreement with the initial specifications required. In fact, despite the presence of a large input capacitance and dealing with the high dc-gain, the Operational Amplifier stability has been guaranteed by at least 82° phase margin with a 60 dB minimum dc-gain.

## V. Conclusions

A Charge-Sensitive Preamplifier for GEM detector readout has been presented, including a previous CMOS technology analysis in terms of power consumption, stability, noise and radiation hardness. In particular, the design has been focused on power reduction keeping other performance at the state-of-the-art. The preamplifier shows a 418 $e^-$ ENC and consumes 1.1 mW. It has been designed in CMOS 0.13 µm and it is well comparable with the state-of-the-art.

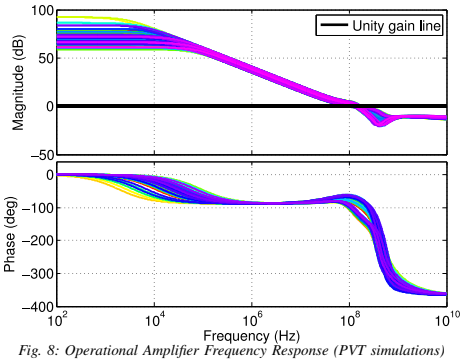


*Fig. 8: Operational Amplifier Frequency Response (PVT simulations)*

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## 8.3 IEEE IWASI 2013

# A CMOS 0.13μm Read-Out Front-End for Triple-Gas-Electron-Multiplier Detectors

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***Abstract*—In this paper a dedicated integrated front-end for the Triple-GEM (Gas Electron Multiplier) detector is presented. The design has been realized in 0.13 μm CMOS technology. This system aims to improve performance with respect to the state-of-the-art on these types of detectors, regarding adaptability, portability, power consumption and on-chip data processing. The front-end is composed by 8-input-channels. Each channel performs the charge-vs-time conversion, and then the signal is definitively converted into digital domain. For this aim a Charge-Sensitive Preamplifier (CSP), and a Charge-to-Time Converter (CTC) are implemented. An automatic on-chip calibration circuit is also included, in order to compensate CMOS technological process/temperature variations. The system is able to manage a 15 pF detector capacitance. The maximum count rate is $4{\cdot}10^6$ counts-per-second (cps) and the power consumption is 3.8 mW/ch. The Equivalent Noise Charge (ENC) is 418 $e^-$. The front-end compares favorably with the state-of-the-art.**

***Index Terms*—GEM detector; front-end; read-out; preamplifier; CMOS; low-power;**

### I. Introduction

In the wide world of particle detectors, gaseous ionization chambers are largely used due to their ability to make energy measurements and to discriminate various radiation types. In last years a particular topology has emerged, named GEM (Gas Electron Multiplier) [1], developed at Gas Detector Development Group at CERN (European Organization for Nuclear Research) in 1997. This detector has several advantages with respect to multi-wire proportional chambers, employed for similar applications.

First of all, the manufacturing costs are much lower and, in principle, wide area GEM detectors are suitable for mass production. Instead, typical multi-wire chambers [2] are very difficult to be assembled and more expensive, compared to GEMs. In addition, GEM detectors features the capability to suppress positive ions, one of the most effective limiting factor in counting rate [3] processing for these class of detectors.

On the other side larger counting rate requires fast front-end electronics, enabling integrated circuit solution.

GEM detectors design features several advantages. Among them they can be easily built in different shapes and volume. Standard fabrication techniques (such as lithography) has strongly increased the possible applications, reducing costs, and improving the interfacing with CMOS integrated circuits.

In fact, several high-energy physics experiments exploit these detectors, especially for beam monitoring. One of the earlier employments was the COMPASS experiment at CERN [4], aiming at the study of hadronic structure and spectroscopy with high intensity muon and hadron beams, where GEMs were used as trackers.

Furthermore, they have been employed as neutron detectors with a Charge-Coupled Device (CCD) front-end system [5], within a radiographic system [6], as an X-Ray polarimeter [7] for astrophysics measures, in ultra-fast soft X-Ray plasma diagnostics [8] and as a new-type photo-multiplier [9]. In addition to physics experiments, this detector has the great potentiality to be included in biomedical instrumentation, especially for diagnostics and monitoring [10].

The research in GEM detectors is pushing towards two mutual research branches.

The first regards the detector physical/structure optimization, especially in the materials choice, in order to increase the signal gain, resolution and the count rate.
This brings to new architectures, including new gas mixtures and shape choices. A recent evolution has been named the Triple-GEM, realized at LNF (Laboratori Nazionali di Frascati) in Italy [11] [12]. It consists in cascading three GEM foils in order to boost the detector signal gain. Furthermore, a particular mixture of gases ($Ar/CO_2/CF_4$ 45/15/40) improves time resolution.

The second research branch is to improve the front-end performance, using dedicated CMOS integrated solutions, suitable to sustain overall count rate (about $10^6$ counts-per-second [12]), while reducing power consumption, and increasing system portability. In particular, the front-end here proposed allows to reduce power with respect to several circuits present in literature [13], enabling the possibility to increase and optimize several input channels in the same silicon area (chip).

In the Triple-GEM Read-out system, an existent front-end has been adapted from other applications; this is the case of the CARIOCA [14], originally developed for Charge-Coupled Devices (CCDs) and included in a primary version of the Triple-GEM. But the limited count-rate and the relatively high power consumption has made the necessity of a dedicated read-out system very real.

As a solution, the development of an ASIC (Application Specific Integrated Circuit) can afford several advantages with respect to other common solutions, i.e. PCBs [15]. For instance, the inclusion of a digital-based data elaboration in here proposed front-end, can greatly increase performance and at the same time reduce the overall read-out system complexity, limiting the inclusion of off-chip devices like FPGAs or standard micro-controllers [16].

Then, silicon implementation allows very dedicated circuital/system-level choices, optimizing overall read-out performance while facing several project design issues, like large detector input parasitic capacitance and relatively low sensitivity.

The paper has been organized as follows. In Section II the main GEM detector features are shown and described. Section III details the most relevant design aspects of the ASIC, while Section IV shows simulation results. At the end of the paper conclusions are drawn.

## II. Gas-Electron Multiplier detector

### A. General Description

The detector for which the ASIC has been designed is named Gas Electron Multiplier (GEM), and belongs to the wide family of proportional counters. This class of detectors is characterized by a proper region of functioning (namely depending on biasing) in which the output charge produced is proportional to the deposited energy at the input. As a consequence these detectors allow to make spectroscopic measures, that is an energy characterization of input particles.

As regards the structure, the GEM is made by a 50 μm thick kapton foil, with a copper clad on each side, perforated with a high-surface density of bi-conical channels and immersed in a particular combination of gases. In figure 1 a SEM (Scanning Electron Microscope) image of the foil is shown.

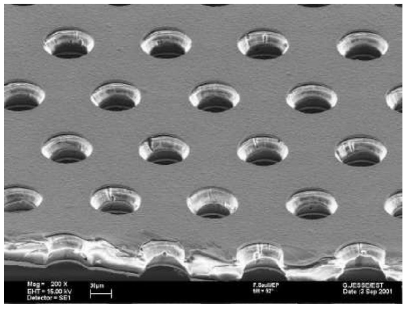

*Fig. 1: SEM image of the GEM foil (from CERN GDD Group)*

It can be shaped in various geometrical configurations (planar, cylindrical, etc.) and also in great sizes, where each foil can reach few hundreds $cm^2$. The GEM has been introduced for particle detection at the end of 90's [1] and it can be used for different families of particle detection, such as neutrons, muons, electrons and also gamma rays. It represents one of the more active object of innovation in this field. Due to this fact, the development of a completely dedicated front-end system is interesting and at the same time challenging.

Furthermore, the GEM detector is very versatile as regards the implementation, and adapting its functioning to different types of radiations (charged, uncharged and depending on the energy/mass) the GEM detector can be included in a very wide range of applications.

So not only high-energy physics can take advantage from the use of this detector. As a possible employment, medicine represents one of the most attractive alternative, including the GEM within radiation-based curative or diagnostic instrumentation (such as the PET (Positron-Emitting Tomography), X-Ray Instruments etc.) as a beam monitor or an unconventional photo-multiplier [10].

### B. Basic principles of functioning

The main process of signal generation inside the detector is the same of a typical gas ionization chamber [2]. In fact, a charged particle which enters the active volume, if energy constraints are respected, ionizes an atom of the gas and creates an electron-ion pair. In presence of an electric field, this two carriers tend to move to the anode and cathode respectively. If the intensity of this electric field overcomes a specific threshold, the kinetic energy of each electron increases till it has sufficient energy to ionize other atoms, creating more active carriers. As a consequence a greater signal is generated at the anode, although keeping the proportionality between the deposited energy and the output signal. This is the reason why GEM detectors can be used for a spectroscopic analysis of the incident particles.
In fact, the great innovation of the GEM with respect to multi-wire chambers is that the high electric field necessary for the carriers multiplication is generated in the foil channels (typically with a 70 μm diameter) by applying a bias between the two foil copper clads. Therefore, due to the very small channel dimensions, a lower bias can be applied in order to obtain the same electric field intensity of conventional proportional detectors (approximately $10^7$ V/m). In channels, as a consequence, an electric field similar to that shown in figure 2 is generated.

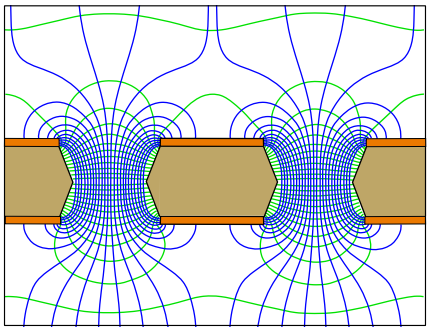

*Fig. 2: Electric field lines in a GEM detector*

The multiplication process takes place inside the channels, where the electric field intensity is higher. In a typical configuration each foil has a multiplication factor between the input and the output carriers in the order of 20. Further signal amplification can be reached cascading more GEM foils into the chamber (three foils, as shown in figure 3, allow to reach a 8000 multiplication factor).

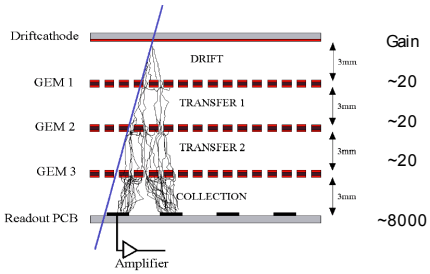


*Fig. 3: Gain of the Triple-GEM*

Another important advantage in employing GEM detectors is the possibility to get information about the position of the particle interaction, due to this detection structure. Making time-of-flight measures, thanks to its very little characteristic time of detection, is also possible.

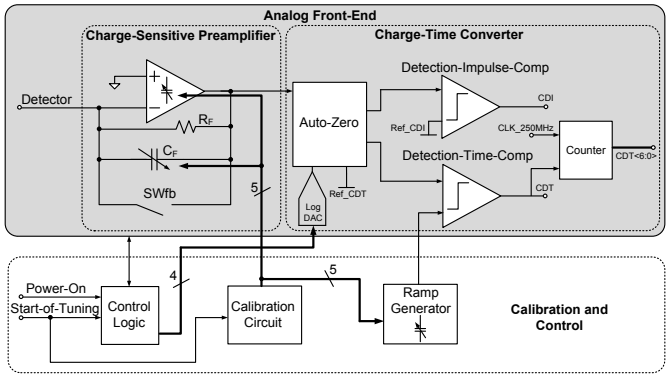


*Fig. 4: The GEM front-end general scheme*

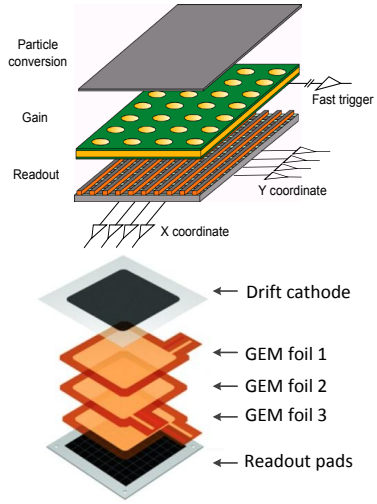


*Fig. 5: The GEM read-out system*

The enhanced GEM adaptability is also one of the key of its success. In fact it can be tuned for several applications changing its geometrical configuration or the materials of its components.

The adopted read-out configuration is like depicted in figure 5. Starting from the top, if neutrons or gamma rays are involved, a conversion layer needs to be placed before the GEM foils, in order to generate charged carriers. Apart from the fast trigger, which gives only counting information, the acquisition system is directly connected with the GEM pixellated output. In detail, every pixel is linked to a specific channel. This is the reason why a high number of detecting channel is needed. Furthermore, every single channel has to face with the parasitic capacitance of the related pixel, which can affect read-out system stability especially for the Preamplifier.

## III. Read-out System Description

In figure 4 the overall read-out system is depicted. The ultimate aim is to measure the arrival time and the amount of charge generated by the GEM detector. It is composed by eight detecting channels made by three main blocks.

The Charge-Sensitive Preamplifier (CSP), connected directly to the detector pixel, is the responsible of the signal amplification, making available at its output a signal whose amplitude is directly proportional to the input charge, included a range between 30 fC and 1 pC.

The Charge-Time Converter (CTC) gets the CSP output and converts it into a logic time signal, also directly proportional to the input charge. This first output signal is named Charge-Detection-Time (CDT). Furthermore, the CTC makes available at its output a logic signal which gives information about the arrival time of the incident particle, named Charge-Detection-Impulse (CDI).

The Calibration System tunes the value of all ASIC capacitors, such as the feedback capacitance $C_F$, very important for the correct CSP functioning, and for the Ramp-Threshold Generator needed by the Charge-Time Converter.

### *A. Charge-Sensitive Preamplifier*

Signal coming from GEM detector goes through the Charge-Sensitive Preamplifier [17], composed by passive feedback net $C_F$-$R_F$, the reset switch SWfb, and the single-ended Opamp. $R_F$ (set very high, about 1 MΩ) maintains input/output Opamp operating point. By closing SWfb, the same operating point is shared by the Opamp input/output nodes, and $C_F$ discharges. Such operation is required every time a signal acquisition is completed.

### *B. Charge-Time Converter*

The CTC main task is the CSP output voltage signal conversion into digital domain. In fact, it generates a logic signal called Charge-Detection-Time (CDT), available as an output. This output is also converted into a 7-bit digital word by a 250 MHz clocked counter (the clock is generated off-chip). In parallel an event detection logic signal is generated, called Charge-Detection-Impulse (CDI). In order to perform these two functions, the CTC is composed by three blocks, namely two comparators and the Auto-Zero circuit.

*1) Comparators:* Two comparators have been implemented. The first, called Detection-Impulse-Comp detects the pulses arrival time generating the Charge-Detection-Impulse logic signal. The second, Detection-Time-Comp, has a dynamic threshold which is a down-going ramp. The intersection between this ramp and the CSP output voltage represents the Charge-Detection-Time logic signal, proportional to the amount of charge coming from the GEM detector.

Ramp signal for charge-to-time conversion is generated by a proper Ramp-Generator circuit. Its implementation is very simple, since it is based on charging a capacitor during a constant time with a constant current. The latter is provided by the external, and it is very precise ($\pm$ 1%), while ramp capacitor is tuned by the calibration circuit in order to guarantee a ramp signal into a $\pm$ 5% tolerance.

The Detection-Time-Comp has been implemented with the circuital scheme in figure 6. Note that the scheme for the Detection-Impulse-Comp is complementary, in the sense that it is based on NMOS input stage. This choice is related to the fact that the Detection-Impulse-Comp has to be fast, because its output information is the incident particle arrival time.

Nevertheless, the structure has been based on the mirrored operational amplifier topology, in order to make the response as symmetrical as possible. So, the main offset contribution can be limited to the variation of the input stage MOSFETs threshold voltage. Since the variation is related to the device active area (Width-Length W·L product) [18], the input stage (M2-M1 in figure 6) has been designed with large dimensions (W is 200 µm). On the other side, the input slew-rate has to be considered, and the L parameter has to be maintained small (L is 350 nm).

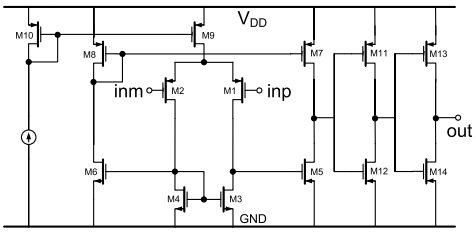


*Fig. 6: Detection-Time-Comp Circuital Scheme*

*2) Auto-Zero circuit:* Considering the switching point of each comparator, the common-mode voltage of the differential input pair must be conveniently set in order to make homogeneous and constant the switching delay.

But, the Detection-Impulse-Comp reference voltage has to be set at lower values with respect to the CSP starting bias, in order to avoid false positive events (due to noise or spikes) depending on specific detection settings (particle type, environment conditions etc.).

At the same time the descending ramp, reference for Detection-Time-Comp, has to last till 400 ns, that is four times the maximum input signal duration, in order to avoid information losses.

Therefore, the Detection-Impulse-Comp switching bias point can reach low values, where input transistors saturation region is not guaranteed (NMOS). In order to overcome this problem, a simple but very effective circuital solution has been adopted, called Auto-Zero, shown in figure 7.

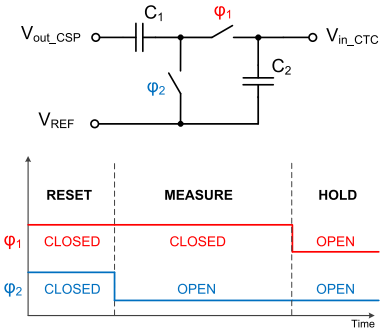


*Fig. 7: Auto-Zero Scheme and Switches Phases*

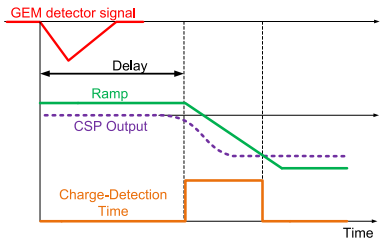


*Fig. 8: GEM front-end main signals*

The Charge-Sensitive Preamplifier output signal is shown in figure 8. It starts from 900 mV, in the middle of the supply range (1.8 V).

For the Detection-Impulse-Comp, the Auto-Zero shifts the CSP output signal higher by a value corresponding to the difference between a bias level generated by a logarithmic DAC and 900 mV, as in (1). The DAC converts an input 4-bit digital word, and the correspondent bias level is in a range going from 901.5 mV to 1.498 V.

$$V_{inCTC} = V_{outCSP} + (V_{REF} - 900mV) \quad (1)$$

By this way the Detection-Impulse-Comp switching point bias is maintained at 900 mV (neglecting comparator offset) and so it is possible to fix the comparator reference input at 900 mV. Therefore, the comparator input stage elaborates every signal with the same bias conditions, and the switching delay parameter can be stabilized.

Considering the Detection-Time-Comp, in order to avoid very short output signal (in time) a 100 ns offset has been inserted into Charge-Detection-Time signal duration. Therefore, the ramp starts from 1.1 V in order to achieve 0 V into a 450 ns range. Moreover, a smaller input charge brings to a smaller CSP output signal amplitude. In order to reduce switching delay even in the case of smallest input charge (30 fC), the Auto-Zero reference voltage $V_{REF}$ has been set to 700 mV, shifting the CSP output signal 200 mV down. This fact is due to the PMOS input stage nature of the Detection-Time-Comp, which is faster at lower gate voltages.

As regards the Auto-Zero functioning, the two switches behavior $\varphi_1$ and $\varphi_2$ is also depicted in figure 7.

Three phases can be identified. The first, called RESET, sets the CTC input operating point at $V_{REF}$ by closing both switches. The second, called MEASURE, is the active phase when $\varphi_2$ is opened, and the CSP output signal is placed over the new bias.

During the third phase, called HOLD, both the switches are opened, holding the CTC input signal.

Unfortunately, some issues have to be considered. First of all, in the MEASURE phase, the signal crosses a capacitive voltage divider, and so it will be attenuated as shown in (2).

$$V_{inCTC}^{REAL} = V_{inCTC}^{IDEAL} \cdot \frac{C_1}{C_1 + C_2} \quad (2)$$

But, in order to limit the signal loss to 5%, $C_1$ is set to be 3.3 pF while $C_2$ is 150 fF.

Secondly, in the HOLD phase, the signal at the CTC input can pass through the R-C net composed by the series of the two switches off-resistances and $C_2$. This fact can affect the measure, moving the crossing point bias between the reference voltage and the CTC input. Therefore, in order to maintain the holding for the maximum measure time (300 ns) within a 3% tolerance, minimum area switches have been implemented, maximizing their off-resistance and the discharge time constant $\tau$ (the R·C product).

### C. Calibration System

The CMOS integration process, due to its nature, brings to a statistical variation of all parameters involved in a circuit [18]. These parameters are related to transistors, resistors, capacitors, and also the silicon wafer. These variations are particularly relevant, and the designer has to take them into consideration because they affect the global performance.

In detail, this project bases its functioning on capacitors, included in the Charge-Sensitive Preamplifier as the feedback capacitor and the Miller compensation capacitor.

It has been demonstrated that the capacitors mean standard variation due to the integration process is within the 18-20% range [19]. This fact can affect seriously the front-end performance.

In this design indeed, the requested precision of capacitance values is 5%. This fact is due to three critical points. The first two regard the CSP feedback capacitor ($C_F$) value, included into the integration constant, and responsible of the loop gain, and so of the Opamp phase margin. The third, linked to the Opamp Miller compensation capacitor value, is responsible of the CSP Opamp stability.

The solution for this issue consists in designing an automatic calibration circuit [20] [21] [22], which tunes the capacitors value directly on-chip and automatically, including only a precise current reference, given as a chip input, and a stable clock signal, as shown in figure 9.

The calibration algorithm is made by three main steps: the sensing, the calibration and the convergence.

The sensing procedure starts at the beginning of the algorithm. It consists in evaluate the effective capacitance implemented value. Namely, the sensing is made by generating a linear descending ramp into a determined time interval, established in multiples of the clock signal period. The reference bias values, the time duration and the clock frequency have been chosen according to a MATLAB™ simulation.

The basic concept behind the calibration logic is to make the capacitance value to change according to the check of the resulting ramp bias. So, a digital programmable capacitor array has been implemented, which allows to select a specific value with a digital word. The precision of the calibration so will depend on the number of the implemented capacitors, acting as bits.

Let be $C_{nom}$ the capacitance nominal value, N the number of array bits and $\Delta C$ the maximum relative variation of the capacitance value due to the CMOS integration process.

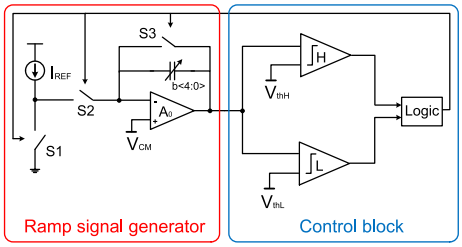


*Fig. 9: Calibration Circuit Scheme*

Therefore, the possible combinations of the capacitance value are $2^N$. The minimum value $C_{min}$ and the maximum $C_{max}$ will be like in (3) and (4) respectively.

$$C_{min} = C_{nom} \cdot (1 - \Delta C) \quad (3)$$

$$C_{max} = C_{nom} \cdot (1 + \Delta C) \quad (4)$$

Hence, the difference between two consecutive values and so the maximum error $\epsilon$ with respect to the nominal value is described by (5).

$$\epsilon = \frac{C_{max} - C_{min}}{2^N} = \frac{2 \cdot \Delta C}{2^N} = \frac{\Delta C}{2^{N-1}} \quad (5)$$

As a consequence, once the maximum variation of the capacitance value is known, fixing the number of bits corresponds to fixing the maximum error.

After that, following the calculations made in equations (3) to (5) and the maximum variation of the capacitance fixed ($\Delta C$ in (5)), the MATLAB™ program calculates the array offset capacitor as the $C_{min}$ and makes a relation between the bit code and the capacitance value in the array. Choosing the bit code corresponding to the nominal capacitance, named $N_{init}$, the program calculates also the two comparators thresholds, respectively $V_{th_L}$ and $V_{th_H}$ as in (6) and (7).

$$V_{th_L} = V_{reset} - \frac{T_{charge} \cdot I_{ref}}{C(N_{init})} \quad (6)$$

$$V_{th_H} = V_{reset} - \frac{T_{charge} \cdot I_{ref}}{C(N_{init} + 1)} \quad (7)$$

## IV. Simulation Results

In order to validate the design and to face with CMOS technology process, temperature and power supply (PVT) variations, 81 simulation corners have been run, based on parameters in table I.

| Parameter | Values |
|---|---|
| CMOS Process | typ-typ; slow-slow; fast-fast; slow-fast; fast-slow |
| Voltage (V) | 1.62; 1.8; 1.98 |
| Temp. (°C) | -40; 27; 120 |
| R-C value | RC Min; RC Max |

*TABLE I: PVT parameters*

In figure 10 the simulation of a complete detection is depicted, in nominal conditions. The Charge-Detection-Impulse and Charge-Detection-Time signals are shown, together with the Detection-Time-Comp reference ramp signal and the CSP output. Note that the crossing point between the ramp and the CSP output corresponds to the end of the CDT signal, and the CSP output reset makes the ramp and the CDI signal to reset also. In figure 11, the CDI and CDT PVT variations are shown. Note that the global behavior is as expected even with PVT variations.

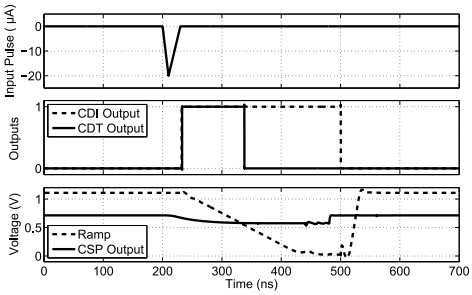


*Fig. 10: Detection Nominal Simulation Results*

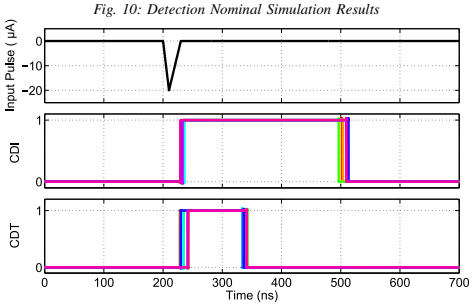


*Fig. 11: CDT and CDI PVT Simulation Results*

In table II the main front-end performance has been shown, in parallel with the previous system implemented for the Triple-GEM [14].

| Parameter | This Work | [14] |
|---|---|---|
| CMOS Technology | 0.13 μm | 0.25 μm |
| Supply Voltage | 1.8 V | 2.5 V |
| Input Parasitic Capacitance | 15 pF | 120 pF |
| Max. Count Rate | $4{\cdot}10^6$ cps | $8{\cdot}10^5$ cps |
| ENC | 418 $e^-$ | 450 $e^-$ |
| Power Consumption | 3.8 mW/ch. | 12 mW/ch. |

*TABLE II: Global Performance*

The reduction in power consumption is evident, more than three times lower, together with the improved maximum count rate, maintaining a similar noise performance. Note that in this design no signal shaping has been implemented, so the calculus of the noise contribution has been made as in [23]. The great difference in the input parasitic capacitance is due to the CARIOCA system original application, namely CCDs.

## V. Conclusions

A novel front-end for the Triple-GEM detector has been presented. It is composed by 8-detecting channels which feature each a Charge-Sensitive Preamplifier and a Charge-Time Converter, including the Auto-Zero Circuit. The on-chip automatic Calibration Circuit has been also detailed. The design has been focused on power consumption reduction while improving count-rate and digital-data processing. The front-end has a maximum $4 \cdot 10^6$ count rate and shows a 418 $e^-$ ENC and consumes 3.8 mW/ch. It has been designed in CMOS 0.13 μm and it is well comparable with the state-of-the-art.

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# 9
# GEMINI Related Papers

The papers dedicated to GEMINI are listed in the next pages.
The first has been presented at IEEE ISCAS 2015 Conference in Lisbon, Portugal. It deals with a general overview of the ASIC.
The second, presented at IEEE SENSORS 2015 Conference in Busan, South Korea, is dedicated to GEMMA Performance, while the third, presented at TWEPP Conference in Lisbon, Portugal and published in JINST 2015 Journal, goes in a deeper detail about the ASIC implementation and the entire readout system.

## 9.1 IEEE ISCAS 2015

# GEMINI: A Triple-GEM Detector Read-Out Mixed-Signal ASIC in 180 nm CMOS

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***Abstract*—This paper presents GEMINI, an entire read-out System-on-Chip (SoC) to be used with the Triple Gas-Electron Multiplier (GEM) detector. Designed in CMOS 180 nm technology, GEMINI pushes towards the state-of-the-art for this peculiar detector front-end, as regards the count rate and detector pixel parasitic capacitance sustainability. It is composed of 16 channels, each performing a charge-to-voltage conversion via a Charge-Sensitive Preamplifier (CSP), a successive event discrimination with channel-independent threshold and an event-triggered reset. The CSP analog output and the LVDS discriminator output are available as chip outputs for each channel. The Q-to-V conversion accuracy is guaranteed by an automatic on-chip calibration unit, compensating for environmental, CMOS process and supply voltage variations. GEMINI is able to sustain a 5 Mcps count rate, managing up to 40 pF pixel capacitance and with a 2.7 mW/ch power consumption.**

***Keywords*—GEM; detector; front-end; read-out; preamplifier; CMOS; low-power; system-on-chip; ASIC;**

### I. Introduction

Developed originally at CERN (European Organization for Nuclear Research) in 1997 [1], GEM detectors have become a straightforward choice in particle physics experiments and for neutron beam monitoring systems when a high count rate is required [2]. In fact, this class of detector has several advantages with respect to multi-wire proportional chambers, employed for similar applications. Above all, the manufacturing costs are much lower and, in principle, wide area GEM detectors are suitable for mass production. Instead, typical multi-wire chambers [3] assembling/manufacturing is quite critical and more expensive, compared to GEMs. Furthermore, dealing with detection efficiency, GEMs intrinsically suppress positive ions, one of the most effective limiting factor in count rate performance. Nevertheless, under a larger count rate only fast front-end electronics is suitable for an efficient read-out, enabling integrated circuits as a straightforward solution. As a plus, GEM detectors design includes standard fabrication techniques (such as lithography) reducing costs, and improving the interfacing with CMOS integrated circuits. One of the earlier employments was the COMPASS experiment at CERN [4], where GEMs were used as trackers. So it is for LHCb experiment [5]. Furthermore, they have been employed as neutron detectors with a Charge-Coupled Device (CCD) front-end system [6], within a radiographic system [7] and in ultra-fast soft X-Ray plasma diagnostics [8]. In addition to physics, this detector has the great potentiality to be included in biomedical instrumentation, for diagnostics/monitoring [9].

As regards GEM detectors read-out, the research aims to improve the front-end performance with dedicated CMOS integrated solutions, suitable to manage the count rate (about $10^6$ counts-per-second [10]). Not a secondary fact is represented by the detector output pads, manufactured in different size factors as shown in figure 1, which are a primary issue in the read-out design. Their parasitic capacitance is directly involved in performance in terms of noise and efficiency.

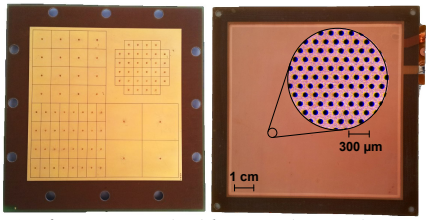


*Fig. 1: **Left:** GEM Output Pads; **Right:** GEM Foil Image with Microscope Detail*

As an example, 2.5 cm x 2.5 cm pads feature a 40 pF parasitic capacitance. In literature, few integrated front-end systems are present [11] [12], but they have been re-adapted from multi-wire chambers and silicon detectors. They show relatively high power consumption, reduced channel number, limited count rate and only analog or digital features. Moreover, some of the older CMOS technologies with which those systems were designed are no more available, making the necessity of a dedicated and updated read-out system very real. As anticipated, integration allows peculiar circuital and system-level choices, optimizing read-out performance while facing project design issues, like large detector input parasitic capacitance and relatively low sensitivity.

Starting from these considerations, the GEMINI SoC, specifically designed appositely for Triple-GEM detector, aims to improve read-out performance while increasing detectors portability and reducing power consumption. The last point is crucial, since avoiding an excessive junction temperature increases the chip lifetime. The main differences between the GEMINI and present ASICs are the mixed-signal capability, with analog and digital outputs for each one of the 16 channels included, and the automatic on-chip calibration allowing to control performance against CMOS process, supply voltage and environmental variations. This allows to increase the count rate up to 5 Mcps and to manage input pad capacitance up to 40 pF. The SoC has been designed with 180 nm CMOS technology, a well modeled node assuring a long term support and accurate simulation results.

The paper has been organized as follows. In Section II the main GEM detector features are shown and described. Section III details the most relevant design aspects of GEMINI, while Section IV shows simulation results. At the end of the paper conclusions are drawn.

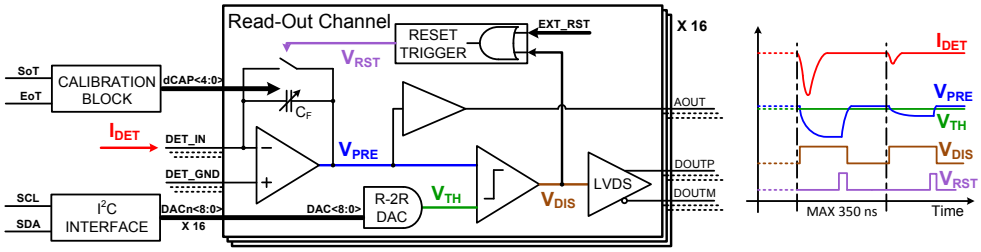


*Fig. 2: The GEMINI SoC Block Scheme*

## II. Triple-GEM Detector Basics

Belonging to the wide family of Micro-Pattern Gaseous Detectors (MPGD), the Triple Gas Electron Multiplier can be identified as a proportional counter, since it can be biased into a proper region of functioning in which the produced output charge is proportional to the deposited energy. This feature enables the possibility to employ it for spectroscopic measurements as well as for event counting. The GEM detector is made by a 50 µm thick kapton foil, copper clad on both sides, perforated with a high-surface density of 70 µm-diameter bi-conical channels and immersed in a particular gas mixture. In figure 1 a GEM foil microscope image is shown. Cascading three GEM foils enables the possibility to boost the detector signal amplification. Biasing the two clad sides at 350 V, each GEM foil has a carrier multiplication factor in the order of 20, but further signal amplification can be reached cascading more foils into the chamber. With three foils, the multiplication factor rises up to 8000. In combination with that, a peculiar gas mixture ($Ar/CO_2/CF_4$ 45/15/40) has shown a strong improvement in time resolution.

One of Triple-GEM strengths is the adaptability. In fact it can be shaped in various geometrical configurations (planar, cylindrical, spherical etc.) and also in great sizes, each foil reaching few hundreds $cm^2$ [13]. The Triple-GEM has demonstrated to be very versatile in the implementation, adapting its functioning to various radiations (charged, uncharged and with different energy/mass). Another important advantage in employing GEM detectors is the possibility to get information about the position of the particle interaction, due to their structure. Making time-of-flight measures, thanks to its characteristic time of detection (in the order of 30-100 ns), is also possible. The acquisition system is directly connected with the detector pixellated output. In detail, every pixel is linked to a specific channel and its dimensions are set starting from particle deposited energy and cross-section into the determined gas mixture. As shown in figure 1, the pixel dimensions have been realized in a wide range for testing the electronic read-out behavior. Therefore, also the pixel parasitic capacitance spreads in a wide range, affecting read-out performance. This is one of the hardest challenges in read-out design.

So, since the Triple-GEM can face several configurations as regards geometry, granularity and spatial resolution, and since ASICs employed so far for this detector read-out are no more available due to the demise of their CMOS process fabrication, the need for a new integrated system able to exploit all the Triple-GEM potential is very real.

## III. GEMINI Read-out System

The specifications imposed for GEMINI in order to be efficiently compliant with the detector are listed in table I.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Count Rate | $> 3$ Mcps | Max Pixel Cap. | 40 pF |
| # of Channels | 16 | Sensitivity | 1 mV/fC |
| Min Detectable Q | $< 3$ fC | Reset Trigger | Event |
| Max Det. Jitter | 9 ns | Gain Accuracy | 5% |

*TABLE I: GEMINI specifications*

### A. GEMINI Channel Design

In figure 2 the GEMINI read-out scheme is depicted. The SoC is made of 16 channels where, with the inclusion of a Charge-Sensitive Preamplifier (CSP), the signal from the detector is converted from charge to voltage domain. Then, the discriminator compares the CSP output voltage level with a channel-specific threshold, set by an R-2R Resistive DAC, generating the event detection output signal. The output is then converted into LVDS standard through a dedicated driver.

The CSP composes of a Class-A Miller Opamp with $C_F$ capacitor connected in feedback, in parallel with a switch. The CSP sensitivity, $K_{QV}$, and the efficiency in charge collection from the detector, $\eta_Q$, are indicated in Eq. (1), depending from the Opamp Open-Loop DC Gain, A, $C_F$ and $C_D$, the detector parasitic capacitance. The ENC dominant contribution can be calculated as in Eq. (2), starting from the input in-band integrated noise, $v_{ni_{OPAMP}}$.

$$K_{QV} \simeq \frac{1}{C_F}; \quad \eta_Q = \frac{1}{1 + \frac{C_D}{C_F(A+1)}} \tag{1}$$

$$ENC \simeq v_{ni_{OPAMP}}(C_D + C_F) \tag{2}$$

Note that $C_F$ is the only parameter to set the sensitivity, as well as $C_D$ plays a critical role on ENC. On the other hand, the efficiency can be maximized increasing the Opamp DC-Gain. So the Opamp design is a key-point. The sensitivity imposed by specifications sets directly $C_F$ to 1 pF. Imposing the ENC to be 2 fC with a 40 pF $C_D$ in order to comply with the minimum detectable charge, the Opamp has been designed to obtain 65 dB DC-Gain and 50 $\mu V_{RMS}$ input in-band integrated noise. The efficiency so is 98%.

As regards the discriminator (DISC), the main target is to reduce the input stage offset, in order to achieve the sensitivity

and the detection jitter required (3 fC and 9 ns respectively). This means that the maximum tolerated offset is 3 mV after the CSP conversion, as well as for the R-2R Resistive DAC LSB, representing the minimum threshold. Designing the discriminator with a mirrored structure and exploiting the inter-digitated layout technique allows to limit the offset within specs. At the same time, since the detector charge polarity is intrinsically negative (the signal is generated by electrons), the CSP output signal embeds a decreasing behavior. For this reason, a PMOS discriminator input stage has been preferred to NMOS.

Dealing with the threshold, the 9-bit R-2R Resistive DAC has a 1.2 mV LSB and 500 mV full-scale. The input digital words, independent for each channel, are stored into dedicated registers managed from the $I^2C$ interface.

The event-driven reset signal is generated starting from the DISC output. In fact, with the simple use of a passive RC net and an OR logic gate, the reset pulse delay can be set. In detail, the RC time constant is applied to the DISC output signal and sent to one OR input. When the voltage is high enough the OR switches high, closing the CSP feedback switch. The other OR input can be used as a general channel reset. In this case, a 150 ns time constant has been set.

### B. Calibration

The channel structure of GEMINI relies on capacitors, included in the CSP feedback and in the CSP Opamp for stability compensation. For correct functioning, their maximum spread has not to exceed 5%. In fact, the CSP feedback capacitor ($C_F$) value controls the CSP gain, as well as the loop gain and the Opamp phase margin. But the CMOS integration process, due to its nature, leads to statistical variations of all parameters involved in a circuit [14] and its precision by itself is not enough. The solution for this issue consists in designing a calibration circuit [15], able to tune the capacitors value directly on-chip and automatically, including only a precise current reference and a stable clock signal. Practically, cited critical capacitors has been implemented with a switchable binary weighted capacitor array. A logic unit algorithmically manages the array opportunely with a digital word, limiting the maximum error in capacitances $\epsilon_c$ with respect to the nominal value as in Eq. (3). $\Delta C$ represents the maximum capacitance spread due to CMOS process variations.

$$\epsilon_c = \Delta C / 2^{N-1} \tag{3}$$

Note that fixing the number of array bits N corresponds to fixing the maximum error. In this project 5 bits arrays have been chosen to obtain the desired spread range.

### C. Digital Control

The GEMINI embeds an $I^2C$ interface for controlling the calibration and channel settings, exploiting its bidirectional 2-line feature for managing up to 16 ASICs at the same time (256 channels), with a single external master device achieving a strong improvement in portability. As regards the channels, $I^2C$ data registers store the 16 9-bit digital words for threshold R-2R DACs. The $I^2C$ interface also controls directly the calibration unit option for manually setting the capacitor digital word through a dedicated $I^2C$ register.

Note that, in order to minimize disturbance effects on channels due to digital blocks, a Triple-Well CMOS process option has been chosen. In detail, the $I^2C$ and the digital part of the calibration unit are isolated from the analog substrate, so their biasing is completely independent from the analog counterpart.

## IV. Post-Layout Simulation Results

The GEMINI layout is depicted in figure 3, occupying 6.89 $mm^2$. In the center the 16 channel are clearly visible. The $I^2C$ interface has been placed to their left side, while the calibration unit to their right.

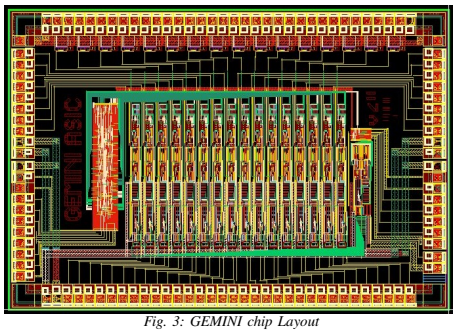

*Fig. 3: GEMINI chip Layout*

After parasitic extraction, transient noise and Monte-Carlo post-layout simulations have been run, including temperature variation between −40 °C and 120 °C, as well as supply voltage 10% maximum spread. The input pixel capacitance has been set to 40 pF. This worst-case scenario represents an optimum testbench also for radiation hardness. Although measurements during irradiation are a must, these results can prove for an overall robustness. Figure 4 shows the transient noise simulation related to the CSP output signal generated from the minimum input charge (30 fC). This simulation demonstrates that, also with the 40 pF pixel capacitance, the CSP design is valid in terms of noise, since setting the threshold for the minimum detectable charge specification (3 fC) will not generate false-positive events. The ENC has been calculated to be 2 fC.

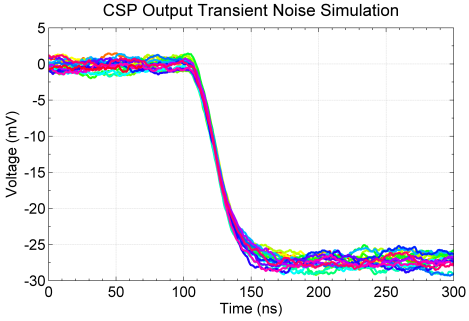


*Fig. 4: Post-Layout Transient Noise CSP Simulation*

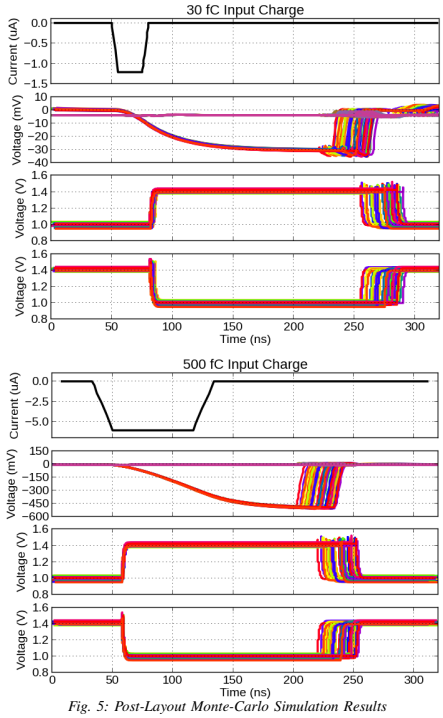


*Fig. 5: Post-Layout Monte-Carlo Simulation Results*

Figure 5 shows the Monte-Carlo results. Together with the input signal, the channel analog and the digital outputs are shown. Note the effect of event-triggered reset on output signals. This evident spread in reset time (25 ns) is justified by reset time constant variation (passive RC net) due to CMOS process. This variation is not critical, since the output signal does not contain any information in the time duration. On the contrary, the trailing edge is very precise through corners, with a 6.2 ns maximum spread. In table II the main GEMINI performance has been shown, in parallel with CARIOCA [12] and a recent development, GASTONE64 [11].

| Parameter | GEMINI | CARIOCA | GASTONE64 |
|---|---|---|---|
| CMOS Tech. | 180 nm | 250 nm | 350 nm |
| Supply Voltage | 1.8 V | 2.5 V | 3.3 V |
| # of Channels | 16 | 8 | 64 |
| Max Pixel Cap. | 40 pF | 120 pF | 100 pF |
| Max Count Rate | 5 Mcps | 0.8 Mcps | 30 Kcps |
| Min Detectable Q | 2.5 fC | 10 fC | 5 fC |
| Sensitivity | 1 mV/fC | 8 mV/fC | 3 mV/fC |
| Power Cons. | 2.7 mW/ch [§] | 12 mW/ch | 8 mW/ch |

*TABLE II: Performance.* [§] *With LVDS Driver: 6.3 mW/ch*

The reduction in power consumption is evident, together with the improved maximum count rate. Note the difference in the input pixel maximum capacitance. In fact either the CARIOCA chip or the GASTONE64 show a limited count rate, relaxing CSP stability constraints. Moreover, the area of a 100-120 pF pixel would be overly large for exploiting the pixellated detector spatial resolution [15]. The high number of channels in GASTONE64 has been reached with the inclusion of post-processing digital unit in the ASIC enabling serial channel read-out. GEMINI instead, guarantees a parallel and real-time operation.

## V. Conclusions

A SoC dedicated for the Triple-GEM detector read-out, GEMINI, has been presented. It composes of 16 detecting channels, each featuring a Q-to-V conversion followed by an event discrimination with an event-triggered reset. The focus has been put on improving count rate and managing input pixel capacitance. Post-Layout Simulations show a 5 Mcps count rate and 2.7 mW/ch power consumption with a 40 pF pixel capacitance. The design has been made with a 180 nm CMOS technology with digital Triple-Well isolation.

## References

[1] F. Sauli, "GEM: A new concept for electron amplification in gas detectors," *Nucl. Instr. and Meth. in Phys. Res. Section A*, vol. 386, no. 2, pp. 531–534, 1997.

[2] G. Croci *et al.*, "GEM-based thermal neutron beam monitors for spallation sources," *Nucl. Instr. and Meth. in Phys. Res. Section A*, vol. 732, pp. 217–220, 2013.

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## 9.2 IEEE SENSORS 2015

# GEMINI, a CMOS 180 nm Mixed-Signal 16-Channel ASIC for Triple-GEM Detectors Readout

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***Abstract*—GEMINI is a readout ASIC dedicated to the Triple-GEM detector. Fabricated in CMOS 180 nm technology, GEMINI pushes towards the state-of-the-art for this peculiar detector front-end, as regards the count rate and detector pixel parasitic capacitance sustainability. It features 16 channels, each one including a charge-sensitive preamplifier, an event discriminator with channel-independent threshold and an event-triggered reset. An embedded automatic calibration unit compensates performance for environmental, CMOS process and supply voltage variations. GEMINI sustains a 5 Mcps count rate, managing up to 40 pF GEM detector capacitance and consuming 2.7 mW/ch.**

***Keywords*—GEM; detector; front-end; readout; preamplifier; CMOS; low-power; system-on-chip; ASIC;**

### I. Introduction

Research in GEM detectors [1] readout aims to improve the front-end performance with dedicated CMOS integrated solutions, suitable to manage the count rate. Front-end integration admits peculiar circuital and system-level choices, optimizing readout performance while facing project design issues, like large detector input parasitic capacitance and relatively low sensitivity. In literature few integrated front-end systems explicitly devoted to GEM detectors are present, most of them being re-adapted mainly from multi-wire chambers and silicon detectors systems, such as CARIOCA chip [2]. They show relatively high power consumption, a reduced number of channels, limited count rate and only analog or digital features. In case they have higher number of channels, like GASTONE64 [3], those can only be read digitally in series, affecting the global counting rate sustainability.

The GEMINI (GEM INtegrated Interface) ASIC, devoted for Triple-GEM detectors, improves readout performance while increasing the system portability and reducing power consumption. The target application includes time-of-flight and counting measurements, with the option to make spectroscopic analysis externally via the analog preamplifier output. In fact, the GEMINI has a mixed-signal capability, with analog and digital outputs available in parallel for each one of the 16 channels included, and an automatic on-chip calibration compensating for CMOS process, supply voltage and environmental variations. This allows managing a count rate up to 5 Mcps and an input pad capacitance up to 40 pF, while consuming 2.7 mW per channel. The SoC has been designed with 180 nm CMOS technology, a well modeled node assuring a long term support.

The paper has been organized as follows. In Section II the GEMINI and its front-end are described, while Section III shows performance results. At the end of the paper conclusions are drawn.

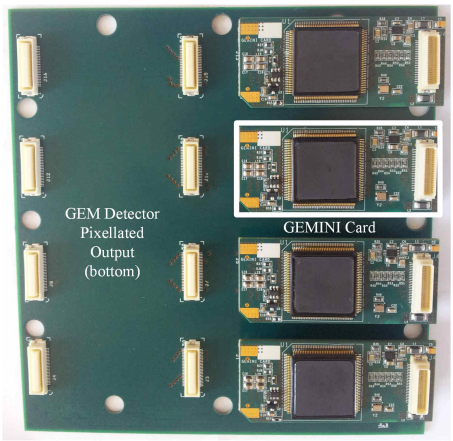


*Fig. 1: GEMINI Front-End System*

### II. GEMINI Front-End System

The detector output pixels can be realized in different size factors, depending on measurement concerns on particle deposited energy and cross-section into the determined gas mixture [4]. Therefore, also the pixel parasitic capacitance spreads accordingly, affecting readout performance. This is one of the hardest challenges in front-end design.

The acquisition system, depicted in Figure 1, is directly connected with the Triple-GEM detector pixellated output, composed by 128 pixels. Every pixel is linked to a specific channel (8 GEMINI chips required). A dedicated mezzanine board has been designed for the GEMINI. This boards are managed by a Mother Board including an FPGA for post-processing.

#### A. Front-end Specifications

The specifications imposed for GEMINI in order to be efficiently compliant with the detector are listed in table I.

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| Count Rate | $>$ 3 Mcps | Max Pixel Cap. | 40 pF |
| # of Channels | 16 | Sensitivity | 1 mV/fC |
| Min Detectable Q | $<$ 3 fC | Reset Trigger | Event |
| Max Det. Jitter | 9 ns | Gain Accuracy | 5% |

*TABLE I: GEMINI specifications*

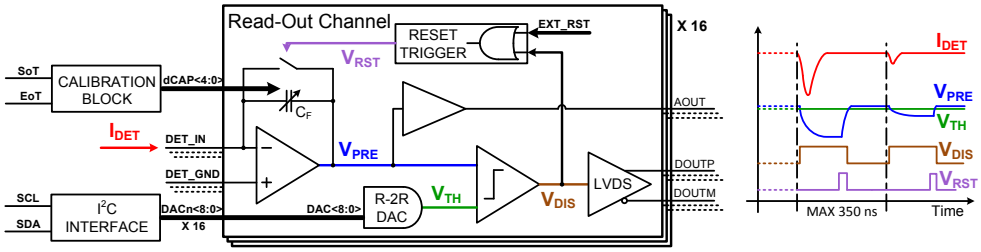


*Fig. 2: The GEMINI SoC Block Scheme*

### *B. GEMINI Channel Design*

In figure 2 the GEMINI readout scheme is depicted. The SoC is made of 16 channels where, with the inclusion of a Charge-Sensitive Preamplifier (CSP), the signal from the detector is converted from charge to voltage domain. Then, the discriminator compares the CSP output voltage level with a channel-specific threshold, set by an R-2R Resistive DAC, generating the event detection output signal. The output is then converted into LVDS standard through a dedicated driver.

The CSP composes of a Class-A Miller Opamp with $C_F$ capacitor connected in feedback, in parallel with a switch. The CSP sensitivity, $K_{QV}$, and the efficiency in charge collection from the detector, $\eta_Q$, are indicated in Eq. (1), depending from the Opamp Open-Loop DC Gain, A, $C_F$ and $C_D$, the detector parasitic capacitance. The ENC dominant contribution can be calculated as in Eq. (2), starting from the input in-band integrated noise, $v_{ni_{OPAMP}}$.

$$K_{QV} \simeq \frac{1}{C_F}; \quad \eta_Q = \left(1 + \frac{C_D}{C_F(A+1)}\right)^{-1} \tag{1}$$

$$ENC \simeq v_{ni_{OPAMP}}(C_D + C_F) \tag{2}$$

Note that $C_F$ is the only parameter to set the sensitivity, as well as $C_D$ plays a critical role on ENC. On the other hand, the efficiency can be maximized increasing the Opamp DC-Gain. So the Opamp design is a key-point. The sensitivity imposed by specifications sets directly $C_F$ to 1 pF. Imposing the ENC to be 2 fC with a 40 pF $C_D$ in order to comply with the minimum detectable charge, the Opamp has been designed to obtain 65 dB DC-Gain and 50 $\mu V_{RMS}$ input in-band integrated noise. The efficiency so is 98%.

As regards the discriminator (DISC), the main target is to reduce the input stage offset, in order to achieve the sensitivity and the detection jitter required (3 fC and 9 ns respectively). This means that the maximum tolerated offset is 3 mV after the CSP conversion, as well as for the R-2R Resistive DAC LSB, representing the minimum threshold. Designing the discriminator with a mirrored structure and exploiting the inter-digitated layout technique allows to limit the offset within specs. At the same time, since the detector charge polarity is intrinsically negative (the signal is generated by electrons), the CSP output signal embeds a decreasing behavior. For this reason, a PMOS discriminator input stage has been preferred to NMOS.

Dealing with the threshold, the 9-bit R-2R Resistive DAC has a 1.2 mV LSB and 500 mV full-scale. The input digital words, independent for each channel, are stored into dedicated registers managed from the $I^2C$ interface.

The event-driven reset signal is generated starting from the DISC output. In fact, with the simple use of a passive RC net and an OR logic gate, the reset pulse delay can be set. In detail, the RC time constant is applied to the DISC output signal and sent to one OR input. When the voltage is high enough the OR switches high, closing the CSP feedback switch. The other OR input can be used as a general channel reset. In this case, a 150 ns time constant has been set.

### *C. Calibration*

The channel structure of GEMINI relies on capacitors, included in the CSP feedback and in the CSP Opamp for stability compensation. For correct functioning, their maximum spread has not to exceed 5%. In fact, the CSP feedback capacitor ($C_F$) value controls the CSP gain, as well as the loop gain and the Opamp phase margin. But the CMOS integration process, due to its nature, leads to statistical variations of all parameters involved in a circuit [5] and its precision by itself is not enough. The solution for this issue consists in designing a calibration circuit [6], able to tune the capacitors value directly on-chip and automatically, including only a precise current reference and a stable clock signal. Practically, cited critical capacitors has been implemented with a switchable binary weighted capacitor array. A logic unit algorithmically manages the array opportunely with a digital word, limiting the maximum error in capacitances $\epsilon_c$ with respect to the nominal value as in Eq. (3). $\Delta C$ represents the maximum capacitance spread due to CMOS process variations.

$$\epsilon_c = \Delta C / 2^{N-1} \tag{3}$$

Note that fixing the number of array bits N corresponds to fixing the maximum error. In this project 5 bits arrays have been chosen to obtain the desired spread range.

### *D. Digital Control*

The GEMINI embeds an $I^2C$ interface for controlling the calibration and channel settings, exploiting its bidirectional 2-line feature for managing up to 16 ASICs at the same time (256 channels), with a single external master device achieving a strong improvement in portability. As regards the channels, $I^2C$ data registers store the 16 9-bit digital words for threshold R-2R DACs. The $I^2C$ interface also controls directly the calibration unit option for manually setting the capacitor digital word through a dedicated $I^2C$ register.

## III. GEMINI Performance Results

The GEMINI photo is depicted in figure 3. The die occupies 6.89 mm$^2$. The 16 channels are in the center, while the I$^2$C slave interface has been placed to their left side, while the calibration unit to their right. The LVDS drivers have been placed in the top, close to the output pads.

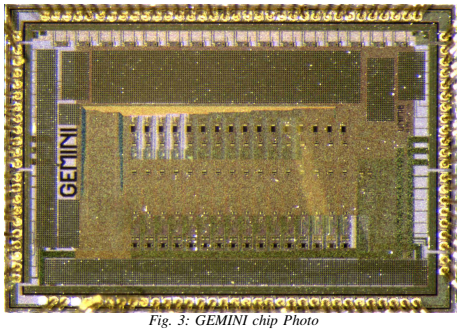


*Fig. 3: GEMINI chip Photo*

### A. Post-Layout Simulation Results

After parasitic extraction, transient noise and Monte-Carlo post-layout simulations have been run, including temperature variation between −40 °C and 120 °C, as well as supply voltage 10% maximum spread. The input pixel capacitance has been set to 40 pF. This worst-case scenario represents an optimum testbench also for radiation hardness. Although measurements during irradiation are a must, these results can prove for an overall robustness.

Figure 4 shows the transient noise simulation related to the CSP output signal generated from the minimum input charge (30 fC). This simulation demonstrates that, also with the 40 pF pixel capacitance, the CSP design is valid in terms of noise, since setting the threshold for the minimum detectable charge specification (3 fC) will not generate false-positive events.

Figures 5 and 6 show the Monte-Carlo results. Together with the input signal, the channel analog and the digital outputs are shown. Note the effect of event-triggered reset on output signals. This evident spread in reset time (25 ns) is justified by reset time constant variation (passive RC net) due to CMOS process. This variation is not critical, since the output signal does not contain any information in the time duration. On the contrary, the trailing edge is very precise through corners, with a 7.7 ns maximum spread.

To clarify the timing performance of GEMINI, in Figure 7 the detection delay is plotted versus the input charge, with different pixel capacitance values. The global effect of delay reduction is evident while decreasing the pixel capacitance value, but also is the delay spread over the entire charge range. In fact, in Figure 8 the detection jitter is depicted versus the pixel capacitance, showing a maximum value of 7.7 ns.

As regards noise performance, the ENC dependence from the pixel capacitance is plotted in Figure 9. The results confirm Eq. (2), with a linear dependence from the input pixel capacitance. The maximum ENC value, obtained at maximum pixel capacitance (40 pF), corresponds to 1.48 fC.

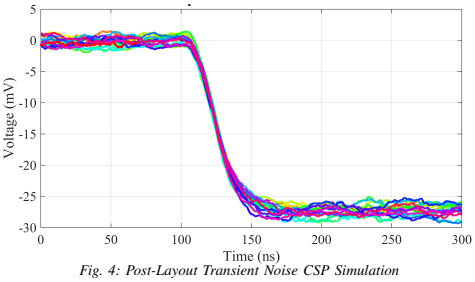


*Fig. 4: Post-Layout Transient Noise CSP Simulation*

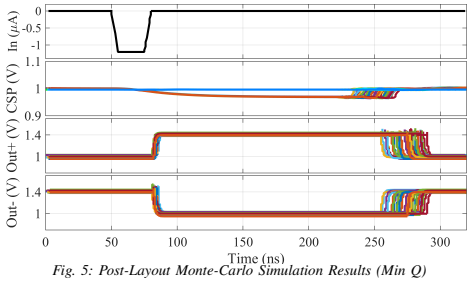


*Fig. 5: Post-Layout Monte-Carlo Simulation Results (Min Q)*

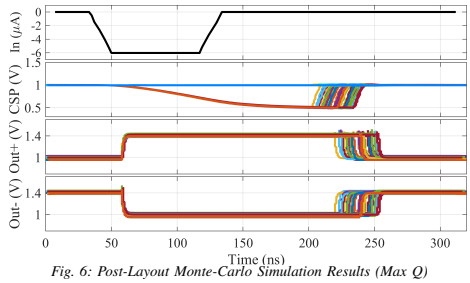


*Fig. 6: Post-Layout Monte-Carlo Simulation Results (Max Q)*

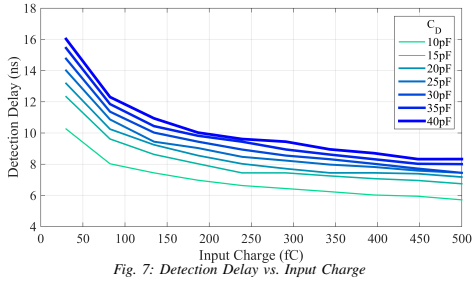


*Fig. 7: Detection Delay vs. Input Charge*

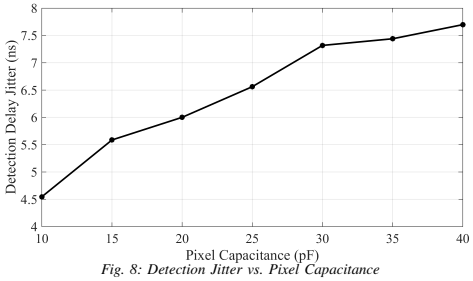


*Fig. 8: Detection Jitter vs. Pixel Capacitance*

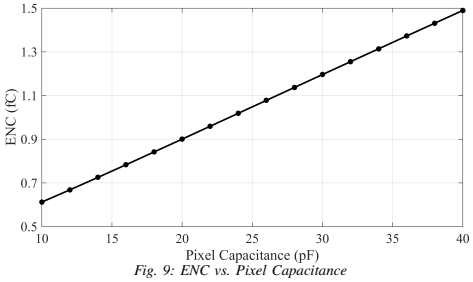


*Fig. 9: ENC vs. Pixel Capacitance*

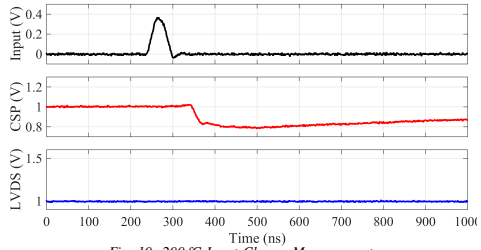


*Fig. 10: 200 fC Input Charge Measurement*

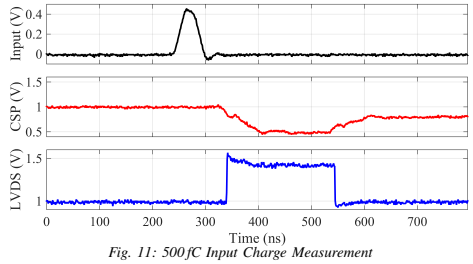


*Fig. 11: 500 fC Input Charge Measurement*

### B. Preliminary Measurements Results

Preliminary measurements on GEMINI prototypes are depicted in Figures 10 and 11. In both cases the threshold has been set to maximum charge (500 fC). In fact, the LVDS signal becomes available only in the second case. In addition to this, the extracted sensitivity is 1 mV/fC, as expected.

### C. Summary

| Parameter | GEMINI | CARIOCA | GASTONE64 |
|---|---|---|---|
| CMOS Tech. | 180 nm | 250 nm | 350 nm |
| Supply Voltage | 1.8 V | 2.5 V | 3.3 V |
| # of Channels | 16 | 8 | 64 |
| Max Pixel Cap. | 40 pF | 120 pF | 100 pF |
| Max Count Rate | 5 Mcps | 0.8 Mcps | 30 Kcps |
| Min Detectable Q | 2.5 fC | 10 fC | 5 fC |
| Sensitivity | 1 mV/fC | 8 mV/fC | 3 mV/fC |
| Power Cons. | 2.7 mW/ch § | 12 mW/ch | 8 mW/ch |

*TABLE II: Performance.* § *With LVDS Driver: 6.3 mW/ch*

In table II the main GEMINI performance has been shown, in parallel with CARIOCA [2] and a recent development, GASTONE64 [3]. The reduction in power consumption is evident, together with the improved maximum count rate. Note the difference in the input pixel maximum capacitance. In fact either the CARIOCA chip or the GASTONE64 show a limited count rate, relaxing CSP stability constraints. Moreover, the area of a 100-120 pF pixel would be overly large for exploiting the pixellated detector spatial resolution [6]. The high number of channels in GASTONE64 has been reached with the inclusion of a post-processing digital unit in the ASIC, enabling serial channel readout. GEMINI instead, guarantees a parallel and real-time operation.

## IV. Conclusions

A SoC dedicated for the Triple-GEM detector readout, GEMINI, has been presented. It composes of 16 detecting channels, each featuring a Q-to-V conversion followed by an event discrimination with an event-triggered reset. Analog and LVDS digital signals are available in parallel for each channel. The focus has been put on improving count rate and managing input pixel capacitance. The channels are able to sustain a 5 Mcps count rate with a 40 pF pixel capacitance, while consuming 2.7 mW/ch and with an ENC of 1.48 fC. The prototype has been fabricated in 180 nm CMOS technology.

## References

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# Part V

# Conclusions

# 10
# Conclusions

## 10.1 Comparison with the state of the art

Two prototypes, GEMMA and GEMINI, have been designed for Triple GEM detector readout.
The aim of GEMMA (GEM Mixed-signal Asic) is to measure the arrival time and the amount of charge from the Triple-GEM detector.
It composes of 8 detecting channels including a Charge Sensitive Preamplifier (CSP) and a Charge-Time Converter (CTC). It is able to manage up to 15 pF of pixel parasitic capacitance. The embedded calibration system tunes all channels' CSP feedback capacitances, to match the target sensitivity of 0.5 mV/fC within a 5% tolerance. The CTC converts the CSP output voltage signal into digital domain.
In detail, the CTC gets the CSP output and generates two logic output signals. The first, named Charge-Time Signal (CTS), includes information into its time duration, directly proportional to the input charge. The second, named Event Detection Signal (EDS) gives information about the arrival time of the incident particle. In channel 6, for prototyping concern, the CTS is also converted into a 7-bit digital word by a 250 MHz clocked counter (the clock is off-chip). In order to control and stabilize comparators performance, an effective circuital block named Auto-Zero acts as an adjustable level shifter for the CSP output signal, adapting it separately for the two comparators. The shifting is set by a 4-bit logarithmic DAC, representing the actual channel threshold for measurements. The device is able to sustain a count rate up to 4 Mcps consuming 3.8 mW/ch.
On the other hand, GEMINI (GEM INtegrated Interface) target application includes time-of-flight and counting measurements, with the option to make spectroscopic analysis externally via the analog preamplifier output.
The GEMINI has a mixed signal capability, with analog and digital outputs available in parallel for each one of the 16 channels included, also with automatic on chip calibration acting on channel capacitors, keeping performance constant against CMOS process, supply voltage and environmental variations. This allows managing a count rate up to 5 Mcps and an input pad capacitance up to 40 pF, while consuming 2.7 mW/ch.
As a whole, GEMINI channels include a charge-sensitive preamplifier (CSP) with a sensitivity of 1 mV/fC. Then, a discriminator (DISC) with a channel-specific threshold set by a 9-bit R-2R Resistive DAC, generates the Event Detection Signal (EDS), then converted to LVDS. The CSP composes of a Class-A Miller Op-Amp with a capacitor and a switch in parallel connected in feedback. The reset generation is event triggered, without the inclusion of a clock signal.

In table 10.1 a parallel with similar designs present in literature, through the principal specifications of each project, is reported.

| PARAMETER | GEMMA | GEMINI | CARIOCA | GASTONE64 | [20] | [21] |
|---|---|---|---|---|---|---|
| *Technology* | 130 nm | 180 nm | 250 nm | 350 nm | 350 nm | 350 nm |
| *Power supply* | 1.8 V | 2 V | 2.5 V | 3.3 V | 3.3 V | 3.3 V |
| *Sensor parasitic cap.* | $\leq$ 15 pF | $\leq$ 40 pF | 120 pF | 100 pF | 100 pF | 10 pF |
| *Max count rate* | 4 Mcps | 5 Mcps | 1 Mcps | 30 Kcps | 0.8 Mcps | - |
| *Power consumption* | 3.8 mW/ch. | 2.7 mW/ch. | 12.5 mW/ch. | 8 mW/ch | - | 9 mW/ch. |
| *ENC* | 418 $e^-$ | 224 $e^-$ | 450 $e^-$ | 941 $e^-$ | 932 $e^-$ | 196 $e^-$ |

Table 10.1: Comparison of GEMMA and GEMINI with the state of the art

The reduction in power consumption is evident, together with the improved maximum count rate. Note the difference in the input pixel maximum capacitance. In fact either the CARIOCA chip or the GASTONE64 show a limited count rate, relaxing CSP stability constraints.
Moreover, the area of a 100-120 pF pixel would be overly large for exploiting the pixellated detector spatial resolution [22]. The high number of channels in GASTONE64 has been reached with the inclusion of a post-processing digital unit in the ASIC, enabling serial channel readout. GEMMA and GEMINI instead, guarantee a parallel and real-time operation.
As regards ENC performance, GEMMA and GEMINI have been evaluated in table 10.1 with no pixel parasitic capacitance, in order to better compare them with other works. If the maximum pixel capacitance is considered, the ENC for GEMMA is equal to 3550 $e^-$, while for GEMINI the value is 9230 $e^-$.
A particular role in this challenge is played by the calibration process, which adapts the implemented capacitors to the particular conditions in which the ASIC has to work. In prevision of employing these chips for several uses, the great adaptivity shown in a so different range of working conditions is encouraging.

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