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Characterization of Chalcogenide Phase Change Nanostructures

Submitted in accordance to the requirements
for the degree of Doctor of Philosophy

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The candidate confirms that the work submitted is his own and that appropriate credit has been given where reference has been made to the work of others.

to my family

Table of contents

List of abbreviations and acronyms

ACE	Acetone
ADF	Annular Dark-Field
AFM	Atomic Force Microscope(-y)
ALD	Atomic Layer Deposition
Bit	BInary digiT
CD	Carrier Density
CG	Control Gate
CHR	Constant Heating Rate experiments
CMOS	Complementary Metal-Oxide-Semiconductor technology
CRN	Continuous Random Network
CT	Charge Trapping flash memory
CVD	Chemical Vapor Deposition
DC	Direct Current
DFT	Density Functional Theory
DRAM	Dynamic Random Access Memory
DRP	Dense Random Packing
DUT	Device Under Test
DVD	Digital Versatile Disk
EDX	Energy Dispersive X-ray spectroscopy
EEPROM	Electrically Erasable and Programmable Read Only Memory
EFM	Electrostatic Force Microscope(-y)
EXAFS	Extended X-ray Absorption Fine Structure
fcc	face centered cubic
FeFET	Ferroelectric Field Effect Transistor
FG	Floating Gate
FIB	Focused Ion Beam
GCR	Gate Coupling Ratio
GST	GeSbTe
GT	GeTe
HAADF	High Angle Annular Dark Field
hcp	hexagonal close packed
HDD	Hard Disk Drive
HR-TEM	High Resolution Transmission Electron Microscope
IC	Integrated Circuit
IPA	IsoPropyl Alcohol
ITRS	International Technology Roadmap for Semiconductors
I/V	Current/Voltage (measurement or plot)
JDOS	Joint Density Of States
MIBK	Methyl IsoButyl Ketone
MIM	Metal-Insulator-Metal
MLS	Multi Level Storage
MOCVD	Metal-Organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTJ	Magnetic Tunnel Junction
MUX	Multiplexer box

NVM	Non Volatile Memory
NW	NanoWire
OS	Oscilloscope
PCM, PRAM, PCRAM	Phase Change [Random Access] Memory
PGU	Pulse Generator Unit
PIDS	Process Integration, Devices, and Structures
PMMA	Poly (Methyl Methacrylate)
PVD	Physical Vapor Deposition
RAM	Random Access Memory
RF	Radio Frequency
RHEED	Reflection High Energy Electron Diffraction
ROM	Read-Only Memory
rpm	revolutions per minute
R_S	Sheet Resistance
RS	Raman Spectroscopy
RW-DVD	Re-Writable Digital Versatile Disk
SE	Spectroscopic Ellipsometry
SEM	Scanning Electron Microscope(-y)
SMU	Source-Meter Unit
SONOS	Silicon/Oxide/Nitride/Oxide/Silicon
SRAM	Static Random Access Memory
STEM	Scanning Transmission Electron Microscope(-y)
STTRAM	Spin Transfer Torque Memory
TEM	Transmission Electron Microscope(-y)
TFT	Thin Film Transistor
UMD	Universal Memory Device
VLS	Vapor Liquid Solid
XANES	X-ray Absorption Near-Edge Structure
XRD	X-Ray Diffraction
XRR	X-Ray Reflectivity

Introduction

Objective of this thesis

The relentless shrinking of electronic devices is rushing the research of novel devices and architectures. This is particularly true for non volatile memories (NVM), which showed unprecedented development in the last 20 years. Among the emerging NVM, phase change memories (PCM) are posed to be a good candidate for replacing conventional Flash technology, promising better performances and higher scalability.

However, further development is needed to achieve the power consumption reduction and the data retention improvement in PCM. These issues are being addressed by the scientific community by investigating materials properties and exploiting novel device architectures. Moreover, device scaling is mandatory for their ultra large scale integration, and the functional characterization of phase-change nanometric structures is of great interest.

This work basically pursues the same objectives, i.e. the investigation of the physical properties and functionality of phase-change nanostructures as a function of geometry and composition. The first objective will be pursued by characterizing nanoscaled films and wires of phase-change materials based on chalcogenides. The second objective will be pursued by investigating the effect of stoichiometry on the physical properties of the material.

In addition, novel growth techniques (namely, metalorganic chemical vapor deposition), which offer better compositional control, will be employed to synthesize these materials. The characterization of thin films and nanowire of phase change materials, based on chalcogenides, will be carried out by means of various techniques. In this regard, a special

focus will be put to the investigation of the electrical properties of these materials/devices, both at the macroscopic and the nanoscopic level. To this end, sample preparation and technological issues play a significant role and will be discussed thoroughly.

This Thesis work was carried out at the Laboratorio MDM (Materials and Devices for Microelectronics), part of the National Research Council of Italy, located in Agrate Brianza (Italy). A short intern period (May-July 2011), consisting of experimental research, was conducted at LRSM (Laboratory for the Research on the Structure of Matter), University of Pennsylvania, Philadelphia (USA).

Map of the manuscript

In Chapter 1, a comprehensive introduction on the status of semiconductor technology is presented, with a special focus on non volatile memory devices.

In Chapter 2, properties and features of chalcogenide phase change materials are highlighted.

In Chapter 3, the techniques employed in this work are illustrated, from a theoretical point of view.

In Chapter 4, the novel experimental setup, which was implemented for this work, and the sample preparation is detailed.

In Chapter 5, results of characterization of two-dimensional nanostructures are discussed.

In Chapter 6, results of characterization of one-dimensional nanostructures are discussed.

In Chapter 7, conclusions are reported in light of the results achieved so far.

In the Appendixes, additional information are given concerning the algorithms and measurement techniques used in the experiments.

1. Materials for non volatile memories: science and technology

"By 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer"
Gordon E. Moore

The pervasiveness of electronics

Nowadays, electronic devices are ubiquitous. They control cars, elevators, airplanes, and satellites, and can be found in a remote control, in a TV set, as well as in a toaster. Portable electronic devices can be handheld as smartphones, worn as clocks, or even carried in our own body – such as insulin probes or heart pacemakers.

In 1946 electronic devices were as cumbersome as a whole room. The first computer, ENIAC, had a remarkable computational power at that time but a great amount of energy was needed to operate it. In the time span of sixty-five years, we got from ENIAC 385 multiplication operations per second[1] to ≈ $40 \cdot 10^9$ floating point operations per second (an entry-level pc processor[2]). This astonishing evolution owes to several reasons.

One reason is to be found in the extraordinary research effort put out in these years. The invention of new electronic devices and the improvement of existing ones made it possible to have faster and better 'building blocks' for the electronic appliances. In this regard, significant milestones in this field are the inventions of the bipolar junction transistor by Shockley,

Bardeen, and Brattain in 1947, the manufacturing of the first integrated monolithic operational amplifier by Widlar in 1963, coming to the announcement of full 3D-gate transistor[3], as of 2011. Alongside, the discovery and understanding of the physical properties of semiconductors, and in particular of silicon (Si) and silicon dioxide (SiO_2), opened the path to the low cost, high yield, mass production of high performance devices.

Another reason is to be found in this intrinsic trait of semiconductor devices, that is often taken for granted but that deserves to be mentioned here. The energy/speed ratio of electronic devices is a constant and is given by the geometry of the device. To better describe this statement, suppose we are to scale a transistor dimensions by keeping the electric field constant across the channel. Doing so requires scaling down the channel length L, oxide thickness d, junction resistance r_j, threshold voltage V_T, drain voltage V_D, while increasing the doping N_A by the scaling factor k as shown in Table 1.1.[4] As a consequence, the power consumption of the device scales as:

Parameter	Scaling factor: Constant-$\mathscr{E}$	Scaling factor: Actual	Limitation
L	$1/\kappa$	/	/
$\mathscr{E}$	1	>1	/
d	$1/\kappa$	$>1/\kappa$	Tunneling, defects
r_j	$1/\kappa$	$>1/\kappa$	Resistance
V_T	$1/\kappa$	$\gg 1/\kappa$	Off current
V_D	$1/\kappa$	$\gg 1/\kappa$	System, V_T
N_A	κ	$<\kappa$	Junction breakdown

Table 1.1 – Scaling effect in integrated devices[4]

$$P \propto L(V_D - V_T)^2 = \frac{1}{k^3} \tag{1.1}$$

That is to say, power consumption scales as the third power of the scaling factor k. Although constant-*E* scaling is not feasible in real devices, eq. 1.1 holds true – at least qualitatively – for all scaling rules. Furthermore, since the power-frequency ratio is a constant for electronic devices, this implies that geometrical scaling makes it to have either faster or low-power devices, or a combination of the two.

The shrinking of the device geometry enables packing more and more devices into a single *chip*. In this context, a chip is defined as a single monolithic integrated circuit. By monolithic we indicate that the chip is fabricated in a single manufacturing process that makes use of one semiconductor substrate. By integrated circuit (IC) we indicate that one chip contains one or more devices. This is usually the case for conventional semiconductor manufacturing process based on thin wafers (few tenths of mm in thickness, up to 400 mm in diameter), obtained from a silicon single crystal of cylindrical shape.

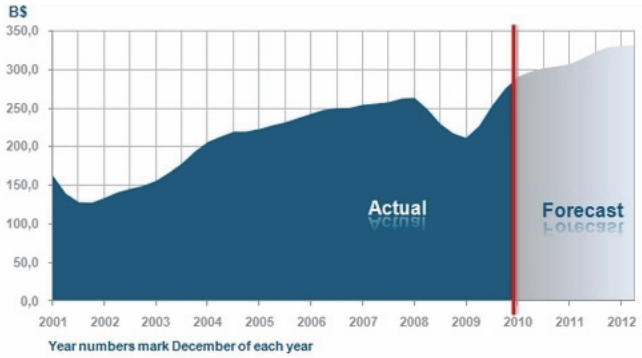

Figure 1.1 – Worldwide semiconductor billings (US$) per 12 months rolling average and forecast[5]

Semiconductor industries keep pursuing device scaling. This trend is being boosted not only by the desire to have faster devices, but by economic reasons as well: in the last 10 years, the worldwide billings value for semiconductor industry doubled, as shown in Figure 1.1, and it amounts to an outstanding US$ 313.8 billion (as of 2011)[5].

Scaling trend in electronics

"No exponential is forever… but we can delay forever"
Gordon E. Moore

The relentless pace of improvement of electronic devices has been well described by the so-called Moore's Law. Gordon E. Moore, Ph.D. in Physical Chemistry and Director of the most

important semiconductor firm at that time (Fairchild Corp.) was endowed with great scientific knowledge and economic insight. The first formulation of his empirical law dates back to 1965 on the scientific journal *Electronics*[6]; a refinement was released in occasion of the 1975 speech at Electronic Device Meeting[7]. Moore described and forecasted the increase rate of transistor density in integrated circuits as a function of time, to double every two years. The resulting plot is summarized in the following Figure, where the logarithmic Y-axis scale should be noted.

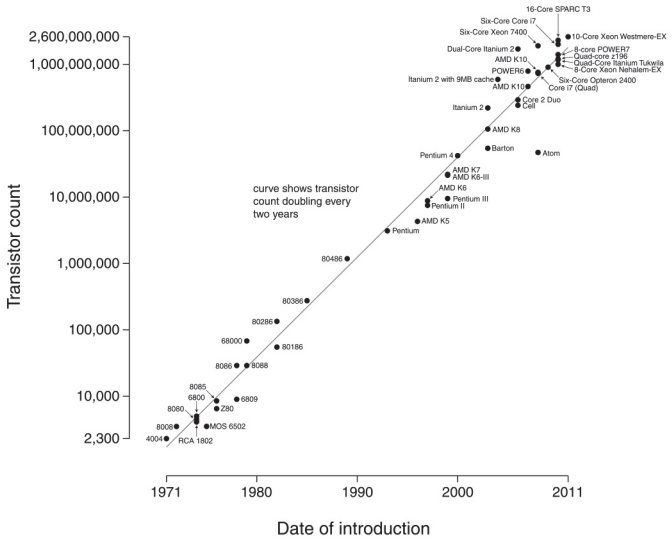

Figure 1.2 – Plot of CPU transistor counts against dates of introduction. The fitted line corresponds to exponential growth, with transistor count doubling every two years[8]

Although Moore's Law accuracy is striking, it must be noted that this is more of an economic law than a technologic one. In his paper, Moore indicated the trend of transistor density at which the production costs achieve a minimum. In other words, his Law specifies the pace at which industry can improve manufacturing technology and yield, while minimizing costs. For this reason some, including Moore himself, believe that the current trend is a consequence, rather than a prediction, of Moore's Law[9,10].

The International Technology Roadmap for Semiconductors (ITRS) is a yearly report delivered by a Committee of scientists and technologists, jointly sponsored by all semiconductor industries worldwide. It is a key document that conveys the most exhaustive and accurate assessment of the current state of technology in the semiconductor field. At the same time, it sets both short and long term objectives on the state of the art in semiconductor technology and can be considered an authoritative schedule the manufacturers contribute to and rely on. In the latest 2009 report, the ITRS Committee basically corroborated Moore's Law trend up to (an impressive) year 2024.[11]

So far, the scaling was defined as the "number of transistors per unit area" or as the "smallest device half-pitch between metal lines". As new devices emerge, these definitions, that used to be valid for logic (transistor-based) devices only, are being discontinued. The ITRS now distinguishes between the following categories: logic, volatile memories, non volatile memories. Most of these devices were, and are still, based on complementary metal-oxide-semiconductor (CMOS) technology. In CMOS technology, both n- and p- type transistors are integrated on the same monolithic circuit and logic function is performed by the paired couple. Its main advantage is the reduced power consumption and increased switching speed, thus making CMOS process the leading technology for general purpose integrated circuits[12]. It is interesting to note that the above mentioned device typologies (logic, volatile memory, non volatile memory) are all required components of a *von Neumann machine* (i.e., "a stored-program digital computer that uses a central processing unit and a single separate storage structure to hold both instructions and data")[13,14].

Memories

As mentioned above, one of the components of the *von Neumann machine* is the data storage. It should be pointed out that data storage devices are altogether digital devices. This means that by *data* we are always referring to *digital data* – i.e., an information that can have a finite number of values. It might be redundant to remind that the elementary data unit, that

can take either of two values, is defined as binary digit (*bit*). These two states are conventionally represented by 0 (zero, RESET) and 1 (one, SET).

At the dawn of computer science, memory devices were divided in these two categories: random access memory (RAM) and read only memory (ROM). This distinction has become obsolete now, as most devices can be both read and written.

Two typologies of data storage exist: volatile and non volatile. The following Figure 1.3, reprinted from ITRS, is a helpful summary.

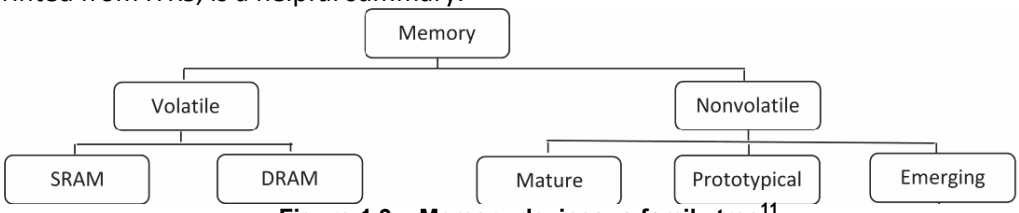

Figure 1.3 – Memory devices: a family tree[11]

Volatile memory devices (Figure 1.3, left) belong to either of two categories, according to the technique employed to store the data: as an electric charge in a capacitor (DRAM) or as the state of a bistable latch circuit (SRAM). Regardless of the differences in performance and speed, both architectures can withhold the logic value as long as they are supplied power to do so – therefore making stored data volatile.

Non volatile memory (NVM) devices (Figure 1.3, right) ought to guarantee data retention even when no energy is supplied. Historically, permanent data storage was achieved by means of punched cards, magnetic tapes, magnetic disks, optical discs, and electrically erasable and programmable read only memories (EEPROM). Starting from year 1990, solid-state semiconductor-based non volatile memories became commercially available. Their commercialization was such a breakthrough that NVM sales overtook EEPROM sales in just 2 years since introduction; nowadays, NVM are replacing nearly all kind of permanent storage media. In general, these devices perform data storage by encoding the digital logic data as a physical property of the matter, while their performances and features depend on the given mechanism, as will be described in the following section.

Non volatile memories: state of the art

There are more non volatile memory cells produced annually in the world than any other semiconductor device and, for that matter, any other human made item[4]

This category of devices is gaining more and more relevance within the semiconductor industry. As mentioned above, the rate at which NVM have been, and still are, overtaking the other recording media is impressive. Figure 1.4 shows how the number of globally shipped NVM units outperforms conventional magnetic hard disk drives (HDD) by at least one order of magnitude (as of 2011), the gap getting wider and wider[15]. The main stimulus to this trend is given by the wide spreading of portable devices[16] (smartphones, tablet computers, netbooks) and the increasing demand for digital contents (which are often available to download remotely and store locally). Such portable devices require lower power and smaller form factor NVM devices to work, hence triggering increasingly demanding requirements and production of more and more NVM units.

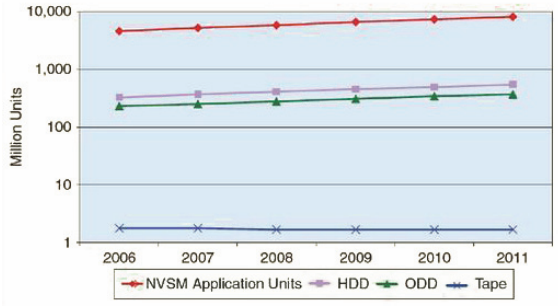

Figure 1.4 – Number of NVM units shipped vs. HDD[15]

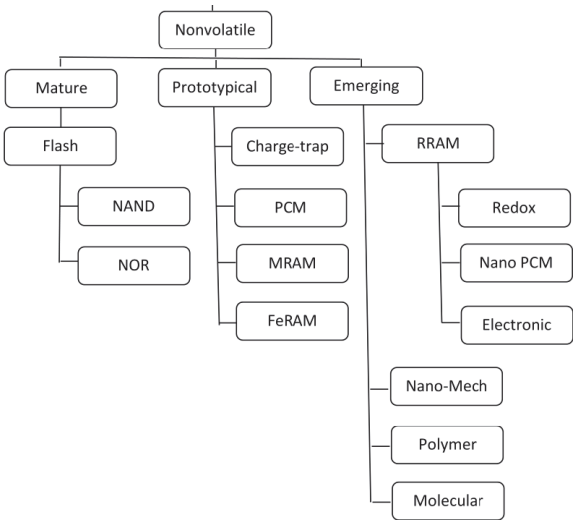

Figure 1.5 - Non volatile memory family tree[11]

Let us now have a look at the working principle of NVM. The ITRS committee classifies nonvolatile memories according to the maturity level of the technology. In Figure 1.5 (reprinted from ITRS Roadmap[11]), a comprehensive overview of volatile and non volatile memory devices is presented. The most mature technology in NVM category, whose devices have been commercially available since 1990, is to the so called *Flash* memories

A Flash device resembles a Metal Oxide Semiconductor Field Effect Transistor (MOSFET), with the addition of an electrically insulated, floating gate (FG) where an electric charge is stored (see Figure 1.6 for details). The FG is buried between thin dielectric films so that charging and discharging is achieved by tunnel effect from and toward the MOSFET channel. The external gate (EG) is used to perform the read, write and erase operation of the device. To read the stored value, the EG measures the shift in the threshold voltage of the MOSFET due to the charge stored in the FG. Flash memories come in two architectures, known as NAND and NOR. The features of these Flash architectures are summarized in the following Table 1.2.

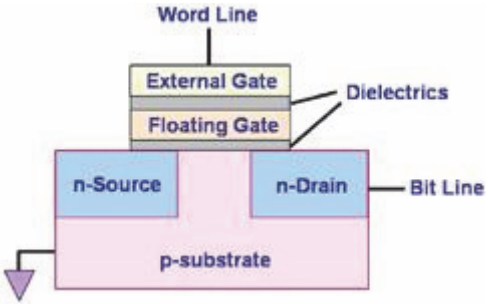

Figure 1.6 – Layout of a flash memory cell

NAND	NOR
faster programming times	slower programming times
higher endurance	lower endurance
page block addressing	bit-level addressing
higher density	lower density
lower cost per bit	higher cost per bit
good replacement for hard disks	good replacement for ROM

Table 1.2 – Flash architecture features

The unmatched success of Flash memory owes to the ease of implementation into the existing CMOS fabrication process, thus being convenient and dependable. Although the prototypal Flash devices required a higher voltage to perform programming of the cell, newer devices have overcome this limitation. By optimizing the dielectric (latest device use oxide–nitride–oxide layers), it is possible to manufacture fast and reliable devices with good data retention and low supply voltage. Since their introduction, these devices down-scaled better than transistors in the 1999-2005 time span, and as much thereafter, thus improving performance and packing density[11]. Featuring a cyclability of 10^5 cycles, a data retention of ≈ 10 years at 85 °C, these devices are still unsurpassed from the technological and economical point of view[17].

Flash technology is also compatible with multi level storage (MLS) techniques to increase data density. By fine-tuning the stored charge in the floating gate, a single cell can hold 2 (or more) bits of information instead of 1. This technique requires the charge to be stored in a controlled manner so as to achieve 4 (or more), well-defined, threshold voltage windows. The result is an 2^n-fold increase in data density. A comparison between a 1 bit/cell and a 2 bits/cell threshold voltage is shown in the following Figures.

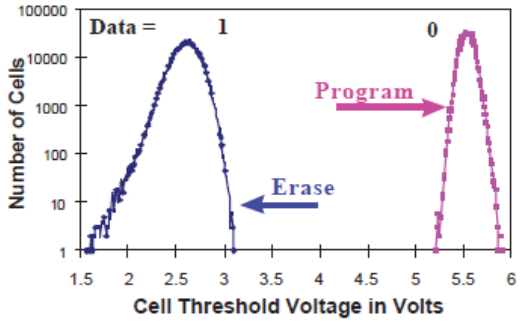

Figure 1.7 - Single-bit/cell array threshold voltage histogram[18]

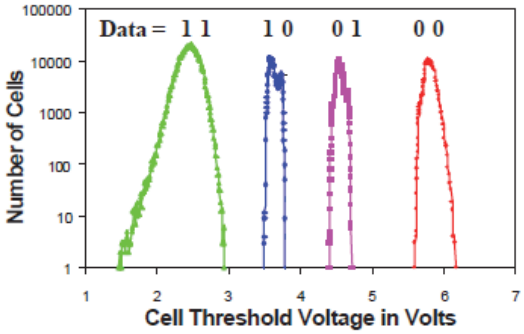

Figure 1.8 - Two-bit/cell array threshold voltage histogram[18]

As of April 2011, 19 nm technology node – defined as the smallest half-pitch of contacted metal lines – memories have already been implemented in commercially available multilevel, 2 bit/cell, Flash device[19].

Scaling issues of conventional NVM

Notwithstanding the continuous improvements, Flash technology is eventually going to run into the scaling limit at the <16nm node[20]. In this regard, both physical and geometrical limitations are impending. The main geometrical limitation to the shrinking of memory cells is the unfeasibility of reducing tunnel oxide and interpoly dielectric thickness below 8 and 12 nm respectively, owing to a parasitic effect known as gate coupling ratio (GCR) (shown in Figure 1.9). In other words, the gate coupling ratio issue involves the shrinking of the gate spacing X to zero, beyond which the neighboring cell cross talk (i.e., interference in the programming voltage/currents) would increase correspondingly.

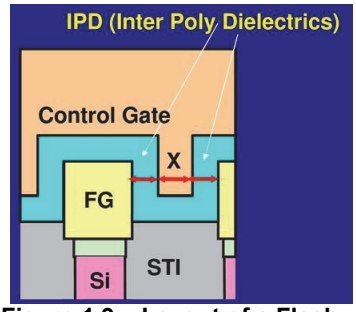

Figure 1.9 – Layout of a Flash memory cell

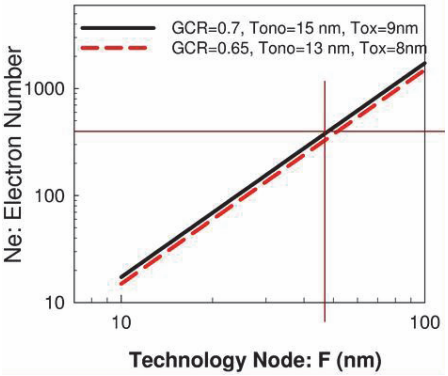

Figure 1.10 – Electron number in the stored charge of a floating gate NVM cell[15]

Another limitation, of physical nature, originates from the actual number of electrons stored as a charge in the floating gate. Upon scaling, the stored charge decreases exponentially as shown in Figure 1.10 (the two plots corresponding to different architectures). Taking into account a statistical ± 10 electron number fluctuation, it is clear that the scaling limit is going to be reached at, or below, the 16 nm node. Notably, this problem does affect all NVM devices based on charge storage, making multi level storage harder to implement.

Once again let us refer to the International Technology Roadmap for Semiconductors to visualize the near term challenges for Flash memory. In the following table, a white cell background indicate that that particular technology node is already achieved and implemented. A yellow background means that technological issues are being addressed but is generally feasible. A red background indicates that the actual implementation requires further research. In Table 1.3, the current status and forecast on technological viability for Flash technology are shown.

Table PIDS5 NAND Flash Technology Requirements--UPDATED								
Year of Production	2009	2010	2011	2012	2013	2014	2015	2016
Poly 1/2 pitch (nm)	34	32	28	25	22	20	19	18
Poly 1/2 pitch (nm)		26	24	22	20	19	18	16
Highest density	32G	32G	64G	64G	64G	128G	128G	256G
Highest density		64G	64G	128G	128G	256G	256G	256G
Cell type (FG, CT, 3D, etc.)		FG	FG	FG/CT	FG/CT	FG/CT	CT-3D	CT-3D
3D NAND number of memory layers		1	1	1	1	1	4	4
Maximum number of bits per cell (MLC)	3	3	3	4	4	4	4	4
Maximum number of bits per cell (MLC)		3	3	3	3	3	3	3
Cell size – area factor a in multiples of F2 SLC/MLC	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Cell size – area factor a in multiples of F2 SLC/MLC		4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3
Endurance (erase/write cycles)		1.0E+05	1.0E+05	1.0E+04	1.0E+04	1.0E+04	1.0E+04	1.0E+04
Nonvolatile data retention (years)		10-20	10-20	10-20	10-20	10-20	10-20	10-20
Tunnel oxide thickness (nm) (Floating gate device)		6-7	6-7	6-7	6-7	6-7	6-7	5-6
Interpoly dielectric material (Floating gate device)		ONO	ONO	ONO	ONO	ONO	High-K	High-K
Interpoly dielectric thickness (nm) (Floating gate device)		10-13	10-13	12	12	9-10	9-10	9-10
Gate coupling ratio (GCR) (Floating gate device)		0.6	0.6	0.6	0.6	0.6	0.6	0.5-0.6
Control gate material (Floating gate device)		n-poly	n-poly	n-poly	n-poly	n-poly	Metal	Metal

Table 1.3 – Flash memory taxonomy[21]

The most critical near-term issues – highlighted in yellow or red – concern: the viability of multilevel storage (beyond 4 bit/cell), cell area factor scaling (after year 2012), interpoly dielectric thickness (below 10 nm). These issues have to be dealt with in the very next future.

By now, it should be clear that even though flash memories are the best currently available technology, alternative non volatile memories are required in the near future. The emerging technology must assure a steady and sustainable cost/bit ratio far beyond the Flash market timescale. A number of choices are being looked into by researcher and scientists. An assessment on the current state of the art for alternative NVM technology will be given in the following paragraph (freely adapted from ITRS Roadmap[11]).

Emerging non volatile memory devices

Charge Trapping Flash memories (CT) – It is an evolution of the conventional flash. The charge trapping layer (typically made of nitride) high-κ band-gap engineered tunnel and blocking dielectrics have been proposed to overcome some of the scaling limits of planar Floating Gate Flash devices without changing the basic architecture of the memory cell. The single gate controls the MOS device channel directly and thus there is no GCR issue, and the cross talk between thin nitride storage layers is insignificant. Nitride trapping devices may be implemented in a number of variations of a basic silicon/oxide/nitride/oxide/silicon (SONOS) type device.

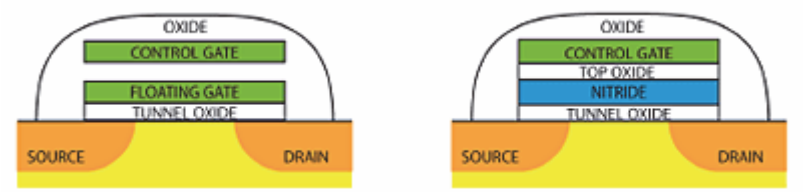

Figure 1.11 - Floating gate (left) versus SONOS (right) memory cells[22]

3-D Arrays – When the number of stored electrons reaches statistical limits, even if devices can be further scaled and smaller cells achieved, the threshold voltage distribution of all devices in the memory array will become uncontrollable and logic states unpredictable. The memory density cannot be increased by continued scaling, but may be increased by stacking memory layers vertically. Successful stacking of memory arrays vertically has been demonstrated in recent years. One approach uses Si single-crystal by lateral epitaxial growth, another uses polycrystalline Si thin-film transistor (TFT) device.

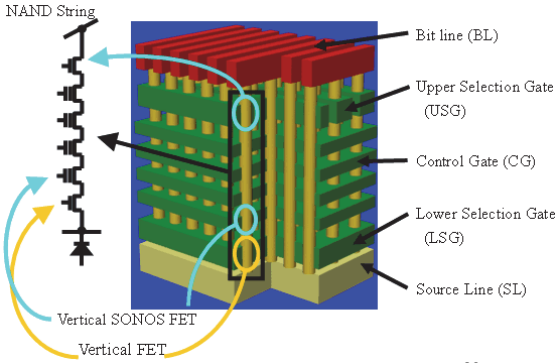

Figure 1.12 – 3D layout of Flash cell[23]

Ferroelectric FET Memory – The Ferroelectric FET (FeFET) is a one-transistor memory device where a ferroelectric capacitor is integrated into the gate stack of a FET. The ferroelectric polarization directly affects charges in the channel and leads to a defined shift of the output characteristics of the FET. A typical ferroelectric material used is $SrBi_2Ta_2O_9$, with a dielectric constant greater than 300. The conductivity of the MOSFET channel is determined partly by a remnant polarization formed in the ferroelectric layer following application of a gate voltage, which is sufficient to exceed the coercive voltage of the ferroelectric layer. Scaling is projected to end approximately with the 22 nm generation, because the insulation layer becomes too thin and the properties of the ferroelectric with respect to thickness dependence of the coercive field will not allow further reduction. Another important challenge is the very short retention time, approximately 30 days, for the FeFET.

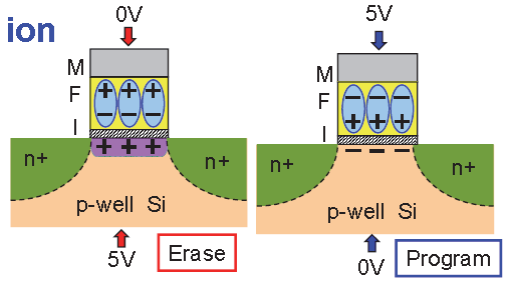

Figure 1.13 – -Ferroelectric-Insulator-Semiconductor structure and operation

Spin Transfer Torque Memory (STTRAM) — These devices employ a magnetic tunnel junction (MTJ) as the memory element. The memory cell consists of a semiconductor isolation device and an MTJ with two ferromagnetic layers separated by an MgO-based tunneling barrier layer in which thickness is controlled to approximately 1 nm. Switching MTJ states occurs as a result of the flow of spin-polarized conduction electrons through the MTJ. The spin-polarized current transfers angular momentum to the spins of the core electrons in the magnetic free layer causing it to switch.

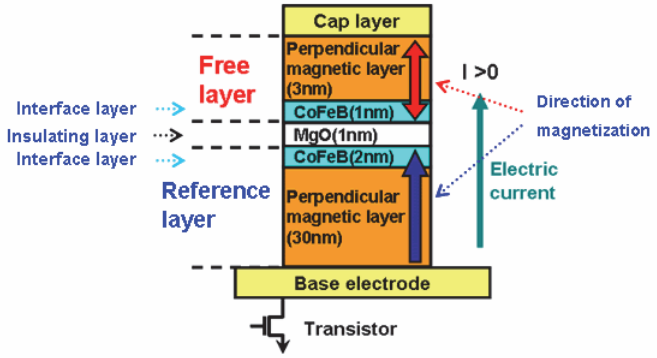

Figure 1.14 – Layout of STTRAM[24]

Resistive RAM (RRAM) — In RRAM elements, consisting of a nano-scale metal-insulator-metal (MIM) structure, typical resistive switching phenomena are based on thermal effects which result in unipolar switching characteristics. Thermal process is initiated by a voltage-induced partial dielectric breakdown in which the material in a discharge filament is significantly modified due to Joule heating. Because of the current compliance, only a weak conductive filament with a controlled resistance is formed. This filament may be composed of the electrode metal transported into the insulator, carbon from residual organics, or decomposed insulator material such as sub-oxides. During the reset transition, this conductive filament is disrupted thermally because of high power density in the order of 10^{12} W/cm^3 generated locally.

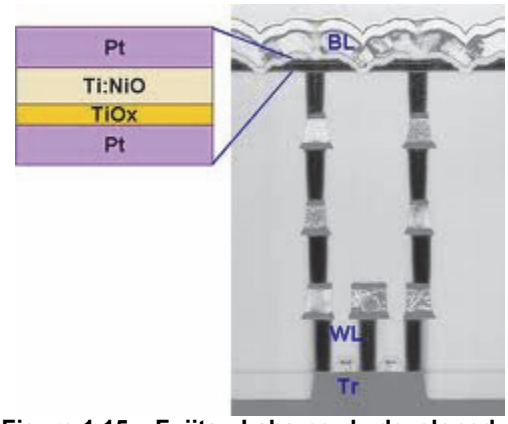

Figure 1.15 – Fujitsu Labs newly developed ReRAM device (left) in combination with a transistor (right)[25]

Phase Change Memory (PCRAM or PRAM or PCM) – These devices exploit the resistivity difference between the amorphous and the crystalline states of a chalcogenide glass (the most commonly used compound is GeSbTe, or GST) to encode the logic '0' and '1' levels. The device consists of a top electrode, the chalcogenide phase-change layer, and a bottom electrode. The leakage path is cut off by an access transistor (or diode) in series with the phase-change element. The phase-change write operation consists of: (1) RESET, for which the chalcogenide glass is momentarily melted by a short (≈ ns) electric pulse and then quickly quenched into amorphous solid with high resistivity, and (2) SET, for which a lower amplitude but longer pulse (> 100 ns) anneals the amorphous phase into low resistance crystalline state. The 1T1R (or 1D1R) architecture can be implemented, and the resulting cell size is larger (or smaller) than a NOR Flash, depending on whether MOSFET or BJT (or diode) is used. The device may be programmed to any final state without erasing the previous state, hence providing substantially faster programming speed. Additional details on PCM technology and materials will be presented in Chapter 2.

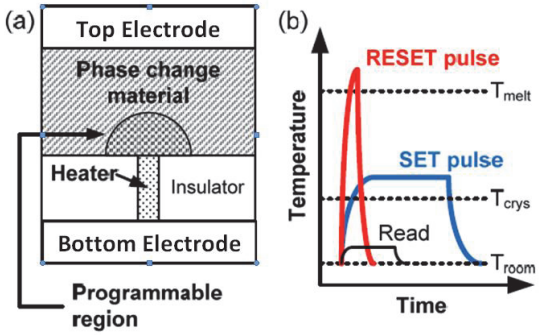

Figure 1.16 – Phase change memory cell and principle of operation

Maturity level of emerging non volatile memories

Some of the above mentioned technologies are still in their early development stage, while the close competitors to NAND flash in the near future are: CT, 3D stacking, FeRAM, PCRAM, MTJ, and STT. Understanding the maturity level of these technologies is crucial to their implementation and is a useful indication for scientists in the field as well (for additional details on the challenges of emerging non volatile memory devices, see also[26]). Once again let us consider the International Technology Roadmap for Semiconductors. The following Figure 1.17 documents the prediction of the committee for "Process Integration, Devices, and Structures (PIDS)" sector on the stage of completion for these new architectures in the time span 2009 – 2024.

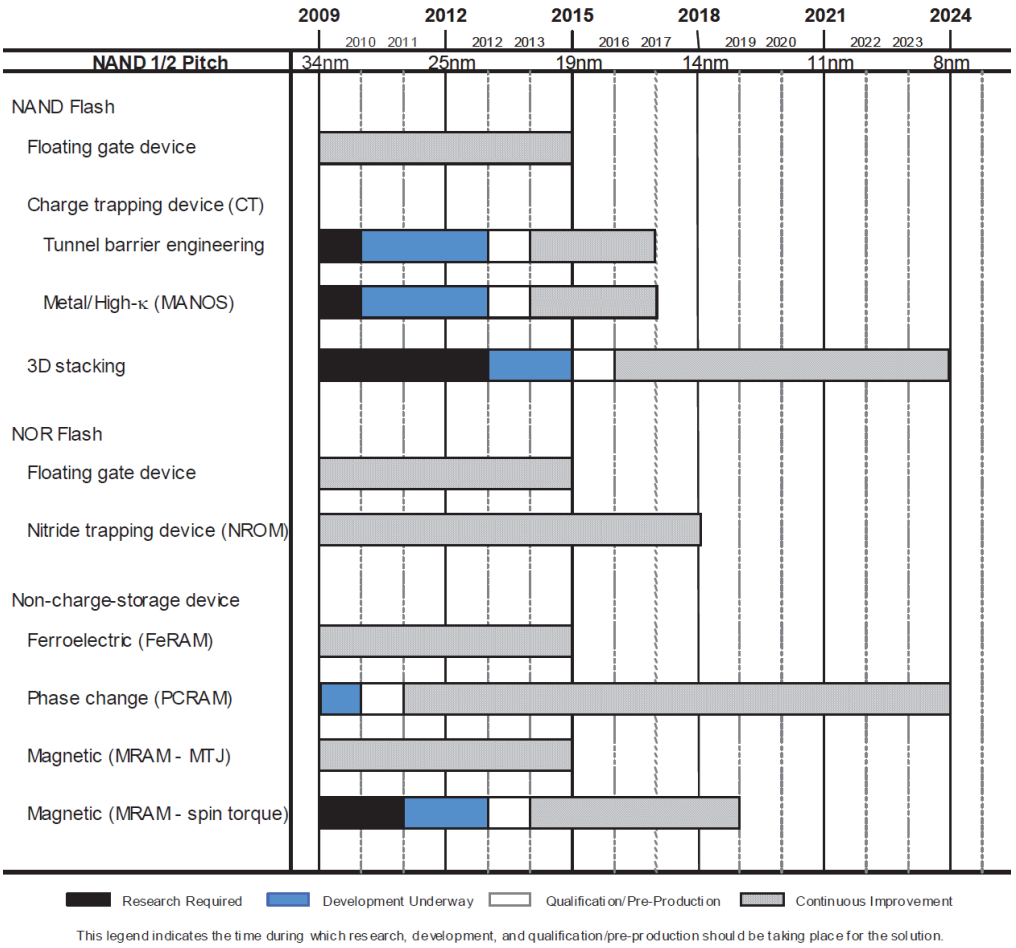

Figure 1.17 - Non-Volatile Memory Potential Solutions

According to ITRS forecast, FG-based flash memories will reach obsolescence in 2014. In the near future there will be a transition period as charge trapping devices – featuring improved materials and architecture – will coexist along with FG flash. Beyond that time, only 3D architecture will make the survival of charge storage devices possible, if viable, until 2024. NOR devices will follow a slightly different route, with an even more limited scope – this architecture being limited to niche applications. Among novel devices, spin transfer torque and phase change are the only promising candidates for long term replacement of Flash. STTRAM, however, are in a prototypal stage in research, and further development is due in the future. On the opposite, PCM functionality has been demonstrated and is already implemented in commercially available devices. Let us summarize the main features and issues in the following Table, where a comparison is shown between the 16 nm scaled NAND Flash and the emerging technologies[20] (for the sake of clarity, the best and worst performing technologies have been highlighted for each feature).

	NAND FLASH	FeFET	NEMS	STT-MRAM	Redox RRAM	PCM RRAM	Electronic Effects RRAM	Macromol RRAM	Molecular RRAM
Minimum F -Scaling	16nm	22nm	5-10nm	7-10nm	5-10nm	5-10nm	5-10nm	5-10nm	5-10nm
Cell Size	2.5F^2	8-4F^2	6-12F^2	20-40 F^2	8/5F^2	6F^2	8/5F^2	8/5F^2	5F^2
MultiLevel	3-bits/cell	NA	Yes	MLC 2bits/cell	Yes	4 bit/cell	Yes	NA	NA
Write/Erase Voltage	18-20V	0.6/-0.2V	1.5V	< 1.8V	<0.5V	<3V	<3V	1V	80mV
Read Voltage	0.1-0.5V	NA	3V	0.5V	<0.2V	<3V	0.7V	0.7V	0.3V
Write Erase Current	Low	NA	NA	<100μA	0.4μA	>100μA	NA	NA	NA
Write Erase Time	>10μs	20ns	0.9ns/0.3ns	<100ns	<5ns	<50ns 120ns	<20ns	<10ns	<40ns
Read Speed	15-50 □s	20ns	>1.5ns	10-20ns	<10ns	<60ns	<10ns	<10ns	<10ns
Retention Time	10yrs	~33ds	10yrs	10yrs	10yrs	10yrs	10yrs	10yrs	10yrs
Endurance Cycles	10^4-10^5	10^{12}	NA	2E12@10ns 2E6@10ms	10^{16}	10^{15}	10^{16}	10^{16}	10^{16}
Write Energy per Bit	>1fJ	2fJ	0.03fJ	<4pJ	1fJ	<2pJ	<100pJ	NA	0.2aJ
Ease of Integration	10 Masks	NA	NA	3-4 Masks BEOL	1fJ	2-3 Masks to BEOL	NA	NA	NA

Table 1.4 - Performance parameters projected for the fully scaled emerging research memory technologies, compared with NAND Flash scaled to the 16nm technology generation[20]

Phase change memories

When considering the requirements for emerging non-volatile memory devices, phase change memories are more appealing than any other competitor thanks to these features:

- not based on charge storage
- down-scalable to ≈ 2.5 nm
- ≈ ns write/erase speed
- multi-level storage feasibility
- bit level addressing
- direct bit programming
- unipolar electrical operation
- low operating voltage (< 3 V)
- cyclability up to 10^{12}
- less power-hungry
- cell size as small as 1D1R

The main weakness of phase change memories is the high current required to reset (amorphize) the cell – as a consequence of the high conductivity of the SET state. This and other issues can be addressed by engineering the material, since chalcogenide properties can be tuned by composition, as will be shown in the following Chapter. In addition, SET operation time is markedly longer than RESET, owing to the longer crystallization time. This issue, and the power consumption issue are expected to be solved by down scaling the active area of the cell[17,27].

The invention of PCM devices is a result of the discovery of the fast, reversible, electrically-triggered phase switching in chalcogenides materials by Stanford R. Ovshinsky in 1968[29]. The implementation of this discovery was secured by several patents, the most notable of which is US Patent 3,271,591[30] in which Ovshinsky described "more specific yet covering broad possible device configurations and operations"[31] than others' patents. Nowadays Ovshinsky-founded Ovonyx, Inc. holds most of patents on this technology. Actual implementation of PCM became recently viable owing to a combination of technological factors such as controllable deposition of thin films, materials availability, low-temperature deposition process, and so forth.

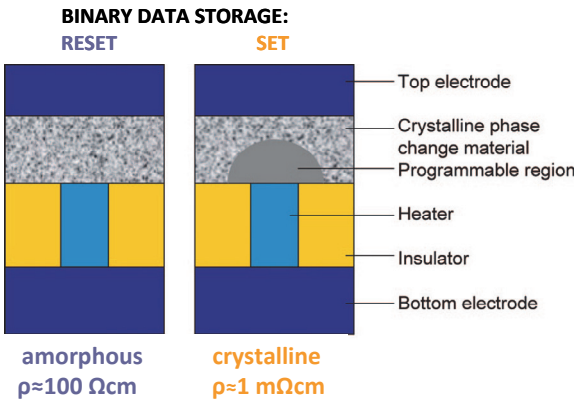

Figure 1.18 – Principle of operation of PCM[28]

As a matter of fact, non volatile memories featuring chalcogenide phase change materials have been made commercially available by at least two major manufacturers in the last 18 months, according to press releases by Micron Technologies, Inc.[32] and SAMSUNG[33].

One of the strengths of phase change memories owes to the non-charge based operation. On the contrary, data is encoded as the structural phase of a small volume of phase-change material. Notably, full functionality was recently demonstrated in aggressively down-scaled PCM nanodots, ≈ 2.5 nm in diameter[34]. The archetypical PCM device is shown in Figure 1.18, where the '0' value is stored as amorphous phase (left) while the '1' value is stored as crystalline phase (right).

The following definitions will be used in the following chapters:

RESET	the binary 0, i.e. the amorphous, high resistance state
SET	the binary 1, i.e. the crystalline, low resistance state
WRITE	the operation of changing the cell to SET state (i.e. crystallize)
ERASE	the operation of changing the cell to RESET state (i.e. amorphize)

Table 1.5

Contrarily to conventional non volatile memories, PCM is a bit-addressable type of memory device, hence the ERASE operation is not required prior to the WRITE operation.

The performance of PCM closely depends on the physical properties of the phase change material. Among the broad variety of phase change materials, research is now focused on a very special class thereof: chalcogenides. In Chapter 2, a comprehensive description of these materials will be provided.

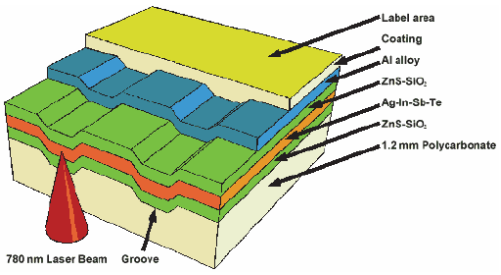

Figure 1.19 – Cross section of layers in a RW-DVD[35]

From the device design point of view, the main requirement of PCM is a large difference in any of the following physical properties: electrical resistivity, reflectivity. The latter is already exploited in optical data storage devices. Rewritable Digital Versatile Disks (RW-DVD) feature a thin AgInSbTe layer, which gets amorphized/crystallized by the focused heating of the laser beam in the optical drive. The recorded data is then read by measuring the variation in reflectivity by a (weaker) laser beam. Since the phase transition is reversible, these disks can be rewritten about one thousand times before failure (which is due to technological limitations and not the material).

As an evidence of the effect of material engineering in the performance of the device, let us consider the following Figure 1.20, where the crystallization dynamics of a RW-DVD featuring two different alloys ($Ge_2Sb_2Te_5$ and $Ag_{3.5}In_{3.8}Sb_{75.0}Te_{17.7}$) have been investigated[36].

Similarly to rewritable DVD, phase change in solid-state non volatile memory devices is triggered upon heating, generated by Joule effect of an electrical current flowing through a metallic heater – as shown in the following Figure 1.21 of a prototypical 'mushroom'-type PCM cell. Note that the programmable volume is a substantially small part of the chalcogenide thin film.

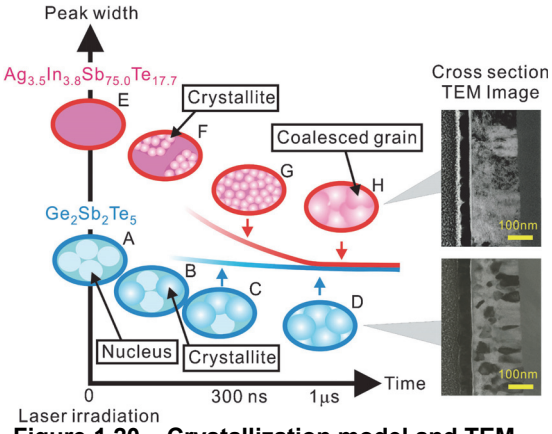

Figure 1.20 – Crystallization model and TEM image in two chalcogenide alloys[36]

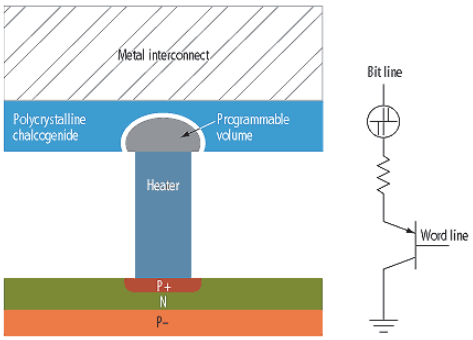

Figure 1.21 – Schematic of a prototypical 'mushroom' type PCM cell[37]

The principle of operation is basically the same in both optically- and electrically-driven phase change devices (RW-DVD and PCM respectively). In order to crystallize the material, a longer (≈ µs), weaker current pulse has to be flowed through the heater. During this time span, the chalcogenide heats by Joule effect up to its melting temperature. Subsequently, it cools down (relatively) slowly enough so as to rearrange into a (poly-)crystalline phase. On the contrary, supplying a shorter (≈ ns), more intense current pulse triggers a rapid heating/quenching process which results in the amorphization of the chalcogenide. Provided that the current pulse has steep enough falling edge, heat will dissipate quickly for the melt to amorphize[38]. Further insight on the phase change transition of chalcogenide will be given in Chapter 2. Operation is shown schematically in the following Figure 1.22.

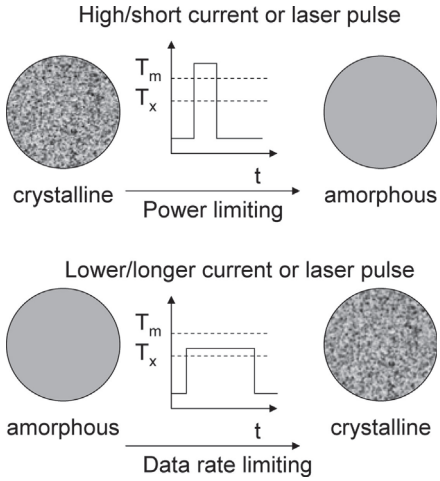

Figure 1.22 – Optically or electrically driven operation: RESET (top) and SET (bottom)[28]

Note that intensity and duration of the pulses required to SET or RESET the cell are not known *a priori* and depend on the specific device and material. However, as a rule of thumb, smaller phase-change areas require less energy (as a matter of fact, decananometric devices require roughly hundreds ns pulse length, hundreds pJ pulse energy). In DVDs and in NVM, the active area of the chalcogenide is as small as the spot of the laser beam or the technological node – in both cases, some tens of nm. From the implementation point of view, fast quenching is achieved by burying the chalcogenide amid layers so as to provide quick heat dissipation from the active area within the required timescale.

The main drawback of PCM is the heat propagation from one cell to the neighboring – a disturb which can trigger the (unwanted) phase-change of the adjacent cells. This phenomenon, called *thermal crosstalk*, poses a substantial limitation to the packing density of devices in a PCM. Two approaches are taken to overcome this limit: 1) thermal design to control the heat flow, and 2) the research of improved capping materials. Most actual implementations of PCM consist of several capping layers and a significant research is devoted to the modeling and development of a viable layout. In Figure 1.23, the temperature gradient and the final temperature in the neighboring, disturbed, cell is shown.

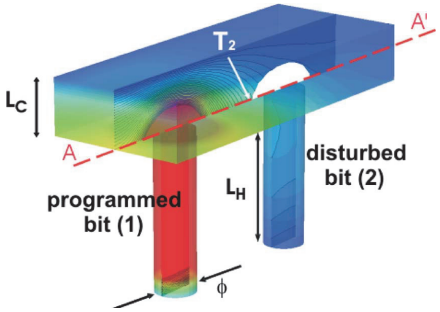

Figure 1.23 – Calculated 3-D thermal map for two adjacent cells, assuming that the left cell is being programmed while the right cell is in a reset state[39]

Finally, some experts believe that PCM could in principle become the Universal Memory Device (UMD). In such architecture, one device would provide both long term and short term data storage and computation. The UMD should feature timings as fast as a SRAM (≈ 5 ns), along with non volatility, high density, and low-cost manufacturability. This concept device has been theorized[40] but no real device has succeeded in meeting these requirements so far. It is the opinion of many technologists that such a universal memory device will never exist, due to the intrinsic incompatibility among these requirements. However, it might be possible that further scaling of devices shall lead to the successful implementation of faster, lower-power, cheaper non volatile memories. Until that day, it seems wiser to focus on the development and improvement of non volatile memory as we know it. Therefore, no matter whether you believe in UMD or not, phase change memories possess "truly remarkable"[41] features. The present work focuses on the investigation of the physical properties of chalcogenides for phase change memory applications.

Nanostructures and Nanotechnology

By now, it should be clear that device shrinking is the main way to improve performances and reduce power consumption in electronic devices. So far, device scaling has been successfully and (relatively) straightforwardly pursued in planar devices as transistors (BJT, MOSFET) by reducing the film thickness. This trend eventually led to reaching submicrometric features size. In particular, electronic devices are currently in the 32 nm technology node (as of 2011), hence involving nanometric scaling along one dimension.

By extension of this concept, we can imagine to scale down the other dimensions as well. Such a device will have 2 nanoscaled and 1 macroscopic dimensions and is referred to as nanowire (or nano-rod, or nano-tube if hollow). Further shrinking along the remaining dimension leads to a fully 3-dimensional nanostructure, the so-called nano-dot. The resulting geometries have only 2, 1, or 0 macroscopic dimensions and are shown in the following Figure respectively.

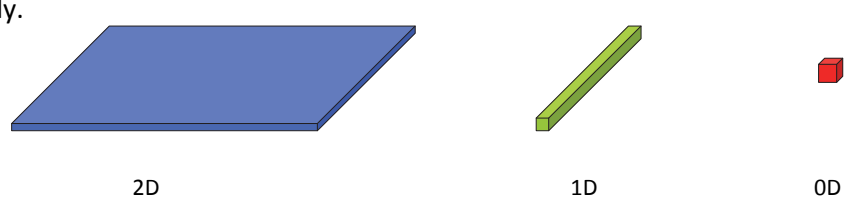

Figure 1.24 – Classification of nanostructured geometries

The exploration (and exploitation) of nano-scaled materials belongs to new discipline called *nanotechnology*. This term was first coined by Norio Taniguchi at the International Conference on Precision Engineering in 1974, to refer to the "production technology to get extra high accuracy and ultra fine dimensions, i.e., the preciseness and fineness on the order of 1 nm"[42]. A better, general purpose definition has been given by NASA: "Nanotechnology is the creation

of functional materials, devices and systems through control of matter on the nanometer length scale (1-100 nanometers), and exploitation of novel phenomena and properties (physical, chemical, biological, mechanical, electrical...) at that length scale". A thesis on nanotechnology (such as this work) would not be complete without a citation of Richard Feynman's first seminal lecture on nanoscaled materials "There's plenty of room at the bottom"[43], presented at the American Physical Society meeting in 1959, where he envisioned the development of never before imagined applications. The mirage of nanotechnology became real a few years later, with the invention of nano-tools such as the scanning electron microscope and the scanning tunneling microscope.

The key feature of nanostructured materials is that their physical properties differ from those of their bulk counterparts, all other conditions being equal. This is a consequence of the role geometry plays in properties such as: melting temperature, hardness, magnetization, reflectivity, electrical conductivity, band energy, and so forth. At lower dimensions even quantum confinement effects occur. The region which lies between the bulk level (ruled by classical physics) and the atomic/molecular level (ruled by quantum physics) is referred to as mesoscopic scale. It must be noted that the border line between these dimensional scales is not uniquely determined, but it depends of the system under observation. In the following Chapters, this border line will be drawn for chalcogenides and it will demonstrated that semi-classical interpretations are valid up to at least 40 nm.

The reader might be wondering what role nanostructures could play in electronics. Let us consider phase change memories, which were introduced in the previous paragraphs. Conventional PCM rely on the deposition of thin films of chalcogenide. In this regard, the active area of the device is nanostructured (a 'mushroom'-shaped volume as shown in Figure 1.21). However, the scaling trend is leading to the shrinking of film thickness far beyond the 100 nm limit.

A novel type of memory device can be designed by shrinking the phase change material along another dimension, thus obtaining a nanowire phase change memory cell. In such a device, the phase transformation between amorphous and crystalline phases occurs in pretty much the same way as in a conventional PCM. The device geometry makes fabrication of dense arrays of thin diameter (< 100 nm) nanowires viable and convenient. In addition, it is expected (and has been recently proven) that the phase-change material properties are improved in nanostructures[44,45,46]. Namely, the required current/laser energy for switching resulted to be considerably lower than in conventional PCM, owing to: a) the superior geometrical scaling of nanowires, b) the reduction of programmable volume of the phase-change region, and c) the improved structural properties of the nanostructure. Therefore, in comparison with geometrically scaled thin films, the energy/geometry ratio favors nanostructures. It is thought that 1-dimensional nanostructures are one of the best way to address the high-current (and high power) issue of PCM. Recently, analytical model of isotropic downscaling of phase change nanowires size by a factor of 1/k (k > 1) has proven that: thermal crosstalk is lessened, speed is increased by k^2 times, and operation energy (current) is reduced by more than k^3 (k) times[46].

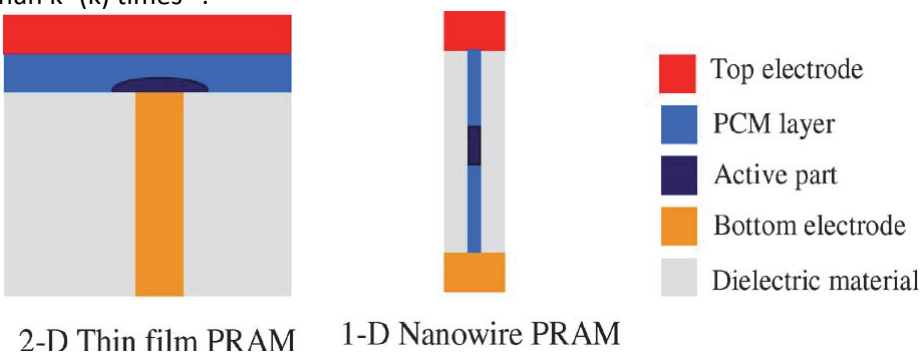

Figure 1.25 – Nanostructured phase change memory devices

The main issue in achieving nanostructured devices is fabrication. For instance, current technology is mainly based on physical vapor deposition techniques of thin films, which can deliver < 100 nm thick layers straightforwardly. On the opposite, self-assembly ('bottom-up' approach) is more convenient for producing 1- and 0-dimensional nanostructures, where the nanostructure is obtained as a result of the growth conditions and not by down-scaling (i.e. 'top-down'). Some of these techniques will be looked into in the next chapters.

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2. Phase-change and Chalcogenide materials

Phases change materials

Allotropy is when a chemical element is naturally found in different forms, which may differ in the arrangement, order, and quantity of atoms. These forms are also called phases and usually exhibit different morphological, structural, and physical properties. Allotropes may be monotropic, in which case one of the forms is the most stable under all conditions, or enantiotropic, in which case different forms are stable under different conditions and undergo reversible transitions from one to another at characteristic temperature and pressure.

These materials are commonly referred to as "phase change materials".

In this Chapter, a special focus will be put on chalcogenides, a very peculiar class of phase change materials which suitably fits into non volatile memory applications.

Chalcogenides

"The new terms were soon used in publications by other members of the Biltz group, and also by outsiders."[1]

Elements belonging to group 16 of the periodic table are called *chalcogens*, and their compounds are called *chalcogenides*. (For additional details on this nomenclature see Appendix D.) Some of the physical properties of these elements are summarized in Table 2.1. It must be noted that oxygen is not unanimously considered a chalcogen, and its compounds, oxides, are a category on their own, due to their peculiar properties.

	S	Se	Te
Atomic mass	32.07	78.96	127.60
Atomic number	16	34	52
Electronic structure	[Ne]$3s^2 3p^4$	[Ar]$3d^{10} 4s^2 4p^4$	[Kr]$4d^{10} 5s^2 5p^4$
Melting point (°C)	119 (S_β)	220.5 (gray)	449.8
Boiling point (°C)	444.6	684.8	989.8
Density (g cm^{-3})	2.06 (S_α)	4.82 (gray)	6.25
Atomic radius (10^{-10} m)	1.00	1.40	1.37
$X^{(II)}$ covalent radius (10^{-10} m)	1.03	1.16	1.37
Electronegativity (Allred–Rochow; Pauling)	2.44; 2.58	2.48; 2.55	2.01; 2.10
First ionization potential (eV)	10.38	9.75	9.01

Table 2.1 – Physical properties of S, Se, and Te

Most of S, Se, and Te compounds occur in two or more phases, both crystalline and amorphous, hence belonging to phase change materials. The amorphous-crystalline (and vice versa) transition is reversible, and is employed in non volatile memory applications through the PCM architecture discussed in the previous Chapter. Following the discovery by S. R. Ovshinsky, the phase change can be triggered by electrically-induced Joule effect[2]. In addition, two features make these materials particularly fit for implementation in NVM: a) the transition is fast enough (in the nanosecond timescale), and b) the phases present pronounced differences in the physical properties (such as resistivity, reflectivity).

Chalcogens are electronegative elements that form covalently bonded solids and are strongly associated with metal-bearing minerals. Their metallic character is increasingly marked with increasing atomic mass: sulfur is non metallic, while selenium and tellurium show semiconductor like behavior. All of these elements have negative temperature coefficient of resistivity, just like semiconductors. The oxidation states are -2 (Se), 0 (Se), +2 (all), +3 (S), +4 (all), +5 (S), and +6 (all). The maximum coordination number can be five, six or even seven. The heavier chalcogens may utilize *d* orbitals in bonding, so that there is no limitation to ligand atoms. Elemental chalcogens have the tendency to form ring-like (S and Se) and chain-like (S, Se, and Te) structures with no branches, as a consequence of the +2 valence of the element.

All chalcogens react easily with oxygen, metals, and non-metals at room temperature and higher. When heated in oxidizing atmosphere, S, Se, and Te burn to form dioxides. As a result, undesired compounds might form in presence of contaminants. Oxidation occurs in exposed surfaces of thin films and nanostructures – an undesired effect that will be looked into in the following paragraphs.

Chalcogenides occur in a huge variety of stoichiometries and structures, which exhibit substantially distinct physical properties. Moreover, both non stoichiometry and phase separation can occur and a wide literature is present on their categorization. In Table 2.2, a non exhaustive list of chalcogenides is shown.

Sulfides	Selenides	Tellurides
AsS	AsSe	GeTe
SnS	GeSe	SbTe
CdS	InSe	CdTe
ZnS	SnSe	InSbTe
AgS	CdSe	GeSbTe
	HgSe	AgInSbTe

Table 2.2 – Some popular chalcogenides

As a matter of fact, non-transition metals compounds like SbTe and AsSe are often found in chalcogen-rich phases such as Sb_2Te_3, As_2Se_3. It is also interesting to note that ternary chalcogenides such as MnY_2S_4, $CdCr_2Te_4$, show very unusual combinations of electrical, optical and magnetic properties. Concerning ternary systems of the type $A_xB_{1-x}C$ (C = S, Se, Te), these do often coexist in separate phases (A_xC + $B_{1-x}C$) and a broad variety of phase diagram combinations can be achieved, according to the thermal stability of each phase. To the scope of this work, only a limited selection of compounds will be examined.

Finally, it must be pointed out that chalcogenide glasses share several peculiar properties: bi-stability, photoconductivity, thermoelectricity, ionic conduction. The next paragraph will describe in details the most important property for application in non volatile memories: the amorphous-crystalline phase transition.

Chemistry of the phase transition

"The deepest and most interesting unsolved problem in solid state theory is probably the theory of the nature of glass and the glass transition"[3]

Properly speaking, "phase change" should be referred to as bi-stability (or quasi-stability) – the reversible, thermally-triggered transition from amorphous to crystalline phases and vice versa.

Chalcogenides are glass-formers, i.e. they turn into vitreous (amorphous) form upon cooling from a given temperature. The *International Union of Pure and Applied Chemistry* defines amorphization (vetrification) as "a second-order transition in which a supercooled melt yields, on cooling, a glassy structure"[4]. In other words, a glass is formed when a liquid is undercooled below the melting point (T_m) of the corresponding crystalline solid and then freezes at a glass transition temperature (T_g) without crystallizing. It must be noted that this process is a matter of both: 1) the quenching temperature difference ΔT, and 2) the time span Δt employed to do so.

Therefore, the critical cooling rate $\Delta T/\Delta t$ (from the melting temperature) dictates whether amorphization or crystallization occurs upon quenching, as shown in Figure 2.1 for glass transition of metallic glass Vitreloy 1.[5]

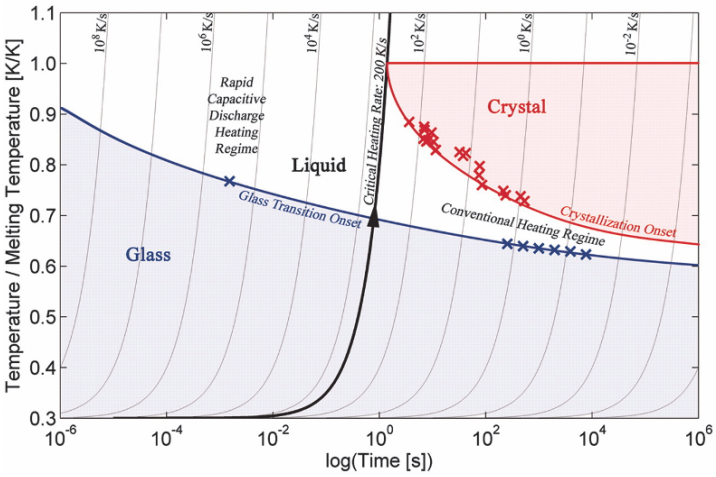

Figure 2.1 – Glass-transition onset temperature and crystallization onset temperature versus time for the metallic glass Vitreloy 1 at varying heating rates[5]

To appreciate the difficulty of avoiding crystallization while processing a liquid at intermediate undercooling, let us consider the time scale required to relax spatial temperature variations caused by heat conduction within a sample. For a typical chalcogenide, T_g/T_m ratio is ≈ 1000/500 K/K. In PCM cell with active area ≈ 1 μm^2, assuming thermal diffusivity of the chalcogenide ≈ 20 cm^2/s,[6] the diffusion time is as short as 0.5 ns. As a result, the required quenching rate has to be of the order of 10^{12} K/s,[7,8] to achieve amorphization. Such a requirement – which owes to the fast transition of the material – is very demanding and must be accounted for in the implementation in actual NVM device, as will be shown in the following paragraph.

The most notable feature of the glassy phase is the lack of any long range order and periodicity and will be examined thoroughly in a following paragraph. In addition, the glassy phase is characterized by a lack of thermodynamic equilibrium. As a result, glass is a metastable phase that, given sufficient time, shall transform into the (more stable) crystalline form.

From a chemical point of view, the glassy phase can be regarded as a higher-enthalpy state in comparison to the crystalline one. The resulting molar volume (V) and enthalpy (H) of the glass/crystal forming liquid are schematically shown in Figure 2.2 where T_x is the crystallization temperature upon heating and T_l is the liquidus temperature. Note that the glass-forming ability of a material is a measure of its metastability – that is, its hardness to crystallization in the undercooled temperature region between T_g and T_m. In this regard, chalcogenides are a robust category of glasses, having spontaneous crystallization time scales ranging from a few months to a few years at T < 100 °C. Chemical alloying is a convenient and efficient way to engineer the glass transition temperature T_g of chalcogenide glasses. For example, the pure Se glass temperature can be increased from 40 to 400 °C by alloying 33 at.% Ge.[10]

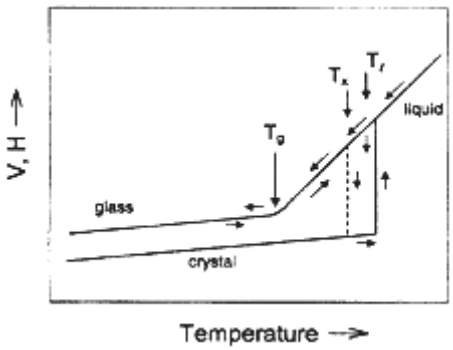

Figure 2.2 - Schematic temperature dependence of molar volume (V) and enthalpy (H) of a glass forming liquid[9]

Another characteristic temperature of a phase change materials is the crystallization temperature T_c (or T_x) – i.e. the temperature at which the amorphous to crystalline transition occurs. The T_c is a figure of merit of the stability of the amorphous phase – and its retention – to which it is roughly proportional. When several high-temperature phases are present, these will be referred to as 1st, 2nd, 3rd,… crystallization temperatures. It must be noted that the crystallization temperature T_c, is not a fixed reference (as the melting temperature is). As mentioned before, the phase transition is – from a chemical point of view – a second-order transition (just like ferromagnetic, superconductor, or superfluid transitions) and not a transition between states of matter. Therefore the value of T_c is not univocally determined but depends on how the temperature itself is reached – for instance, by the thermal budget delivered to the material.

Overview of Te compounds for PCM

In the following, the physical characteristics of binary, ternary and quaternary alloys of Te will be reviewed.

Germanium belongs to group 14 and is the most popular semiconductor for electronics, after silicon. It is chemically versatile, since it can hybridize its *s* and *p* orbitals to achieve various bonding configurations. In addition, it is the element with the smallest atomic mass and highest diffusivity among those alloyed with tellurium.

Antimony is a non metal, belongs to group 15, and is commonly found in minerals species (where it bonds with sulfur). It has similar properties as arsenic, and oxidized in compounds with the +3 or +5 states.

Indium is a true metal belonging to group 13, which oxidizes to +1 and (more often) +3 states. It is frequently used as additive in materials for semiconductor devices.

Nitrogen and carbon are used as dopant in all tellurides, by injecting the species during deposition. Because chalcogenides are, in general, very insensitive to doping effect, actual doses can be as high as 10 % at., in which case the term 'doping' is still commonly, albeit improperly, used.

These few elements form a broad variety of Te compounds.

Germanium telluride is a solid whose semiconducting properties were discovered in the 1950s by the soviet scientist Kolomiets[11,12,13]. In the same years, Ovshinsky investigated the electrically triggered phase change of similar compounds (XAs, XTe, XAsTe, X belonging to group III, IV, or VI)[14,15]. Phase diagram indicate an eutectic at the stoichiometric $Ge_{0.5}Te_{0.5}$, as shown in the following Figure 2.3.[16]

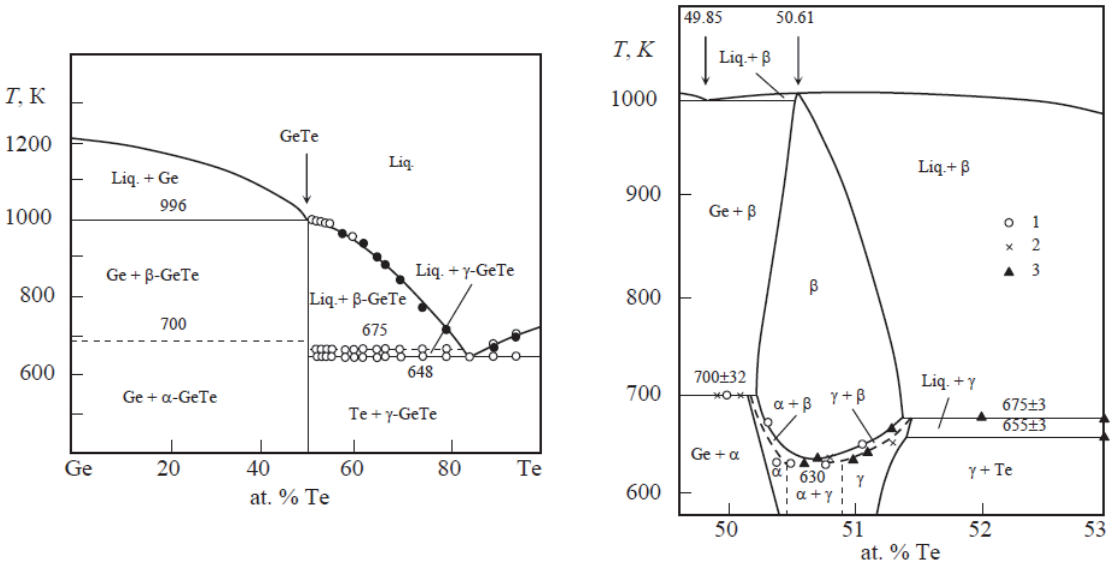

Figure 2.3 – Left: phase diagram of the system Ge-Te[17]. Right: detail of the homogeneity domain of GeTe[18,19] by: 1.dilatometry, 2. electro-physical measurements, 3. dihedral transition analysis

Germanium telluride exists in one amorphous and three major crystalline forms, room-temperature α (rhombohedral) and γ (orthorhombic) structures and high-temperature β (cubic, rocksalt-type) phase. The latter phase shows up above 400 °C, and consists of two fcc sublattices shifted by half the lattice parameter in each direction with respect to each other; one sublattice is occupied by Te atoms, the other one by Ge atoms. At lower temperature, a rock-salt phase is also found (Figure 2.4), as a so called metastable phase after annealing amorphous GeTe thin films at ≈ 180 °C. In fact, in the crucial phase transition employed in phase-change data storage, the material switches between the amorphous and the metastable rock-salt (Figure 2.5, a) structure. However, in the ground state at lower temperatures, GeTe adopts a trigonal phase, which can be thought of as a slightly distorted rock-salt structure (shown in Figure 2.5, b). The first crystallization temperature for GeTe is high (185 °C) and accounts for a very good retention of the amorphous phase. Second crystallization occurs at a much higher temperature (≈ 350 °C) toward the rock-salt phase. Besides, crystallization speed is one of the highest among tellurides (≈ ns). Unfortunately, these advantages are lost when stoichiometry changes – even slightly – from $Ge_{0.5}Te_{0.5}$. Therefore, actual implementation of this alloy requires perfect deposition control and is not very robust from this point of view. In this regard, the addition of a dopant (Sb, In, Si, N, C) in GeTe has beneficial effects as it improves the robustness of the alloy. Finally, it must be noted that stoichiometric GeTe presents no structural vacancies in its crystalline phases, contrarily to antimony telluride and ternary tellurides.

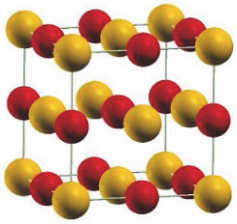

Figure 2.4 - Rock-salt structure of GeTe

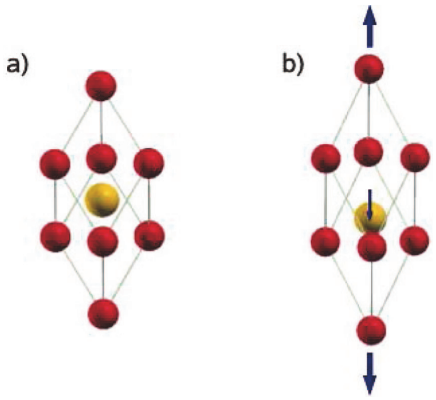

Figure 2.5 – Rock-salt (a) and trigonal (b) structure of GeTe in the primitive unit cell. The latter is obtained by stretching the rocksalt cell along the (111) direction and shifting the central atom[21]

Antimony telluride is found in a variety of continuously soluble stoichiometries. The most stable phase, which corresponds to the eutectic point (and the lowest enthalpy of mixing), is at 60 %at. Te concentration, with a melting point of 617.7 °C. Phase diagram for the Sb-Te system is shown in the following Figure 2.6.

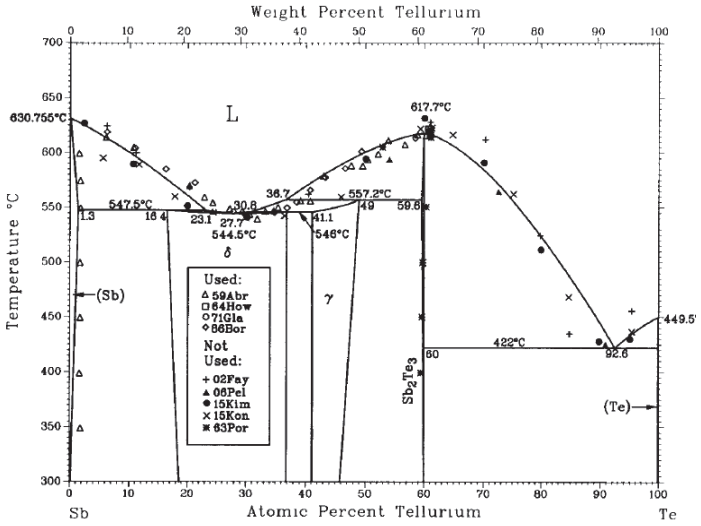

Figure 2.6 – Phase diagram for the Sb-Te system[20]

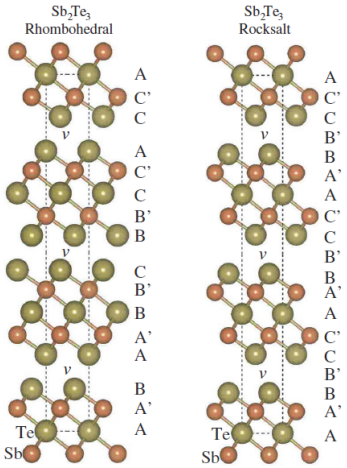

Figure 2.7 – Plane stacking in antimony telluride crystal phases[21]

Sb_2Te_3 occurs in the amorphous and in two crystalline phases – rhombohedral and rocksalt. The atoms stacking in the ordered structures are shown in Figure 2.7. Unfortunately, implementation of Sb_2Te_3 in PCM devices is undermined by its low first crystallization temperature (110 °C), which results in poor stability of the amorphous phase and, as a consequence, poor data retention. For this reason, antimony is almost always associated with other elements when alloyed with tellurium; Ge, In, or Si, are employed as dopant so as to improve retention by inhibiting crystallization. As a final point, crystalline antimony telluride possesses structural vacancies in the Sb sublattice as GeSbTe compounds do, which is a consequence of the valence of the Sb (V) and Te (VI) atoms and the electron octet counting rule[21].

Indium telluride alloys in the stable form In_2Te_3, a semimetallic compound with a 1.1 eV band gap. Its applications are mainly in IR detectors, thermoelectric generator, gas sensors, strain gauges and solar cells[22]. It crystallizes in zinc blend structures with ⅓ of structurally vacant indium sites, exhibits negative temperature coefficient, and has very high electrical resistivity at room temperature. Despite In_2Te_3 being of little interest for phase change memory application, indium is used as a dopant in ternary and quaternary alloys of Te in addition to, or as a replacement for Ge, Sb, Si, C, and N. In this regard, it is beneficial in improving the stability and resistivity of the amorphous phase of Te alloys.

Ternary compounds of tellurium belonging to the pseudobinary line between GeTe and Sb_2Te_3 gained popularity after the discovery of fast switching by Yamada[23]. These ternary alloys are formed owing to the mutual solid solubility of the above mentioned binary compounds at any composition. As a result, their stoichiometry is given by the formula

$$(GeTe)_m + (Sb_2Te_3)_n = Ge_mSb_{2n}Te_{m+2n} \quad (2.1)$$

and their position in the Gibbs map is shown in Figure 2.8.

These compounds are of considerable technological interest since their physical properties are well fitted to PCM application, and vary continuously in the whole range through variations in composition. Let us consider, for instance, the crystallization temperature T_c: as shown in Figure 2.9, T_c varies continuously and monotonically as a function of stoichiometry. In this respect, both crystallization temperatures increase monotonically. Note that the Ge:Sb:Te composition 2:2:5 is highly regarded as a good tradeoff between crystallization speed and retention.

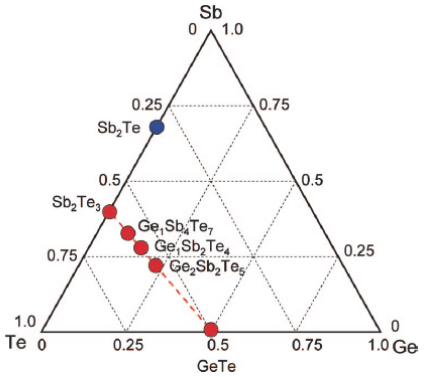

Figure 2.8 – Stoichiometries of interest along the pseudobinary line[24]

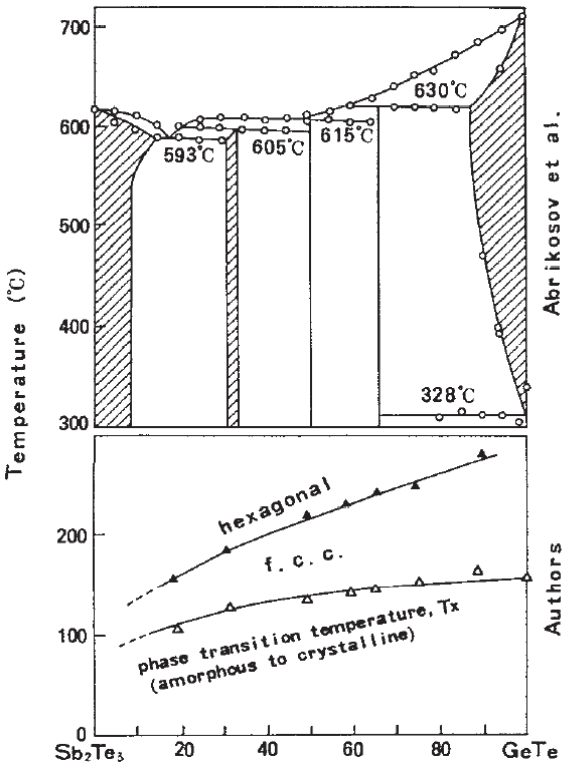

Figure 2.9 – Phase diagram[25] (top), and phase transition temperatures (bottom) of GeTe-Sb_2Te_3 pseudobinary amorphous alloy films[26]

Structural data on ternary tellurides have been known since the 1970s. In this regard, the plane stacking of the GeSbTe crystals varies greatly with stoichiometry, with most of compounds exhibiting two type of crystalline phases: 1) a metastable phase with NaCl-type simple structures appearing over a wide composition range of GeTe from 100 mol.% to at least 33.3 mol.%, and 2) a wide variety of stable phases crystallizing into complicated structures with cubic close-packing periodicity belonging to the $(GeTe)_n+(Sb_2Te_3)_m$ homologous series[27]. All the ternary systems so obtained belong to Type I: the binary constituents both have the same crystal structure as their stable form in the given temperature range; in addition, a single Bravais lattice of this structure is formed at all alloy compositions for which solid solubility exists. All of the ternary alloys under investigation in this work present a NaCl-type metastable phase (of the face-centered cubic type, in the following: *fcc*) and a stable phase (hexagonal close packed: *hcp*). The following Figure 2.10 and Figure 2.11 display the crystallographic stacking for three important stable ternary compounds along the pseudobinary line: $Ge_2Sb_2Te_5$, $Ge_1Sb_2Te_4$, $Ge_1Sb_4Te_7$.[28]

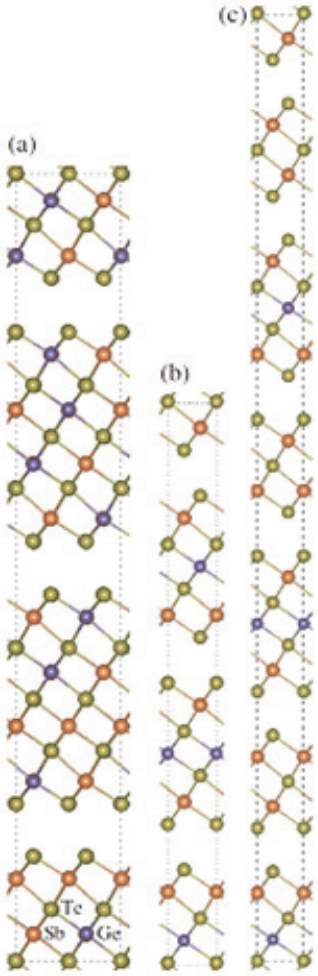

Figure 2.10 - Atomic structure of the GST compounds in the metastable fcc crystalline phase for the $Ge_2Sb_2Te_5$ (a), $Ge_1Sb_2Te_4$ (b), and $Ge_1Sb_4Te_7$ (c) compositions, employing a conventional hexagonal unit cell representation (dashed lines)[28]

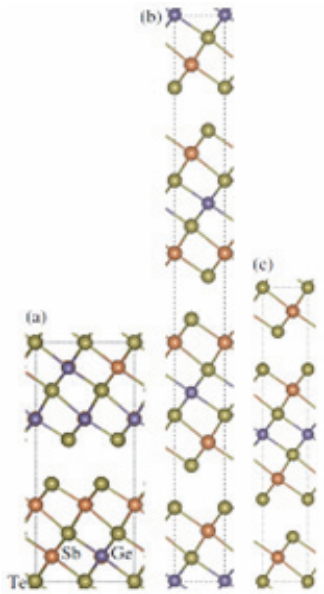

Figure 2.11 - Atomic structure of the GST compounds in the stable hcp crystalline phase for the $Ge_2Sb_2Te_5$ (a), $GeSb_2Te_4$ (b), and $GeSb_4Te_7$ (c) compositions, and employing a hexagonal unit cell representation (dashed lines)[28]

It is worth noting a few peculiarities in the atomic arrangement of the crystalline phases. In the distorted rocksalt-like structure of $Ge_2Sb_2Te_5$, Te atoms occupy 4(a) site while Ge, Sb occupy ≈ 80 % of 4(b) sites; and vacancies occupy ≈ 20% of 4(b) sites. In $Ge_1Sb_2Te_4$, vacancies occupy as much as 25% of the sites of the Ge/Sb sublattice. Such a vacancy concentration is surprisingly high for these structures. This experimental finding has been explained in terms of energy lowering upon formation of the vacancy[29] which, in turn, is a consequence of the high electron density in the lattice.

Quaternary compounds of Te (such as AgInSbTe, InGeSbTe) have been designed to achieve specific features. As a matter of fact, metallic elements (such as Ag, In) are added to the alloy for several reasons as: prevent crystallization, increase resistivity, increase reflectivity, widen the programming window, and/or improve retention. The most significant example of quaternary compound is employed in rewritable DVDs, which comprises silver, in various compositional ranges. In this case, the addition of Ag alters the crystallization dynamics, so as to make growth of crystal seeds, rather than nucleation of new crystallites, the dominant mechanism. Doing so is convenient for optical rewritable disks, where crystallization is optically induced at once over the entire device.

Oxidation in tellurides

Oxidation is especially critical for all GeTe and GeSbTe compounds, regardless of composition. The electronegativity of Ge, Sb, and Te, according to the Pauling scale, is 2.01, 2.05, and 2.1, respectively[30]. Ge has the highest oxygen affinity and is thus preferentially oxidized. As a result, a thin layer of GeO_2 is spontaneously and rapidly formed on every surface of thin chalcogenide films and nanostructures exposed to oxidizing agents. This phenomenon occurs in air at room temperature, and more markedly at higher temperature. For thin chalcogenide films, oxide thickness has been documented to be as much as 20 nm (out of 100 nm $Ge_2Sb_2Te_5$) by means of XRD and secondary ion mass spectroscopy[31]. Nanowires are more affected by oxidation of the lateral surface area, due to the smaller volume/surface ratio; as a result, even small traces of O_2 can, in the long run, deteriorate the wire.

It has been proven that the oxidized surfaces have a detrimental effect on electrical current transport and are therefore undesirable, regardless of the oxide[32]. Besides, this phenomenon also causes the remaining part of the chalcogenide to get depleted in germanium[33]: the stoichiometry should therefore be corrected to account for the capture of Ge atoms. (Note, however, that tellurium sublimes rapidly at high temperatures, thus depriving the material from Te, as well.) In addition, it is not unusual to find Sb oxides (in the form Sb_2O_5), or the other Ge oxide (in the form GeO_4), or the tellurite (in the form TeO_2); whereas the monoxide GeO is unstable. It is still debated whether the oxidation of thin film (nanowire) is a self-limiting process or it carries on throughout the thin film thickness (nanowire diameter).

Oxidation is an issue in phase change memory devices, which originally featured SiO_2 as insulating layer. In these prototypes, oxygen migration from the neighboring layer towards the chalcogenide material was triggered by the heating/quenching operation of the device, eventually leading to the failure thereof. Alternative capping layers should feature carbon, TiAlN[34], or other materials.

In the measurements shown in the following Chapters, sample oxidation has been prevented whenever possible, or otherwise taken into account.

Electronic properties

As a consequence of the structural vacancies in the Ge (or Ge/Sb) sublattice, most Te compounds exhibit p-type conduction, regardless of composition. Their electronic properties have been modeled by Joint Density of States (JDOS): it has been found that $Ge_2Sb_2Te_5$ is semiconducting and robust with respect to stoichiometry changes[35]. Moreover, Ge/Sb deficiency (excess) causes an increase in holes (electrons) concentration in the valence (conduction) band respectively, without affecting the bandgap width and thus preserving a semiconductor-like behavior.

Tellurides are a peculiar class of semiconductors when it comes to their bonding configuration: contrary to Si, Ge, or III-V alloys which exhibit strong sp^3-hybridization, hybridization is not found in materials such as GeTe or $Ge_1Sb_2Te_4$, due to the large energy separation between the *s* and the *p* orbitals. As a result, only *p* orbitals are involved in chemical bonding in chalcogenides[36].

Electronic band structure of GeTe has been found to have a band gap of 0.1-0.15 eV in the rock-salt phase[37,38]. However, this band gap widens in the distorted structure, resulting in a gap of 0.73-0.95 eV[39] for the trigonal phase.

The electronic band structure of ternary crystalline GeSbTe depends on stoichiometry and phase, and can be simplified as a band-gap with localized energy levels in between (Figure 2.12). In the crystal phases, the Fermi level is approximately located closely to, or inside of the valence band. This corresponds to semiconductor-like and metallic behavior respectively, as will be shown in the following Chapter 5. In the amorphous phase, no band gap can be defined; rather, a high density of localized states is present within the mobility gap, with the Fermi level calculated to be approximately pinned at the center thereof ($Ge_2Sb_2Te_5$ at T=0 K)[35]. In this regard, electronic transport mechanisms in the amorphous phase (among which: Poole, Poole-Frenkel, polaronic, variable range hopping) are still being debated.

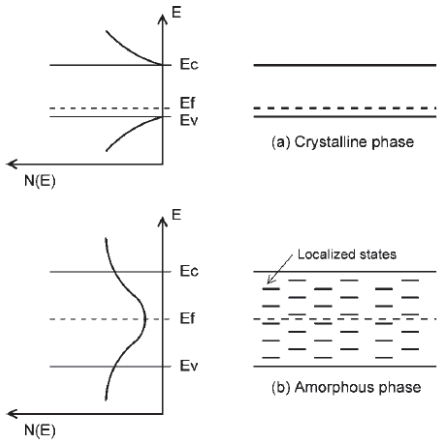

Figure 2.12 – Band structure of ternary chalcogenides[40]

Phase change at the atomic scale

Several models have been suggested to shed light on the ordered-disordered phase transition at the atomic scale, but a definitive explanation is still missing. So far, no theory has been able to account for the speed (on the picoseconds timescale) of the structural transition. Research is being carried out on two routes. On one hand, density functional theory (DFT) is used for modeling and understanding the relationship between structure and bonding. On the other hand, experimental investigations are employed to probe the arrangement of atoms, according to the chemical bonding information. To this end, Extended X-ray Absorption Fine Structure (EXAFS), X-ray Absorption Near-Edge Structure (XANES), and Raman Spectroscopy (RS) are being employed to determine the average coordination number, the bond lengths, the chemical nature of the neighboring species, as well as the bond length disorder parameter.

The "umbrella-flip" model, proposed in 2004 by Kolobov[41], attempted to explain the phase transition on the basis of the breaking of weaker Ge-Te bonds and subsequent shift of germanium atoms from the octahedrally- to the tetrahedrally-coordinated sites, as shown schematically in Figure 2.13. However, recent experimental evidences (by EXAFS[42] and reverse Monte-Carlo methods[43]) seem to indicate that the octahedral/tetrahedral site ratio is basically unchanged from amorphous to crystalline structure, thus overthrowing this model.

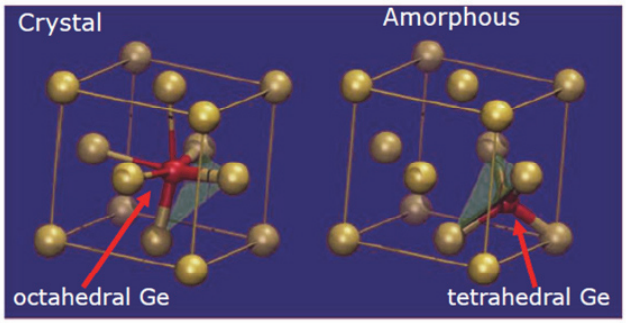

Figure 2.13 – Local structure of GST around Ge atoms in the crystalline (left) and amorphous (right) states according to Kolobov's model[41]

Some Authors support the theory of resonance bonding (a configuration when electron delocalization lowers the potential energy of the molecule thus making it more stable). In this picture, the amorphous phase structure is dictated only by ordinary covalent bonding, while the crystal lattice is dominated by resonance bonding which would account for the material's high electronic

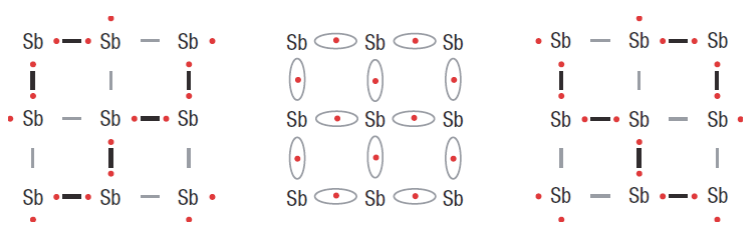

Figure 2.14 – Resonance bonding in crystalline Sb[44]

polarizability, small band gap, lattice distortions, high effective charges, soft modes[44]. This theory is schematically shown for an elemental Sb crystal in Figure 2.14. On the left and right sides of the picture, two compatible, limiting cases for bonding in an undistorted Sb phase are shown. The solid can minimize its energy by forming a hybrid wave function, i.e. by resonance bonding, as shown in the middle picture. The pronounced electron delocalization gives rise to an increased electronic polarizability. In addition, the presence of distortions might explain why the optical contrast between the phases is more marked in phase change tellurides than in conventional covalent solids.

Most recently, other investigators have employed Fast Fourier transform (FFT) of high-resolution transmission electron microscopy (HR-TEM) image to calculate the total radial distribution function of the structure, and have concluded that the fcc-GST contains both octahedrally- and tetrahedrally-bonded cations (Ge)[45]. In light on these findings, these Authors have stated that "upon amorphization or crystallization, the basic near-neighbor structural motifs of the octahedral and tetrahedral Ge atoms remain largely intact; i.e., ≈30% Ge are in the tetrahedral locations and the rest in the octahedral environments (similar proportions are known for the local structures in the amorphous phase)". In this respect, it is the substantial similarity of the Ge near-neighbor structure between cubic and amorphous phase that might account for the fast switching mechanism.

Ab initio calculation have shed further light on the fast switching mechanism. It has been found that crystal-nuclei seeds (fragments of octahedral rocksalt structure, e.g. 4-rings) are already present in both the melt and the amorphous states[46]. Therefore, minimal atomic diffusion is required for crystal nucleation and growth. Evidence of the coexistence of tetrahedrally- and octahedrally-coordinated Ge (33 and 66 %, respectively) in the lattice of the amorphous phase has been brought[47]. Moreover, the high density of vacancies in the crystalline phase is thought to play a role in the phase transformation although, as some have stated, "currently only very little is known about vacancies in Te alloys"[29].

Additional research on this topic includes calculation of surface/bulk energy balance[48], interpretation in terms of Mott-Anderson transition[49], effect of voids in non-stoichiometric compounds[50], and much more.

Finally, it must be noted that the phase transition can be triggered not only by delivering thermal energy, but also by providing a compressive/tensile stress. Recent investigation, carried out by *ab initio* molecular dynamics, showed that ternary compounds subject to pressure as high as 30 GPa can achieve amorphization from the cubic crystalline phase[51]. At higher pressure, amorphization occurs since the amorphous phase is denser that the crystal (because it lacks the vacancies of the crystal phase).

Features of the amorphous chalcogenides

The most evident peculiarity of an amorphous solid is the lack of long-range order and periodicity, hence neither the unit cell, nor the position of atoms/molecules thereof can be defined *a priori*.

Notably, most experimental techniques have been developed for investigating ordered, periodic solids. In this regard, it can be mentioned: Bragg's law of scattering (upon which X-ray diffraction is based), the band structure model for electric conduction (upon which the Hall effect is based), Ewald's sphere construct (upon which RHEED spectroscopy is based).

On the opposite, in the amorphous solid, the lack of long range order hinders any chance of unveiling the exact position and arrangement of atoms and molecules. The only tools available for investigating such materials are those which probe the global, average, statistical properties such as: mean coordination number, bond length, bond strength, correlation function, electronic density. Even though no long range order is present, each atom in the alloy has to obey the chemical laws that dictate the bond formation with neighboring atoms. For instance, the both the crystalline amorphous elemental solids of S, Se, and Te, arrange in long intertwined chains/rings (up to 10^4 atoms long) as a consequence of the spontaneous

tendency to catenation (each atom having only 2 covalent bonds available). However, the amorphous character shows up in the unpredictable variety of geometries and angles formed by the chains and rings that shape a globally disordered solid (even though a chemically dictated short-range order is still present), as shown in Figure 2.15.

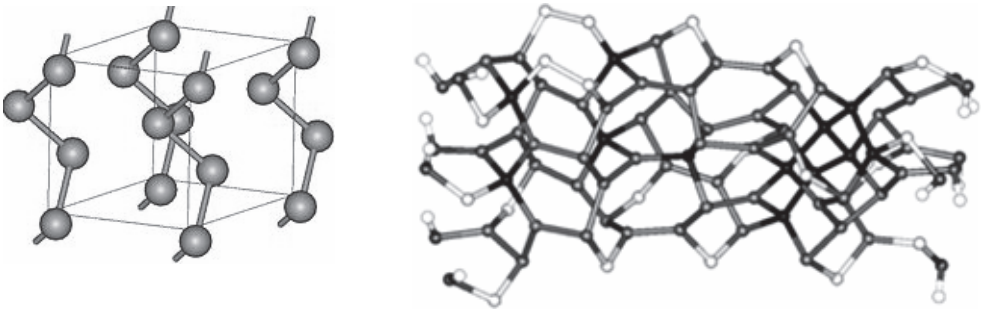

Figure 2.15 – While crystalline (trigonal) elemental Se arranges in chain-like structures (left)[52], amorphous Se displays a mixture of chain-like and ring-like structures, featuring various bond lengths and angles (right)[53]

Complex alloys of chalcogens do amorphize in complex forms, in which the atoms arrangement is not straightforwardly evident. From the theoretical point of view, several models have been proposed to describe amorphous solids. The simplest model is the Dense Random Packing (DRP), applicable to metallic glasses. In this model, atoms are represented as 3-dimensional spherical solids; no assumption is made concerning the bonding type between them, so that it is assumed that they pack as close as possible and (if two or more elements are present) in any possible position relative to one another. For this reason, this theory is valid only for solids made of elements that form weak metallic bonds.

The Continuous Random Network (CRN) model is particularly fit for covalently bonded glasses like amorphous silicon, oxides, chalcogenides. In this model, one additional assumption is made with respect to DRP: the elements that form the solid must obey near-neighbor bonding rules concerning the number and type of bond, but regardless of bond strength (length) and angle. The resulting structure looks like a continuous network because the species are bonded according to the chemical rules, and the additional degrees of freedom make it possible for the elements to arrange in twists, rings and chains. As a result, a short range order is present around just each atom closest neighbors, not any further away. CRN structures were modeled by Zachariasen[54] and an example of these structures is shown in Figure 2.16. In chalcogenide alloys, the doping species (Ge, Sb, In, C, and N) alter the overall structure. For example, while elemental S forms chained, intertwined amorphous solids, the addition of small amounts of arsenic atoms causes the sulfur chains to branch (each As atom bonds to three other S atoms).

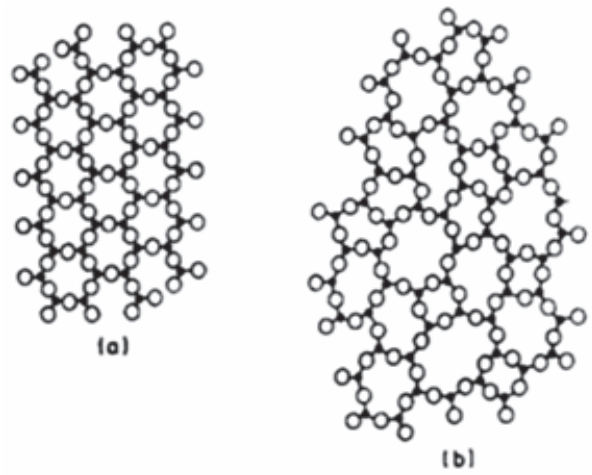

Figure 2.16 – 2-D structure of crystalline (a) and amorphous (b) generic V-VI compound (i.e.: AsSe)[54]

The electronic band structure in amorphous solids is more complex than in their crystalline counterparts. In a (theoretically infinite) crystal, the atomic bonding configurations give rise to the discretization of the electron bonding energy levels, i.e. the well known allowed and forbidden energy bands. On the contrary, the lack of long-range order prevents the electrons from forming a continuous band of allowed bonding energies. Nevertheless, as the near-neighbor bonding configuration is solely dictated by the chemistry of the elements, most of atoms exhibit the same electron energy arrangement of orbitals as in a crystal, and therefore

the energy dispersion (k-dispersion) is similar to that of a crystal. From the energetic point of view, the most notable difference is the presence of localized, discrete energy levels within the energy gap formerly known as bandgap. Such localized energy levels arise owing to the occurrence of defective, missing, or dangling bonds. The energy bandgap in amorphous solids is referred to as "mobility gap" because these localized states lay energetically very close to the Fermi level, are partially filled by charge carriers and play a role in electric conduction (not by drift/diffusion, but by variable-range-hopping mechanisms among these traps[55]). The mobility gap breadth is comparable to that of its crystalline counterpart; for example, $Ge_2Sb_2Te_5$ has a bandgap of ≈ 0.6 eV.[46]

Another feature of the amorphous phase is its lower density with respect to the crystalline phases (as the latter belong to the fcc or hcp lattice, feature the highest packing density). The density change upon crystallization has been estimated to be around 6% and 8% for the amorphous to fcc and amorphous to hcp transition of $Ge_2Sb_2Te_5$ respectively[56].

As mentioned previously, the amorphous (glassy) solid is characterized by an excess of enthalpy. When kept at T<Tg, it will loose its excess of enthalpy by molecular relaxation to reach more favourable thermodynamic states, i.e. by crystallizing[57].

Another consequence of the chemically-dictated atom arrangement, is that the coordination number follows the 8-N rule in amorphous, but not in crystalline chalcogenides. In the former, the dominant bonding is covalent, with strictly 2 bonds for Te, 4 for Ge, 3 for As, and so forth. In the latter, however, experiments and model indicate an over-coordination of elements (i.e., the bonding configuration tends toward a more marked ionicity). These differences are briefly summarized in the following Table 2.3.

	Amorphous	Crystalline
	sp^3- and p-bonded systems like Si and GeTe	p-bonded phase-change materials like $Ge_2Sb_2Te_5$ (sp^3-bonded systems)
Bonding	covalent	resonant (covalent)
Short-range order	8-N rule	higher co-ordination number (8-N rule)
Thermal conductivity	low	low (high)
Optical reflectivity	–	high contrast (small contrast)

Table 2.3 – Amorphous vs. crystalline chalcogenides[58]

A model arrangement of the amorphous phase for these chalcogenides is thought to look like in the following Figure 2.17, where the occurrence of 4-fold rings should be noted.

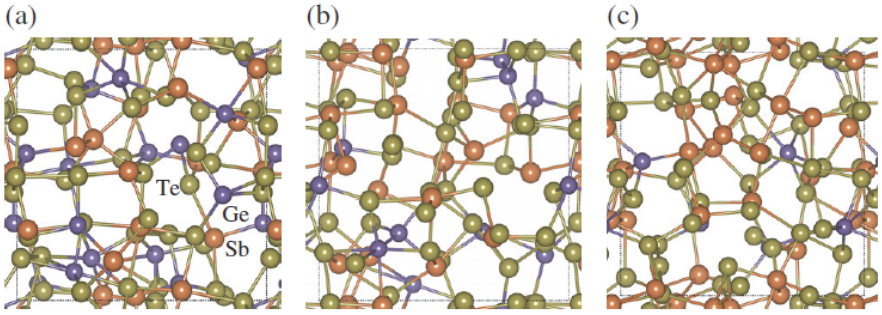

Figure 2.17 - Amorphous phase structure for $Ge_2Sb_2Te_5$ (a), $GeSb_2Te_4$ (b), and $GeSb_4Te_7$ (c)[28]

In addition, recent experimental findings suggest the existence of several amorphous phases. In particular, the amorphous chalcogenide "as deposited" by sputtering differs from that obtained by amorphization from the crystalline phase.

Classical crystal kinetic interpretation

Despite lacking a throughout explanation of the amorphous to crystalline transition, classical crystal kinetic is widely employed in device design owing to its simplicity, accuracy and low

computational power requirements. Historically, physical models (that require no knowledge of the underlying atomic/molecular mechanism) have been derived to describe crystallization[59]. In these models, reaction is assumed to be triggered by either or both growth/nucleation, as schematically depicted in Figure 2.18.[60]

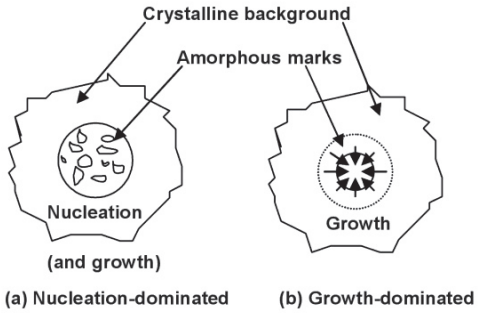

Figure 2.18 – Principles of crystallization in phase change materials[60]

The kinetics parameters can be extracted by isothermal or constant heating rate experiments (CHR), which add to the simplicity of this technique. Let us assume that the transformation rate during the reaction (amorphous to crystalline) is the product of two functions, depending solely on temperature and the fraction transformed α[61], respectively. Then the evolution of the reaction is described by the differential equation:

$$\frac{d\alpha}{dt} = f(\alpha)k(T) \tag{2.2}$$

where it is assumed that the temperature-dependent function has an Arrhenius-type behavior:

$$k = k_0 \, \mathrm{e}^{\left(-\frac{E}{RT}\right)} \tag{2.3}$$

and *E* is the effective activation energy. The main advantage of this technique is that the function *f(α)* (a very complex, reaction-specific function that relates the transformation rate to the transformed ratio) does not need to be known in the so-called Kissinger model-free methods[62]. By using heating (isothermal or CHR) experiments, equation 2.2 can be integrated by parts and becomes:

$$\ln t_f = \frac{E}{RT_i} + c \tag{2.4}$$

where t_f is the time needed to reach a certain fraction transformed at temperature T_i, *c* is a constant, and the activation energy *E* can be determined by the slope of the plot of *ln* t_f vs. 1/*T*.

Using this technique, chalcogenide materials have been classified in two categories, according to the crystallization mechanism: growth or nucleation dominated. A non-exhaustive list of crystallization mechanisms for some chalcogenides is shown in the following Table 2.19. Note that in most applications where the chalcogenide material is deposited in thin layers, the actual crystal growth follows a two-dimensional propagation because of geometrical constraints; the crystals so formed exhibit preferential alignment with the *c* axis (i.e., perpendicular to the film).

Alloy	Mechanism
Ge_1Te_1	growth
$Ge_{12}Sb_{88}$	growth
$Ge_2Sb_2Te_5$	nucleation
$Ge_4Sb_1Te_5$	nucleation
AgInSbTe	growth

Table 2.19 – Growth vs. nucleation mechanism for some chalcogenides[63]

Open debates

Despite having been investigated for more that 50 years[64], full understanding of chalcogenides still poses considerable challenges. A non exhaustive list of open debates includes:

- Experimental evidence of negative hall coefficient sign in amorphous $Ge_2Sb_2Te_5$, despite *p*-type conduction[65]
- Negative Seebeck coefficient[66]
- Coexistence of Poole / Poole-Frenkel conduction depending on: deposition, annealing, and process[67,68]
- Evidence of polaronic conduction[69]

In the next Chapter, the characterization techniques employed in this work will be described.

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3. Experimental

Growth tool: the MOCVD

Deposition techniques can be roughly divided in two categories. Physical vapor deposition (PVD) is based solely on the condensation of elemental/molecular components on the surface of the material, while in chemical vapor deposition (CVD), the growth arrangement is dictated by the chemical bonding of the depositing elements. PVD techniques include: sputtering, e-beam deposition, evaporation of powders, pulsed laser deposition, molecular beam epitaxy; while CVD techniques include: atomic layer deposition (ALD), MetalOrganic-CVD (MOCVD), hot-wire liquid injection CVD (HW-LI), plasma-assisted CVD, vapor phase epitaxy (VPE). Advantages and disadvantages are summarized in the following Table.

Feature	PVD	CVD
Purity	medium	high
Growth rate	high	medium
Step coverage	poor	excellent
Hazard	low	medium
Complexity, cost	low	medium

Table 3.1 – Comparison of growth techniques[1]

The main advantage of CVD over PVD is the low defect density of the as-grown sample: since the bonding of atoms to one another is driven by the chemistry of the species, incorporation of external species is not favored. This feature is especially convenient when growing

nanostructures. CVD delivers a good step coverage and conformality in the deposition of thin films, which is crucial for filling high aspect ratio trenches, required in integrated circuit processing. The main drawback of the chemical vapor deposition is the increased complexity: while PVD only requires the availability of high-purity elements ('target' or powders), CVD may employ complex molecular 'precursors'. Besides, the growth rate, performance, and yield of the deposition are dependent on the choice of the precursors and a large amount of research and development is required to evaluate the viability thereof.

MOCVD (also known as Metalorganic vapor phase epitaxy, MOVPE, or organometallic vapor phase epitaxy, OMVPE, when epitaxial structures are obtained) differs from conventional CVD in the usage of precursors that contain metals and organic ligands (C, H). Ultra-pure precursors (as far as 99.9999% purity) shall be utilized to preserve the final purity of the grown film/structure. Notably, MOCVD reactors are viable for large scale deposition at industrial level, where the so called showerheads deposition chamber can process up to fifty-eight 2'' or three 12'' diameter wafers at a time[2].

The process involves the heating of precursors up to a given temperature and at a given vacuum pressure when they are inside a proper container (bubbler), into which the carrier gas (typically hydrogen or nitrogen) is compelled to flow, thus becoming saturated with the precursor vapors. The bubbler temperature, internal pressure, and gas mass flow ultimately set the concentration and amount of precursor that volatilizes to take part in the reaction. The mixture of carrier gas and precursor vapors is used to transport the reactants from the bubbler to the deposition chamber, controlling the molar flow of each precursor with a precision of the order of μmol/min. Parameters vary from precursor to precursor and do not depend on the final element to be deposited.

Upon approaching the surface of the sample, the precursor dissociates into: 1) the element to be deposited, and 2) one or more additional molecules, typically hydrocarbons, as byproduct of the reaction. For the dissociation to be activated, energy has to be supplied to the molecule in the form of: heat, a plasma, or chemical. The deposition occurs when the partial pressures of the species to be deposited inside the reaction chamber reach a thermodynamic supersaturation condition with respect to the temperature and pressure: the system is therefore induced to restore equilibrium by lowering the concentration of the species in the vapor phase, namely realizing the vapor → solid transition. In the usual working conditions (normally controlled by mass transport or kinetics) the higher the growth temperature, the higher the deposition (i.e. dissociation) rate; for this reason, the substrate has to be heated during growth. Plasma is a natural enhancer of reactions (also employed in some sputtering techniques). Chemical activation employs other chemical species in the reaction as molecular hydrogen, or ammonia, in the growth ambient, leading to improved growth rate and conformality. The principle of the deposition process is sketched in the following Figure 3.1.

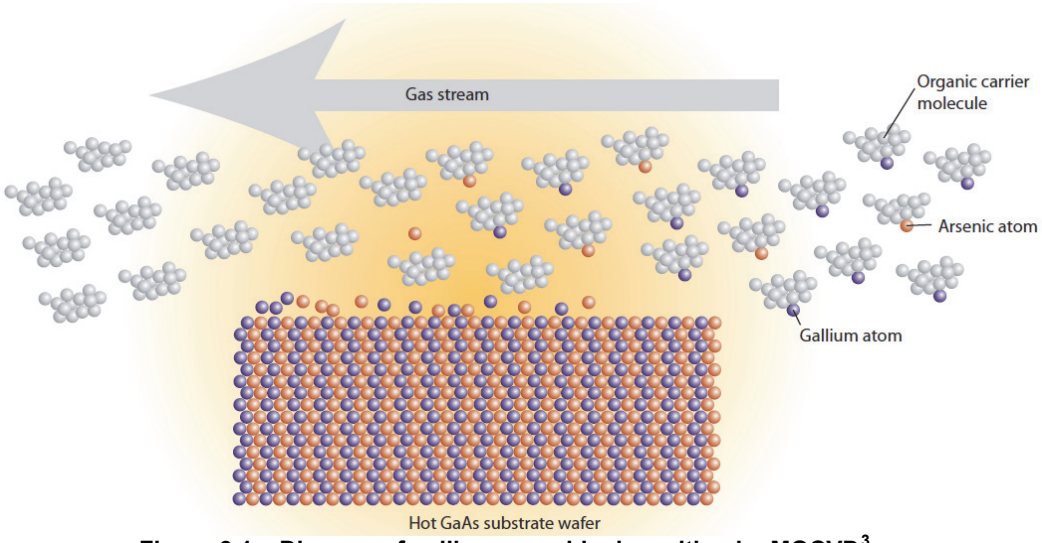
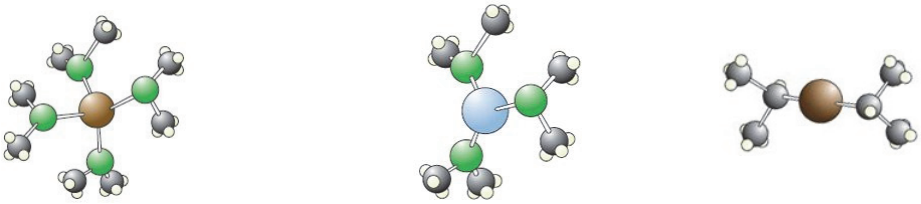


Figure 3.1 – Diagram of gallium arsenide deposition by MOCVD[3]

A thermal MOCVD AIX 200/4 reactor at Laboratorio MDM of CNR-IMM, Agrate Brianza (Italy) has been employed for the growth of nanowires. Manufactured by AIXTRON SE (Germany), within the framework of European Project CHEMAPH[4], it features: up to four precursor lines plus two lines for dopants; infrared-lamps heated growth chamber; 4 ” wafer substrate holder with rotating disk (to enhance uniformity); nitrogen gas glove box; and vacuum pumping system. The whole deposition process is computer-controlled and the valve system allows to perform also ALD-like depositions (where precursors are delivered one at a time, instead of together). This reactor has been employed to prepare samples of both thin films and nanowires of chalcogenides.

Figure 3.2 – The MOCVD reactor and growth chamber (inset) at Laboratorio MDM

In this reactor the carrier and process gas is nitrogen instead of hydrogen. It must be noted that the use of N_2 brings the advantage of a simpler, safer operating conditions than in reactors where H_2, hydrides, or ammonia are used. However, as N_2 is inert at the growth temperature employed, the activation rate of the deposition is remarkably lower than normal. The N_2 purity requirements are: concentration below 0.1 ppb for H_2O and below 0.5 ppb for O_2. Electronic grade Tetrakisdimethylaminogermanium ([N(CH3)2]4Ge, TDMAGe), Trisdimethylaminoantimony ([N(CH3)2]3Sb, TDMASb) and Diisopropyltelluride ((C3H7)3Te, DiPTe) were used as Ge, Sb, and Te precursors (see Figure 3.3), respectively, due to their comparable vapor pressures.



TETRAKISDIMETHYLAMINOGERMANIUM $[N(CH_3)_2]_4Ge$ | TRISDIMETHYLAMINOANTIMONY $[N(CH_3)_2]_3Sb$ | DIISOPROPYLTELLURIDE $(C_3H_7)_2Te$

Figure 3.3 – Precursors employed in MOCVD deposition

Nanowires self assembly

As mentioned in Chapter 1, novel devices for memory application might employ 1-dimensional nanostructures, which offer several advantages with respect to conventional thin film based devices.

The Vapor-Liquid-Solid (VLS) technique, developed by Wagner and Ellis[5] in 1964, is by far the simplest, most widely, and highest yielding process for the self-assembly of nanoscaled wires. Its main feature is the use of noble metal particles to catalyze the self-assembly growth reaction during the deposition process. It is compatible with most vapor deposition techniques. First, nanoparticles of catalyst are deposited onto the substrate (gold, platinum, palladium, and other alloys are suitable, according to the specific reaction). The substrate is then loaded into the growth chamber and heated up to a suitable temperature, so that the vapor-phase precursors mix with the nanoparticle to form a liquid eutectic mixture, according to the phase diagram of the considered system. As an example of the gold-catalyzed growth of chalcogenide nanowires, the phase diagram of the Au-Ge-Te system (shown in the following Figure 3.4), indicates the eutectic temperature at 480 °C, for the given concentration of ≈ 45 at.% Au.

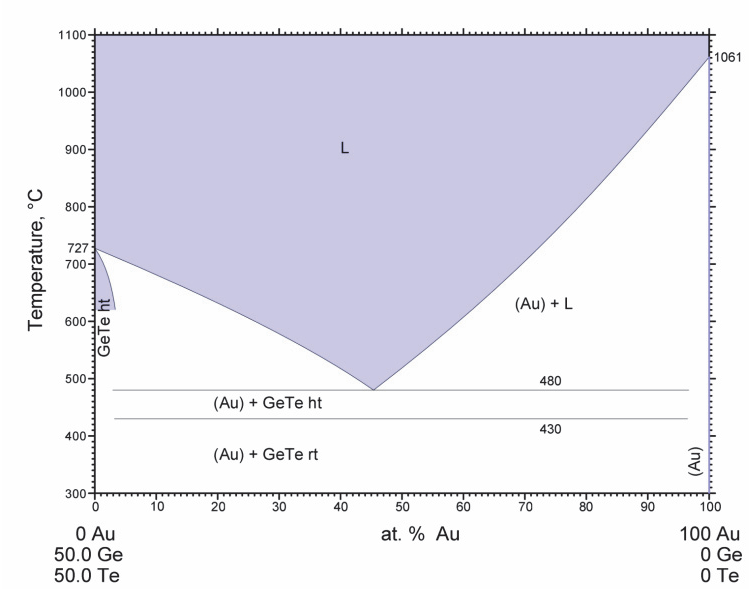


Figure 3.4 – Phase diagram of the Au-Ge-Te ternary system[6]

Under the aforementioned growth conditions, the gold catalyst droplet is supersaturated with precursors and causes the elements to precipitate to the bottom thereof. Because the precipitation of the species carries on in a ordered, self-limited manner, a single crystal is grown, the shape and size of which is dictated by the shape and size of the noble metal particle. Note that the substrate temperature must be set low enough so as to prevent spontaneous deposition on the flat substrate, but high enough to reach the eutectic temperature for the noble metal-precursor alloy. The VLS mechanism is shown schematically in the following Figure 3.5 (for the growth of self-assembled GaAs nanowire).

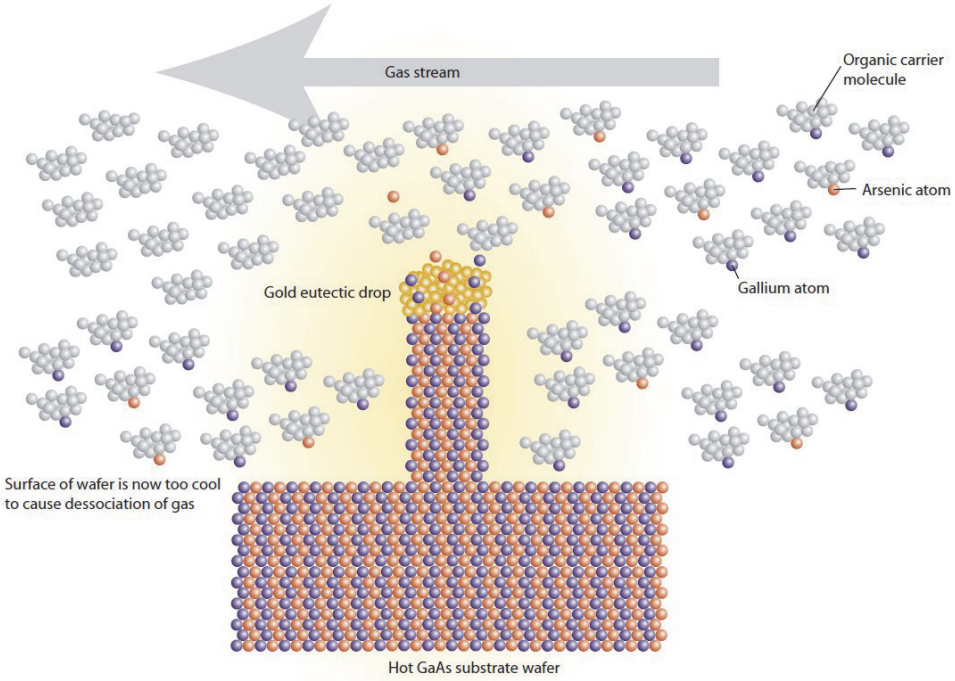


Figure 3.5 – VLS mechanism diagram for the growth of self-assembled GaAs nanowire on a GaAs substrate[7]

The gold droplet plays a key role in the growth from the early stages of deposition, when it dictates the geometry of the wire (its shape being related to the nanoparticle shape). Besides, the catalyst-driven growth favors the vertical growth of the wire, rather than its lateral growth (which is desirable to achieve high aspect ratio devices).

By using nanometer-sized gold nanoparticles, single-crystal binary (GeTe) and ternary (Ge-Sb-Te) chalcogenide nanowires have been synthesized at Laboratorio MDM[8]. A gold thin film (deposited by e-beam evaporation, 1 to 2 nm thick), was employed to obtain the catalyst seed layer in the form of Au nanoislands with a diameter in the range of a few tents of nm. The yield of the VLS mechanism turned out to be strongly dependent on the shape and distribution of the gold nanoparticles. In order to hinder the deposition where the catalyst is not present, thin amorphous silicon dioxide films was employed as substrates. As a result, nanowires grew in randomly oriented directions, with a little fraction thereof exhibiting 'turns' and 'twists' at well-defined angles that testify to edge/screw dislocations during deposition. The occurrence of such dislocations seems to suggest the existence of several minima of energy in the growth directions (in this regard, further investigation is in progress).

The scanning electron microscope

The invention of the scanning electron microscope (SEM) in the 1930s represented a breakthrough in nanotechnology because it extended imaging capabilities to unprecedented resolution. SEM can be thought of as the evolution of optical microscope, where electrons, instead of photons, are employed. In this tool, the morphology of the sample surface is probed by collecting the electrons scattered back to the sensor while sweeping a high-energy electron beam. Two reasons guarantee a higher resolution than optical microscope. First, electrons can be accelerated to higher energies and, therefore, smaller equivalent de Broglie wavelength[9]:

$$\lambda_e = \frac{1.226}{\sqrt{E_e}} \left[\text{nm}\right] \tag{3.1}$$

where E_e is the electron energy in eV. That corresponds to a wavelength of 0.012 nm for a 10 keV accelerating voltage. Second, the electron beam (e-beam) can be sharply focused by electromagnetic plates to nanometric size (see Figure 3.6), and even swept in a raster. Therefore details can be resolved up to a minimum feature size equal to the theoretical e-

beam focusing spot, its size being the limiting factor. Imaging magnification is achieved by shrinking the raster-scan width, and is therefore dependent on the resolution of the electromagnetic deflector plates, rather than the beam spot size. Up to 500,000 times magnification can be achieved in SEM equipped with a 16 bit resolution analog-to-digital controller of the beam deflection.

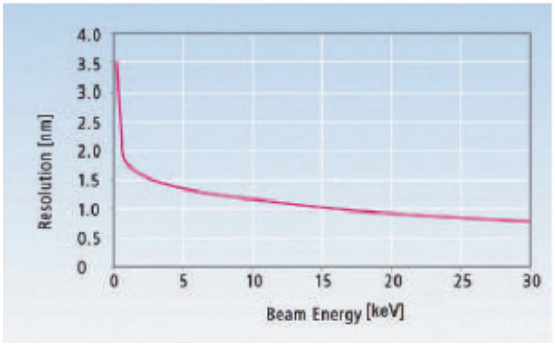


Figure 3.6 – E-beam spot size versus accelerating voltage[10]

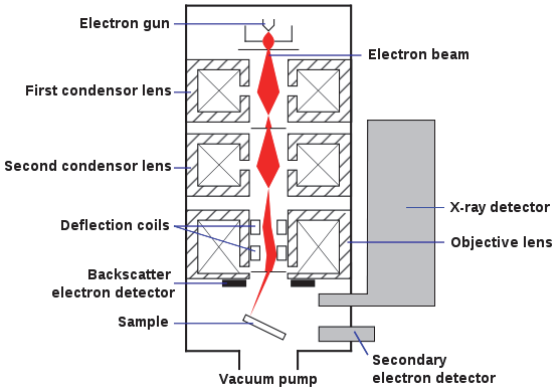


Figure 3.7 – SEM schematic diagram[11]

The SEM schematic operation principle is shown in Figure 3.7. Electrons are sourced by a combination of thermoionic and field emission effects from a metal cathode (W or LaB_6), then accelerated by an electromagnetic field in a ultra-high-vacuumed column, and finally focused and rastered as needed by electromagnetic deflection coils. The energy of the beam, which is ultimately set by the electronic high tension (EHT) acceleration voltage, usually ranges from 1 to 30 keV.

Upon impacting the sample, these primary electrons (PE) undergo several scattering events, releasing energy and momentum to the sample atoms and electrons. Because of their high energy and small mass, PE penetrate the sample according to a distribution of trajectories exhibiting a distinctive ”pear-like” shape. In the PE-sample interaction, other electrons are extracted from the sample. Part of these electrons are the highly energetic, elastically back-scattered electrons (BSE) originating from both the surface and depths. Other PE trigger the emission of electrons from the atomic core or electrons of the atomic shell of (mainly superficial) atoms in inelastic scattering events: these are the weakly energetic secondary electrons (SE). In general, as a consequence of PE trapping into the sample, sample ionization occurs locally. If the sample is a dielectric or is electrically insulated from the surroundings, a negative charge builds up just below the sample surface. This charge can be detected as a darker area in the SEM images; conductive paste can be used to form a conductive path to ground and avoid the shading effect.

For SEM imaging, two different detectors are employed.

The annular detector (inlens) is located along the booster column. The retarding field of the electrostatic objective lens acts as a collector for the BSE, in such a way to minimize the crossover between forward- and backward-travelling electrons. This results in a high collection efficiency and image resolution, also because the backscattered secondary electrons are more energetic, and spatially distributed close to the cone having the e-beam as axis. Inlens imaging is related to the chemical species in and on the sample because the backscattering efficiency is higher for heavier atoms – the resulting image contrast thus being roughly proportional to the Z-contrast. In addition, because BSE originate from the sample depths, the inlens detector actually probes beyond the sample surface.

SE electrons have, on the opposite, low energy (≤ 50 eV) and their emission mostly originates from the very surface of the sample. The SE detector is located sideways with respect to the beam column, and employs an accelerating field (ranging from -300 to +400 V) to increase collection efficiency. As a consequence, only those SE that are emitted with a given angle and direction are collected by this detector. Due to the nature of secondary electrons, the resulting

image solely reveals the surface morphology and features a three-dimensional effect, which helps figure out shapes and contours.

A schematic summary of electron-sample interactions is detailed in the following Figure 3.8. Note that the emission of other X-rays, photons, and Auger electrons (occurring upon removal of an inner shell electron) is beyond the scope of this work and will be neglected.

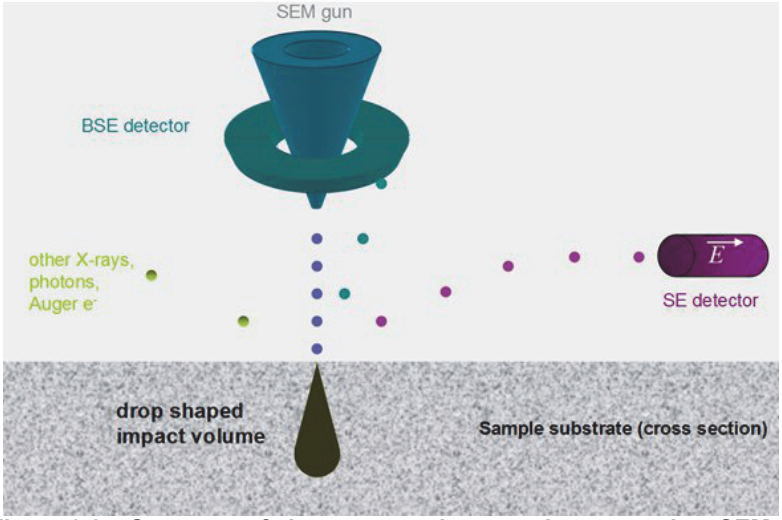


Figure 3.8 – Summary of electron-sample scattering events in a SEM

In the present work, a Zeiss SUPRA 40-25-45 scanning electron microscope, featuring a Gemini acceleration column, was employed for both imaging and electron beam lithography (detailed in the next paragraph).

Electron Beam Lithography

The electron beam sourced by a scanning electron microscope can be employed to selectively pattern nanostructures in a similar way to optical lithography. In electron beam lithography, electron – rather than photon – energy is used to expose a thin solution of a polymer in a solvent, known as *resist*. Two varieties of resist exist: positive and negative. Upon exposure to the e-beam, the positive (negative) resist solubility increases (decreases) as a result of the dissociation of C-C bonds in the polymeric chain (because of bond cross-linking and forming a highly stable structure).

By exploiting the SEM e-beam resolution detailed in the previous paragraph, electron beam lithography (EBL) can achieve a much higher resolution than optical lithography. A side advantage is that the layout patterning is controlled via software, so that very complex structures can be designed and fabricated "on the fly".

The maximum theoretically achievable resolution of EBL is actually hindered by several factors. The main drawback is the forward- and back-scattering of electrons within the resist layer, shown in the following Figure 3.9, where a highly energetic primary electron (purple trajectory) is scattered and generates multiple secondary electrons (blue trajectories). Because PE and SE electrons can cross considerable distance before scattering, they spread throughout the resist film, effectively broadening the exposed area: this phenomenon is known as "proximity effect".

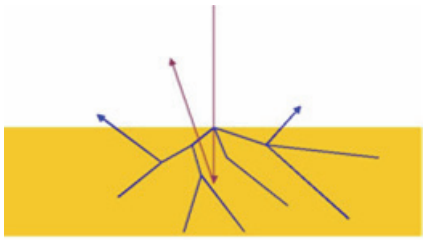


Figure 3.9 – Drawbacks of EBL: forward (blue) and back (red) scattering[12]

Furthermore, a percentage of PE crosses the resist layer until backscattered by the denser, thicker substrate, back to the resist film.

Finally, the pear-shaped impact volume (described in the previous paragraph) is a negatively charge region that deflects the incoming e-beam. As a result, the lateral distribution of beam energy is always broader than the dimension of the exposed pattern.

One of the main concerns in EBL preparation is the deposition of a flat, uniform, thin film of resist. This requirement can be met by employing spin coating. The final thickness of film depends on: amount of resist, sample size, spin time, spin speed, and resist specific molar weight. As a matter of fact, higher molar weight resists have lower sensitivity. Subsequent curing is needed for stabilization and hardening of the film. Afterwards the resist is ready for exposure to the electron beam. In this regard, additional preparation details are provided in Chapter 4.

Calibration of the e-beam operational parameters is mandatory: in particular, electron high voltage (EHT), and aperture size (AP). The former should be as high as possible to improve beam focusing; the latter sets the beam current (I_{beam}). In combination with the raster sweep dwell time per step (T_{dwell}), and the step size ($\Delta x \Delta y$) these parameters eventually set the electron dose per unit area (Dose), in $\mu C/cm^2$, according to the formula[13]:

$$Dose = \frac{I_{beam}}{\Delta x \cdot \Delta y} T_{dwell} \tag{3.2}$$

Beam magnification (MAG) and working distance (WD) set the exposed area width, height, and step size. In the SEM employed in this work, the (mostly used) 500x magnification area size was 560x560 μm^2, the step size was $\Delta x = \Delta Y = 2.86$ nm.

Several techniques have been attempted to improve resolution, a not exhaustive list of which include: lower e-beam energy, wider depth of field, smaller aperture sizes, resist multi-layering, and so forth[13,14,15,16].

Finally, the resist type must be suited to the specific application. Several type of resist are available to this aim, which differ by: sensitivity, molecular weight, dilution, etc.

A Zeiss SUPRA 40-25-45 scanning electron microscope, featuring a Gemini acceleration column and equipped with “ELPHY Plus” electron beam lithography system (manufactured by Raith GmbH, Dortmund, Germany), available at Laboratorio MDM, was employed to fabricate some of the metallizations and electrodes required to prepare NW devices.

The transmission electron microscope

The high-resolution transmission electron microscope (HR-TEM) resolution is unsurpassed by any other probing tool at the atomic level. Contrarily to the SEM, in a TEM the electron beam source and detector are located on opposite sides with respect to the sample (see Figure 3.10). As a result, the e-beam crosses the section of the specimen and is then collected by the sensor. The interaction between the electron small equivalent de Broglie wavelength and the sample lattice delivers an image, with resolution as fine as 0.18 nm. Therefore, the TEM can discern the position of lattice planes in a crystalline solid. Moreover, a lattice diffraction pattern can be obtained by computing the Fast Fourier Transform (FFT) on the HR-TEM image, which reveals information on the lattice spacing and orientation. However, for the e-beam to cross the sample, complex sample preparation is required to produce thin slices (< 500 nm thick) by micro or nano machining.

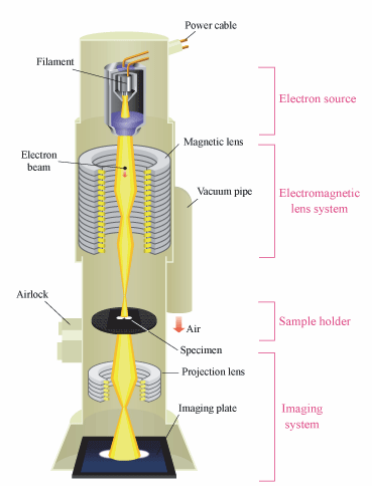


Figure 3.10 – TEM schematic diagram[17]

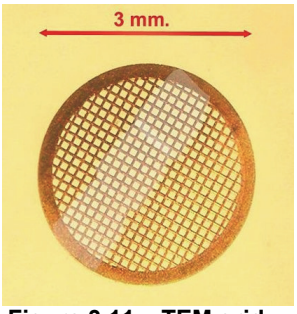


Figure 3.11 – TEM grid

The TEM is convenient for imaging nanostructures and nanowires (which have diameter smaller than 200 nm, thus requiring no special preparation). To this end, the nanowires need to be dispersed on dedicated, micromachined holey carbon grids (see Figure 3.11). The grid is available with pitches of as little as 1 µm. After depositing the nanowire, it sticks to the grid by electrostatic force and can be looked for in the microscope. The sample holder makes it possible to vary the incident angle of the electron beam, thus investigating the different crystallographic directions.

Additional capabilities are available in TEM equipped with scanning e-beam. In this tool, called STEM, the e-beam is swept in a raster over the sample. The rastering of the beam across the sample makes these microscopes suitable for analysis techniques such as mapping by energy dispersive X-ray (EDX) spectroscopy, electron energy loss spectroscopy (EELS) and annular dark-field imaging (ADF). These signals can be collected simultaneously, allowing direct correlation of image and quantitative data[18].

Analytical and conventional TEM studies for this work were performed on selected nanowires in a High Resolution (0.18 nm) Field Emission JEOL 2200FS, equipped with energy filter, two High Angle Annular Dark Field (HAADF) detectors, and Energy Dispersive X-ray spectroscopy (EDX) available at Istituto dei Materiali per l'Elettronica ed il Magnetismo (IMEM-CNR) in Parma, Italy.

Structural characterization

The X-Ray diffraction (XRD) is a well-established technique for probing the long-range arrangement of atoms and molecules in a crystal. It is based on Bragg's law, which describes how X-rays are reflected by the lattice, according to the incident angle of the wave itself. By varying the incident angle θ, a diffraction pattern is generated and it can be interpreted to determine the presence of given crystalline phases (each atomic lattice exhibiting a different peak pattern). This tool is especially useful for providing information on the orientation, axis, and size of crystal grains. However, because the probing beam has a diameter of about 5 mm, this instrument can only probe large areas of crystals, not microscopic structures. Nevertheless it is usually possible to discriminate, for example, the contribution of nanowires from substrate and therefore retrieve useful information on the phase and stoichiometry of the wires. On the other hand, this technique is of limited use for investigating the amorphous chalcogenides, where long-range order is lacking.

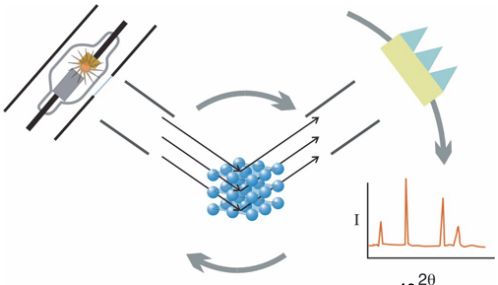


Figure 3.12 – X-ray diffraction[19]

Some of the samples of chalcogenide nanostructures in the present work were characterized by XRD (Cu-kα source, 40 kV) at Laboratorio MDM.

Surface and charge characterization

The atomic force microscope (AFM) is a versatile surface characterization technique. In non-contact mode operation, a nano-fabricated, sharp tipped silicon cantilever is made oscillate at its resonance frequency while closely approaching the sample surface. The harmonic oscillation is perturbed by the short-range van der Waals forces interacting between tip and surface. Because of the high sensitivity of the oscillator, it is possible to map the surface with very high vertical resolution (somewhat less that 1 Å). The displacement of the cantilever is detected by measuring the reflection of a laser beam onto a four-quadrant sensor. On the opposite, lateral resolution is limited by the sharpness of the cantilever's tip (some tens of nanometers). The AFM can be operated in vacuum or in air, in the latter case a water condense 'meniscus' is always formed on the cantilever, further degrading its lateral resolution. This instrument is capable of producing detailed morphological images of the surface roughness and defects in a non destructive manner. Another operational mode is the 'contact mode' where the tip is lowered enough to touch down the surface.

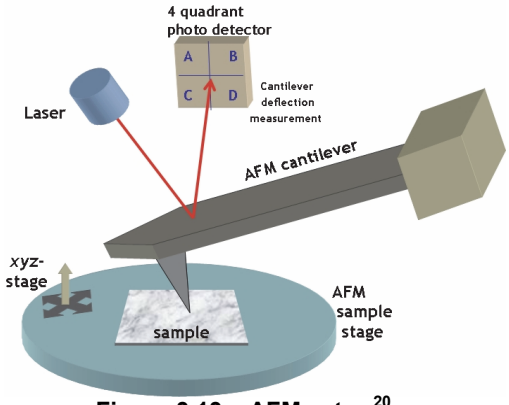


Figure 3.13 – AFM setup[20]

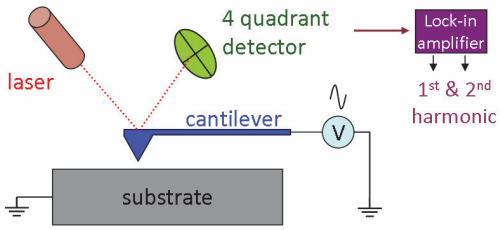


Figure 3.14 – EFM schematic diagram

In addition to morphology, the AFM can be operated to map the electrostatic contrast between tip and substrate; exploiting the longer range of electrostatic compared to van der Waals forces, the morphology and electrostatic contrast can be collected simultaneously. In this non-contact variant of the AFM, called electrostatic force microscopy (EFM), a continuous (DC) or sinusoidal voltage is applied to the tip. In the latter case, a lock-in amplifier has to be used for providing higher sensitivity and distinguish between potential and capacitive contrast by measuring the first and second harmonic of the signal, respectively. The EFM setup is schematically shown in Figure 3.14.

An AFM/EFM facility at Laboratorio MDM was used to investigate the morphology and electrostatic contrast of some devices in this work.

Thin metal film deposition

Sample preparation for electrical measurements requires the deposition of metal electrodes or pads, in several process steps, that subsequently imply the removal or etching of the metal, as will be detailed in the next Chapter. Evaporation is the most straightforward and highest yield technique to do so. Two techniques will be detailed, which differ in the way the metal is vaporized. In electron-beam evaporation, an electron source (located in high vacuum chamber) delivers an electromagnetically-focused beam which heats a ultra-high purity metal, contained in a crucible, up to its evaporation (Figure 3.15). In DC/RF sputtering, an inert gas is brought to plasma and focused onto the metallic target. As the high energy ions impact onto the target, atoms and molecules are extracted from the material and deposit onto the

substrate (Figure 3.16). In both cases, as the direction of ejection has a high directivity, the step coverage of a sample is very poor (i.e., surface features are preserved by the deposition and no lateral growth can be achieved).

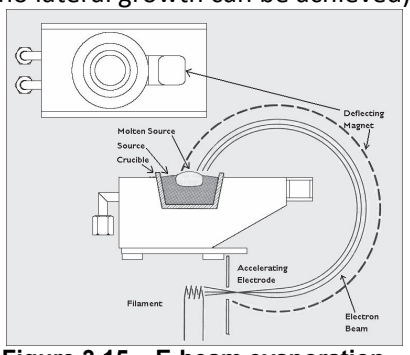


Figure 3.15 – E-beam evaporation

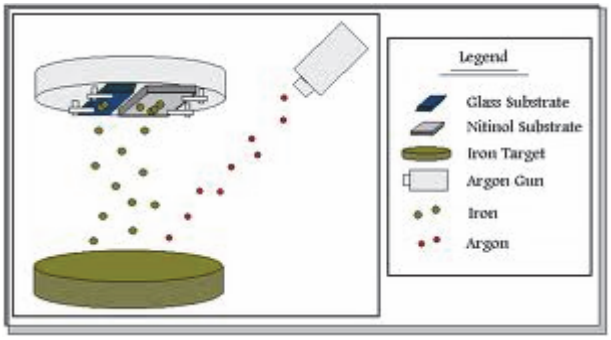


Figure 3.16 – Sputtering deposition

Nanofabrication by Dual Focused Ion/Electron Beam

The dual focused ion/electron beam (FIB) is a fabrication tool featuring two separate columns for the extraction, focusing, and raying of both ions and electrons at once. The ion column employs a gallium Liquid Metal Ion Source (LMIS) to focus Ga^+ ions into a narrow beam (i-beam) by means of magnetic lenses, which serve also for sweeping the beam in a raster (≈ 7 nm resolution), whereas the electron beam (e-beam) is provided by a SEM column, the setup of which has been described in a previous paragraph. Ion acceleration energy ranges from 5 to 30 keV. Given the – relatively – high atomic mass of Ga, the ion beam can be used for local micromachining (milling), deposition, as well as for imaging of the sample. In addition, the two beams can be fired simultaneously, and the accelerating columns are placed in such a way to focus over the same spot on the sample surface, their axis being shifted by a 52° angle, as shown in the following Figure 3.17.

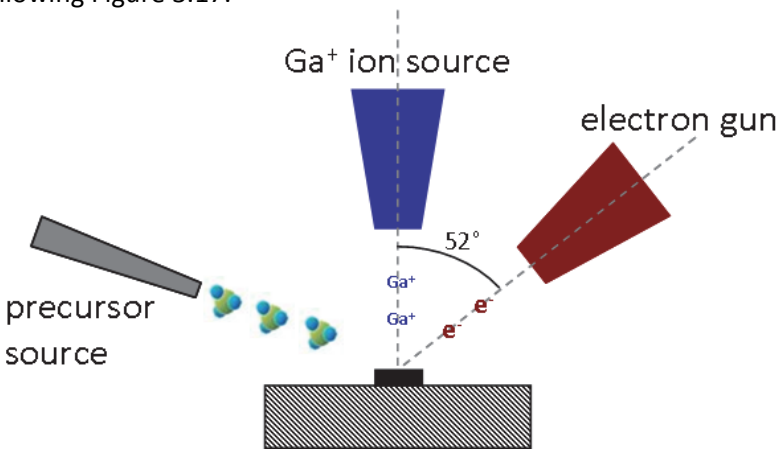


Figure 3.17 – Schematic of FIB/SEM dual beam setup

In imaging mode, the incident ions collide with the surface of the sample under investigation, causing both primary and secondary electrons to be extracted from the sample and be collected by a detector, similarly to the SEM. Because of the higher Ga^+ ions mass in comparison to electrons, the i-beam penetration depth is shallower and only the very first layers of material contribute to the back-emitted electrons (and to the final image)[21]. For this reason, in dual beam instruments, the SEM column is usually utilized for imaging, due to its higher efficiency.

In nanofabrication mode, ion/electron beams perform selective deposition (also referred to as electrochemical deposition, or focused deposition). A gaseous organometallic precursor of platinum (formula: $C_5H_5Pt(CH_3)_3$) is injected on the sample surface, while the ion/electron beam performs a raster sweep. Upon impacting the precursor, the i-/e-beam delivers energy to dissociate the molecule into elemental Pt, which precipitates according to the beam

position. The thickness of the deposition is controlled by both aperture size (i.e., current) and accelerating voltage (i.e., energy) of the beam.

The benefit of selectively-controllable Pt deposition, however, has the drawback of the poor quality of the deposited metal. According to previous studies in this field, FIB deposition produces a polycrystalline platinum, rich in contamination by: gallium (from the ion beam), carbon (from the precursor gas), and oxygen (when the base pressure is not optimal)[22]. Most of contaminants gather at the grain boundaries, with a detrimental effect on electrical conductivity. In addition, Pt deposited by e-beam has been reported to have higher electrical resistivity (0.8 vs. 0.0045 Ωcm) and higher C contamination (60 to 75 at.% vs. 40 to 55 at.%) than that deposited by i-beam, respectively[23]. In both cases, it has been demonstrated that the resistivity of Pt can be improved (i.e. decreased) by thermally annealing in forming gas ($Ar:H_2$), as shown in Figure 3.18. However, in doing so, the improvement is small, while the risk of contaminating the wire with additional impurities is high.

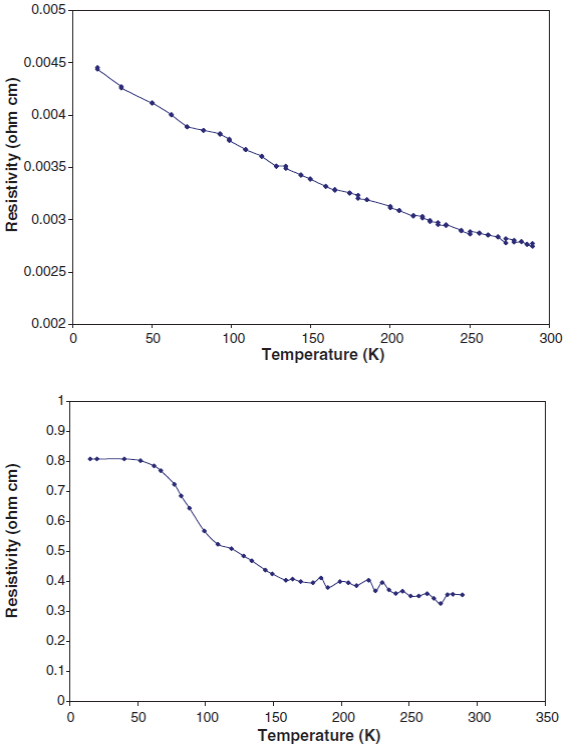


Figure 3.18 – Resistivity vs. temperature for i-beam (top) and e-beam (bottom) deposited Pt strip[23]

Contamination of the FIB-deposited Pt is especially detrimental when involves electrodes for electrical characterization, because it increases the overall resistance of the device. This parasitic resistance includes two terms: the Pt strip resistance itself and the Pt/sample contact resistance.

Two issues arise as a consequence of the high electrode resistance. First, a smaller amount of voltage (energy) is effectively delivered to the wire. For example, it has been proven that the Pt strip series resistance accounts for over 85% of the total resistance measured in SnO_2 nanowires by 2-probe measurements[24]. In nanowires, this resistance cannot be measured because 4-probe (Kelvin) measurements are not viable, due to the nanowire reduced length. In this work, this value has been estimated by measuring nanowires of various lengths and interpolating the resistance value at zero length, as will be detailed in the following Chapter 6. Second, the strip resistance R increases the time constant ($\tau=RC$) of the network by coupling with the capacitance C of the Pt-wire contacts, making it harder to deliver sharply edged voltage pulses in the nanosecond timescale, an issue that will be detailed in Chapter 6 as well.

It has been proven that the contact resistance between Pt and nanowire can be improved by flowing a current in the strips. Because of the high interfacial resistance, Joule heating locally occurs at the joining points, improving the intermixing and decreasing the overall resistance[25]. This effect was detected in nanowire samples investigated in this work (see Chapter 6 for additional details).

For the above mentioned reasons, i-beam was preferred over e-beam whenever possible. However, it should be noted that the highly energetic Ga^+ atoms yield a greater momentum when rastering the nanowire ends, which can displace it during the deposition. Therefore, the use of i-beam adds to the complexity of the fabrication and requires additional care.

Some of the devices characterized in the present manuscript were prepared in a FEI Strata™ DB 235 Dual Focused Electron/Ion Beam during the Author's three-month internship at Laboratory for the Research on the Structure of Matter, University of Pennsylvania, Philadelphia (USA).

Thin film electrical characterization

The electrical characterization of thin films aims at measuring intrinsic properties of materials, which cannot be determined otherwise.

Resistivity (ρ) measurement as a function of temperature delivers information on the metallic/insulating behavior of a material. While classical resistivity of bulk samples used to be measured by two-probe techniques, submicrometric thin films and nanoscaled materials pose a considerable challenge. This concern arose along with the availability of the first vapor-phase deposited thin films in the 1930s and 1940s. In thin films, one of the geometrical dimensions is accurately controlled (thickness), whereas both lateral dimensions depend on the shape of the substrate, and can vary in geometry. Moreover, the contact effect of the two-probe technique adds a series resistance that prevents the correct estimation of the intrinsic resistivity of the material. To overcome these limitations, four-collinear probes can be used, so as to decouple the effect of current flowing in the first two probes, from the voltage measurement across the other two.

A significant improvement in the resistivity measurement of samples of any shape is, doubtlessly, the van der Pauw method[26], a four-probe technique based on the conformal mapping of two dimensional fields[27]. Under the assumptions that:

- the probe tips are reasonably small
- the contacts are placed on the circumference of the sample
- the film thickness is constant throughout the sample
- the sample surface is a simply connected shape

then the film resistivity ρ is given by the formula:

$$\rho = \frac{\pi}{\ln 2} t \frac{\sum_{i=1}^{8} V_i}{8I} \tag{3.3}$$

where t is the thickness, I is the electric current supplied by the first pair of probes, and V_i (i=1…8) are the averaged voltages measured across the other two probes in eight measurements performed throughout all possible combinations of adjacent probe positions, as shown in Figure 3.19. Note that eq. (3.3) is an approximation; see Appendix A for the exact formula.

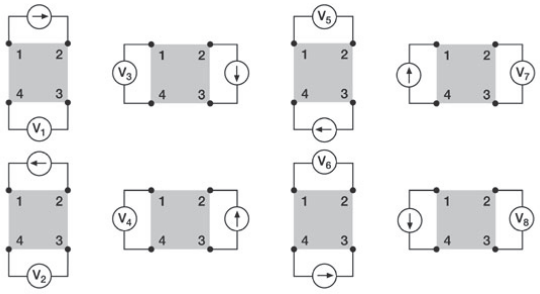


Figure 3.19 – The van der Pauw method for resistivity

Although the need of four probes adds to the complexity of the measurement, the van der Pauw method represents a huge improvement over the 4-collinear-probes technique: it has the advantage of being viable for samples of arbitrary shape, and excludes the effect of contact resistance. van der Pauw himself, and others estimated and calculated the correction factors due when using non zero-sized probes, which are not placed exactly at the borders of the sample[28,29,30,31,32]. In this work, chalcogenide thin films were characterized as a function of temperature by this technique, taking into account the non idealities in the measurements.

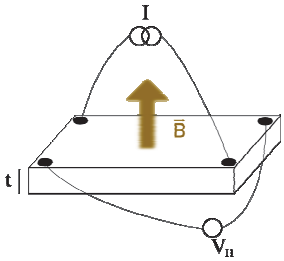


Figure 3.20 – Hall effect in the van der Pauw geometry for thin films

Charge carriers in a (semi)conductor are the means of electrical conduction. Their density (CD) and mobility (μ) are parameters to take into consideration for device design and implementation. The Hall effect was employed to determine these parameters for chalcogenide thin film of various stoichiometry. Conventional Hall measurement are carried out on 'bar' or 'cross bar' geometries, which are either not feasible, or require additional processing/fabrication in the case of thin films. Instead, the van der Pauw geometry can be used. Similarly to the resistivity measurement, this is a 4-probe configuration involving the averaged measurement of the voltage drop across two opposite (diagonal) terminals; while the magnetic flux $\vec{B}$ is set perpendicular to the film surface (shown in Figure 3.20). This measurement outputs a Hall voltage:

$$V_H = \frac{R_H B I}{t} \tag{3.4}$$

where *B* is the applied magnetic flux density, *I* the current flowing across two terminals, *t* the film thickness, R_H the Hall coefficient. In the most general case – assuming both electrons and holes are involved in the conduction – R_H is given by:

$$R_H = \frac{-n\mu_e^2 + p\mu_h^2}{q(n\mu_e + p\mu_h)^2} \tag{3.5}$$

where *q* is the electron charge, *n* the electron density, *p* the hole density, μ_e the electron mobility, μ_h the hole mobility. In the limit of high magnetic field, it becomes:

$$R_H = \frac{r}{q(p-n)} \tag{3.6}$$

where *r* is the Hall scattering factor:

$$r = \frac{\langle\langle \tau^2 \rangle\rangle}{\langle\langle \tau \rangle\rangle^2} \tag{3.7}$$

i.e., the specially averaged scattering times τ. It is also equal to the ratio between Hall mobility and drift mobility. For most semiconductors r ≈ 1, but its exact measurement is not straightforward because it requires the measurement of the sample in the high magnetic field limit, as from the formula[30]:

$$r = \frac{n|_{B=0}}{n|_{B=\infty}} \tag{3.8}$$

The previous formulas can be simplified under the hypothesis that the concentration of either carrier is dominant (*n*>>*p* or vice versa); then R_H is related to the reciprocal of carrier density:

$$R_H = \frac{1}{q(p \text{ or } n)} \tag{3.9}$$

Finally, carrier mobility can be estimated from the joint knowledge of electrical resistivity ρ and concentration:

$$\mu = \frac{1}{q\rho(n \text{ or } p)} \tag{3.10}$$

In this work, the Hall effect was used to investigate the transport properties of thin chalcogenide films by calculating carrier density and mobility from room temperature to cryogenic temperature (see Chapter 5).

Nanowire electrical characterization

The electrical properties of nanowire devices were investigated by pulsed I/V (current/voltage) measurements to the aim of calculating the device resistivity in the amorphous and crystalline states, and to determine the threshold voltage at which the switching occurs.

In doing so, usage of pulsed I/V measurement, instead of conventional I/V, was required. While conventional I/V is based on continuous current measurement (also known as direct current, or DC), pulsed I/V employs voltage pulses to probe the current through the device at given discrete voltage values. The former technique is easily implemented as it requires only the generation of a staircase-like voltage; the current is measured during the voltage plateau, after a given settling time which depends on the sample. On the opposite, the pulsed mode requires voltage to be supplied in pulses of a given width (t_{pulse}) and periodicity (t_{period}); the current through the device is measured during the plateau part of the pulse, after a given settling time has elapsed. In this case, the current measurement has to be much faster, thus requiring an oscilloscope (OS). The voltage vs. time plots of these two modes are displayed in the following Figure 3.21, respectively.

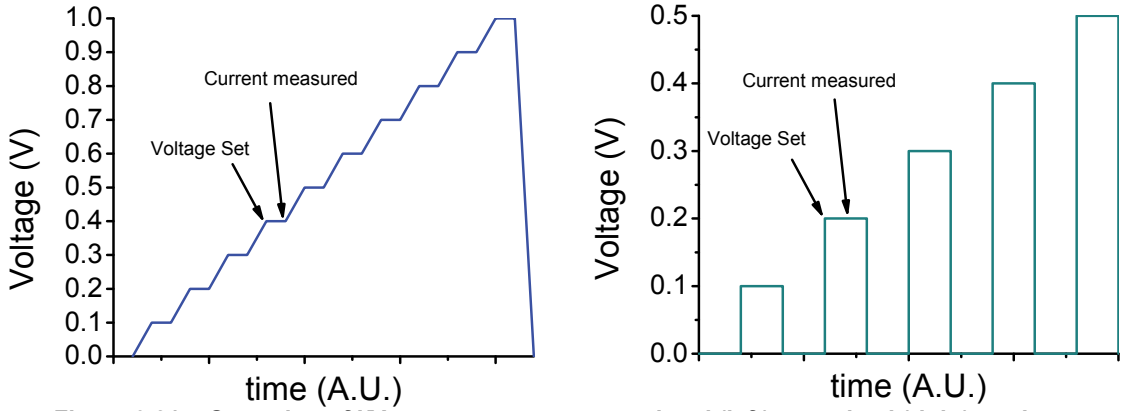


Figure 3.21 – Operation of I/V measurement: conventional (left) vs. pulsed (right) mode

Although the pulsed I/V technique adds to the complexity of the instrumentation (as it requires a pulse generator and an oscilloscope), it is mandatory in preventing: 1) self heating and 2) failure of nanoscaled devices.

The first issue is related to the inevitable Joule heating that occurs in devices. Because nanoscaled devices have smaller volume/area ratio, the temperature rise does significantly affect those device parameters which have a temperature dependence (such as resistivity, thermal conductivity, thermal expansion, transconductance). As the energy delivered to the sample is proportional to the square of the area below the V(t) plots in Figure 3.21, it is clear that pulsed I/V can reduce Joule heating by a factor equal to the duty cycle of voltage pulse (usually, $t_{pulse}/t_{period} < 1\%$). Figure 3.22 shows a comparison of conventional and pulsed I/V performed on the same device (a MOSFET transistor): the DC-measured transcharacteristic exhibits anomalous behavior at higher drain voltages, because of the detrimental effect of heating on the device transconductance.

The second issue with conventional I/V concerns device failure. This is related to the maximum sustainable current density, which is much lower than that of macroscopic devices and scales either with the layer thickness (for thin films), or with the square of radius (for nanowires). In nanoscopic devices, high current density triggers electromigration – i.e. the rapid deterioration thereof due to the highly energetic electrons impacting onto the lattice, up to the degree of removing atoms from their former position and consuming the conductive path. This eventually leads to damaging the device beyond recovery, as in Figure 3.23, where a chalcogenide nanowire damaged by excessive current density is shown.

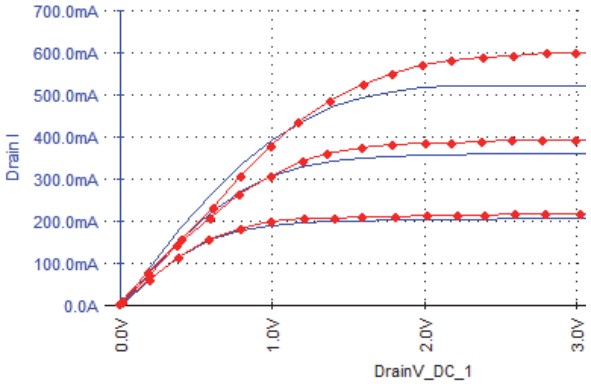


Figure 3.22 – MOS transistor Vd/Id plot, measured in DC (blue line) and pulsed mode (red dotted line)[33]

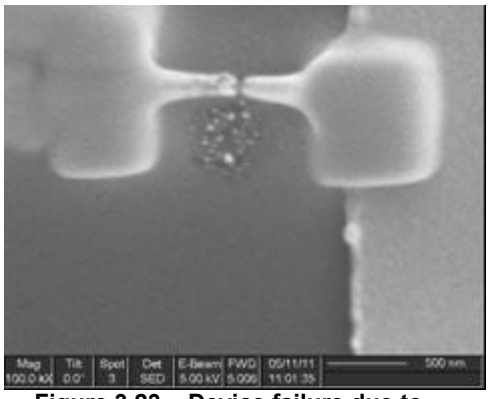


Figure 3.23 – Device failure due to electromigration

The pulsed I/V characterization is especially useful for phase change devices. Indeed, the phase change can be detected in the measurement by the coexistence of two I/V plots, exhibiting two different slopes, related to the low resistance and high resistance state, as shown in the following Figure 3.24 (relative to a 90 nm pitch phase change memory device). When in the crystalline phase, a steeper, linear (empty symbols) curve is obtained. On the opposite, when it is in the amorphous phase, little current flows and the plot (full symbols) is flat up to a given threshold voltage (V_{th}). Above V_{th}, the heat (energy) delivered by the current pulse is large enough to onset the phase transition. From that point on, the IV plot merges with the SET-state IV plot. While the slope of the plots give information on the SET and RESET resistance, the threshold voltage is equally important as it is roughly proportional to the switching energy required.

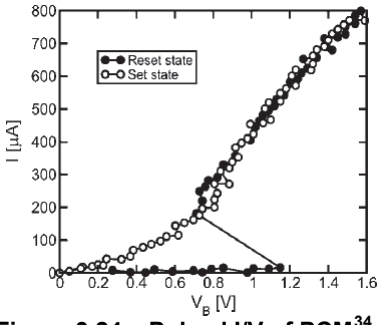


Figure 3.24 – Pulsed I/V of PCM[34]

In the next Chapter, the instrumentation setup used for pulsed I/V and available at Laboratorio MDM will be detailed.

Electro-thermal modeling by finite elements

The electro-thermal modeling of phase change transition in nanowires can be accomplished by analytical or numerical methods. Although analytical models feature faster computational times, their validity is limited to few specific geometries[35]; while numerical methods grant applicability to any system regardless of shape. The latter involves numerical solving of a set of physical equations governing the Joule heating and electric flow. Model geometry is defined by means of a computer-aided design tool, so as to match the actual device shape. The geometry is then transformed into a mesh of finite elements, the size of which eventually sets the resolution (and computational complexity) of the solution. Finally, boundary conditions of the model are set in agreement to the actual device constraints. These tools are commonly exploited by phase-change memory system designers in order to evaluate the transient temperature variation during set and reset operation. Notably, estimation of thermal crosstalk between neighboring cells (see Chapter 1) is of particular interest for PCM devices.

In this work, numerical models were employed to estimate (qualitatively and quantitatively) the temperature profile of a nanowire-based device. In addition, the limitations and drawbacks of single-nanowire device preparation were highlighted.

To this aim, COMSOL Multiphysics suite[36] was employed to define geometry, meshing, physics model, solving, and visualizing of the results. Material properties, source terms and boundary conditions of known materials were used, or extracted from experimental data available in literature if needed.

"The loveliest theories are being overthrown by these damned experiments; it's no fun being a chemist anymore"
Justus von Liebig

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4. Implementation

Sample preparation and fabrication, carried out by the instrumentation described previously, is detailed in this Chapter. In addition, several technological issues concerning the characterization are discussed.

Concerning the electrical characterization of single nanowire (NW), two techniques were mainly employed to prepare the single nanowire device. The first, relied on e-beam lithography (EBL) to produce the electrodes, across which the nanowire is drop in a non-deterministic way (statistical). The second technique employed focused ion/electron beam (FIB) to prepare *ad hoc* electrodes.

NW electrode fabrication by EBL, positive resist

E-beam lithography was employed in combination with lift-off technique to produce electrodes for NW electrical measurement. EBL makes it possible to fabricate high resolution metallic patterns, easy reproducible on a large scale. The goal was to employ EBL to design and produce a metal interdigit array featuring:

1. 300 to 500 nm pitch
2. ≥ 300 nm width
3. made of Al, Ti, Au, or Pt
4. a couple of millimetric pads
5. 1 to 4 cm^2 substrate size

The first requirement is dictated by the nanowire length, which was at least 500 nm long. The second feature ensured the NW is connected through a low resistance path along the interdigit. Various metals were to be tested to check the viability and yield of the process. The millimetric-sized pads were required in order to perform the electrical characterization by means of macroscopic electrical probe in a test bench. Finally, the process had to be compatible with a substrate (silicon, 550 µm thick, with silicon dioxide insulating layer, 50 nm) of the given size – due to geometrical constraint in the SEM sample holder.

Poly(methyl methacrylate) (PMMA) is a very renown polymer used as a positive resist in optical and electron beam lithography. It is commercially available in powder, that requires dilution in a solvent (typically anisole, *Methoxybenzene*) before use. As detailed in the previous Chapter, exposure to the electron beam causes the polymeric C-C bonds to dissolve, thus increasing the positive resist solubility. PMMA sensitivity depends on its molecular mass: the higher the relative molecular mass, the lower the sensitivity[1].

Two techniques were attempted: in the first, the nanowire was cast on top of the metal interdigit (wire-on-metal); in the second, the metal interdigit was fabricated on top of the nanowire (metal-on-wire).

Wire-on-metal

In this technique, first the metal pattern was fabricated on the dielectric substrate; then the nanowire was cast across the interdigit. Given the high density of wires on the as grown sample, it was expected that several of them were to fall across the interdigit. Sample fabrication consisted of the following processing steps (portrayed in Figure 4.1):

- Substrate cleaning in acetone (ACE) and isopropyl alcohol (IPA)
- Substrate pre-bake at 90 °C, for 1 minute
- PMMA spin coating at 4000 revolutions per minute (rpm), 30 seconds
- Substrate post-bake (curing) at 180 °C, 10 to 20 minutes
- EBL exposure:
    - 10 keV beam acceleration
    - 30 µm aperture Ø for large areas, 7.5 µm Ø for small areas
    - Dwell time ≈ 1E-5 s per step
    - Magnification 500x, working distance 4 to 5 mm
    - Dose 100 to 160 $\mu C/cm^2$
- Development by stirring in MIBK:IPA 1:3 solution, 30 seconds
- Evaporation of metal
- Lift-off by stirring in hot acetone (40 °C) and/or ultrasonic acetone bath, as needed
- Sample cleaning in IPA
- Nanowire cast/drop

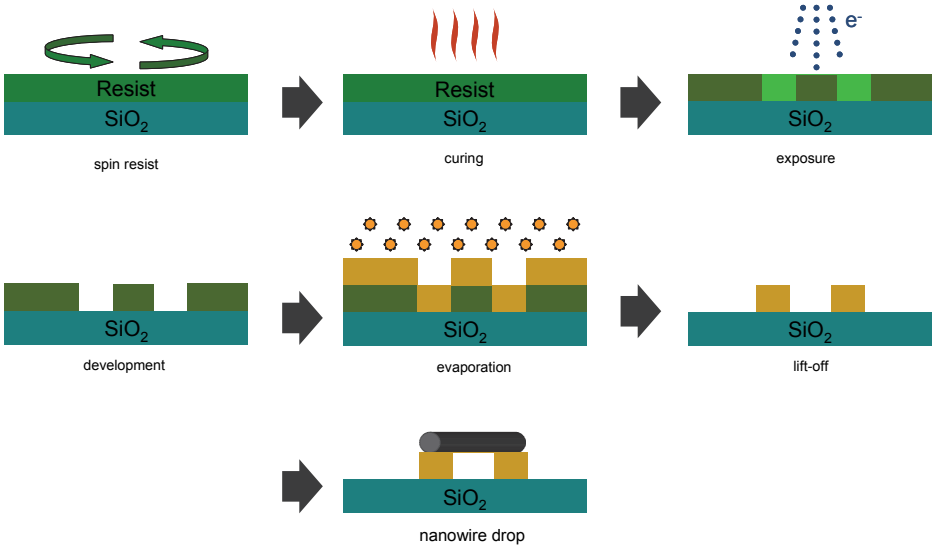

Figure 4.1 – Main process steps in wire-on-metal technique.

The first two steps were required to remove both organic and inorganic contaminants from the sample and to dry up the surface before the resist deposition. While multi-layering of PMMA might be required to achieve higher resolution[2], doing so was not required in this work. Moreover, using a single PMMA layer brought the advantage of a faster, more robust fabrication process. Spin coating ensured a good uniformity of the film; film thickness and flatness were set by spin speed and time. Edge effects were more marked in smaller samples; however, most of prepared samples were no larger than 1 cm^2, due to EBL sample holder constraints. PMMA solution was previously prepared from a 996K molar mass powder, diluted in anisole (6% concentration). This specific PMMA molar mass was chosen as a tradeoff between the requirements of high resolution (i.e. higher molar mass) and short exposure time (i.e. lower molar mass). Finally, post bake (curing) improved the film hardness and the lithographic yield.

Concerning the EBL process, the goal was to achieve both high resolution in the interdigit area and high exposure speed in the pad area. Several EBL masks were designed to optimize the yield. The prototypical mask used to produce the pattern is shown in the following Figure 4.2.

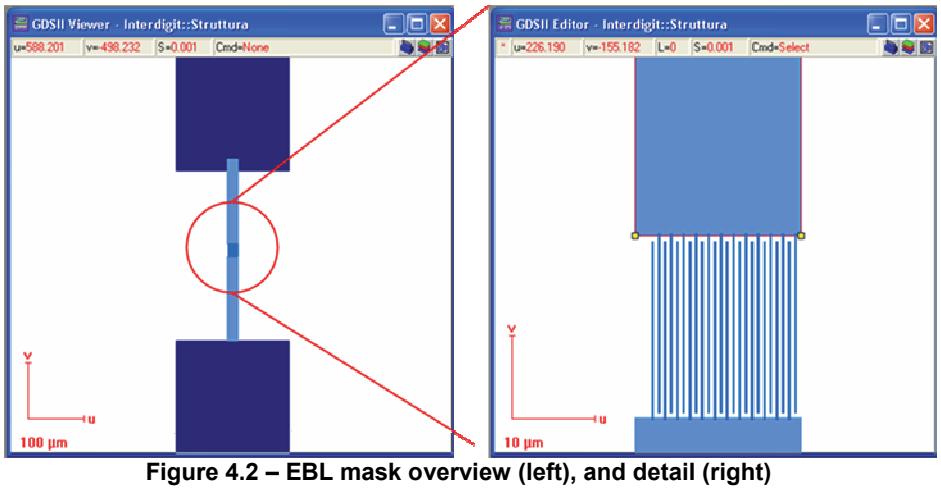

Figure 4.2 – EBL mask overview (left), and detail (right)

It has to be noted that the coexistence of low and high resolution areas in the mask demanded the calibration of the electron dose per unit area. This was achieved by tuning the e-beam current, that is, by using different aperture diameter (Ø) sizes: 30 µm Ø for coarse areas, 7.5 µm Ø for fine details. The other key parameter was area dose, which is independent of the beam current, and is set by the dwell time, as detailed in the previous Chapter. Dose tuning was performed to minimize side effects, such as line width widening. Optimal dose was

found to be within 1.4 to 1.6 times the base dose (the base dose is conventionally defined as 100 μC/cm^2), as a result of several attempts at dose ranging from 0.1x to 5x.

E-beam acceleration voltage was set to 10 keV instead of 30 keV. In principle, higher EHT is expected to improve the beam focusing, as discussed Chapter 3. However, during process optimization it was found that resolution did not improve when increasing the EHT beyond 10 keV. This finding was backed up by experts in the field[3]. In addition, lower EHT brought the advantage of lessening space-charge buildup in the substrate, which in turn reduced parasitic beam deflection and backscattering, a cause of line width broadening. (Some of these EBL fabrication issues are detailed at the end of this paragraph.)

After exposure, the sample was developed in a solution of *Methyl isobutyl ketone* (MIBK) and *isopropyl alcohol* (IPA), 1:3 ratio respectively. Note that, as the dilution ratio of developer is related to the area dose, the process calibration involved the evaluation of their mutual effect on the final result (the patterned trenches).

The pattern, so fabricated in the PMMA film, was then filled by evaporating a metal film on the whole sample surface. E-beam evaporation of a metal is featured by a poor step coverage, so that metal does not adhere to the trenches edges. Provided that the metal film is thinner than the PMMA layer, the excess metal can be removed from the rest of the sample by lift-off, i.e. by stirring in hot acetone. As a result, the pattern transfers from the PMMA to the metal.

Several metals (with and without additional adhesion layers) were employed in this process. Although most of them were found viable to the fabrication, each one showed peculiar advantages and disadvantages, as summarized in the following Table 4.1.

metal (adhesion layer)	adhesion	coverage	electrical conductivity	inertness
Al	**++**	**–**	**+**	**–**
Ti	**+++**	**+**	**++**	**–**
Au	**–**	**–**	**++**	**++**
Pt	**–**	**–**	**++**	**++**
Au (Cr)	**++**	**+**	**++**	**++**
Pt (Ti)	**+++**	**++**	**++**	**++**

Table 4.1 – Pro and contra of metals used in fabrication

Aluminum featured the highest ease of deposition, with good adhesion; however it had poor electrical properties because it is quickly oxidized. Titanium had excellent adhesion and conductivity, but was known to intermix with chalcogenides[4] and had to be discarded. Pure noble metals, like gold and platinum, exhibited poor adhesion to SiO_2, thus being unable to withstand lift-off. Eventually, the combination of a noble metal with a thin adhesion layer (< 5 nm) yielded the “best of both worlds” solution: good adhesion and good electrical properties. Both gold(chromium) and platinum(titanium) delivered good results, with the latter outperforming the former in terms of: adhesion, coverage, and yield. For these reasons, most of devices were fabricated in Pt(Ti).

The obtained devices are shown in the following SEM images.

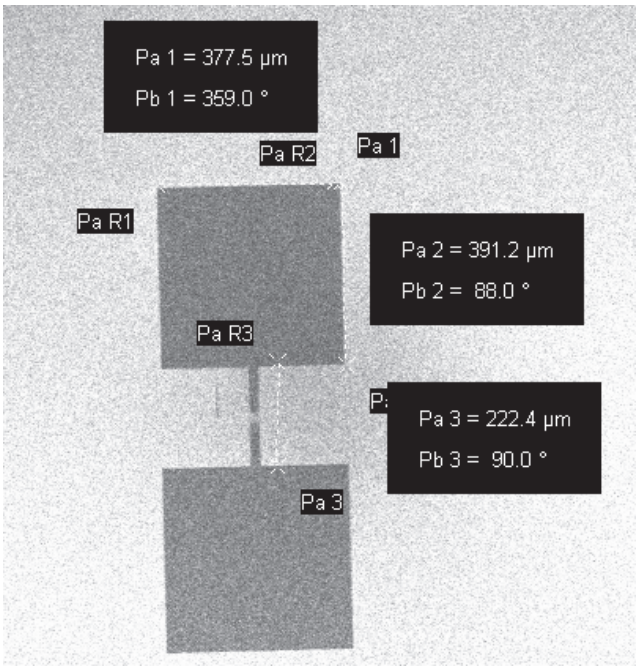

Figure 4.3 – SEM dimensioned image of pattern for nanowire characterization

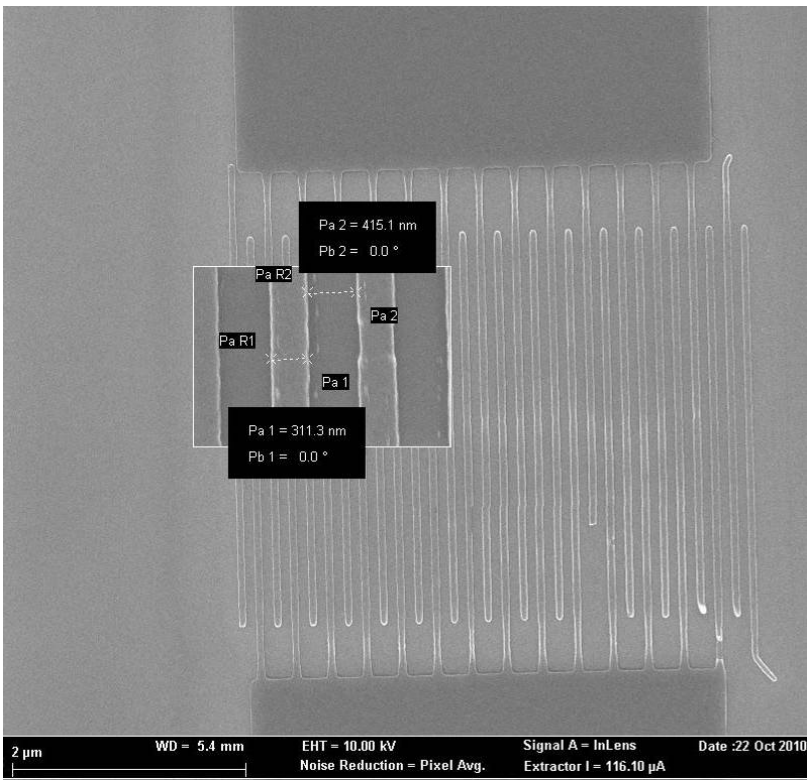

Figure 4.4 – SEM detail of the interdigit region

The base pattern was reproduced several times on each sample, as shown in the following Figure 4.5. The repeated matrix was employed to: 1) maximize the chance of having a nanowire drop in the right position, and 2) produce a dose gradient and find the right developer concentration for the process. In the following, the EBL mask and the resulting array are shown.

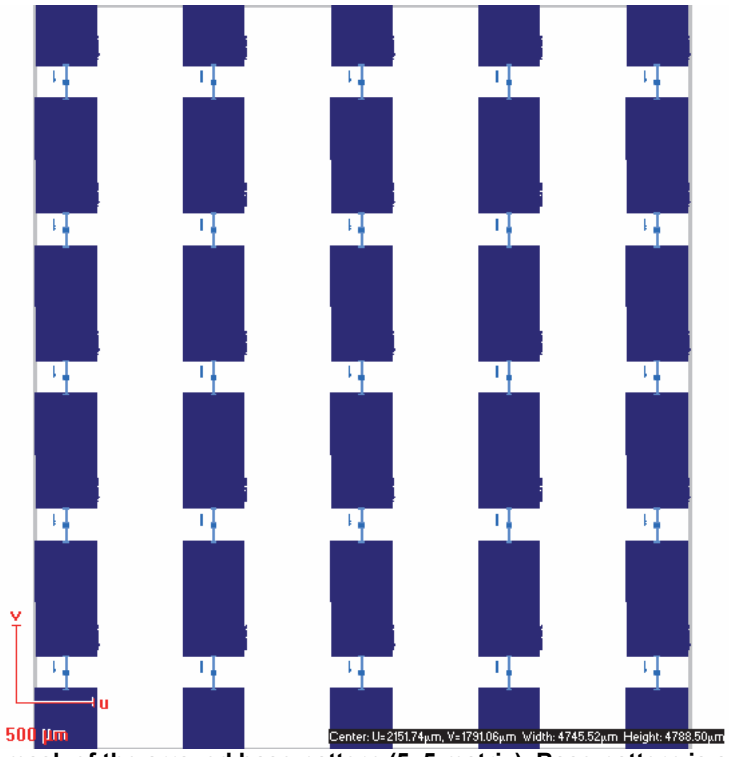

Figure 4.5 – EBL mask of the arrayed base pattern (5x5 matrix). Base pattern is shifted so as to achieve an overlap of the pads

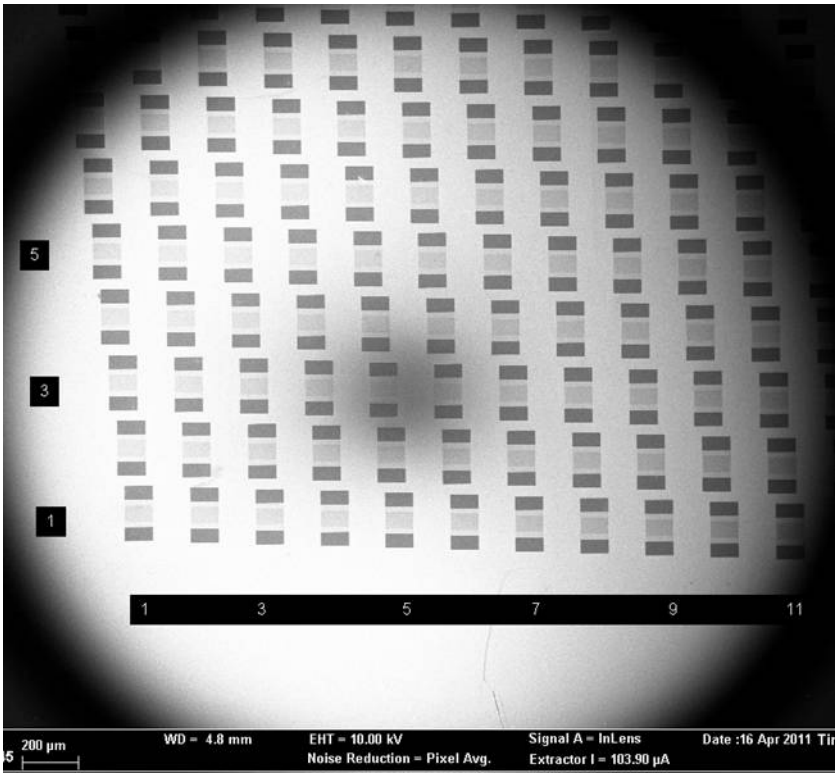

Figure 4.6 – SEM wide image of repeated pattern of 10-by-10 base devices on a single substrate. Note the drift in the position of devices, due to thermal drift in the SEM stage coordinates during the long (≈ 16 hours) exposure process

The main drawback of the wire-on-metal technique is the low efficiency: large areas of the as-grown sample got damaged, as few nanowires drop in the right position across the interdigit. Next Figure 4.7 shows the device consisting of a nanowire dropped across the interdigit. (NW casting techniques are detailed in a following paragraph.)

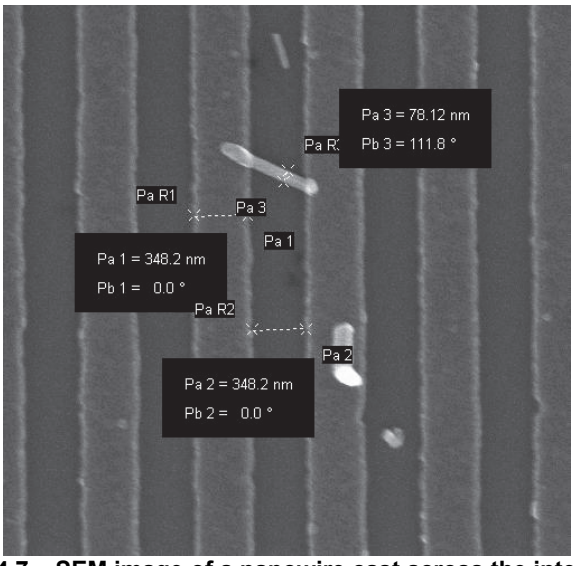

Figure 4.7 – SEM image of a nanowire cast across the interdigit

EBL fabrication parameters are closely correlated to one another, in such a way that fabrication fails unless the right combination is used. In the following Figures, some EBL fabrication issues are shown. For instance, excessive area dose caused the interdigit width widening (Figure 4.8); poor adhesion of metal causes damage after lift-off (Figure 4.9); insufficient area dose led to too thin electrodes (Figure 4.10); and excessive e-beam acceleration induced charge buildup in the substrate, causing the deflection of the beam, and altering the shape of the exposed pattern (Figure 4.11).

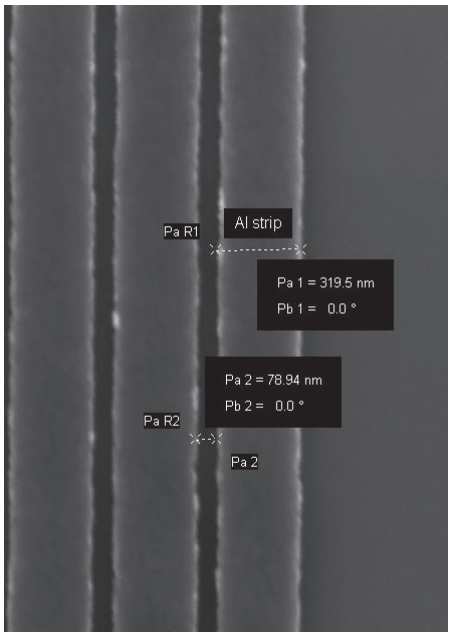

Figure 4.8 – Dose too high

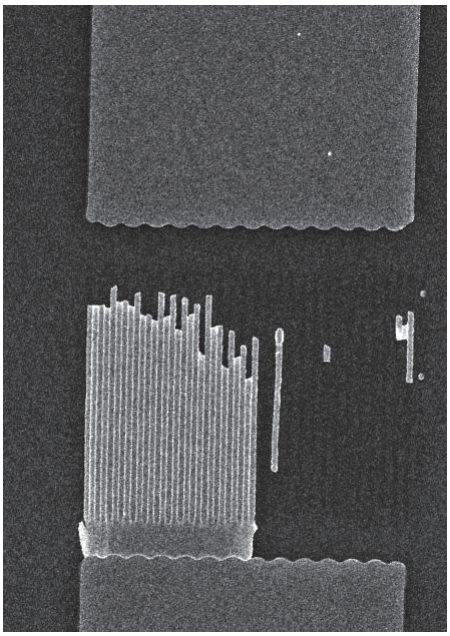

Figure 4.9 – Poor metal adhesion

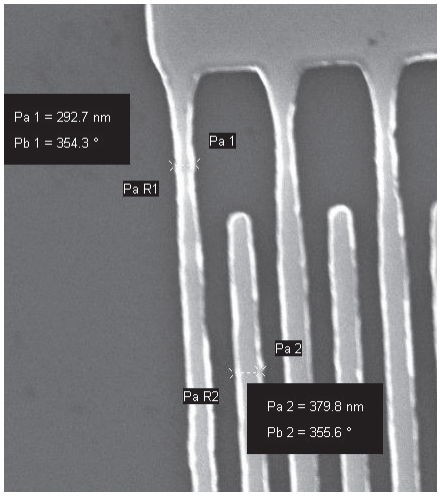

Figure 4.10 – Dose too low

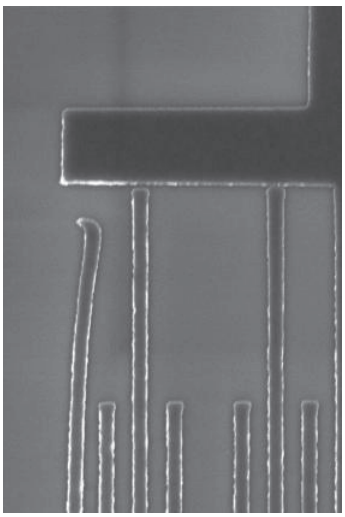

Figure 4.11 – EHT too high

Metal-on-wire

In this technique, the metal interdigit was fabricated on top of the nanowire, instead of casting the nanowire on top of the metal pattern. The preparation of the sample required the nanowires to be spread on top of the clean SiO_2 surface beforehand. EBL process was similar to that of the wire-on-metal method (detailed in the previous paragraph), and is based on positive resist PMMA as well. The fabrication steps are here summarized (see Figure 4.12):

- Substrate cleaning in acetone (ACE) and isopropyl alcohol (IPA)
- Substrate pre-bake at 90 °C, for 1 minute
- Nanowire cast/drop
- [optional: SEM inspection]
- PMMA spin coating at 4000 revolutions per minute (rpm), 30 seconds
- Substrate post-bake at 180 °C, ≈ 2 minutes
- EBL exposure:
  - 10 keV beam acceleration
  - 30 µm aperture Ø for large areas, 7.5 µm Ø for small areas
  - Dwell time ≈ 1E-5 s per step
  - Magnification 500x, working distance 4 to 5 mm
  - Dose 100 to 160 µC/cm^2
- Development, 30 seconds in MIBK:IPA 1:3 solution, with stirring
- Evaporation of metal
- Lift-off in stirring hot acetone (40 °C) and/or ultrasonic acetone bath, as needed
- Sample cleaning in IPA

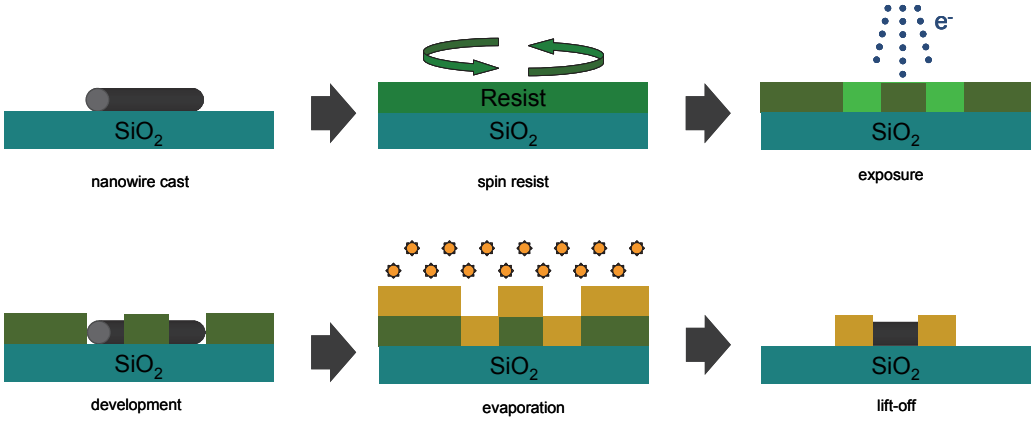

Figure 4.12 – Main processing steps in metal-on-wire

Contrarily to the former process, here curing of the PMMA layer was carried out for a much shorter time (2 instead of 10-20 minutes) to prevent contamination of the nanowire by the polymer.

The soft mask used was slightly different than that used in wire-on-metal technique. Here, pads were smaller, and the interdigit area was widened throughout all the pad length to maximize the chance to catch nanowires.

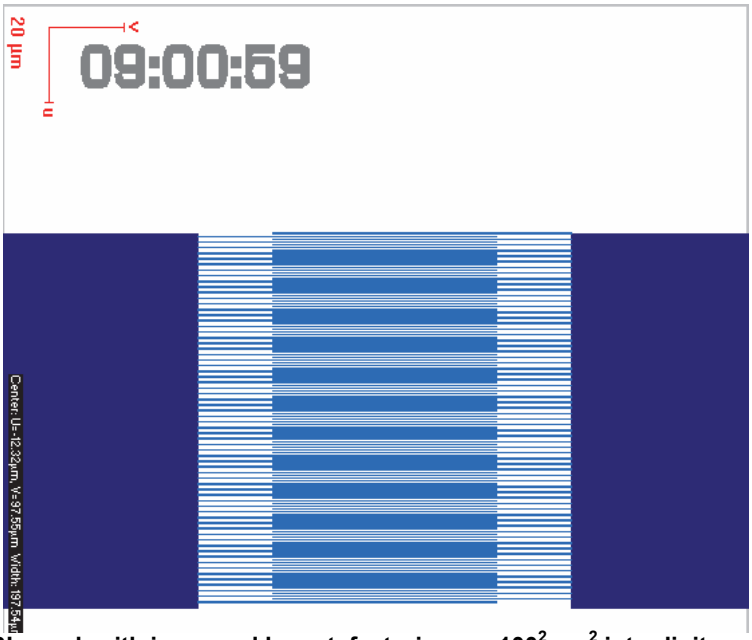

Figure 4.13 – EBL mask with improved layout, featuring a ≈ 100^2 µm^2 interdigit area, and smaller pads to reduce exposure time; the current time in the upper left corner is exposed on the resist for device recognition

At least 25 masks were exposed on each sample to maximize yield. Several wires could be contacted in this process as detected by scanning electron microscopy in the following Figure 4.14.

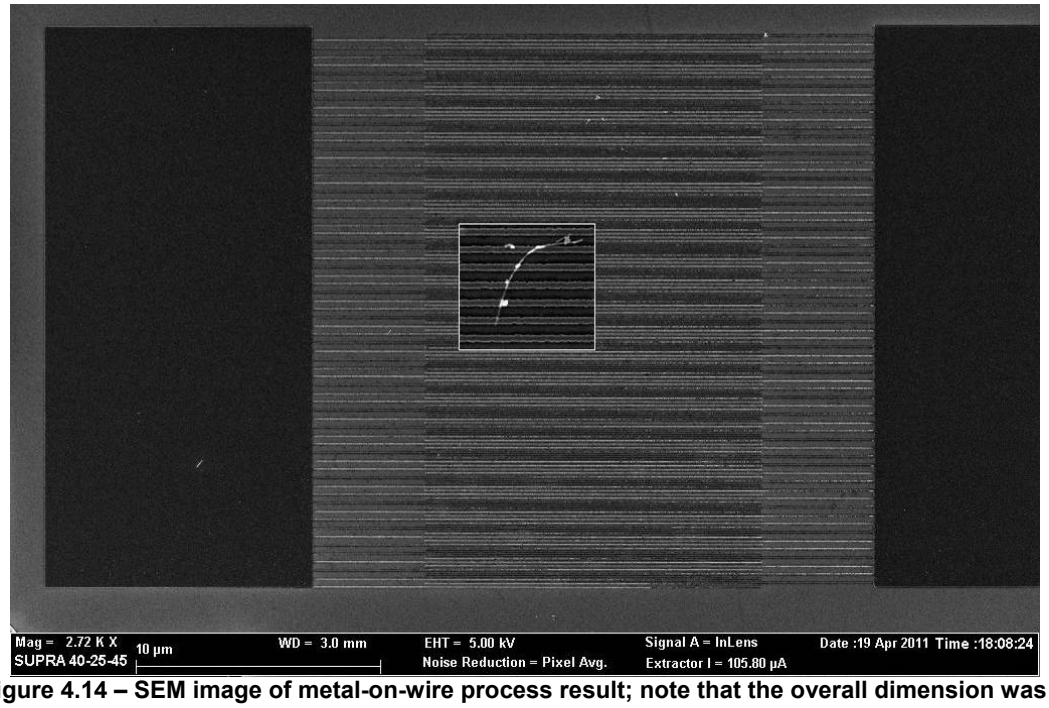

Figure 4.14 – SEM image of metal-on-wire process result; note that the overall dimension was scaled with respect to the EBL mask

A very high amount of nanowires were caught in the interdigit by this technique, mostly owing to the high density of the cast nanowires and to the larger interdigit area (20 x 20 µm).

However, all devices fabricated by this technique turned out to be defective from the electrical measurement. The reason might be the poor electrical contact between the nanowire and the metallization, which might contain remains of PMMA. To improve the electrical contact and to dissolve the residues, rapid thermal annealing (RTP) in forming gas ($Ar:N_2$) was attempted without success.

Nanowire electrode fabrication by EBL, negative resist

AR-N 7500 is a commercially available negative resist composed of novolak resins, bisazides, acid generators, and amine components + methoxy propyl acetate as solvent. AR-N was employed to fabricate an ordered array of gold nanoparticles for the VLS catalysis (see Chapter 3) and achieve an ordered position and geometry of the nanowires. In negative resist processing, areas exposed to e-beam become less soluble and impervious to the developer, while non exposed areas are removed during development. Moreover, a metal etching is employed instead of lift-off, as detailed in the processing steps (depicted in Figure 4.15):

- Substrate cleaning in acetone (ACE) and isopropyl alcohol (IPA)
- Evaporation of gold (1 to 10 nm thickness)
- Substrate cleaning in acetone (ACE) and isopropyl alcohol (IPA)
- Substrate pre-bake at 90 °C, for 1 minute
- AR-N 7500.08, 20 µl spin coating at 4000 revolutions per minute (rpm), 30 seconds
- Substrate post-bake at 90 °C, 1 minute
- EBL exposure:
    - 10 keV beam acceleration
    - 30 µm aperture Ø for large areas, 7.5 µm for small areas
    - Dwell time ≈ 1E-5 s per step
    - Beam speed ≈ 5 mm/s
    - Dose 160 to 180 µC/cm^2
- Development, 60 seconds in developer IPA 3:1 solution, with stirring
- Wet etching of gold by $KI:I_2$ solution
- Resist removal in acetone

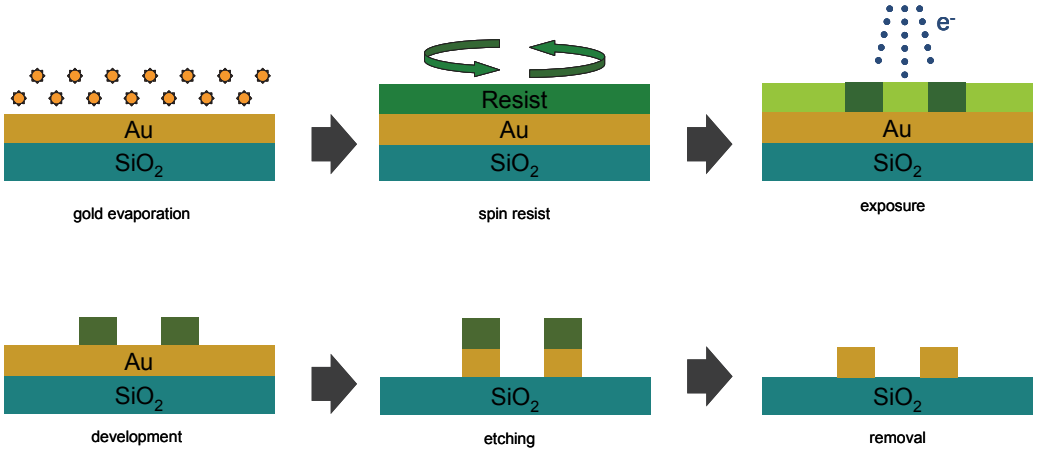

Figure 4.15 – Main fabrication steps in negative resist based processing

Starting from a SiO2 substrate, a gold film was first deposited. Thickness had to be as low as possible (few nanometers), for the gold nano-islands to coalesce. Any noble metal could be used as catalysts (see previous Chapter); gold was chosen for reasons discussed below. After EBL, unexposed resist was developed and only nano-islands were left. These nano-islands were used to protect the underlying metal during the etching of the metal. Finally, the surface was left with resist-capped gold nanoislands; the remaining resist was cleaned in acetone.

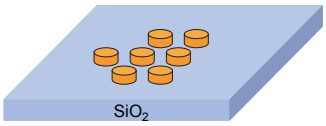

Figure 4.16 – Schematic picture of ordered nanopattern

The following problems prevented the successful outcome of this process.

First, the choice of the metal was dictated by etching issues. As a matter of fact, a noble metal is required as a catalyst for the VLS reaction. However, platinum is impervious to all chemical attacks; whereas few wet etchants exist for gold. A potassium iodide ($KI:I_2$) solution was employed because of its etching selectivity to Au, but not to the underlying SiO_2 or Si substrate. Pure potassium iodide has a 1 µm/min etch rate, thus requiring throughout dilution (1:50) in order to etch the thin gold film (1-2 nm) without overetching below the resist islands. However, the etching process was nor robust nor reproducible.

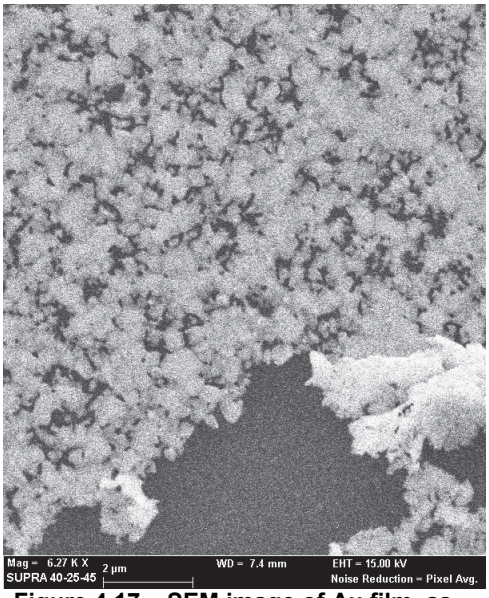

Figure 4.17 – SEM image of Au film, as deposited

Second, gold has a poor adhesion on SiO_2 substrate (see Figure 4.17), which leads to its peeling upon development. While chromium might be used as adhesion layer, this is not compatible to the VLS growth process.

Finally, calibration of the EBL dose for exposure of nanoislands of the required diameter (10 to 30 nm) by means of the AR-N resist, was hindered by the poor sensitivity this resist exhibits at this scale.

For the above mentioned reasons, the fabrication by negative resist was abandoned.

Device preparation by FIB

Several of the devices characterized in this work were prepared by focused ion beam, exploiting the versatility of use of this tool.

Samples were prepared in three different facilities: 1) S3 Istituto Nanoscienze (CNR), Modena (Italy); 2) Micron Technology, Italy, Agrate Brianza (Italy); 3) Laboratory for Research on the Structure of Matter, University of Pennsylvania, Philadelphia (USA). All of these facilities employed the same tool, FEI Strata™ DB235 Dual Focused Ion/Electron Beam (FIB). As far as possible, the instruments were operated according to the same parameters, so as to obtain comparable results:

- e-beam acceleration: 30 keV
- i-beam acceleration: 30 keV
- i-beam aperture: 30 µm Ø for fine areas, 300 µm Ø for coarse areas
- chamber pressure: 10^{-6} mbar or better

For what concerns the geometry of Pt electrodes deposition, the following constraints had to be taken into account when employing FIB:

- Electrodes not too long → excessive resistance
- Electrodes not too wide → excessive deposition time
- Electrodes not too narrow → excessive resistance
- Large pads not manufacturable → excessive deposition time

For these reasons, Pt electrode geometry had to be chosen as a tradeoff between minimization of electrode resistance and reduction of deposition time to reasonable timescales. To meet these requirements, additional sample preparation was required prior to FIB deposition, namely large pads and one or more large interdigits. Despite optical

lithography would have sufficed for this task, e-beam lithography was employed for the sake of simplicity. Basically, the same EBL mask was used to produce the couple of millimetric-sized 'branched pads', deprived of the interdigit area (Figure 4.18).

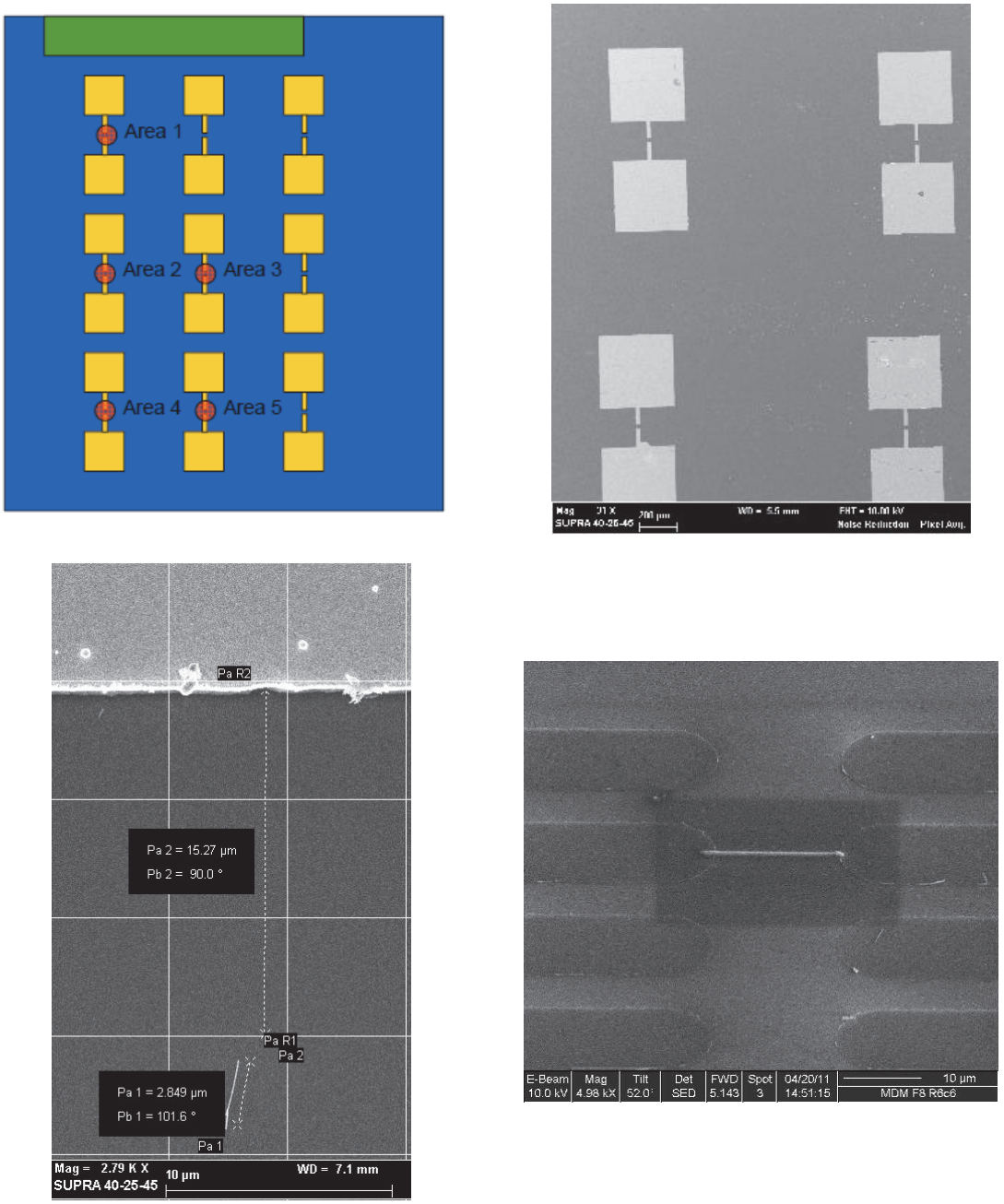

Figure 4.18 – Sample preparation prior to FIB deposition. Top left: EBL mask for large area structures; top right: pre-patterned metal structure fabricated by EBL + lift off; bottom left: nanowire cast and localization; bottom right: bridge test structure

Afterward, the nanowires were cast on the sample, their location was marked, and FIB processing was carried out to electrically connect the nanowires to the existing structures. In addition, some bridge structures were fabricated for verifying the Pt strip characteristics as electrodes.

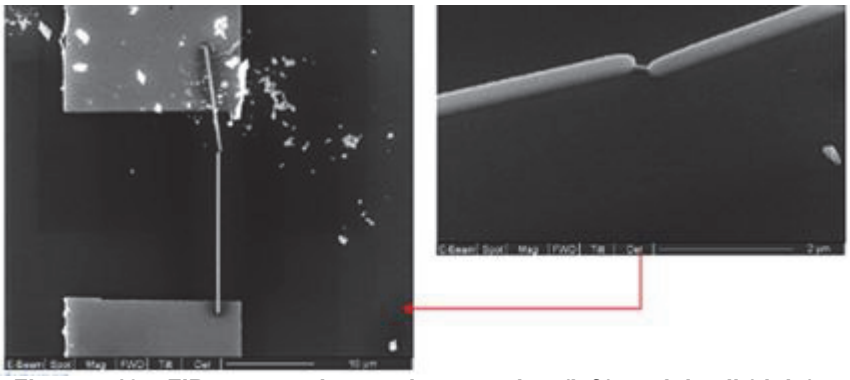

Figure 4.19 – FIB contacted nanowire: overview (left), and detail (right)

Bearing in mind the properties of FIB-deposited platinum (discussed in Chapter 3), i-beam induced deposition is to be preferred to e-beam deposition, owing to its lower resistivity. However, the high momentum of the ion beam caused the displacement of some nanowires during fabrication of the electrodes. To prevent that, e-beam was occasionally employed to stick the nanowire to the substrate beforehand. Subsequently, a strip of i-beam deposited platinum (i-Pt) was laid over the e-beam deposited platinum (e-Pt) to improve conductivity.

In addition, some platinum strips (called bridges) were deposited just across the macroscopic electrodes (Figure 4.18, bottom right). Then, the bridge geometry was assessed by SEM, its resistance was measured electrically, and the resulting resistivity calculated. When the nanowire resistance is comparable to, or lower than the electrode resistance, knowledge of the latter is mandatory to find out the former. This holds especially true for crystalline chalcogenide nanowires, having low resistivity (≤ 10 mΩcm), comparable to that of i-Pt (4.5 mΩcm).

Nanowires of various lengths were contacted and measured. By ruling out the contribution of the electrode resistance, and by knowing the nanowire geometry, it was possible to calculate the intrinsic nanowire resistance, its actual resistivity, and the value of the contact resistance, as shown in the following Chapter 6.

The main causes of failure of FIB-fabricated devices were: nanowire displacement due to i-beam, nanowire contamination by Ga atoms, too high Pt resistance, too thin Pt electrodes. The following Figure 4.20 illustrate some features of the fabrication in progress, and after completion.

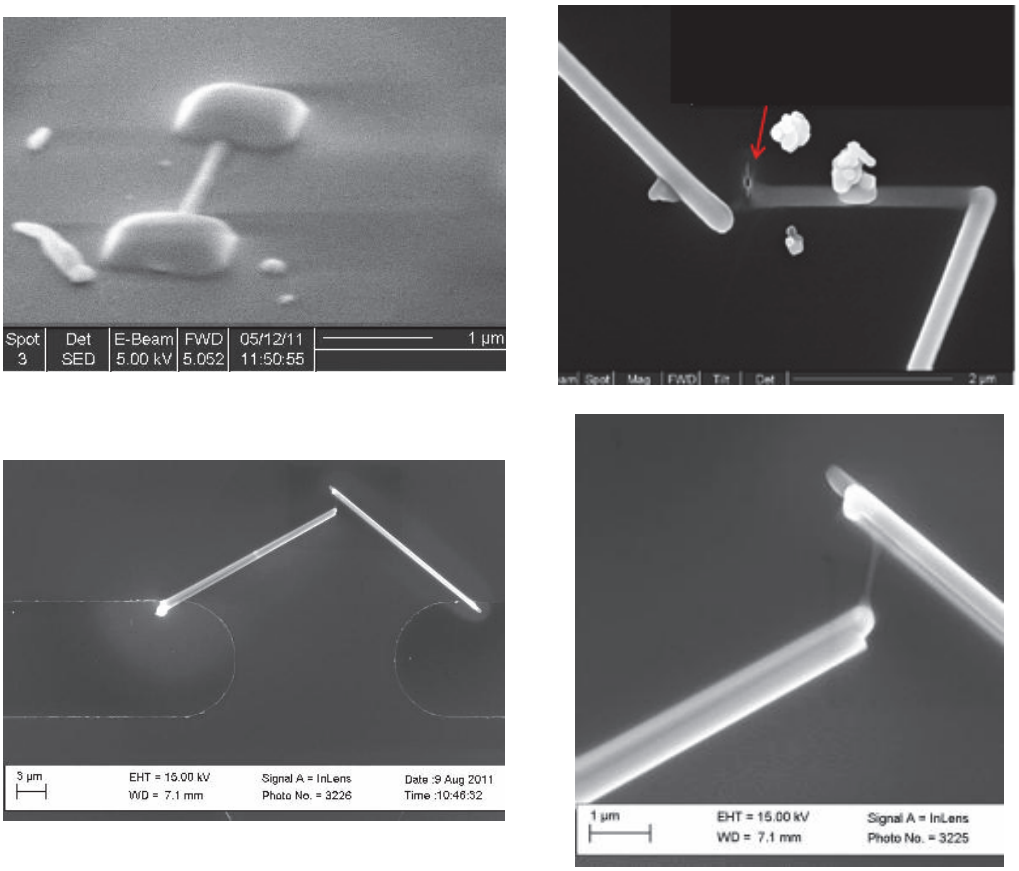

Figure 4.20 – SEM images of FIB fabrication: nanowire 'soldered' to the substrate (top left); overshoot during ion beam deposition (top right); overview of metal electrodes connections to the large pads (bottom left); detail thereof (bottom right)

Nanowire manipulation

Nanowire transfer from the as grown sample to the clean SiO_2 substrate was prerequisite to the processing discussed in the previous paragraphs. Transfer was carried out by either mechanical rubbing or suspension drop.

The most straightforward method required just rubbing the as-grown sample and the target sample surfaces together. The amount of transferred nanowires was roughly proportional to the applied pressure. As shown in the as grown sample picture (Figure 4.21), both crystals and wires were present. According to empirical observation, the adhesion of nanowires on the as grown sample surface was lower than that of crystals – i.e. the former were more easily transferred than the latter – as a consequence of the smaller contact surface. Increasing the sheer force beyond a given level, only crystals were removed. Notably, once nanowires were removed from the as grown sample, they stuck to the flat SiO_2 substrate with much higher adhesion force, owing to the van der Waals electrostatic force acting on the large lateral surface contact area. As a result, stirring and cleaning in acetone/IPA was not sufficient to remove the nanowires cast on SiO_2.

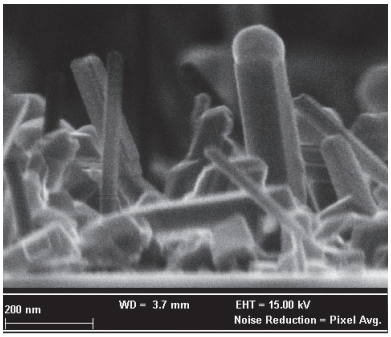

Figure 4.21 – As grown sample; note the presence of both wires and crystals

To improve the transfer ratio between nanowires/crystals to favor the former, another technique was attempted. The as grown sample was put in ultrasonic bath with 25 ml of

isopropyl alcohol (IPA), at 30 kHz frequency. Different sonication times were employed in order to evaluate the nanowire/crystal transfer ratio: 20, 60, and 300 seconds. Afterward, each suspension was dropped onto a clean SiO_2 substrate by using a micro liter pipette. The IPA was either left to dry up, or dried up by blowing nitrogen. Subsequently, samples were observed by SEM. It was found that the sample was contaminated with a large amount of micrometric-sized dust from the environment (which could be originating from the pipette, beaker, or IPA). Therefore, another pipette was used and equipped with a 250 nm pore diameter filter made of GH Polypro (hydrophilic polypropylene).

The resulting SEM images are shown in the following. Although the nanowire spreading was more controllable by using the suspension, a lot of crystals were still present after sonication. Even the lower sonication time was sufficient to remove the crystals from the as grown sample. Therefore, no significant improvement could be achieved by this technique.

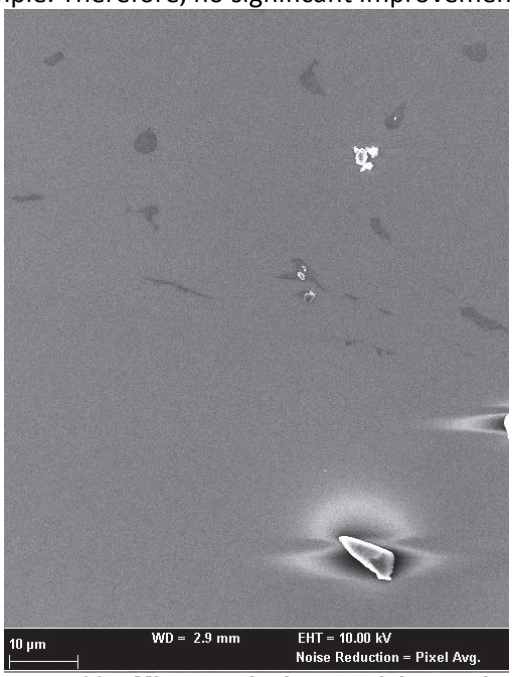

Figure 4.22 – Micrometric dust particles on the sample surface

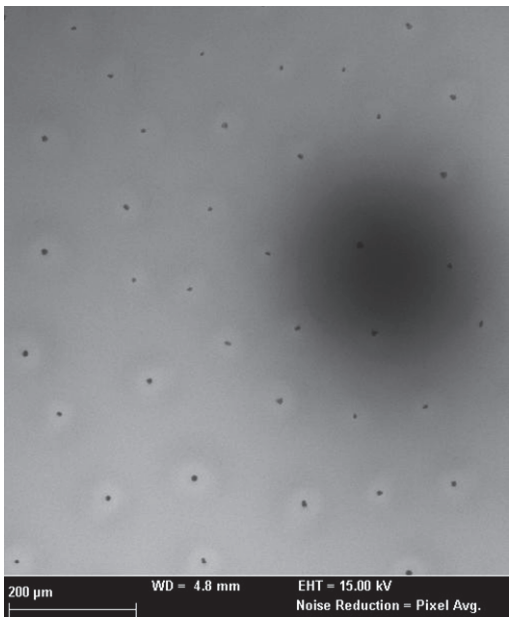

Figure 4.23 – The distribution of the nanowire cast is controllable by tuning the suspension

Pulsed I/V setup

"Nothing tends so much to the advancement of knowledge as the application of a new instrument"
Sir Humphrey Davy

In the previous Chapter 3, the advantages of, and the need for a pulsed I/V measurement setup over the conventional DC I/V were discussed. A dedicated electrical setup was therefore implemented to perform pulsed I/V measurement on nanowire devices (DUT), prepared as described in previous paragraphs.

Three instruments were employed in the setup: 1) a high sensitivity current sourcemeter unit (SMU) to measure the low-field resistance of the device, 2) a voltage pulse generator unit (PSU), and 3) an oscilloscope (OS) to measure the instantaneous current flow in the device. In addition, a computer-controlled matrix card (MUX) was designed and fabricated to switch the DUT terminals between the instruments during the I/V sweep.

The schematic of the electrical setup is shown in the following diagram (Figure 4.24). The Agilent B1500 “Semiconductor parameter analyzer” was a cluster of electrical instruments, comprising of both SMU and PSU. The pulse generator could supply voltage pulses as short as 10 ns (3.03 ns leading and trailing edges), in the range ± 10 V, so as to electrically induce the phase transition in chalcogenide nanowires. The oscilloscope was an Agilent MSO6104,

featuring a high (4 Gb/s) sampling rate to detect the current during the voltage pulse. The MUX box handled the switching between instruments and DUT; it required a ± 15 V power supply. All of the tools shown were remotely controlled by a personal computer (not shown), by means of General Purpose Interface Bus (GPIB) wired connection. Dedicated EasyExpert and LabVIEW™ software was written to control the instruments and automate the measurement.

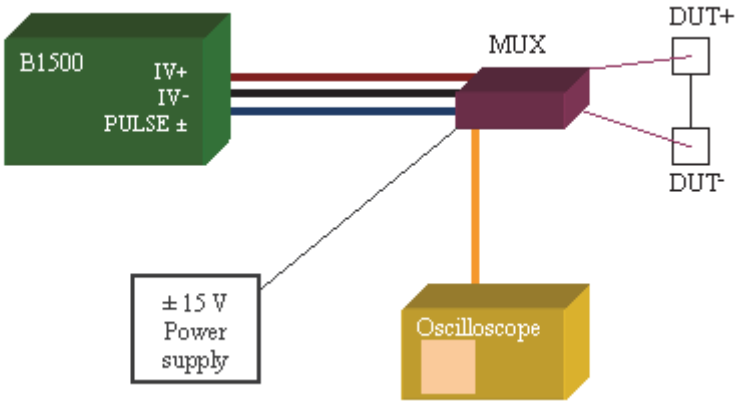

Figure 4.24 – Electrical setup for pulsed I/V measurement

The matrix card (MUX) schematic is shown in Figure 4.25 and described in the following. The core of the circuit is component U$1, the analog multiplexer ADG409. Signal inputs (outputs) X0, X1, X2, and X3 (Y0, Y1, Y2, and Y3) are selectively routed to output X (Y), according to the binary encoding on address bits A0 (A1) indicated by orange LED 1 (2). The internal switches are solid state transmission gates (i.e. paired n- and p- MOSFET). The multiplexer is a break-before-make type. When input EN is low, all switches are opened. For improved operation of the switches (i.e., to minimize the transmission gate resistance in the ON state), full rail double-sided power supply is used (± 15 V). Manual switch S1 controls EN bit and its value is displayed by green Led 3. R1 is a 50 Ω terminator resistor to match the RG58 cable impedance on the Pulse Generator side. All external signals are to be routed by BNC coaxial cables. Bits A0 and A1 of the multiplexer are controlled by either manual switches or digital (TTL-compatible) signals on a DB9 serial port or on a 10-conductors flat cable (ports X2-1...X2-10 and X3-1...X3-9). Resistors R8 and R9 are employed to ground the DUT in a safe state, if needed.

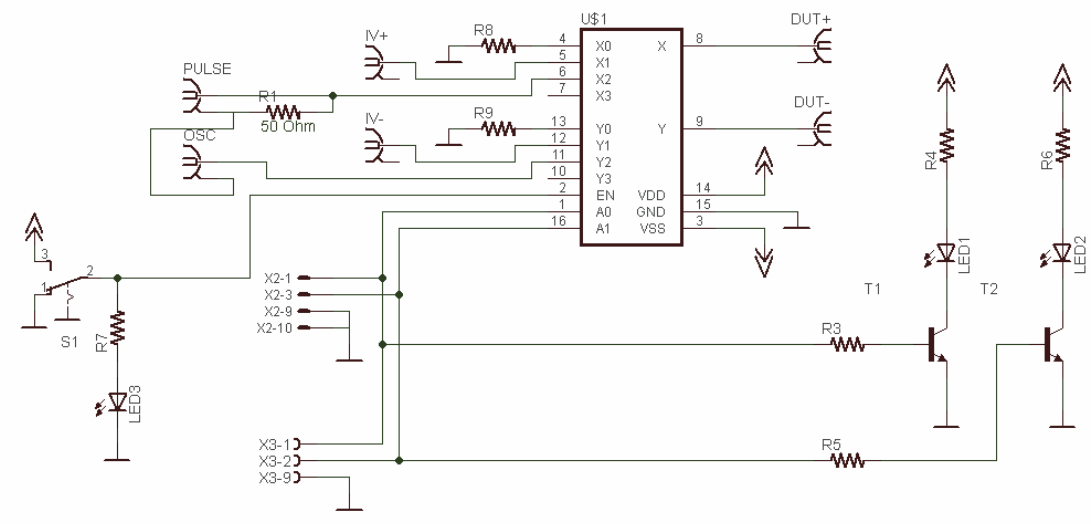

Figure 4.25 – Multiplexer matrix schematic

It has to be noted that the oscilloscope is routed in series to the DUT; its internal resistance is to be set to 50 Ω, so as to convert the current flowing in the device into a voltage.

The truth table and routing for this multiplexing card is shown in the following Table 4.2:

A0 (Pin 1)	A1 (Pin 2 or 3)	Decimal value	EN	Routing	Function
X	X	X	0	-	open circuit
0	0	0	1	X=X0, Y=Y0	grounded thru 1 MΩ
1	0	1	1	X=X1, Y=Y1	I/V mode
0	1	2	1	X=X2, Y=Y2	Pulse mode
1	1	3	1	X=X3, Y=Y3	not used

Table 4.2 – MUX routing table

Contrarily to DC signals, nanosecond timescale signals require careful routing. Let us consider a typical voltage pulse of: 1 V, 300 ns width. Pulsing such short signals implies that the rising and falling edges thereof are ≈ 1/10 of the whole signal duration. As a result, pulse edges range in the 3 to 30 ns timescale, i.e. a slope of 33,333,333 – 333,333,333 V/s. In this regime, the conventional coaxial cable (BNC) behaves like a transmission line, hence the signal is transmitted or reflected whenever an impedance mismatch occurs. The equivalent circuit is depicted in Figure 4.26.

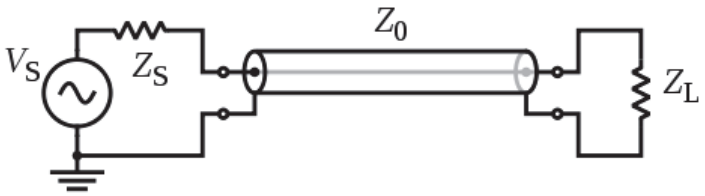

Figure 4.26 – Transmission line schematic[5]

The mismatch of the source (Z_S), cable (Z_0), and load (Z_L) impedances plays a role in the way the signal propagates. As occurs in RF signals, the transmission and reflection coefficients at the Z_0/Z_L boundary are, respectively:

$$T = \frac{2Z_L}{Z_L + Z_0}; \quad \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad (4.1); (4.2)$$

Signal reflection has a detrimental effect because it: 1) diminishes the actual energy supplied to the load, 2) alters the shape of the pulse, and 3) causes part of the reflected signal to return to the voltage generator, which must be able to withstand it. According to eq. 4.2, it is clear that reflection can be zeroed by setting $Z_L=Z_0$ (also known as impedance matching).

Because the cable characteristic impedance is set to 50 Ω (for the coaxial RG58 cables in use) and the source impedance Z_S is set to 50 Ω in the pulse generator unit, only the load impedance Z_L was to be tuned to this value. As a matter of fact, the DUT resistance was not likely to be equal to 50 Ω; moreover, its value changed upon phase change. For these reasons, resistor R1 in the MUX was placed in parallel to Z_L, thus acting as terminator to the incoming pulse signal (the parallel was negligible, being Z_L >> 50 Ω). The equivalent circuit is schematically shown in the following Figure 4.27.

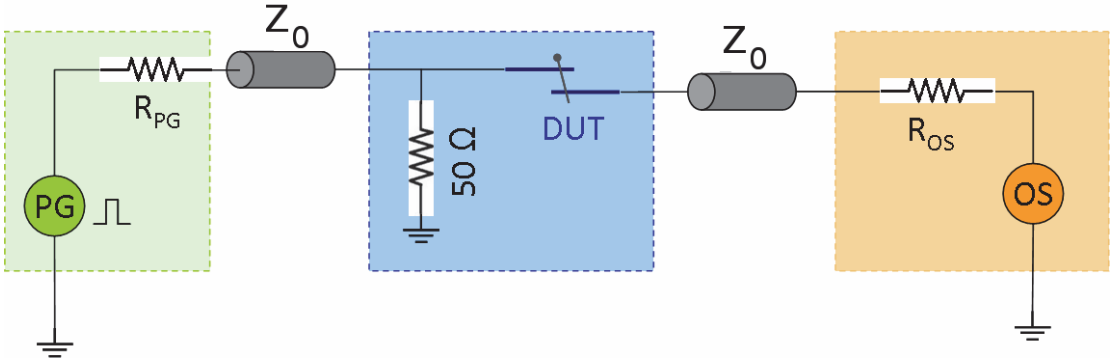

Figure 4.27 – Electrical circuit of the setup comprising the pulse generator (PG), device under test (DUT), oscilloscope (OS), and the line (Z_0), pulse generator (R_{PG}), and oscilloscope (R_{OS}) characteristic impedances

Note that the oscilloscope (OS), which was employed for the current readout, was connected in series to the DUT, and its internal impedance was set to 50 Ω so as to exploit it as a terminator for this other branch of the circuit. Omitting to do so would cause the voltage pulse (300 ns, 1 V) to be reflected at the impedance interface, and the resulting waveform to look as in Figure 4.28, i.e. the first derivative of the pulse.

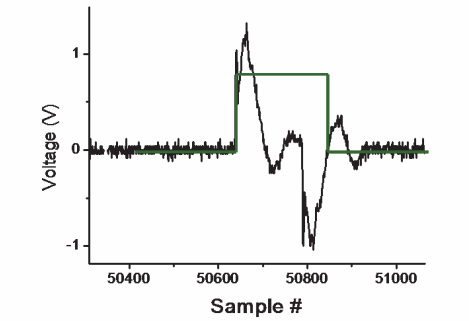

Figure 4.28 – Oscilloscope trace of the supplied voltage pulse (green line), and measured voltage pulse (black line) when impedance mismatch occurs

Finally, it is worth noticing that the DUT resistance (in Figure 4.27) actually consisted of several terms, which accounted for the leads and interfacial resistances, as schematized in Figure 4.29:

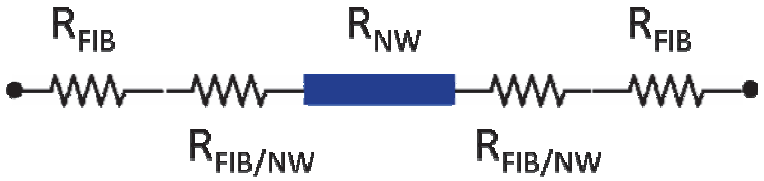

Figure 4.29 – Detailed view of the resistances comprising the DUT

where R_{FIB} was the resistance of the FIB-deposited Pt leads, R_{NW} was the intrinsic resistance of the nanowires, and $R_{FIB/NW}$ was the contact resistance between the former and the latter. This clarification is needed to calculate the actual resistance of the nanowire device by ruling out the effect of the parasitic resistances as will be discussed in Chapter 6.

Hall effect setup at low temperatures

The Hall effect setup comprises the following equipment: electromagnet with variable pole width, teslameter probe, temperature controller, “hall/van-der-Pauw” matrix box, closed-circuit He cryostat and turbomolecular pump. Magnetic field can be set as high as 1.1 T (room temperature configuration) or 0.8 T (low temperature configuration). The pumping system guarantees a chamber pressure of at least 1E-5 mbar, or lower. Samples can be cooled down to ≈ 4 K by employing the closed-circuit He compressor. In addition to the above mentioned instruments, the setup is equipped with a current source, a nanovoltmeter and an electrometer for the measurement of thin films and devices in a wide resistivity range.

The sample holder features four probes that can be placed on the sample edges, according to the van der Pauw configuration (2 probes for current, 2 probes for voltage). In this regard, the hall/vdP matrix box was a home-made tool that was fabricated, within the scope of this work, to perform Hall effect measurements, featuring automatic switching between the two probe configurations: resistivity and Hall effect, as illustrated in the following Figure 4.30.

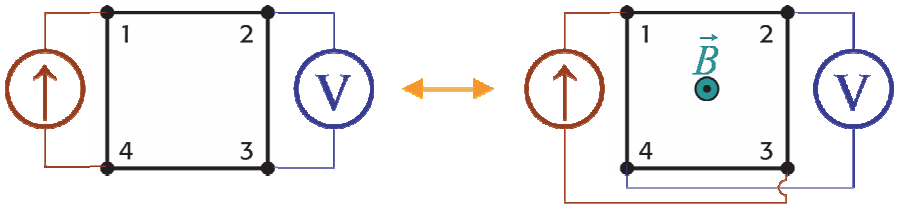

Figure 4.30 – van der Pauw probe configurations for resistivity (left) and Hall effect (right)

Both configurations required 4 probes; the first was used to measure resistivity (ρ), the second to measure charge carrier density (CD). As the measurement of carrier mobility requires both ρ and CD to be known, at the given temperature, the matrix made it possible the simultaneous measurement of Hall effect at any given temperature.

Electro-thermal analysis model geometry

COMSOL Multiphysics suite was used to realize a test model with the same geometry and boundary conditions of a single nanowire contacted by FIB, to the end of evaluating the transient temperature variation during set and reset operation. Because the (nanowire + electrode) geometry lacks any symmetry, it could not be straightforwardly described by 1 or 2 dimensional models. Therefore, a fully 3-dimensional layout had to be designed, and is shown in the following Figure.

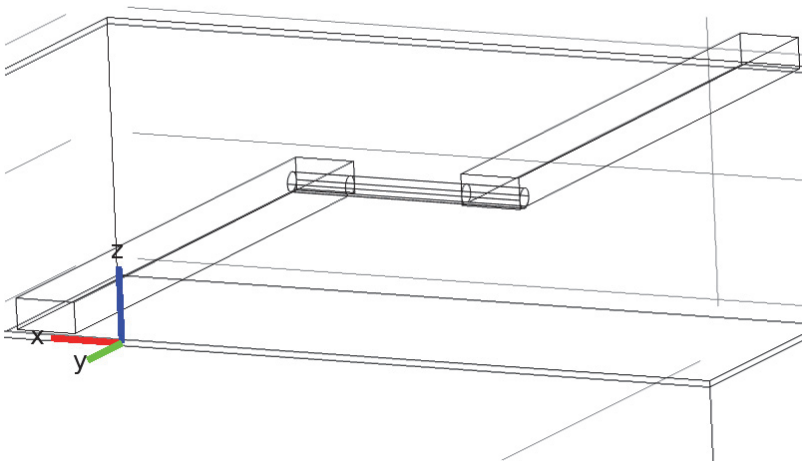

Figure 4.31 – Wireframe view of the finite elements model

In this model, a 80 nm thick, 1 µm long nanowire was drawn. The electrodes cross section was set comparable to that of an actual device; their length was a factor of 3 shorter than the real electrodes to limit the model computational complexity. The geometric dimensions of the above layout are summarized in the following Table.

Dimension	Symbol	Value [unit]
Nanowire diameter	$Ø_{NW}$	80 nm
Nanowire length	l_{NW}	1 µm
SiO_2 thickness	t_{SiO2}	50 nm
Si thickness	t_{Si}	500 µm
Pt electrode thickness	t_{Pt}	250 nm
Pt electrode breadth	w_{Pt}	500 nm
Pt electrode length	l_{Pt}	5+5 µm
Model area	A	$(10\ \mu m)^2$
Ambient pressure	P	0 bar
Excitation voltage	V_1	3 V
Initial temperature	T_i	293.15 K

Table 4.3 – Physical constraints of the model

For the sake of simplicity, it was chosen to mesh the model by using finite elements of tetrahedral shape only. The size of the elements was proportional to the volume of the domains, denser along the regions of high current/heat flux density. The resulting meshed layout is shown in the following.

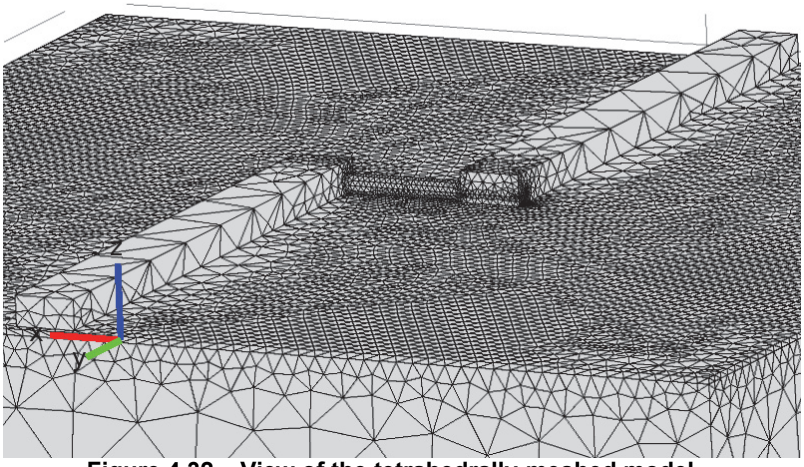

Figure 4.32 – View of the tetrahedrally-meshed model

Note that the finite elements resolution is higher in the nanowire region, and coarse elsewhere (especially the substrate). The whole model consisted of 131323 finite elements. Limiting the model size to 100 μm^2 was mandatory in order to reduce the computation time. For instance, the computational time for full modeling of this – relatively small – model was roughly 140 s.

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[5] Wikipedia [internet], available from: "http://commons.wikimedia.org/wiki/File:Transmission_line_schematic.svg"

5. Chalcogenide thin films

Introduction

This Chapter focuses on the characterization of thin films of binary and ternary chalcogenides. The study of thin films is the only way to determine those intrinsic properties of chalcogenide materials, which cannot be extracted from 1-dimensional devices. To this aim, the resistivity measurement and the Hall effect in the van der Pauw geometry were employed to calculate resistivity, carrier density, and mobility as a function of temperature. As will be shown in the following, films of thickness ≥ 40 nm can still be considered bulk-like from the physical point of view, and the semi-classic interpretation can be employed.

In addition, thin film technology is the mainstream manufacturing process for electronic devices to date. It is thought that this technology will be employed until implementation of 1-dimensional nanostructures becomes convenient and dependable into the existing industrial process.

In Chapter 2, the binary and ternary compounds of tellurium belonging to the pseudobinary line GeTe–Sb_2Te_3 were presented as the most promising for phase change memory application because they deliver the best, tunable combination of switching speed, resistivity values, and phase stability. GeTe is found in the amorphous, rhombohedral (trigonal), and face centered cubic (fcc) phases while the ternary GeSbTe system can be found in the amorphous, face centered cubic (fcc, metastable), and hexagonal close packed (hcp, stable) phases.

Resistivity of GeSbTe thin films

Several thin film of the GeSbTe ternary compound, with different composition, deposited by PVD (sputtering), were investigated at low temperature for resistivity and Hall properties. In what follows, the results for one of these alloys in the two crystalline phases (fcc and hcp), prototypical of the behavior of most chalcogenides, are presented.

Several identical samples were deposited in the amorphous phase (PVD samples provided by Micron Technologies, Inc.). Then, all the samples were thermally annealed at constant heating rate of 10 °C/min, up to a maximum temperature of 200, 212, 225, 250, 300, 325, 350, 375, 400, and 500 °C. Because the quenching rate was much higher (> -30 °C/min) than the heating rate, it can be assumed that the sample phase was 'frozen' upon cooling and no further phase transformation had occurred. As a result, each sample achieved a different crystallization stage. The film resistivity (ρ) thereof was tracked *in situ* during the experiment and the cumulative results are cumulatively shown in the following Figure 5.1.

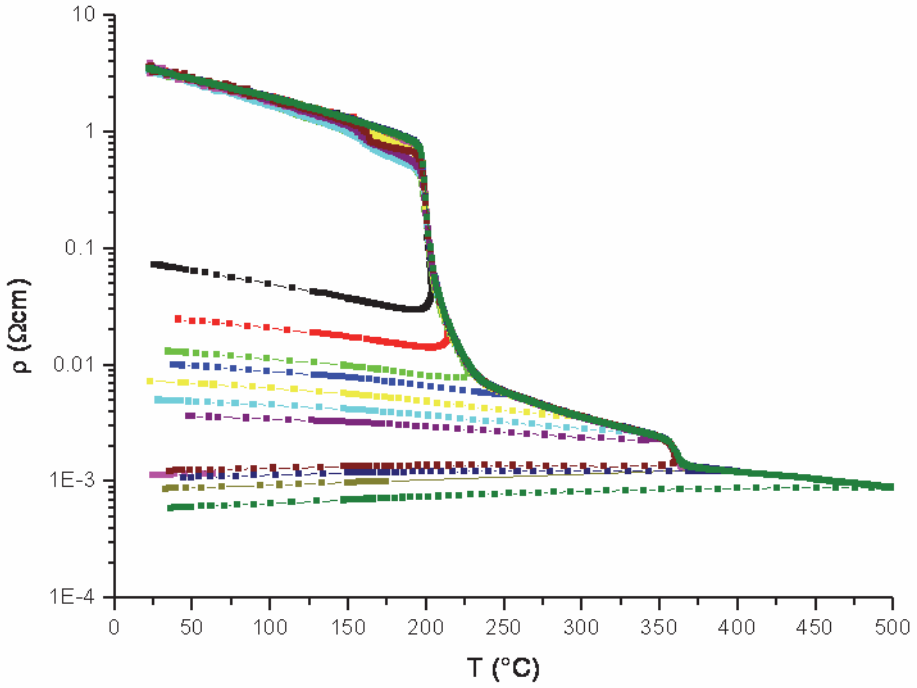

Figure 5.1 – Resistivity (ρ) as a function of temperature (T) of a GeSbTe alloy, as measured by constant heating rate experiments; initial ρ ≈ 4 Ωcm for all samples

According to the above Figure, all plots resulted superimposed within the given temperature range, thus indicating that the temperature precision was very high (i.e., smaller that the symbol size in the plot). The plots exhibit two marked dips, which testify to the transition of the material from amorphous to fcc (at ≈ 200 °C) and to hcp (at ≈ 350 °C) phases. Note that the largest resistivity drop occurred for the amorphous to fcc transition (which is the transition normally employed in phase change memory devices).

The resistivity (ρ) of the quenching part of plot gives useful information on the electric conduction mechanism. Namely, two trends can be detected, according to the slope thereof:

- $d\rho/dT < 0$ when quenched from a temperature lower than 350 °C (semiconductor-like)
- $d\rho/dT > 0$ when quenched from a temperature higher than 350 °C (metal-like)

According to XRD investigation of the samples, these two behaviors originated as a result of the formation of two distinct crystalline phases after quenching: fcc in the former case, hcp in the latter.

By employing two different electrical setups, and by using the van der Pauw configuration described in Chapter 3, it was possible to determine the (post-annealing) film resistivity in the temperature range 4 to 773 K. Two samples, fcc and hcp, out of all the previous set were

chosen for the low temperature characterization. The resulting ρ(T) is shown in the following Figure 5.2, where the resistivity trend still holds valid down to cryogenic temperatures.

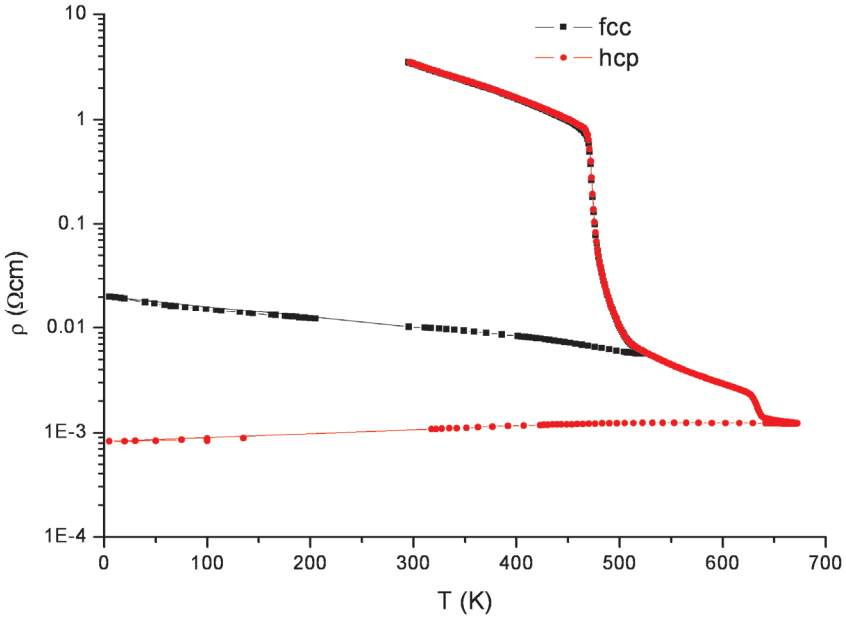

Figure 5.2 – Resistivity (ρ) as a function of temperature (T) of a GeSbTe alloy in the fcc (black) and hcp (red) phase. The black and red lines are a linear interpolation to the data

Hall effect of chalcogenide films grown by PVD

The electronic transport features of crystalline chalcogenides play a significant role in phase change memory devices, but are not yet fully understood. As mentioned in Chapter 2, it has been reported that all crystalline compounds lying along the pseudo-binary line $(GeTe)_n+(Sb_2Te_3)_m$ exhibit p-type conduction, regardless of composition (n,m), owing to: a) structural vacancies in the Ge (or Ge/Sb) sublattice, and b) substitutional Ge atoms on Te sites[1,2]. It has been proven that crystalline chalcogenides are narrow band gap solids, due to the *s-p* interaction among the *s* Ge and *p* Ge-Te bonding states[3]. However, significant differences exist between the crystalline phases, which have to be accounted for in the device design. For instance, while GeTe is thought to be always a degenerate semiconductor, GeSbTe is degenerate only when in the hcp phase, not in the fcc. Extensive studies have been carried out in this regard, both theoretically and experimentally[4,5,6].

In this paragraph, a qualitative interpretation of the electronic transport features of chalcogenide thin films is proposed, in light of the scattering mechanisms determined by Hall effect measurements from room temperature to liquid helium temperature (≈ 4 K). Two GeSbTe samples in the fcc and hcp phase, whose resistivity vs. temperature plot is shown in Figure 5.2, were measured by Hall effect from room temperature to 4 K. The resulting carrier density and mobility are shown, for fcc-GeSbTe, in Figure 5.3, respectively.

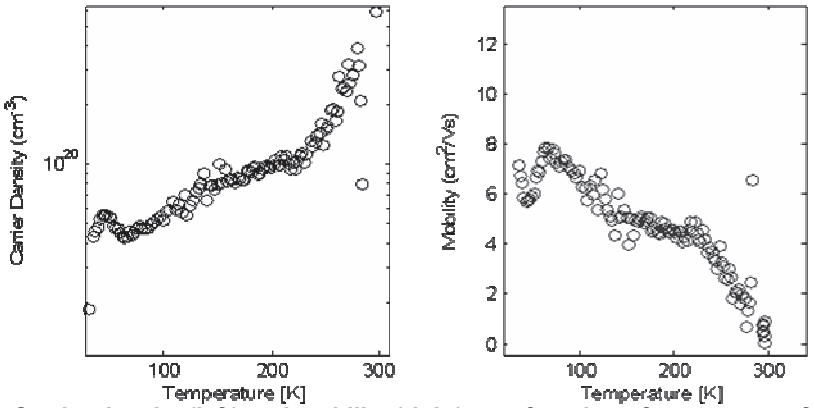

Figure 5.3 – Carrier density (left) and mobility (right) as a function of temperature for fcc-GeSbTe, thin film deposited by PVD

According to the Hall measurement, this ternary chalcogenide in the fcc phase has p-type conduction, and a remarkably high density of charge carriers of few 10^{20} cm^{-3}. Electric conduction in this phase has striking similarities to that of a conventional semiconductor: the slope of the resistivity vs. temperature plot is negative; density of carriers decreases at low temperature due to the freeze-out of carriers; mobility increases at lower temperature. Notable differences exist, however. The carrier density does not decrease with an exponential trend as charge carriers in chalcogenides are a consequence of the intrinsic vacancies in the Ge/Sb sub-lattice (hole conduction). As a result, the slope of CD(T) is not as steep as in a doped semiconductor; and the CD is still remarkably high, even at 4 K. The chalcogenide in the fcc phase can be thought of as an (almost) degenerate semiconductor, having the Fermi level close to the valence band. The high amount of charge makes the Fermi level substantially insensitive to variation in temperature, in such a way that the CD(T) barely changes over the wide temperature range under investigation.

For what concerns carriers mobility, this measurement is affected by a larger uncertainty, which is due to the combined uncertainties of the CD(T) and ρ(T) measurements. In Figure 5.3, right, the scattering of the dots indicate the uncertainty of the measurement (when more than one value is present at a given temperature). Otherwise, the uncertainty is as large as the dot size. At room temperature, carrier mobility is very low (≈ 1 cm^2/Vs), mainly because of the scattering with lattice and charged defects. Roughly two regimes can be detected at lower temperature: a) from 300 to 200 K, mobility increases linearly owing to the smaller scattering events occurring between charge carriers and lattice; b) below 200 K, mobility increases less markedly, and is almost pinned to ≈ 7 ± 1 cm^2/Vs. Note that the mobility saturation in region b seems to be a common feature of chalcogenides, which can be explained in terms of ionized impurity scattering only (as will be shown in the next paragraph).

Hall effect measurement of PVD-deposited GeSbTe in the hcp phase is shown in the following Figure 5.4.

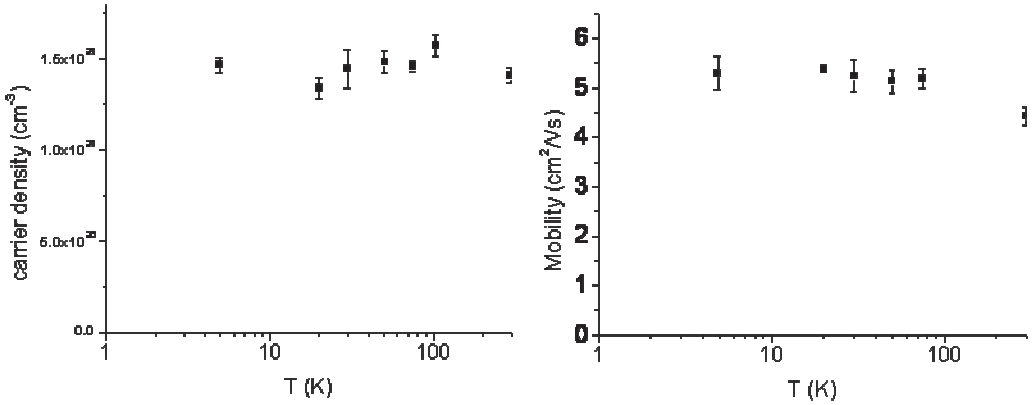

Figure 5.4 – Carrier density (left) and mobility (right) as a function of temperature for hcp-GeSbTe, thin film deposited by PVD

In the hcp phase, less data points could be recorded, but with smaller uncertainty owing to the use of a different instrumentation setup (available at that time). According to the plots, p type conduction is present, and carrier density is substantially unaffected by temperature. By recalling the positive ρ(T) slope, it can be stated that this chalcogenide in the hcp phase has a metallic behavior: the Fermi level lies within the valence band and is almost pinned by the large density of states; the carrier density thus being constant.

Notably, mobility in this phase lies from 4.5 to 5.5 cm^2/Vs, with little temperature dependence. Contrarily to the fcc lattice, conduction in hcp GeSbTe is favored along directions perpendicular to the c axis (i.e. in-plane with respect to the thin film surface just as it happened to occur during the measurement). As a result, mobility (and electrical conductivity as well) at room temperature is nearly one order of magnitude higher than in the fcc phase. At lower temperatures, mobility was expected to increase, with a T^{-1} slope as in a lattice-scattering-limited metal. However, it appears clear (Figure 5.4, right) that some kind of scattering mechanisms happened to limit the mobility of carriers to a constant value. As grain boundary scattering is negligible (presence of large grains was detected by XRD), and no geometrical effect is occurring, the dominating mechanism had to be the ionized impurity scattering (as in the fcc phase). This mechanism causes the low-temperature mobility to saturate to a value similar to that of the fcc phase. Moreover, in hcp phases the saturation mobility is lower than in fcc, as this value is proportional to the density of defects (higher in hcp)[7].

Notably, these considerations hold true for, and are prototypical of the behavior of GeSbTe compounds, as will be shown in the following paragraph.

Hall effect of chalcogenide films grown by CVD

GeTe (samples B, C) and GeSbTe (samples A, D, E, F, G) thin crystalline films were prepared by two CVD techniques: metalorganic chemical vapor deposition (MOCVD, samples A, B), and hot-wire, liquid injection MOCVD (HW-LI, samples C, D, E, F, G). Growth details were detailed elsewhere[8,9]. Films grown by MOCVD were thicker (200 nm) than those grown by the HW-LI (40 to 55 nm). Crystallographic phase and composition of the samples – which span over a wide variety as a result of the different growth conditions – were checked by X-ray diffraction (XRD) measurements. One of the samples (G) was grown by adding a nitrogen precursor; the resulting N content was high enough for the film to be considered an alloy, rather than a doped film. Samples description is summarized in the following Table.

Sample	Deposition	Symbol	Thickness	Composition	Phase
A MOGST73	MOCVD	■	200 nm	$Ge_2Sb_1Te_4$ + Te	hcp
B MOGT161	MOCVD	●	200 nm	$Ge_{0.60}Te_1$	trigonal
C VM628	HW-LI	▲	40 nm	$Ge_{0.66}Te_1$	trigonal
D VM724	HW-LI	▼	45 nm	$Ge_2Sb_2Te_5$	fcc + hcp
E VM731	HW-LI	◀	55 nm	$Ge_2Sb_2Te_5$	fcc
F VM733	HW-LI	♦	50 nm	$Ge_2Sb_2Te_5$	hcp
G VM817	HW-LI	▶	45 nm	$Ge_2Sb_2Te_5$ + N	hcp

Table 5.1 – Samples description (thin chalcogenide films)

Resistivity (ρ), carrier density (p), and carrier mobility (μ_h) of the thin films were recorded at once from room temperature to ≈ 5 K. The four probes configuration in the van der Pauw geometry was employed, as detailed in Chapter 3 and 4. In the resistivity graph, the error bar is assumed to be as large as the dot size, unless specified. In the carrier density and in the carrier mobility graph the error bars are ≈ 10% of the measured value and are mainly due to: a) the non-ideality of the van der Pauw technique (namely the non-zero size of probes), and b) the Johnson voltage noise which is comparable to the Hall voltage when the carrier density is > 10^{20} cm^{-3}. The charge carrier density p was calculated under the hypothesis of single carrier type (holes). This assumption holds true as long as the hole density is much larger than the electron density (which is valid at room temperature and even further at lower temperature). A ± 0.7 T magnetic field was employed in the Hall effect measurement and all samples reported a linear Hall voltage as a function of the magnetic field.

The measurement results are shown cumulatively in Figure 5.5 (top: resistivity, center: carrier density, bottom: carrier mobility).

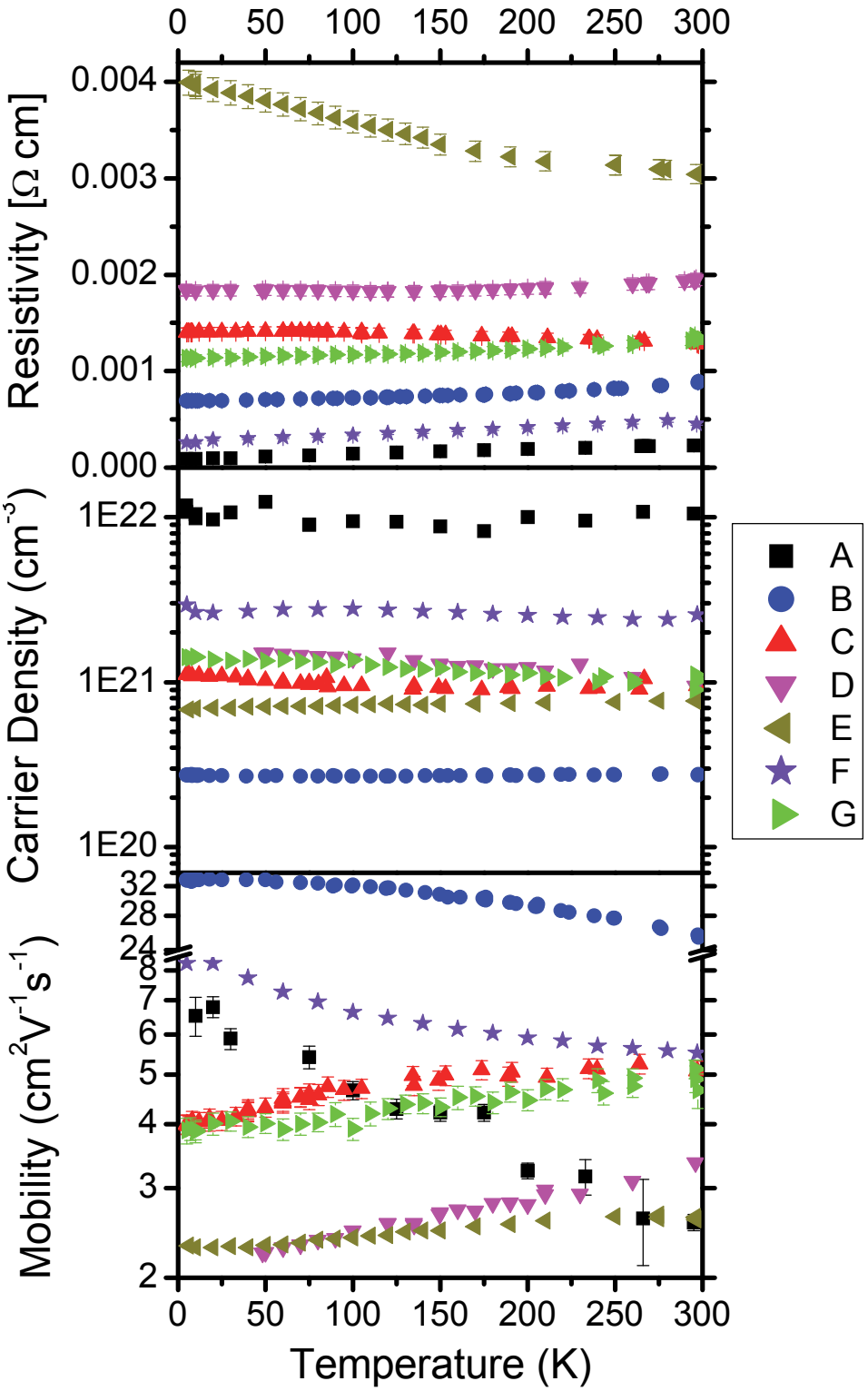

Figure 5.5 – Resistivity (top), carrier density (center), and carrier mobility (bottom) for 7 chalcogenide thin films of various stoichiometry

The resistivity plots reveal two distinct *ρ(T)* behaviors: semiconductor-like (samples C, E), and metallic (samples A, B, F, G). The former is peculiar of fcc-GeSbTe and trigonal-GeTe phase, while the latter is a prerogative of hcp-GeSbTe and cubic-GeTe. Sample D exhibited a mixed behavior, which we ascribe to the coexistence – detected by XRD – of both fcc and hcp phases. In addition, the resistivity plots confirm that: a) the GeTe resistivity was in general lower than that of GeSbTe, b) fcc-GeSbTe was more resistive than its hcp counterpart. Finally, it is worth noting that, since thin chalcogenide films can be treated as bulk material[1] for thickness >≈ 40

nm, the resistivity of these samples was not affected by the low dimensionality along the thickness dimension.

The carrier density (CD) graph indicates that all samples exhibited very high hole concentration, as most chalcogenides do. Although the *p* values spanned over a large range [2 to 22]·10^{20} cm^{-3}, none of the considered samples exhibited any significant trend, *p(T)* being roughly constant from room temperature to ≈ 4 K, thus indicating that no carrier freeze-out occurred even at ≈ 5 K. This effect, previously observed in fcc and hcp $Ge_2Sb_2Te_5$,[6] is believed to be a common feature of most crystalline chalcogenides, even though different explanations are possible. While the hcp-GeSbTe is considered to be a highly degenerate semiconductor with very small bandgap (<0.1 eV), the fcc-GeSbTe is expected to have a larger bandgap, with the Fermi level ≈ 0.15 eV above the valence band; however the shape of the valence band is supposed to be affected by the presence of a defect band due to the high defect density[5] (trap states). Therefore, fcc-GeSbTe has a lower carrier density than its hcp counterparts, as confirmed by the measured value of sample E (lowest of the set). As previously mentioned, *p* is correlated to the density and kind of structural vacancies in the Ge (or Ge/Sb) sublattice. For instance, in GeTe samples, the higher carrier density of sample C than sample B is ascribed to the higher interfacial defect density, and smaller grain size of HW-LI thin films, as compared to those grown by MOCVD. In GeSbTe samples, the carrier density decreased with increasing Te content (from D to E to F), as has been previously demonstrated[10]. Concerning nitrogen doping (which is a alternative way to engineer the PCM device by improving the stability of the amorphous phase[11]), its effect on carrier density resulted negligible (sample G), in comparison to the undoped (sample F). In this regard, as nitrogen (both atomic and molecular) arranges itself in interstitial positions in GeSbTe without distorting its crystal structure (as has been previously demonstrated[11]), it behaved like a non-charged defect and did not contribute to the hole concentration. Finally, sample A exhibited an anomalously high carrier density, which we ascribe to the complex stoichiometry, inducing the 2-phase separation shown in Table 5.1.

Results previously obtained on $Ge_2Sb_2Te_5$ by other Authors are summarized in Figure 5.6, where the trend of fcc and hcp phases is discernible. The results of this work agree and extend the validity of this trend to other chalcogenide compositions. Note that the > 400 K measurement reported below, might be the result of an artifact (as suggested elsewhere)[6].

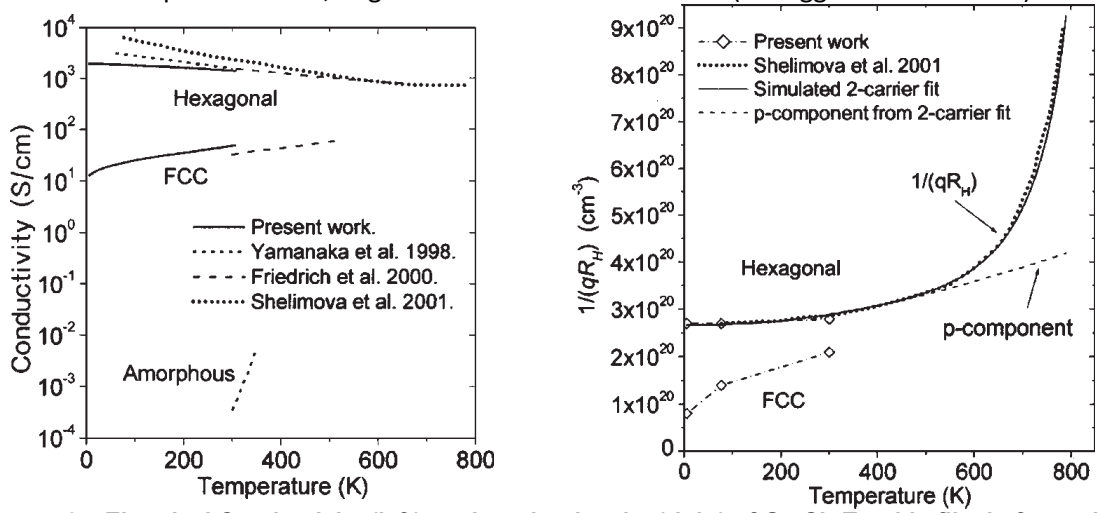

Figure 5.6 – Electrical Conductivity (left), and carrier density (right) of $Ge_2Sb_2Te_5$ thin film in fcc and hcp phases according to previous reports[6]

The carrier mobility μ_h was estimated from the joint measurement of carrier density and resistivity, under the assumption of single carrier type (holes), according to the formula $\mu_h = {}^1/_{\rho p q}$ (as detailed in Chapter 3). It was renowned that the mobility of charge carriers in chalcogenides is much lower than in most inorganic semiconductors. All of the examined samples exhibited μ_h < 8 cm^2/Vs, with the notable exception of the MOCVD-grown GeTe (sample B). Indeed, the higher purity of deposition and the larger grain size of sample B are thought to account for the higher mobility of its charge carriers. Overall, room-temperature

mobility was highest in GeTe (sample C), high in hcp-$Ge_2Sb_2Te_5$ regardless of N-doping (sample F, and G), lowest in fcc and non-stoichiometric GeSbTe (samples E, and A respectively).

Concerning the temperature dependence of mobility, two distinct trends can be discriminated according to the $\mu_h(T)$ plot: negative slope (samples A, B, and F), and positive slope (samples C, D, E, and G). The former can be attributed to a dominant lattice scattering mechanism of the type $T^{-\alpha}$, $\alpha \approx 1$. In these samples, other scattering mechanisms were negligible, as a result of the higher purity and larger grain size of these films. Moreover, lattice scattering occurred in combination with a low temperature mobility saturation of the type T^0, accounting for ionized impurity scattering in a degenerate semiconductor (which showed up more markedly in sample B).

On the other hand, the interpretation of the positive $\mu_h(T)$ slope is less straightforward. Samples C, D, E, and G were all deposited by HW-LI in a polycrystalline form, having smaller thickness and grain size. Film boundary scattering effects can be neglected: from the charge carrier mobility point of view, even the thinnest sample (40 nm) can be still considered bulk-like, because the mean free path of carriers is much smaller than the film thickness. Moreover, since the slope of $\mu_h(T)$ is positive, the effect of phonons on mobility ($T^{-\alpha}$) appears to be negligible, thus indicating that other scattering mechanisms are dominating at low temperature. Having ruled out the geometrical boundary scattering, other possible causes were: a) grain boundary scattering ($\approx Te^{-1/T}$), and b) ionized impurities scattering ($\approx T^{3/2}$). Grain boundary scattering was demonstrated to be negligible in solids with very high carrier density ($<10^{19}$ cm^{-3}),[12] where the grain-grain boundary is significantly thinner. Ionized impurity scattering is related to the high amount of charged vacancies, the density of which is higher in HW-LI-deposited samples. We therefore suggest that a combination of impurity and lattice scattering can account for both the low and high temperature $\mu_h(T)$ saturation, respectively.

The $\mu_h(T)$ values of samples A and B were fitted to the model of electrical conductivity in metals as a function of temperature which leads to the Bloch-Grüneisen relation[13]. The minimization function was:

$$\mu_h = \frac{1}{a_0^{-1} + a_1^{-1} T^5 J(\Theta_D / T)} \tag{5.1}$$

with a_0, a_1, and Θ_D fitting parameters, and:

$$J(\Theta_D / T) = \int_0^{\Theta_D / T} \frac{z^5}{(e^z - 1)(1 - e^{-z})} dz \tag{5.2}$$

In eq. 5.1 and 5.2 Θ_D has the dimension of a temperature; its meaning is comparable to the Debye temperature for the material. a_0 represents the reciprocal of μ_h at T=0 K.

The *fminuit* toolbox[14] for MATLAB® was used to perform the optimization and χ^2 minimization. The resulting fitting parameters are given in Table 5.2.

	a_0 [Vs/cm^2]	a_1	Θ_D [K]
Sample A	0.1515	6.68E-13	265.2
Sample B	0.0304	7.87E-16	642.1

Table 5.2 – Fitting parameters for $\mu_h(T)$

On the other hand, sample F (the other sample featuring negative-slope μ_h) data could be fitted only to the exponential function $T^{-\alpha}$ ($\alpha = \frac{1}{6}$). The data and fit for these samples are shown in the following Figure 5.7.

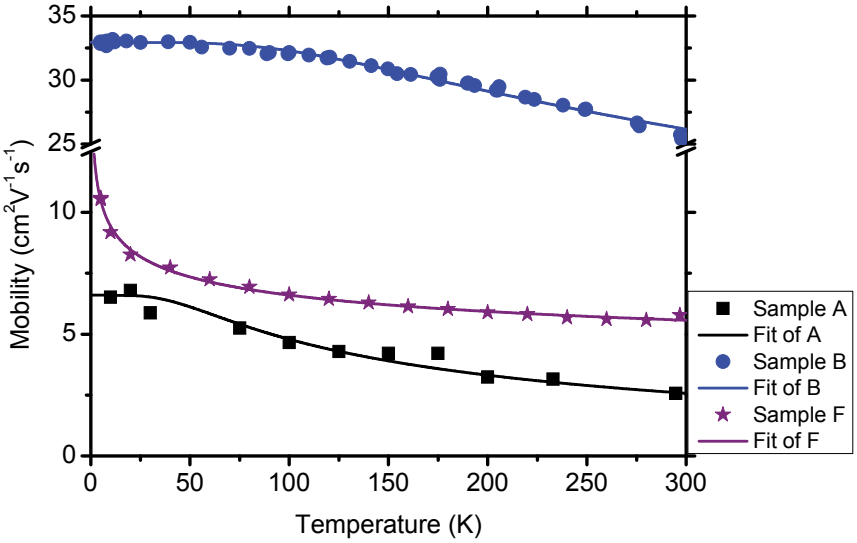

Figure 5.7 – Mobility data and best fit functions thereof for samples A, B, and F

The fit to the data was very accurate, indicating that samples A and B behaved as fully degenerate semiconductors with the Fermi level inside the valence band throughout the given temperature range. According to the model output, sample B has a higher equivalent Debye temperature than sample A, hence testifying to a non-complete excitation of all phonon modes at room temperature. It is expected, therefore, a further decrease of mobility at above room temperature for the MOCVD-grown GeTe samples. Note that parameter a_0 did correctly output the 0 K mobility value for each sample. Concerning sample F, its behavior is well fitted by an exponential function. This result suggests that the phase separation in the material (namely, the excess elemental Te that was detected by XRD) dominates the electric behavior of the film, thus making it purely metallic.

Mean free path of charge carriers in chalcogenides

The semiclassical transport model is a generalization of the theory of free electrons in the case of a spatially-periodic potential, that is, a crystalline solid. According to the free electron theory, electrons under a constant potential field obey to the classical equations of motion (in other words, move by constant acceleration motion). At the same time, their mobility is limited by collisions with: lattice atoms, optical/acoustical phonons, lattice impurities, grain boundaries, geometrical boundaries. The time span between two consecutive collisions is referred to as the scattering time τ. Under these assumptions, the resulting average drift velocity is[15]:

$$\mu = \frac{q}{m^*}\bar{\tau} \tag{5.3}$$

where q is the elementary charge, m^* is the carrier effective mass. When several scattering mechanisms are occurring at the same time, Matthiessen's rule is a very good approximation of the combined effect thereof:

$$\mu = \frac{1}{\sum_i \mu_i^{-1}} \tag{5.4}$$

The MOCVD-grown GeTe film was taken chosen for in depth characterization because of its peculiar features of non-stoichiometry. In this regard, two kinds of scattering mechanisms were taken into account: lattice (T^{-1}) and defects (T^0). The measurement data were qualitatively fit to a combination of these function. Figure 5.8 shows the measurement data along with the interpretation according to these mechanisms.

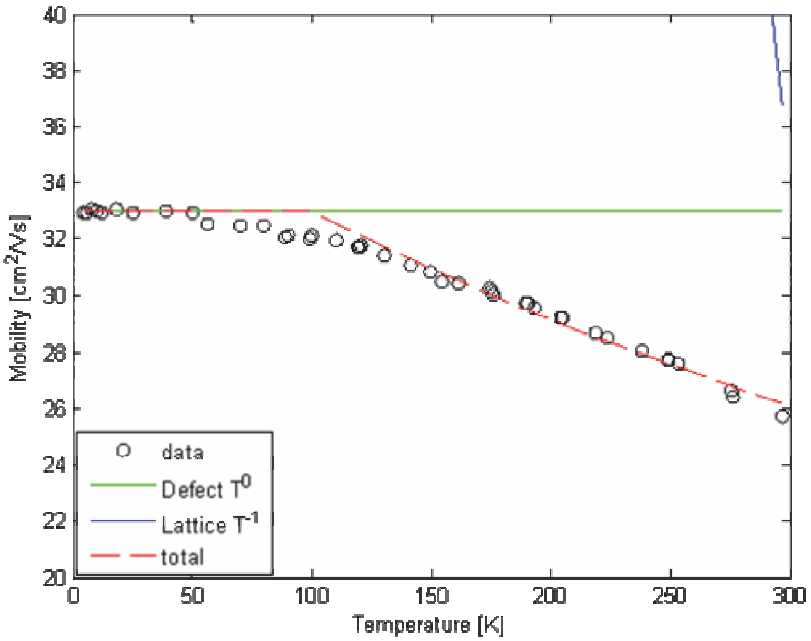

Figure 5.8 – Modeling of scattering mechanisms in GeTe thin film grown by MOCVD

While lattice scattering was always present, it must be noted that defect scattering set an upper limit to the low-temperature mobility (i.e., set a mobility saturation value). This effect occurred even in cubic GeTe in which, given its metallic-like behavior, mobility was expected to increase further at lower temperatures. The mobility saturation value can be employed to determine the effective charge carrier mass, according to Shockley's formula for the defects-scattering limited mobility of a degenerate semiconductor[16]:

$$\mu_{\deg} = \frac{3(\varepsilon\varepsilon_0)^2 h^3 n}{m^{*2} Z^2 e^3 N_i} \tag{5.5}$$

where ε, ε_0 are the relative and absolute dielectric constants, h is the Plank's constant, n is the density of the material, m^* is the effective charge carrier mass, Z is the ionization charge of the defect, e is the electron charge, and N_i is the defect density.

By using known values in the formula above (Z=+1, $N_i=10^{21}$ cm^{-3}, ε=15, n=6.06 g/cm^3), it was obtained an effective mass of carriers:

$$m^* = 0.14\ m_e \tag{5.6}$$

where m_e is the electron rest mass, indicating that the mean free path is ≈ 1 nm at T = 300 K.

This finding suggests that ionized defects are the dominant scattering mechanism, while grain boundaries scattering mechanism ($T^{3/2}$) can be neglected thoroughly the considered temperature range. Finally, this result might explain why the electrical functionality of chalcogenides is preserved even at ultra large scaled dimensions (2.5 nm), as has been recently demonstrated[17].

Conclusions

Despite sharing several similarities – such as dominant *p*-type conduction, very high carrier density – the physical properties of crystalline GeTe and GeSbTe thin films vary considerably and are tunable. In particular it was found that composition and deposition technique affect the amount and concentration of defects which, in turn, determines the structural properties and arrangement of the species in the lattice. Eventually, these features affect the electric transport properties. Thicker, high-purity, MOCVD-grown films exhibited metallic like behavior, where mobility was limited by lattice scattering at lower temperatures. On the opposite,

mobility of charge carriers in thinner, HW-LI grown films was mostly pinned to a low value due to charged impurity scattering throughout the temperature range investigated (4 to 300 K).

The carrier density of chalcogenide films was mostly unaffected by temperature, as no carrier freeze-out was detected down to ≈ 4 K. However, the two phases showed different trends, suggesting to have either a partially (fcc) or a fully (hcp) degenerate band structure, regardless of deposition technique or thickness.

Finally, it was found that the ionized impurity scattering – originating from the high concentration of structural defects in the crystalline chalcogenides – has a dominant role in charge carrier scattering. As a consequence, mean free path of carrier is remarkably small and electrical functionality is preserved even in chalcogenide nanostructures.

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6. Chalcogenide nanowires

Introduction

Chalcogenide nanowires are appealing structures for achieving very large down-scaling of phase change memory by reducing the nanowire diameter, as mentioned in Chapters 1 and 2. Moreover, MOCVD growth and VLS mechanism accomplish a fully “bottom-up” process that is thought to be easily integrated in a manufacturing process. In this Chapter, the phase-change functionality of these nanostructures and the results of their electrical characterization are presented.

Sample preparation

The functional characterization of single, isolated chalcogenide nanowires required a dedicated sample preparation by electron beam lithography (EBL) and/or focused ion beam (FIB). As mentioned in Chapter 4, FIB preparation was carried out in three different facilities by employing similar operational settings. In this section, SEM images of samples prepared by FIB will be presented. Despite the differences in geometry and shape, these sample share some notable similarities as the pictures clearly show: large preexisting metal pads/tracks structures; scattered nanowire on the sample surface; and the thin Pt electrodes connecting the former to the latter.

The following SEM image (Figure 6.1) of sample prepared at CNR (S3): pads and tracks were previously fabricated in Pt(Ti) at MDM Laboratory according to the process detailed in Chapter 4.

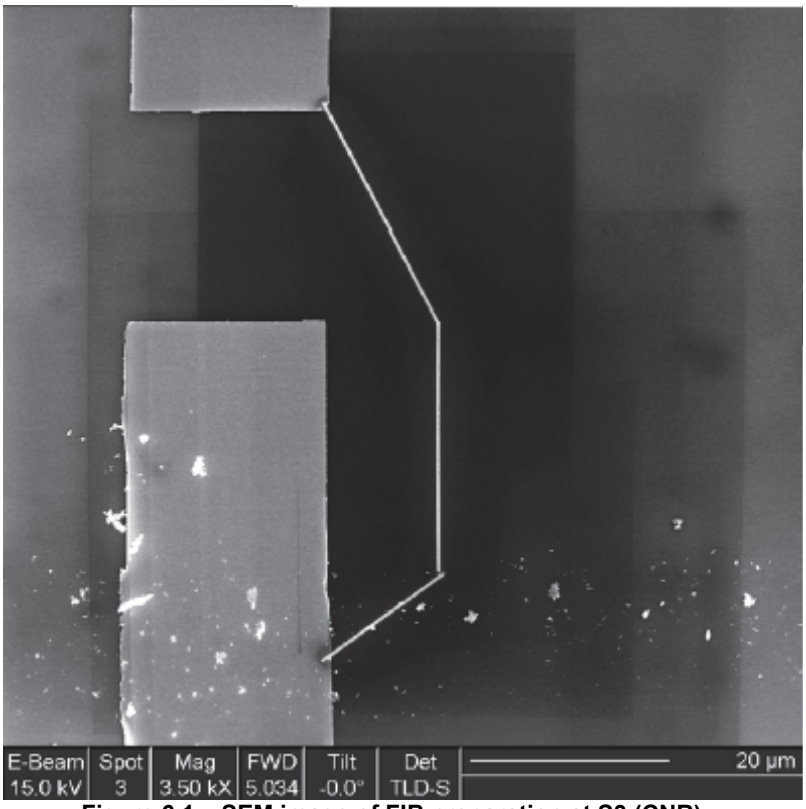

Figure 6.1 – SEM image of FIB preparation at S3 (CNR)

In Figure 6.2, a sample prepared at Physics Lab, Micron Technologies, Italy, is displayed. Platinum strips were shorter that in the previous set of samples, owing to the different geometry of pre-fabricated pad structure. Pads were made of aluminum at Lab. MDM. FIB deposition sometimes looked brighter due to the stronger electron back-scattering (as a result of the smaller, edgier, shape of the FIB strips).

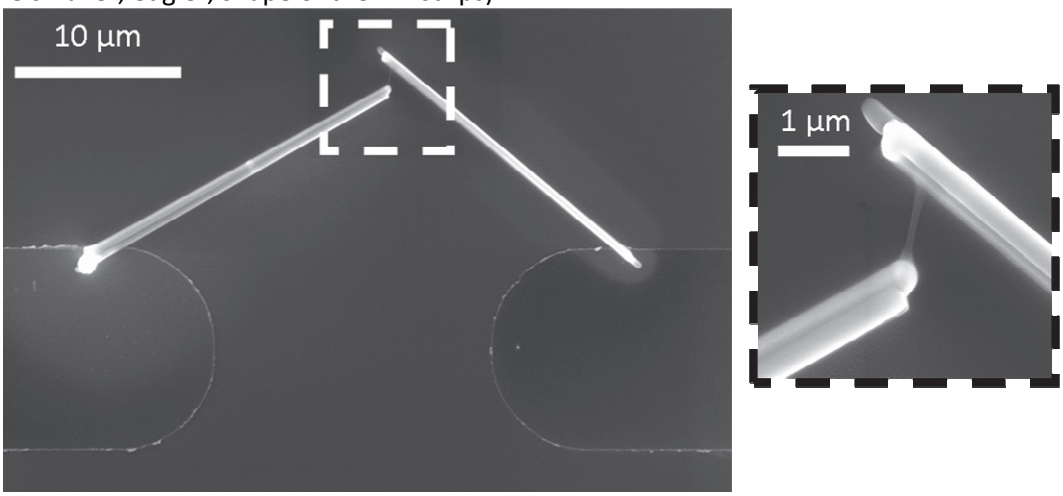

Figure 6.2 – SEM image of FIB preparation at Micron Technologies

The third set of samples was prepared at the Laboratory of Research on the Structure of Matter (LRSM), University of Pennsylvania, USA (Figure 6.3 and Figure 6.4). A specially designed sample holder was employed. It consisted of fourteen large pads/tracks that reach out to the square area in the center. The central area featured several “dead-end tracks”. Nanowires were dropped in between these tracks, which were ≈ 10 µm apart, so as to minimize the FIB-deposited strips length. Thereafter, the tracks were connected to the probes

by using larger Pt depositions. Note the shadowed areas all around the FIB depositions which indicate a charge build-up due to the ion/electron beam.

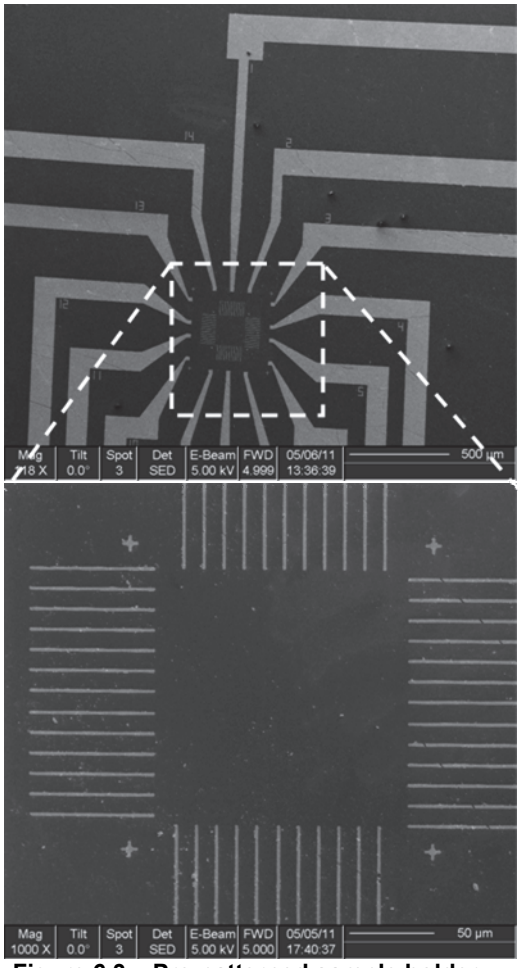

Figure 6.3 – Pre-patterned sample holder employed for FIB deposition at LRSM, consisting of 14-track paths (top) leading to the central area (bottom)

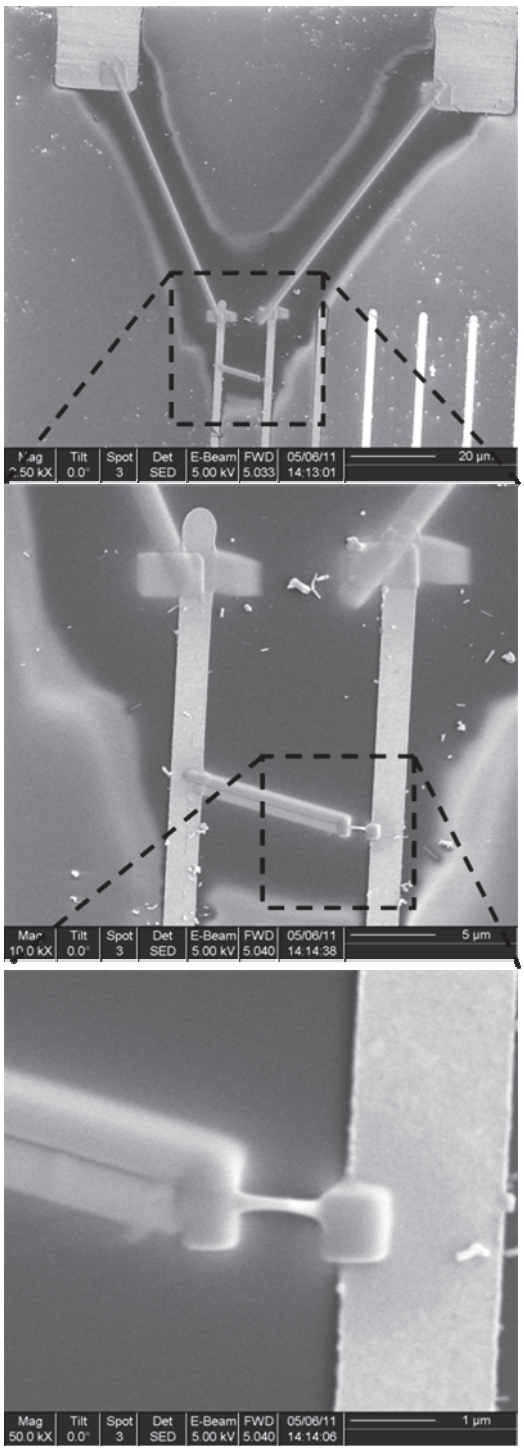

Figure 6.4 – SEM image of nanowire sample preparation performed at LRSM: the large tracks are connected to the strips in the central area by large FIB deposition (top); the nanowire to be contacted is then located in between the strips (middle), to which it is soldered (bottom)

Surface morphology characterization

Atomic force microscopy was used to estimate the geometry of nanowires and FIB deposition of platinum electrodes. The estimation of the nanowire and electrode dimensions is prerequisite to the calculation of the intrinsic nanowire resistivity (which is carried out in the next paragraph).

It has to be noted that AFM resolution is higher along the Z axis, than along the other axis (where it is limited by the lateral size of the tip). In this regard, the resolving capabilities of AFM are complementary to those of SEM. The combined use of both tools was exploited to determine the exact geometry of the nanostructures.

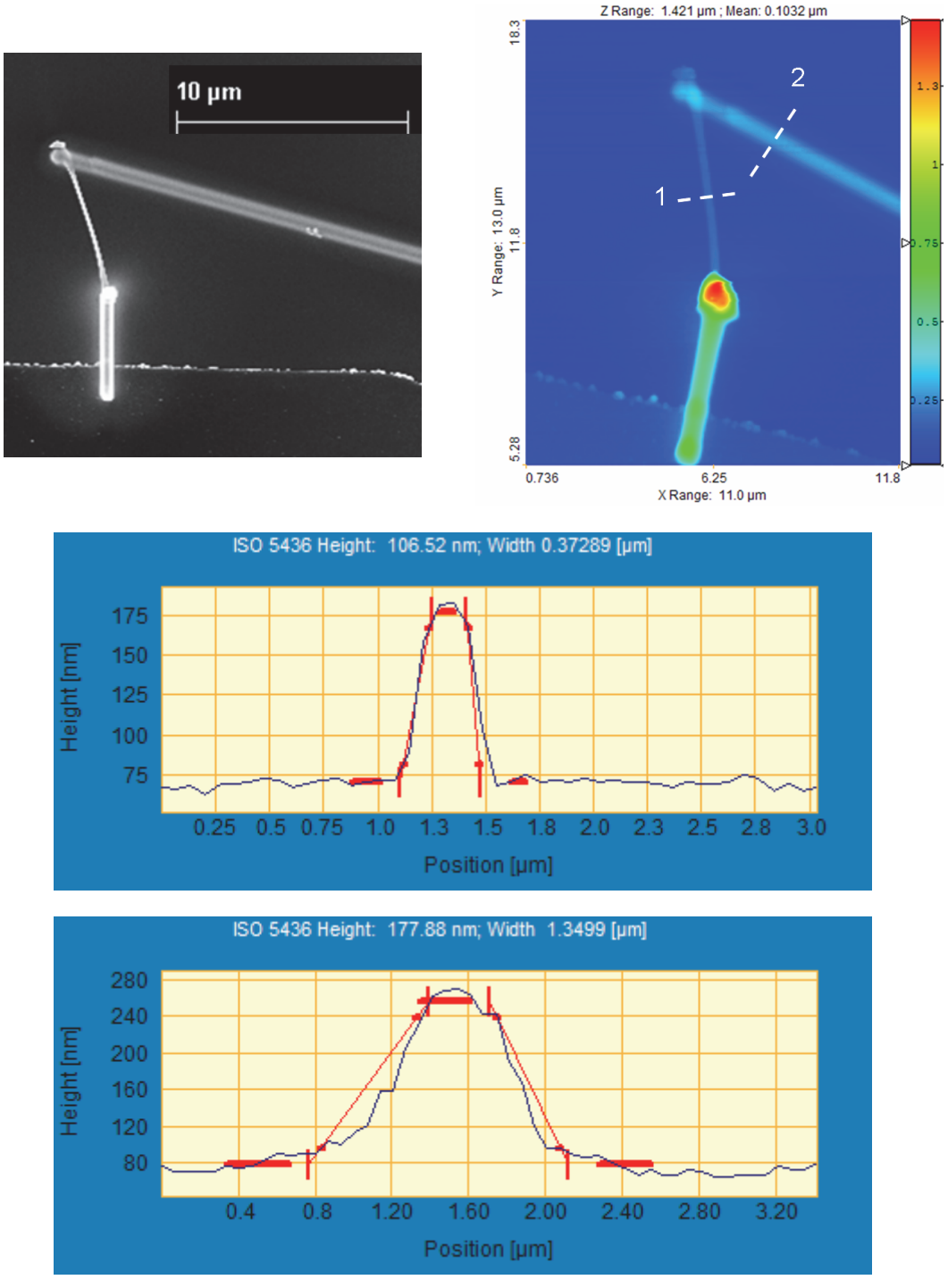

Figure 6.5 – GeTe NW with FIB-Pt electrodes: SEM (top left) and AFM (top right) corresponding image. AFM morphological measurement along cross section 1 (middle) and 2 (bottom)

As shown in Figure 6.5, AFM measurement largely overestimated the lateral width of the structures: 400 nm for the NW, 1 µm for the electrode. However, the height along the Z axis was a reliable measurement of the NW diameter (100 nm) and of the Pt strip thickness (200 nm).

Note that the electrodes thickness was different because of the higher deposition time of the left one (Figure 6.5, top left). The corresponding red area in the AFM image indicated the formation of a pointy Pt-deposit on the nanowire lower end that, however, did not damage the structure.

Device capacitance characterization

The electrostatic force microscopy was employed to probe the electrostatic potential and capacitance of the nanowire. As shown in Chapter 3, the former is proportional to the first harmonic of the signal; the latter to the second harmonic.

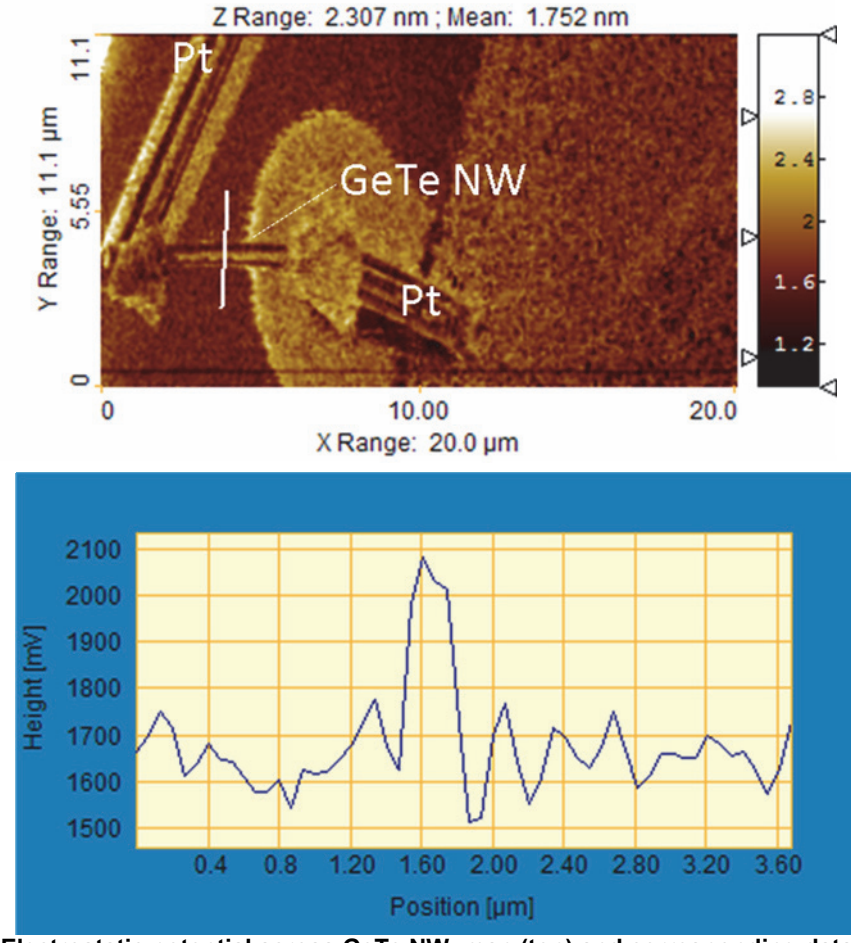

Figure 6.6 – Electrostatic potential across GeTe NW: map (top) and corresponding data along the cross section (bottom)

The electrostatic map (Figure 6.6) exhibited a marked contrast between the metallic, highly conductive structures and the insulating substrate. This measurement indicated the potential is roughly 20 % higher in these areas.

The capacitance map showed a less marked contrast between these areas (Figure 6.7).

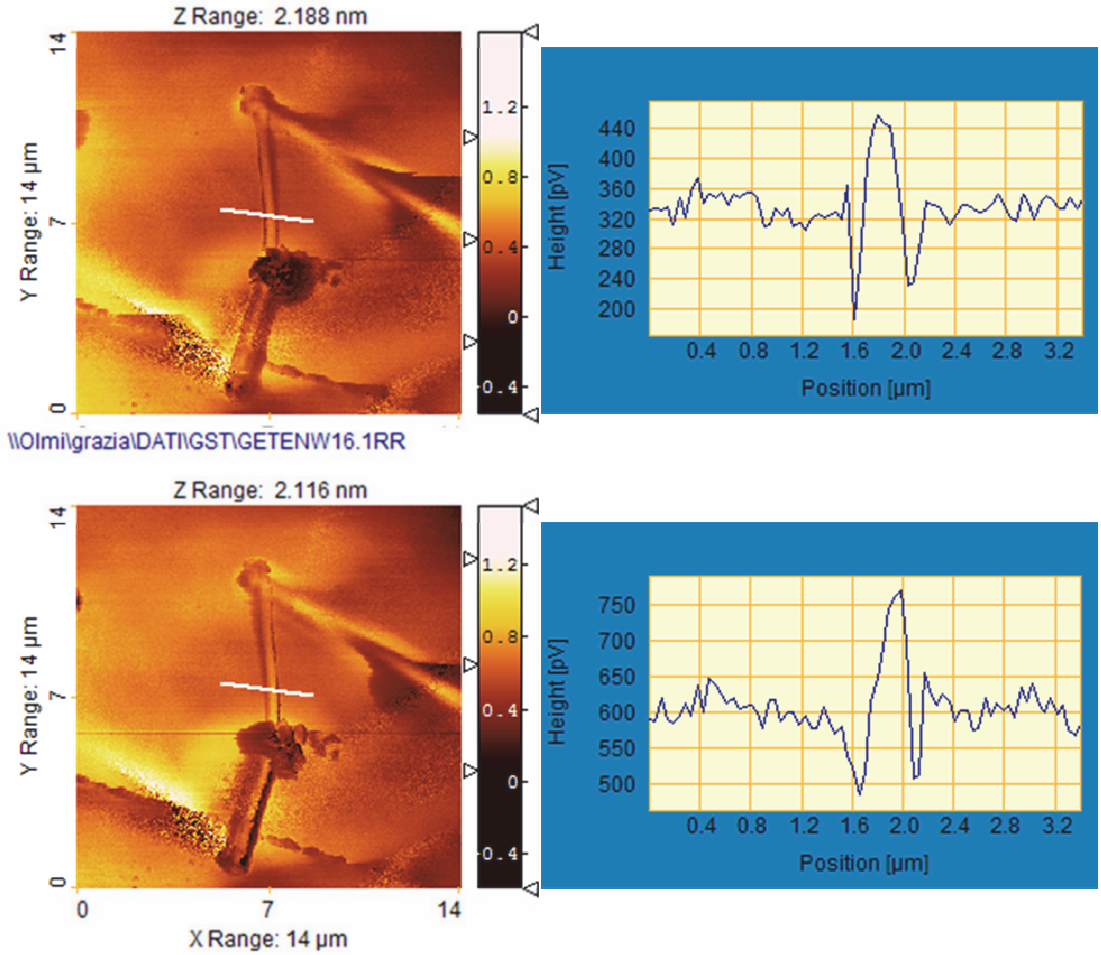

Figure 6.7 – Capacitance measurement of GeTe NW: map (left), and corresponding data along the cross section (right)

A ≈ 15 % increase in capacitance was found between background (50 nm SiO_2) and GeTe nanowire. The map of the second harmonic measurement looked more markedly edgy than the corresponding morphological picture, thus accounting for the inverse proportionality between thickness and capacitance. The nanowire cross section exhibited spikes at the nanowire edges, where a large potential gradient is present (i.e., X = 1.6 and 2.0 µm).

Measurement issues of nanowires

Several single-contacted nanowires of GeTe and Ge-Sb-Te were electrically measured to determine their switching behavior and conductivity. The goal of this characterization was:

- to prove the functionality of a MOCVD-grown nanowire device
- to evaluate the figure of merit of these devices
- to compare these results to state-of-the-art devices

The figures of merit of a nanowire device are:

- the threshold voltage in the pulsed I/V measurement (roughly proportional to the energy of the crystallization)
- the amorphous state resistivity (which determines the set current)
- the crystalline state resistivity (which determines the reset current)
- the amorphous/crystalline resistivity window (roughly proportional to the programming window)

The electrical characterization of nanowires posed several challenges. First, it required careful sample preparation of nanowires, which had to be carried out once at a time. This process was very time consuming and had a low yield in terms of working devices. In light of large scale production of devices, the availability of arrayed structures – where all nanowires in

the device are prepared at once – will be mandatory. Lacking such a structure, only *ad hoc* tools were employed in this work (FIB and EBL), as detailed previously in Chapter 4. The nanostructure had to be contacted to larger pads in order to use the micromanipulator tips for the electrical measurement.

In addition, and related to the above mentioned question, several issues were to be coped with:

- on one hand, the electrical leads have to be long to reach to the device
- on the other hand, too thin/long leads add to the parasitic resistance and capacitance.

Let us consider chalcogenide nanowires. The catalyst-activated vapor-liquid-solid mechanism (Chapter 3) implies that the as-deposited nanowires were grown in the crystalline phase. In this state, the nanowire has a very low resistivity in comparison to the total (electrodes + leads) resistance of the device under test (DUT). During operation as memory device, the phase transition is achieved by electrical pulses. In this condition, only a very small volume of the nanowire undergoes amorphization (usually at the center of the nanowire, where the temperature rise is highest), while most of the wire remains crystalline[1]. Because the resistivity of the amorphous phase is several orders of magnitude higher than that of the crystalline phase, this volume (albeit small) dominates the overall device resistance.

On the opposite, estimating and accounting for the lead resistance is especially critical to calculate the intrinsic resistance of the wire in the SET (crystalline) state. Although the resistivity of bulk chalcogenides is well known, little can be told about the resistivity of chalcogenide nanowires. Most of the electrical characterization of nanowires documented in literature only reports about the wire resistance. As a matter of fact, no information can be inferred on the material resistivity, which would require a (not straightforward) 4-probe measurement on the nanostructure. Recently, four-probe measurement has been carried out on very long (> 10 μm) Sb_2Te_3 nanowires, and their resistivity has been determined, albeit with large uncertainty[2].

In order to address these issues, some workarounds were implemented in this work:

- FIB-deposited platinum 'bridge' structures were prepared
- several crystalline nanowires were measured as a function of length
- the geometry of each nanowire and the Pt leads was estimated by SEM and/or AFM

As a result:

- the effect of Pt leads was ruled out
- the contact resistance between leads and nanowire was estimated and ruled out
- the intrinsic resistivity and resistance of the nanowire was calculated

The latter, in particular, is key to a correct estimation of the programming window (i.e., the resistivity ratio between set and reset). Further details on the electrical aspect of pulsed I/V measurement are also discussed in Appendix B.

Finally, it was found that some devices fabricated by e-beam, rather than i-beam Pt deposition exhibited a resistance two orders of magnitude higher than normal, which supports the findings detailed in Chapter 3 and 4. Therefore, i-beam deposition was employed in all the device prepared.

Results: GeTe nanowires

Germanium telluride has appealing properties for application in non volatile memories, as discussed in Chapter 2. In particular, the resistivity gap between the amorphous and crystalline phases is larger and the retention is higher than in ternary tellurides.

The morphology of the as deposited nanowires, examined by SEM, is shown in Figure 6.8. Nanowires grew in a disordered way, because of the random arrangement of the gold catalyst and of the amorphous substrate (SiO_2) which did not set any preferential growth direction. The growth conditions in the MOCVD reactor were chosen so as to favor the formation of nanowires, rather than that of crystals, which is desirable. It should be noticed that some

nanowire are not completely straight but have some twists and turns: this seems to suggest that several energy minima are present in the growth reaction.

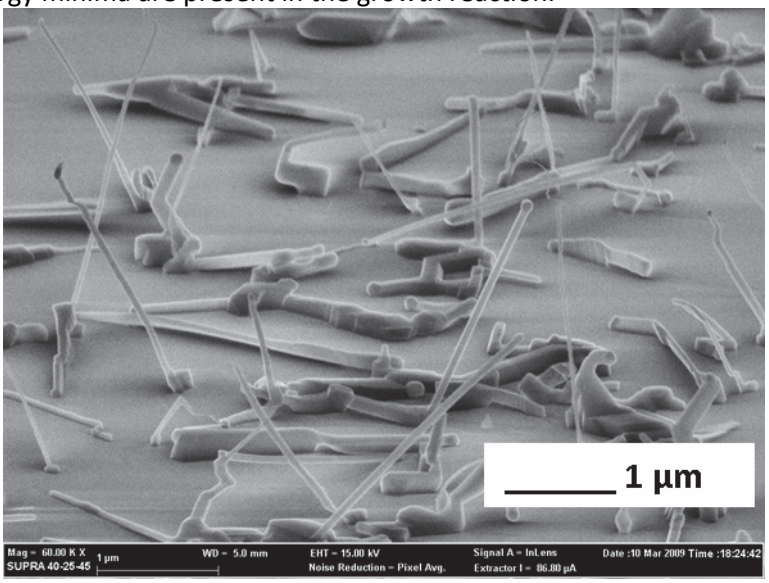

Figure 6.8 – SEM tilted view of the as deposited GeTe nanowires

Structural investigation of a single nanowire, carrier out by energy dispersive X-ray diffraction, revealed the spatial distribution of the species and is displayed in Figure 6.9. As discussed in Chapter 2, germanium telluride properties do vary broadly as composition is shifted away from stoichiometry. In this regard, MOCVD grown nanowires were grown intrinsically stoichiometric, as the reaction favored the arrangement of elements in the 50:50 ratio.

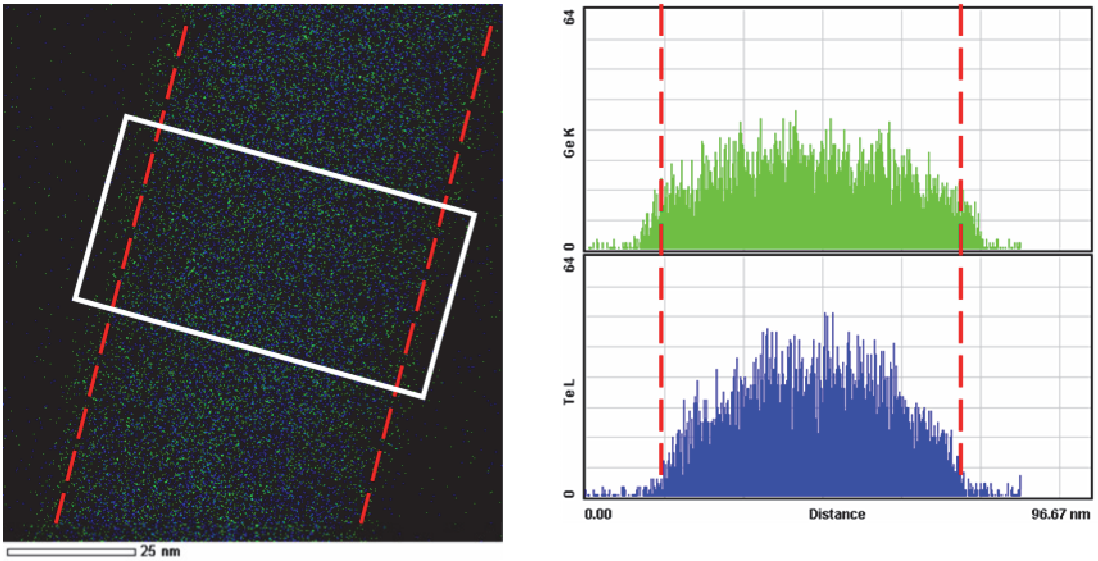

Figure 6.9 – In situ EDX of GeTe nanowire (left) and corresponding composition along the nanowire cross section (right); in the picture, green and blue indicate Ge and Te atoms, respectively

Notably, no contaminant is detectable at this level, thus indicating neither incorporation of carbon from the precursor, nor gold from the VLS catalyst.

The crystallinity of the as grown nanowire was exploited to perform high resolution TEM imaging (Figure 6.10). In addition, the corresponding diffraction pattern was calculated on the TEM image by means of fast Fourier transform (FFT) (Figure 6.10, inset).

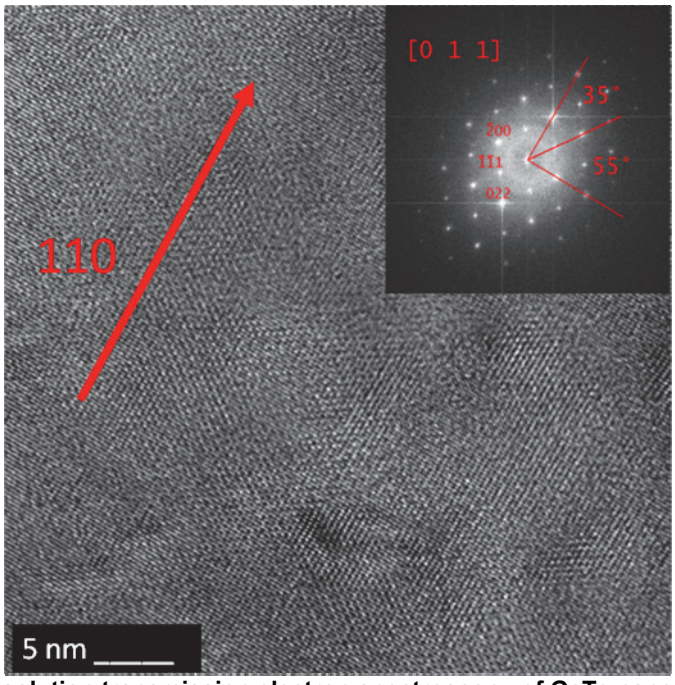

Figure 6.10 – High resolution transmission electron spectroscopy of GeTe nanowires (main figure) and corresponding diffraction pattern obtained by fast Fourier transform (inset)

According to the diffraction pattern, the lattice parameters were found to be compatible with the cubic phase of GeTe:

$$d_{220}= 0.212 \text{ nm} \quad d_{111}= 0.347 \text{ nm} \quad d_{200}= 0.3 \text{ nm}$$

This result is remarkable as the rhombohedral phase was expected to form at the given growth conditions (due to the persistence of the metastable phase formed at the growth temperature 400 °C)[3]. Moreover, GeTe has been thought to revert to rhombohedral structure upon quenching to room temperature, as a consequence of the meta-stability of the cubic phase[4].

To the aim of functional characterization of single nanowires, FIB proved to be the most successful technique for sample preparation (as detailed in Chapter 4). This was mainly due to the small length of nanowires available (≈ 2 µm) in comparison to those reported by other authors (up to ≈ 20 µm)[5]. Typical wire geometry was ≈ 2 µm length, ≈ 60 nm diameter. The output of one sample preparation is shown in Figure 6.11.

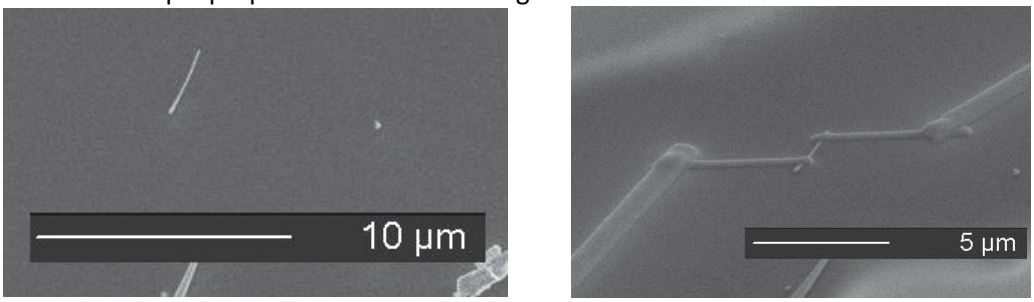

Figure 6.11 – GeTe nanowire before (left) and after (right) electrode preparation

After achieving the preparation of a single GeTe nanowire, the evaluation of its functionality as a non volatile memory device was accomplished by pulsed I/V measurement (as detailed in Chapter 4). This measurement served to prove the functionality of MOCVD-grown nanowires for non volatile memory application. The result is shown in Figure 6.12.

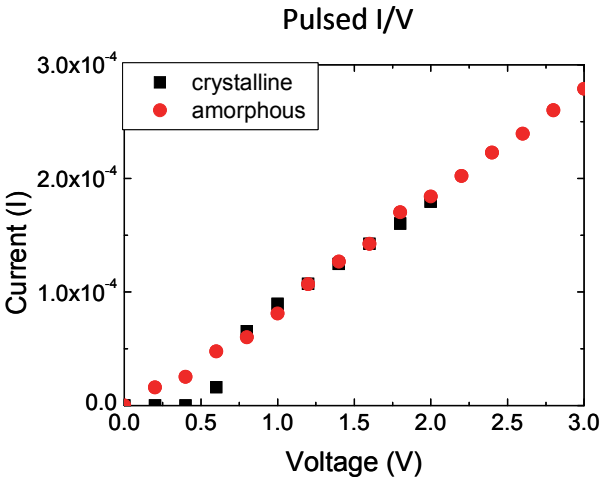

Figure 6.12 – Pulsed I/V measurement of GeTe nanowire

Firstly, the nanowire presented threshold switching – i.e. the reversible phase transition between crystalline and amorphous state – which testifies to its functionality as NVM device. Secondly the phase switching occurred at a given voltage V_{th}, which is one of the nanowire figure of merit (roughly proportional to the crystallization energy). As a comparison, this threshold voltage value ($V_{th} \approx 0.7$ V) was close to that of GeTe nanowires grown by powder evaporation, documented by other Authors and shown in the following Figure 6.13.[6]

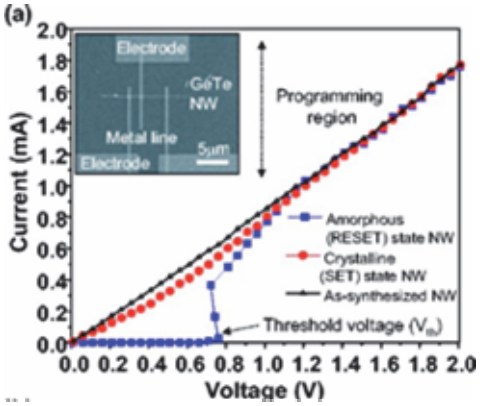

Figure 6.13 – Pulsed I/V of GeTe nanowire grown by evaporation of GeTe powder[6]

The breadth of the resistance window across the phases, which is proportional to the SET/RESET programming window, is an important figure of merit for NVM devices. To estimate its value, the wire resistance was switched several times by applying short voltage pulses: 100 ns, 3 V to amorphize; 300 ns (+300 ns leading edge), 3 V to crystallize. The resulting resistance values are shown in Figure 6.14.

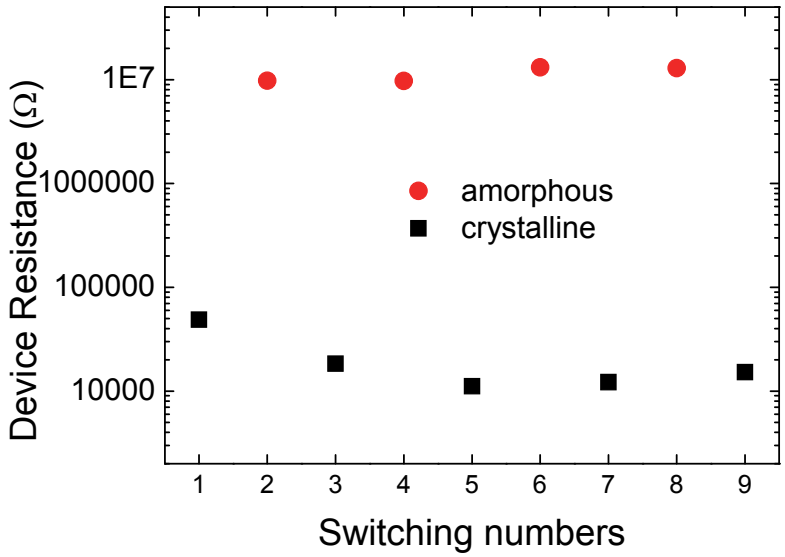

Figure 6.14 – Resistance of GeTe nanowire

Notably, the resistance gap was roughly 3 orders of magnitude, which is less than the bulk value of the amorphous/crystalline resistivity. Moreover, as will be discussed in the following, the wire resistance changed less than in GeTe-based phase change memory devices with conventional thin films. Also note that the resistance of the wire in the crystalline state decreased after the first cycle, owing to the improvement of the wire-electrode contact by local annealing, induced by Joule heating (this effect has been previously reported by other Authors[7]).

The state of the GeTe nanowire was reversibly switched up to 7-9 times before device failure, which was ascribed to incorporation of contaminants from the ambient, from which the wire was not isolated.

It is worth mentioning that amorphization could be achieved by using shorter pulses, too. Namely, the minimum pulse duration required for triggering the phase change was 50 ns, with 2.5 ns leading and trailing edges width. This finding is in agreement with results of fast switching of GeTe thin films by optical and electrical methods and indicate that this alloy has very vast switching times, provided that stoichiometric control (50:50) can be accomplished[8]. In this regard, the leading edge sharpness is thought to be key to achieve proper amorphization.

Nanowire length turned out to be the critical parameter for functionality: among the prepared samples, only the longest nanowire did exhibit the switching from crystalline to amorphous state. In addition, it was found that failure of the device occurred after very few switches. That phenomenon can be ascribed to oxygen incorporation (from the environment) and/or electromigration phenomena within the Pt-wire contact area.

Several nanowires in the crystalline phase and various length were measured so as to estimate the interfacial electrical resistance at the platinum/nanowire interface. The data are shown in the following Figure 6.15. The interfacial resistance was extracted as the intercept (NW_Length → 0 nm) of the linear fit to the NW_Resistance(length) data.

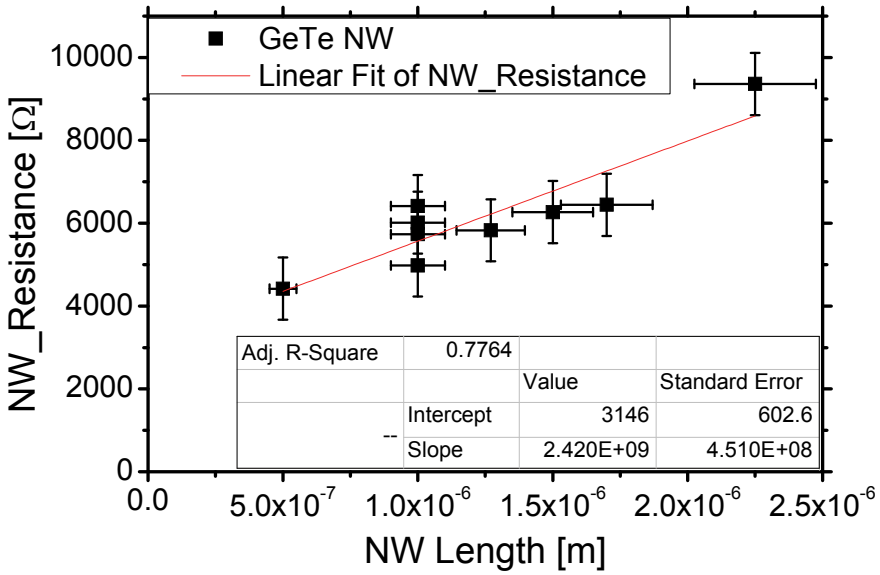

Figure 6.15 – GeTe nanowire resistance vs. length

Note that the fitting to the data was poor (adjusted R^2=0.7764) because of the high uncertainty affecting both the nanowire geometry (estimated by SEM observation) and nanowire resistance (net of the Pt lead resistance).

Nevertheless, it was possible to estimate the contact resistance (intercept) and intrinsic nanowire resistivity (assuming the nanowire diameter ≈ 60 nm):

$$R_{NW/Pt} = 3146 \pm 603\ \Omega$$

$$\rho_{GeTe\text{-}NW} = 2.7 \pm 0.51\ m\Omega cm$$

The latter value is consistent with the resistivity of bulk rhombohedral GeTe (≈ 1 mΩcm).[9]

Programming curves were calculated by current-pulsing the NWs memory device as a function of the current pulse amplitude; 100 ns write and 500 ns erase pulses were used and the resulting plots are shown in the following Figure 6.16.

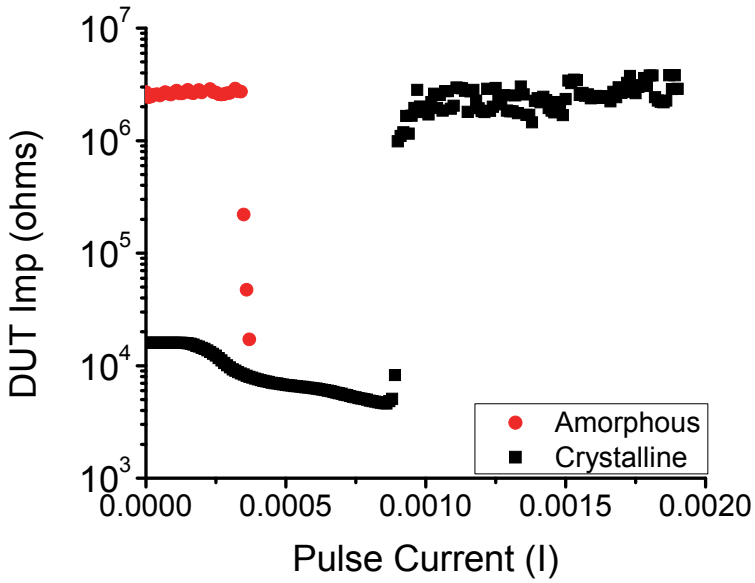

Figure 6.16 – Programming plot (device resistance) as a function of the current pulse

Below 0.25 mA, the pulse intensity was too low to onset phase change, but high enough to improve the NW/Pt contact resistance: this effect is detectable as the lowering of the crystalline DUT resistance (previously reported by other Authors[10]). Approximately 0.3 mA were required to induce crystallization, and 0.8 mA to onset amorphization again. These values are slightly lower than those of GeTe nanowires obtained by evaporation of PVD; however, it

should be kept in mind that this value depends on the nanowire geometry (i.e., thinner wires require less current).

In this regard, the oxidation of the nanowire outer shell might reduce the actual wire diameter, as discussed in Chapter 2. Preliminary TEM investigation on the aging effect in MOCVD-grown GeTe nanowires suggested that this phenomenon is not negligible and is time-dependent. The Z-contrast TEM image of a single GeTe nanowire (Figure 6.17) shows this effect, which is detectable as the rough, uneven look of the wire.

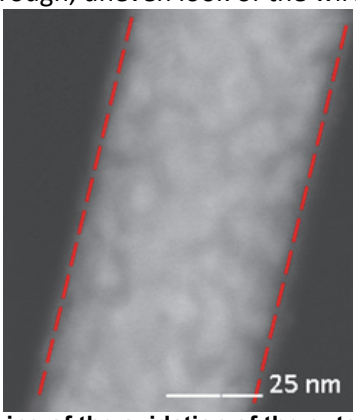

Figure 6.17 – TEM Z-contrast imaging of the oxidation of the outer shell of a MOCVD-grown GeTe nanowire

Results: Ge-Sb-Te nanowires

Ternary compounds of tellurium – especially those in the pseudobinary line between GeTe and Sb_2Te_3 – offer the best tradeoff between performance and ease of integration for PCM applications. As discussed in Chapter 2, these alloys share both the switching speed of antimony telluride and the robustness of germanium telluride. In this paragraph, the results of the electrical characterization of ternary chalcogenide nanowires will be highlighted.

The morphology of nanowires grown by MOCVD deposition of Ge, Sb, and Te is shown in Figure 6.18. As in the case of germanium telluride, Ge-Sb-Te nanowires grew in a disordered manner, because of the random arrangement of the gold catalyst and of the amorphous substrate (SiO_2) which did not set any preferential direction. Note that the amount of crystals in the background was higher than in GeTe nanowires; moreover, shorter, larger wires were also obtained as a result of the different growth conditions.

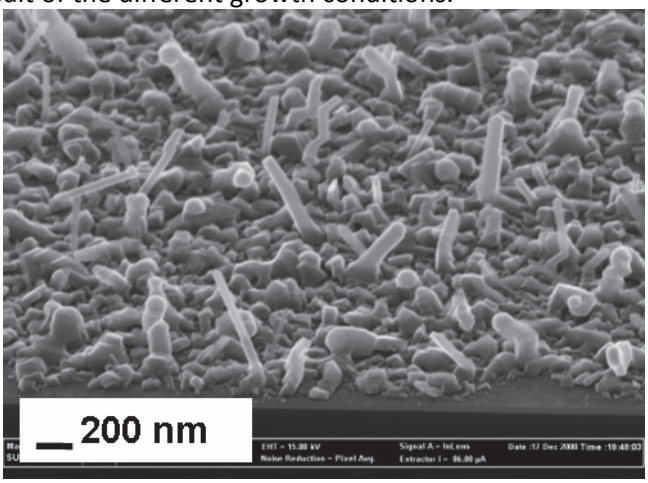

Figure 6.18 – SEM tilted view of the as grown Ge-Sb-Te nanowires

High resolution TEM was employed to investigate the structural arrangement and phase of the Ge-Sb-Te nanowires. In Figure 6.19, the tip of one such nanowire is shown; the gold nanoparticle at the tip is still visible; the growth direction is signaled. In the inset of Figure 6.19, the diffraction pattern (obtained by fast Fourier transform of the TEM image) is shown.

Notably, no contaminant is detectable at this level, thus indicating neither incorporation of carbon from the precursor, nor gold from the VLS catalyst.

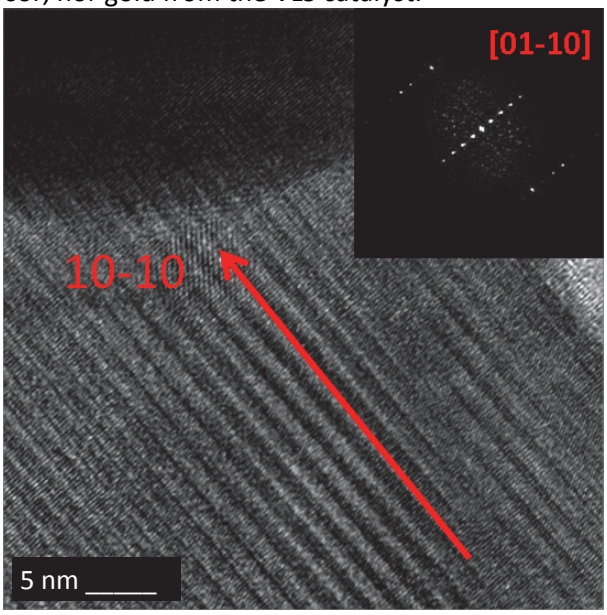

Figure 6.19 – HR-TEM image of a Ge-Sb-Te nanowire with the gold nanoparticle on top; in the inset, the corresponding diffraction pattern calculated by FFT

TEM investigation revealed some peculiarities: the hexagonal in-plane axis is almost parallel to the growth direction; moreover, the diffraction pattern delivered the following lattice parameters:

- d-spacing = 1.39 nm
- growth direction: [10-10]

These parameters are compatible with the hexagonal phase of the $Ge_1Sb_2Te_4$ compound (d_{0003} = 1.367 nm). This result is also supported by energy dispersive X-ray diffraction (EDX) carried out in situ on the same nanowire; its spectrum is shown in Figure 6.20.

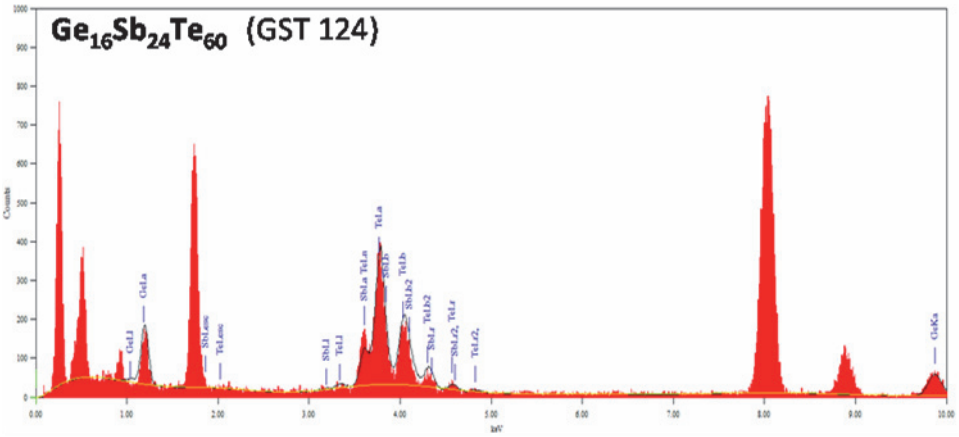

Figure 6.20 – EDX spectrum of a single nanowire of GeSbTe

Notably, $Ge_1Sb_2Te_4$ is one of the stable compounds of the pseudobinary line $(GeTe)_n(Sb_2Te_3)_m$ (see Figure 2.8, Chapter 2). Despite having been implemented in PCM devices, nanowires of this composition have never been synthesized in nanowires before (as of December 2011). It is thought that the compositional control of the MOCVD deposition allows the formation of this stoichiometry, contrarily to conventional evaporation of elemental powders which only grown $Ge_2Sb_2Te_5$. The viability of this alloy, which has already been demonstrated in PCM, might be of interest for nanowire-based device, too.

To the aim of functional characterization of single nanowires, FIB proved to be the most successful technique for sample preparation (as detailed in Chapter 4). This was mainly due to the small length of nanowires available (≈ 2 µm) in comparison to those reported by other

authors (up to ≈ 20 µm)[5]. Typical wire geometry was ≈ 2 µm length, ≈ 80 nm diameter. The output of sample preparation is shown in Figure 6.21.

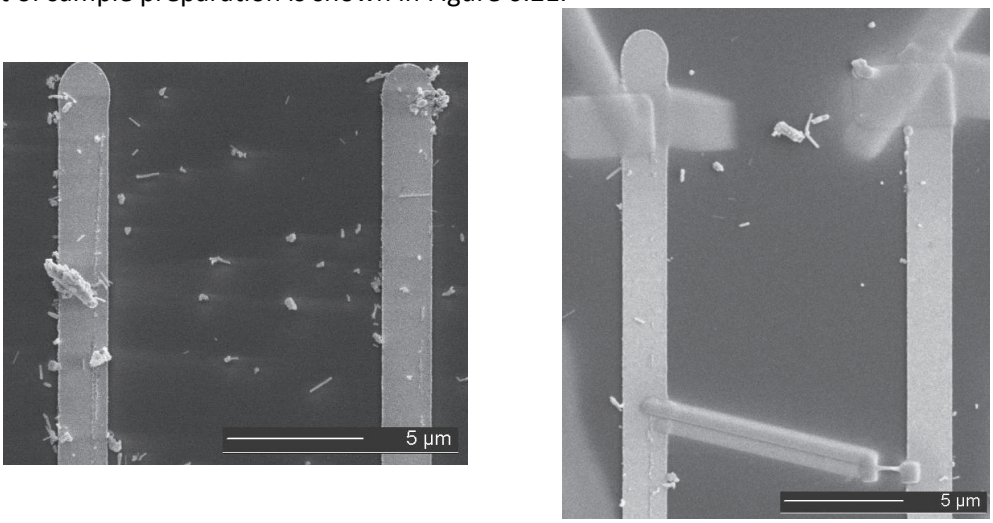

Figure 6.21 – SEM images of $Ge_1Sb_2Te_4$ nanowire identification (left) and after FIB preparation (right)

After accomplishing the preparation of a single $Ge_1Sb_2Te_4$ nanowire, the evaluation of its functionality as a non volatile memory device was accomplished by pulsed I/V measurement (experimental setup detailed in Chapter 4). The result is shown the following Figure 6.22.

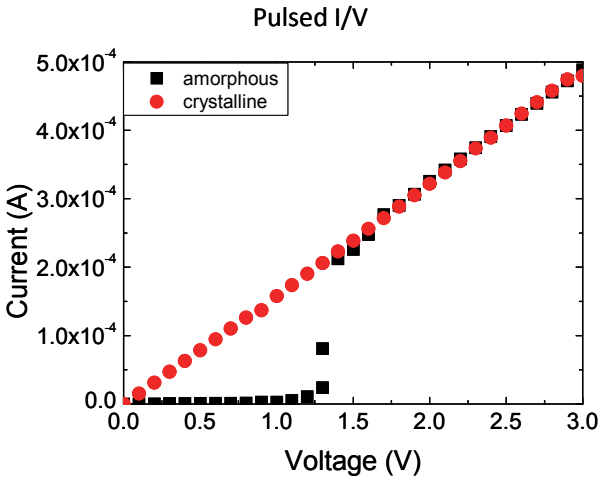

Figure 6.22 – Pulsed I/V from a single $Ge_1Sb_2Te_4$ nanowire

According to the pulsed I/V measurement, the $Ge_1Sb_2Te_4$ nanowire presented reversible threshold switching between its phases, thus testifying to its functionality as a NVM device. It was found that the phase switching occurred at a given voltage V_{th}. Threshold voltage V_{th} is the main figure of merit regarding the performance of switching memory devices, and is roughly proportional to the energy required to program it. Pulsed I/V of the amorphized nanowire displays threshold switching at around V_{th}=1.35 V. As no other nanowires of this composition have been reported so far, this result can only be compared to that obtained on a $Ge_2Sb_2Te_5$ nanowire grown by evaporation of powders, shown in the following Figure 6.23.[11]

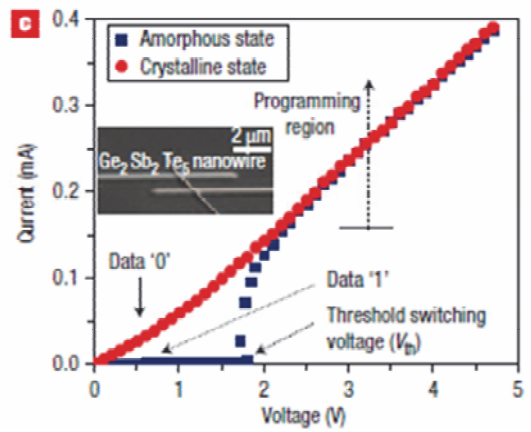

Figure 6.23 – Pulsed I/V of a $Ge_2Sb_2Te_5$ nanowire grown by evaporation of powders[11]

As a comparison to other ternary $Ge_2Sb_2Te_5$ nanowires, other Authors have reported a threshold voltage of 1.8 V, and an amorphous resistance value of 1.8 MΩ.[12] Although these discrepancies could be partly ascribed to differences in wire geometry (this work: 80 nm; Lee et al.: 100 nm), the effect of composition is thought to be significant. Indeed, it is renowned that phase change speed increases and activation energy decreases when going towards Sb_2Te_3-richer compositions along the GeTe–Sb_2Te_3 pseudobinary line. In comparison to $Ge_2Sb_2Te_5$ thin films, $Ge_1Sb_2Te_4$ thin films have lower crystallization temperature (160 vs. 149 °C, respectively), lower activation energy (0.45 vs. 0.42 eV, respectively), and lower amorphous state resistivity (≈ 10000 vs. 1000 Ωcm, respectively)[13]. Besides, this alloy has been implemented in conventional phase change memory cell devices, in which $Ge_1Sb_2Te_4$ has shown lower threshold voltage and lower activation energy than those based on $Ge_2Sb_2Te_5$ (1.41 vs. 1.57 V, and 2.12 vs. 2.28 eV, respectively)[14]. As a result, the $Ge_1Sb_2Te_4$ alloy is expected to deliver faster switching, lower power devices, although at the expenses of a smaller resistance programming window.

According to our results, the above mentioned findings (lower threshold voltage, lower amorphous resistance, and smaller resistance gap) which have already been known for thin $Ge_1Sb_2Te_4$ films, still proved valid for $Ge_1Sb_2Te_4$ nanowires. In addition, the threshold voltage of the nanowire examined in this work was slightly lower than that of a conventional, 50 nm thick, PCRAM cell based on the same composition, which is a desirable feature.

The breadth of the resistance window across the phases, which is proportional to the SET/RESET programming window, is an important figure of merit for NVM devices. To estimate its value, the wire resistance was switched several times by applying short voltage pulses: 100 ns, 3 V to amorphize; 300 ns (+300 ns leading edge), 3 V to crystallize. In the amorphous state, the resistance increased to 450 ± 50 kΩ, and achieving a ≈ 2 orders of magnitude broad programming window – shown in the following Figure 6.24.

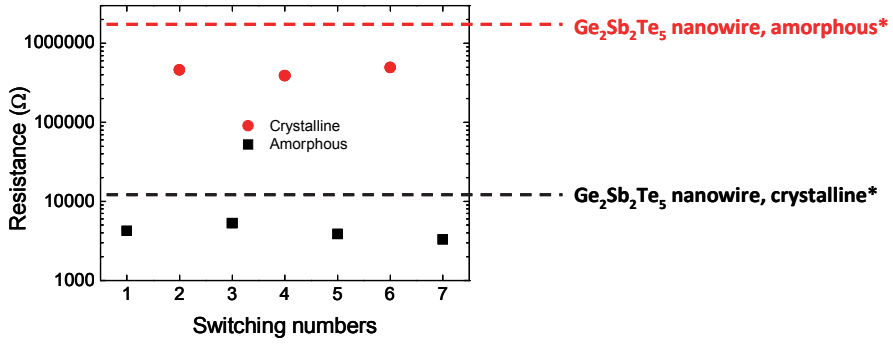

Figure 6.24 – Comparison of resistance programming window: $Ge_1Sb_2Te_4$ nanowires (red and black dots, this work), and $Ge_2Sb_2Te_5$ nanowires grown by evaporation of powders (dashed red and black lines)[11]

The state of the $Ge_1Sb_2Te_4$ nanowire was reversibly switched up to 7-9 times before device failure, which was ascribed to incorporation of contaminants from the ambient, from which the wire was not isolated.

By measuring the electrical resistance of crystalline as deposited nanowires of various length, it was possible to calculate the interfacial electrical resistance at the platinum/nanowire interface. The data is shown in the following Figure 6.25, where the interfacial resistance is calculated as the intercept (NW_Length → 0 nm) of the linear fit to the NW_Resistance(length) data. (Note that two sets of nanowires were measured, roughly longer and shorter, as a consequence of sample processed at different times.)

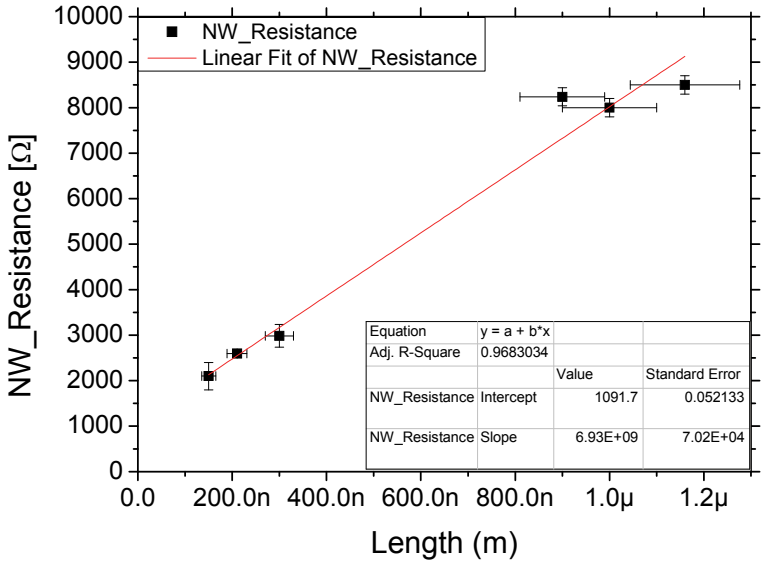

Figure 6.25 – Measured $Ge_1Sb_2Te_4$ nanowire resistance as a function of length

The fit to the data is good (adjusted R^2=0.968), despite the large uncertainty affecting both the nanowire geometry (estimated by SEM observation) and nanowire resistance (net of the Pt lead resistance). It is therefore possible to estimate the contact resistance (intercept) and intrinsic nanowire resistivity, assuming the nanowire diameter ≈ 80 nm:

$$R_{NW/Pt} = 1091 \pm 0.05\ \Omega$$

$$\rho_{GeSbTe\text{-}NW} = 13.93 \pm 0.001\ m\Omega cm$$

The contact resistance was employed to determine the effect (extremely detrimental) of an interfacial resistance to the Joule heating in the nanowire by finite elements simulation, as will be shown in the following paragraph. The wire resistivity was found to lay between that of hcp-$Ge_1Sb_2Te_4$ (≈ 2 mΩcm) and fcc-$Ge_1Sb_2Te_4$ (≈ 30 mΩcm). The resistivity was expected to be lower; it is thought that this value is affected by a systematic error owing to the incorrect estimation of the nanowire dimensions.

For further details on the electrical modeling of the pulsed I/V in the case of nanowire-based phase change memory devices, see Appendix B.

Electro-thermal simulation

"I warn you, in two second a computer can generate more errors than 200 people in 50 years"
Anonymous

The computation of the 3-dimensional finite elements model detailed in Chapter 4, was carried out according to the physical constraints reported in the following Table 4.3.

Both the "Joule heating" and the "Heat transfer" physical models were required to correctly describe the physical phenomena occurring in the device under investigation. These two modules take into account the heating due to a given current flow (upon application of an

excitation voltage), while iteratively evaluating the temperature rise in the material, as heat flow is generated in the materials and dissipated according to thermal conduction.

It should be pointed out that dissipation by convection and radiation were not taken into account in this model. The former has little effect at the nanosecond time scale of the system, hence the ambient gas acts as an insulator. The latter contributes as T^4, thus being negligible when – as a rule of thumb – the temperature difference between nanowire and ambient is less than ≈ 300 °C.

The physical parameters and the boundary conditions used in the simulation are listed in Table 6.1.

Property	Symbol	Value [unit]	Notes
Si thermal conductivity	λ_{Si}	148 $Wm^{-1}K^{-1}$	★
SiO_2 thermal conductivity	λ_{SiO2}	1.4 $Wm^{-1}K^{-1}$	★
NW thermal conductivity	λ_{NW}	1 W/mK	‡
Pt thermal conductivity	λ_{Pt}	20 W/mK	‡
Nanowire resistivity	ρ_{NW}	13 mΩcm	◊
Platinum resistivity	ρ_{Pt}	4.5 mΩcm	★
Boundary temperature	T_b	293.15 K	•
NW/Pt contact resistance	$R_{FIB\text{-}NW}$	1 kΩ	◊
Pt strip resistance	$R_{FIB,\,Pt}$	$\rho_{Pt}l_{Pt}/(t_{Pt}w_{Pt})$	★

Table 6.1 – Physical parameters and boundary conditions of the model. Notes: ★ values known from literature; ◊ values calculated in the previous paragraphs; • boundary conditions; ‡ values chosen arbitrarily (see text)

Note that, in Table 6.1, the thermal conductivity values for the nanowire and platinum strips are not known and cannot be calculated straightforwardly as little or no data is available in literature on thermal properties of 1-dimensional nanostructures. Besides, the characteristics of FIB-deposited Pt are strongly dependent on the deposition parameters. For these reasons, arbitrary values – indicated by the ‡ symbol – were used for λ_{Pt}: 20 W/mK (somewhat lower that the 71.5 W/mK bulk value[15]), and for λ_{NW}: 1 W/mK (instead of the 1.58 W/mK reported for chalcogenide thin films[16]).

This physical model was computed to determine the stationary solution of the temperature profile and the output is shown in Figure 6.26.

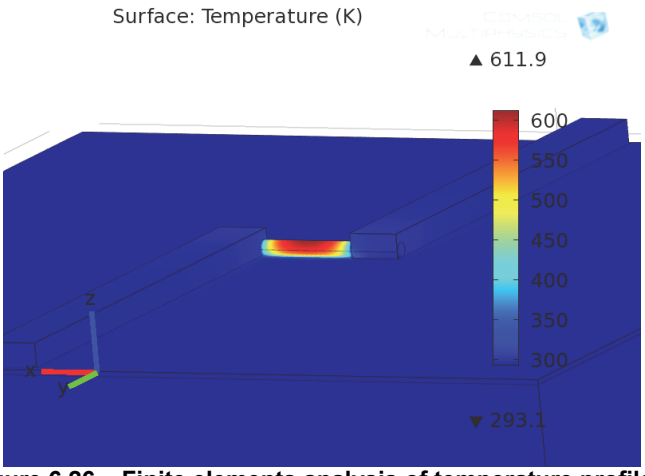

Figure 6.26 – Finite elements analysis of temperature profile

As expected, heat rise was at its maximum in the close center of the nanowire. Moreover the model suggested that the peak temperature reached (611.9 K) was high enough to onset the phase change, the 1st crystallization temperature of most chalcogenides being in the 200 – 300 °C range. Also note that the metal electrodes did contribute prominently to the heat

dissipation (removal) than the SiO_2 substrate, due to the higher thermal conductivity (≈ 20 W/mK the former, 1.4 W/mK the latter).

As mentioned in Chapter 4 (sample preparation), the effect of Pt deposition was crucial to the functionality of the nanowire as a phase-change device. To the end of assessing the effect of sample preparation on the nanowire functionality, another simulation was run with the same parameters as the previous but setting the FIB platinum strip resistivity 1 order of magnitude higher (ρ_{Pt}=45 mΩcm). The stationary temperature profile outcome is shown in Figure 6.27.

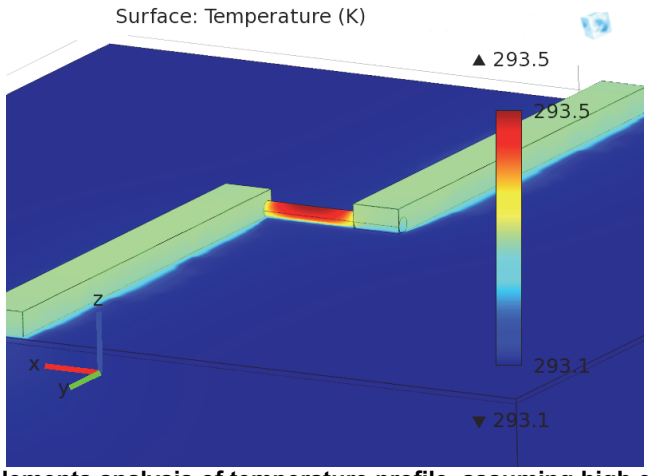

Figure 6.27 – Finite elements analysis of temperature profile, assuming high electrode resistivity

In this second simulation, the temperature rise in the nanowire was remarkably lower (ΔT = 0.4 K), clearly not sufficient to onset the phase change. In addition, most of the voltage drop (not shown) occurred across the longer, more resistive, electrodes. This result proved that poor preparation of electrodes by FIB can prevent phase transition – as was the case for the shorter nanowire devices which did not exhibit threshold switching.

Finally, another simulation was carried out to evaluate the effect of the nanowire/platinum interfacial resistance. In this run, a contact resistance term was added to the original model. By setting $R_{FIB\text{-}NW}$=1 kΩ (roughly the value found in the previous paragraph), the nanowire temperature profile exhibited a marked decrease. As shown in the following Figure 6.28, the maximum temperature reached was 493.6 K, which is barely sufficient to achieve crystallization of – for instance – GeTe material.

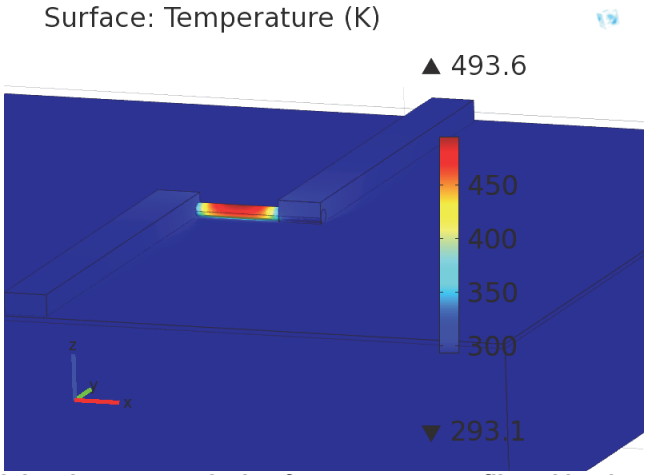

Figure 6.28 – Finite elements analysis of temperature profile, taking into account the nanowire/electrode contact resistance

This simulation proved that the contact resistance is another key factor in the preparation of single nanowires, as it has a detrimental effect on the overall device resistance, and it causes Joule heating to occur at the nanowires edges. This latter effect is undesirable because heat generation ought to be confined to the nanowire.

Adding to the challenge of preparing a nanowire-based phase change device, it should be mentioned that nanowires exhibit less Joule heating in comparison to their bulk counterparts, as it has been recently demonstrated by analytical modeling[17]. In this regard, some Authors have quantified the maximum temperature achievable in such devices, proving that the temperature rise in a 100 nm diameter nanowire could be 0.25 times lower than that of the bulk (its exact value depending on the thermal conductivity of the neighboring layers).

Summary of results on 1-dimensional chalcogenides

The electrical characterization of 1-dimensional nanostructures proved the feasibility of chalcogenide nanowire for non volatile memory applications. Some technological difficulties had to be handled prior to accomplishing the electrically-induced phase transition. These issues have been discussed previously in this Chapter and in Chapter 4.

In particular, nanowires shorter than 1 µm, such as those investigated in the present work, posed an additional challenge as the amount of energy delivered to the device was proportionately smaller (for further details on this subject, see Appendix B). This finding was supported by the lack of switching of the shorter nanowires. It must be noted that this issue could be solved by reducing the leads resistance: indeed, this effect has not been documented in conventional phase change memory cells, where high quality electrodes are employed in thin film technology. Therefore, it is thought that the unfavorable lead/nanowire resistance ratio has a detrimental effect on the nanowire switching functionality, and shall be coped with in the implementation of nanowire for future applications. Further, the electro-thermal simulations shown in the previous paragraph underline the relevance of these issues, which suggest that wire length and neighboring environment play a role in the nanowire heating/quenching thermodynamic.

When integrated into nanoscaled devices, the electrical characteristics of chalcogenides show a distinct trend. The following Table 6.2 sums it up in the light of the results from literature and from the present work.

	GeTe	$Ge_2Sb_2Te_5$	$Ge_1Sb_2Te_4$
thin film / bulk	ΔR ≈ 5, **5** decades	ΔR ≈ 3.5, **3.5** decades	ΔR ≈ 2.5 decades
PCM	V_{th} = 0.9 V ΔR ≈ 4 decades	V_{th} = 1.57 V ΔR ≈ 2 decades	V_{th} = 1.41 V ΔR ≈ 2 decades
NW	V_{th} = 0.8, **0.8** V ΔR ≈ 3.5, **3** decades	V_{th} = 1.8 V ΔR ≈ 2 decades	V_{th} = **1.35** V ΔR ≈ **2** decades

Table 6.2 – Comparison of performances of bulk, PCM, and NW chalcogenides from this work (green) and other Authors' (black)[11,14,18,19]

The main focus is on GeTe, $Ge_2Sb_2Te_5$, and $Ge_1Sb_2Te_4$ (although these findings are thought to hold valid for most chalcogenides). Unsurprisingly, these properties vary when these materials are integrated in nanostructures. Thin chalcogenide films (40 nm or thicker) behave like bulk (as shown in Chapter 5) and their features are shown in the first row. Instead, PCM refers to chalcogenide-based memory devices in the conventional technology. Finally, NW features refer to single nanowire properties.

As a matter of fact, the programming window (ΔR) shrinks in PCM, and further in NW with respect to the resistivity values calculated on thin films. GeTe exhibits the wider ΔR in comparison to the ternary chalcogenides; this result was renowned for thin films, and holds valid in nanostructure as well. The programming window is larger in $Ge_2Sb_2Te_5$ thin films than $Ge_1Sb_2Te_4$, a trend that is roughly preserved in nanostructures too. Concerning the threshold

voltage, it has been proven that the PCM implementation of $Ge_1Sb_2Te_4$ brings the advantage of reducing V_{th}. The results of this work suggest this compound presents a reduced threshold voltage for nanowires as well. In conclusion, compositional control of the chalcogenide is a convenient and dependable way of tuning the device properties.

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7. Conclusions

Novel materials are the frontier for realizing innovative electronic devices. Chalcogenides, in particular, have truly remarkable properties which are still to be fully disclosed. This work was meant to shed more light on the electrical properties of nanostructured chalcogenides for non volatile memory application.

The possibility to scale down the dimension, while preserving the electrical properties and functionalities, is very promising for the implementation of chalcogenides into non volatile memory devices. In this regard, it was found that some intrinsic properties of chalcogenide thin films are mostly unaffected by thickness (down to at least 40 nm), as discussed in Chapter 5. This work showed that crystalline chalcogenides share several features (high carrier density, low mobility, low mean free path), while others are strikingly different (semiconductor-like vs. metallic-like electric conduction, defect- vs. lattice-dominated scattering, arrangement/density of structural defects). It turned out that these properties vary over a great range and, most notably, are tunable by compositional control.

It is widely agreed that higher-density non volatile memory will require further shrinking of the device size. One way to do so is to employ 1-dimensional nanostructures. The joint use of metalorganic vapor deposition and vapor-liquid-solid self-assembly made it possible to accomplish a 'bottom-up' growth of chalcogenide nanowires. On one hand, employing the MOCVD growth brought the advantage of improved compositional control, thus making it possible to obtain chalcogenide nanowires of $Ge_1Sb_2Te_4$ stoichiometry, never obtained before. On the other hand, the electrical characterization of a single nanowire required lengthy sample preparation which is not convenient on industrial scale and is liable to further improvement. In

this regard, technological issues in the electrical characterization of nanowire devices were highlighted in Chapters 4, 6 and Appendix B.

In Chapter 6, electrical and functional characterization of such nanowires was documented, thus proving the viability of MOCVD-grown nanostructures. In the same section, the figures of merit of these devices were determined and compared to those of other nanowires obtained by conventional vapor transport mechanism. It was found that stoichiometry plays a role in the performance of devices. In addition, it was proven that some of these features (programming window, threshold voltage) are preserved in thin films, PCM, and nanowires. In other words, tuning of the physical properties is a viable and convenient way to engineer the behavior of chalcogenides-based devices.

From the technological point of view, it is foreseeable that actual implementation of nanostructured chalcogenides will depend on the feasibility of integration, growth, and fabrication of these materials into fully 'bottom-up', industrial-scale processes for non volatile memory devices. On the opposite, characterization of the physical properties of chalcogenides will be the next scientific challenge toward the throughout understanding of these materials.

8. Appendixes

The crucial lesson was that the scope of things I didn't know wasn't merely vast; it was, for all practical purposes, infinite. That realization, instead of being discouraging, was liberating.[1]

This section is meant to provide additional information and further details on the characterization techniques used in this work, not included in the experimental section for the sake of brevity.

Appendix A: Correction factor for van der Pauw method

In Chapter 3 the approximate value for resistivity was shown. Actually, the full analytical formula from the original van der Pauw's paper is:

$$e^{\left(-\pi\frac{V_2-V_1}{I}\frac{t}{\rho}\right)}+e^{\left(-\pi\frac{V_6-V_5}{I}\frac{t}{\rho}\right)}=1 \tag{8.1}$$

Because eq. (8.1) is transcendental, its numerical solving is very demanding from the computational point of view (especially at the time of its formulation). An approximation was derived by van der Pauw himself, taking into account the lack of symmetry in the resistivity values, defined as:

$$\rho_A=\frac{\pi}{\ln 2}t\frac{V_2+V_4-V_1-V_3}{4I}f_A \tag{8.2}$$

$$\rho_B=\frac{\pi}{\ln 2}t\frac{V_6+V_8-V_5-V_7}{4I}f_B \tag{8.3}$$

The lack of symmetry, which is indicated by parameters f_A, f_B, can be determined by solving equations:

$$\frac{\frac{V_2-V_1}{V_4-V_3}-1}{\frac{V_2-V_1}{V_4-V_3}+1}=\frac{f_A}{0.693}arc\cosh\left(\frac{e^{\frac{0.693}{f_A}}}{2}\right) \tag{8.4}$$

$$\frac{\frac{V_6-V_5}{V_8-V_7}-1}{\frac{V_6-V_5}{V_8-V_7}+1}=\frac{f_B}{0.693}arc\cosh\left(\frac{e^{\frac{0.693}{f_B}}}{2}\right) \tag{8.5}$$

respectively.

The relationship between f and $\frac{V_2-V_1}{V_4-V_3}$, $\frac{V_6-V_5}{V_8-V_7}$ is shown in the following Figure 8.1:

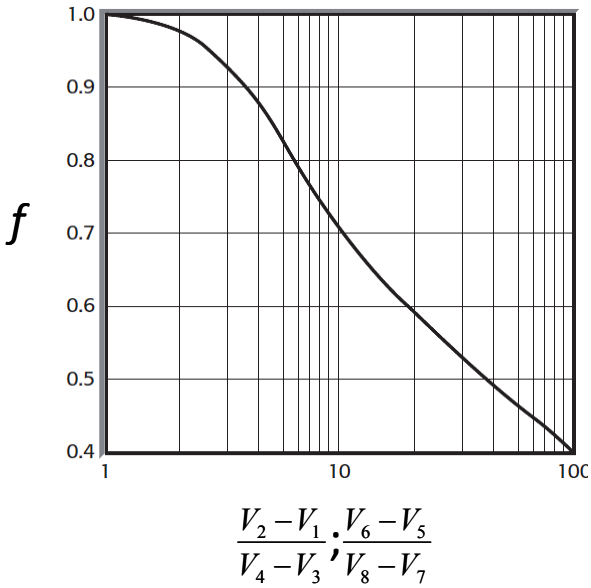

Figure 8.1 – Relationship between measured voltages and factor f in van der Pauw's formula

Note that $f_A = f_B = 1$ for perfect symmetry (which occurs with symmetrical samples like circles or squares when the contacts are equally spaced and symmetrical). The best measurement accuracy is also obtained in this condition. Further, if f_A and f_B are not within 10% of each

other, the sample is not sufficiently uniform to determine resistivity accurately, and should be discarded. In conclusion, and according to Figure 8.1, when the values of asymmetry are very close to each other, no approximation is needed. Because the measuring system reports automatically the recorded value, the simpler formula is employed when these conditions are met; otherwise (i.e. highly asymmetric sample), the exact formula was used.

Appendix B: Electrical model of nanowire-based phase change devices

In this Appendix, the electrical model and the ruling equations for the Pulsed I/V setup will be detailed.

The equivalent electrical model for the Pulse Generator (PG) + device under test (DUT) is sketched in the following Figure 8.2.

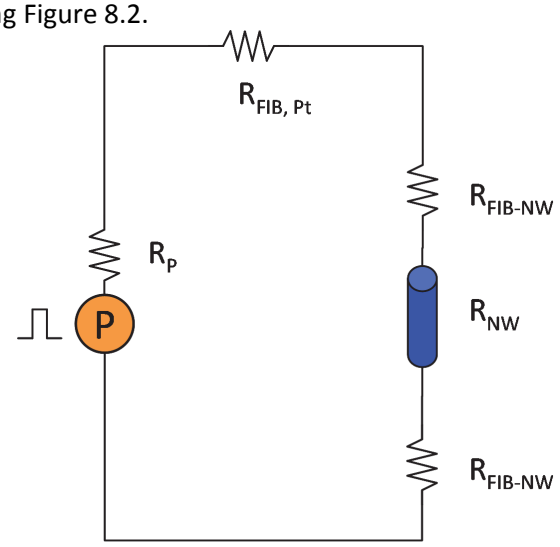

Figure 8.2 – Circuital equivalent of the test fixture

The voltage drop across the nanowire depends on the detrimental effect of the other parasitic series resistances, according to the well-known voltage partition formula:

$$V_{NW} = \frac{V_P}{R_P + R_{Pt} + 2 \cdot R_C + R_{NW}} R_{NW} \tag{8.6}$$

Regardless of the pulse duty cycle, the power dissipated in the nanowire is:

$$P_{NW} = \frac{V_{NW}^2}{R_{NW}} \tag{8.7}$$

Related to the latter, is the energy dissipated in the nanowire (which depends on the voltage pulse width t_P):

$$E_{NW} = P_{NW} t_P = \frac{V_{NW}^2}{R_{NW}} t_P = \left(\frac{V_P}{R_P + R_{Pt} + 2 \cdot R_C + R_{NW}} R_{NW} \right)^2 \frac{t_P}{R_{NW}} = \left(\frac{V_P}{R_P + R_{Pt} + 2 \cdot R_C + R_{NW}} \right)^2 R_{NW} t_P \tag{8.8}$$

In eq. 8.8, the Pt electrode resistance is related to the strip resistivity and geometry according to the well-known formula:

$$R_{Pt} = \frac{\rho_{Pt} L_{Pt}}{t_{Pt} W_{Pt}} \tag{8.9}$$

The nanowire resistance is related to the resistivity thereof (calculated in Chapter 6) and the geometry of the wire – assumed to be cylindrical:

$$R_{NW} = \frac{\rho_{NW} L_{NW}}{A_{NW}} = \frac{\rho_{NW} L_{NW}}{\pi d^2 / 4} \tag{8.10}$$

The contact resistance R_C (also referred to as $R_{FIB\text{-}NW}$ in the picture) is a function of the resistance per unit area, and the contact area between wire and electrode:

$$R_C = \frac{R_{Contact}}{A_{Contact}} = \frac{R_{Contact}}{L_{overlap} \pi d / 2} \tag{8.11}$$

In the following Table, data and geometrical values used in the calculation are shown.

Property	Symbol	Value [unit]
Pulse generator resistance	R_P	50 Ω
Pulse duration	t_P	300 ns
Contact width	$L_{Overlap}$	W_{Pt}
NW diameter	d	100 nm
Platinum electrode resistivity	ρ_{Pt}	2 mΩcm
Platinum electrode length	L_{Pt}	5 µm
Platinum electrode width	W_{Pt}	300 nm
Platinum electrode thickness	t_{Pt}	300 nm
Nanowire resistivity	ρ_{NW}	1 mΩcm

Table 8.1

To evaluate the goodness of these values, let us consider two Pt bridge structures which were deposited across two macroscopic aluminum pads. The first bridge was deposited by electron beam deposition and the resistance was:

$$R_{Pt\_ebeam} \approx 540\ k\Omega$$

The second bridge, with the same geometry, was deposited by Ga^+ ion beam:

$$R_{Pt\_ibeam} = 2\ k\Omega$$

The strip geometry was determined by SEM and AFM observation: 15E-6 m long, 700E-9 m wide, 300E-9 thick.

As a result, the resistivity of the FIB-deposited platinum (neglecting the contact resistance between Pt and Al, ideally small) was:

$$\rho_{e\text{-}beam} = 0.00756\ \Omega m = 0.756\ \Omega cm = 756\ m\Omega cm$$
$$\rho_{i\text{-}beam} = 0.000028\ \Omega m = 0.0028\ \Omega m = 2.8\ m\Omega cm$$

These values are very close to the experimental data documented by other Authors[2]. Moreover, the gap between e-beam and i-beam deposition was almost two orders as magnitude, as reported in literature.

Concerning the electrical modeling, the aim was to calculate the energy delivered on the nanowire as a function of wire length L_{NW}. According to some Authors[11], the required energy for amorphization (the most pricey process) of a $Ge_2Sb_2Te_5$ nanowire, as a function of the wire diameter:

$$d=[60\ 100\ 150\ 200]\ nm$$

has been roughly assessed to be, respectively:

$$E=[75\ 100\ 175\ 225]\ pJ$$

In this framework, eq. 8.8 was fed into a MATLAB script, for the case of $Ge_1Sb_2Te_4$ nanowires. Assuming a 5 V, 300 ns voltage pulse, the energy delivered to the wire as a function of its length is shown in Figure 8.3.

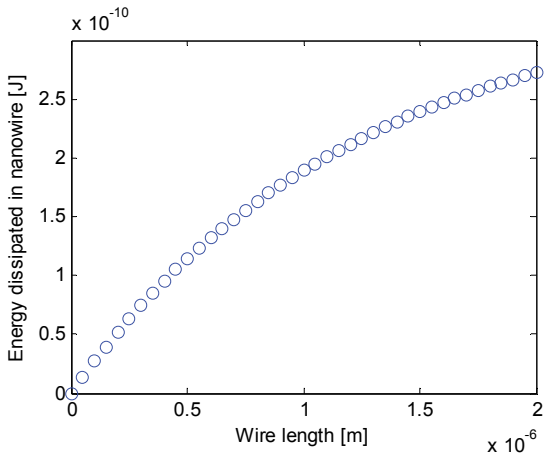

Figure 8.3 – Energy dissipation in crystalline chalcogenide nanowire as a function of length

This result proves that the nanowire has to be at least 0.5 µm long to absorb the required amount of energy for phase change (although a length of 1 or more µm is suggested in actual devices). In addition, experimental evidence of nanowires of various length, discussed in Chapter 6, seems to support this finding.

Note that a state-of-the-art device based on nanowire should account for the detrimental effect of the electrodes by, for example, improving the contact resistance or reducing the electrodes length.

Appendix C: Additional bibliography

The physics of the amorphous phase of solids is a challenging field of study. I tried to provide some insight thereof in Chapter 2. For further reading:

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Appendix D: A Second Note on the Term "Chalcogen"

by Werner Fischer, Emeritus Professor of Inorganic Chemistry, University of Hannover, Germany

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In a recent note Jensen[3] traced the etymology of the term "chalcogen" or "ore former" and showed that many of the derivations of this word given in modern textbooks are incorrect. However, he did not indicate when this term was first introduced into the chemical literature or who first proposed its use. The purpose of this follow-up note is to provide the missing information.

Around 1930, Wilhelm Blitz of the Institute of Inorganic Chemistry at the University of Hannover, Germany, and his staff were engaged in studies concerning the relationship between physical properties (e.g. volume) of chemical elements and their position in the periodic table. In their daily discussions it became useful to refer to certain groups of elements by characteristic names. However, the group of the elements O, S, Se, and Te lacked such a name. In about 1932, one of W. Biltz's co-workers proposed the term "chalcogens" ("ore formers" from *chalcos* old Greek for "ore") for these elements and "chalcogenides" for their compounds. These names quickly became popular in the work group of Hannover because they were analogous to the well-known terms "halogens" ("salt formers") and "halogenides" for the neighboring elements in the periodic table, the majority of halogenides being salts and chalcogenides being ores.

The new terms were soon used in publications by other members of the Biltz group[4,5] and also by outsiders[6,7]. Heinrich Remy, the author of a comprehensive text book on inorganic chemistry, also supported the new term. He became the German member of the Committee of the International Union of Chemistry (later IUPAC) for the Reform of the Nomenclature of Inorganic Chemistry, which met in Berlin and in Rome in 1938. Heinrich Remy's suggestion led to the recommendation "the elements oxygen, sulfur, selenium and tellurium may be called chalcogens and their compounds chalcogenides"[8]. Within just a few years, the term was used worldwide, particularly in textbooks.

None of the above-cited references mentions the name of the original proposer of the new terms. Only in a footnote concerning their justification and usefulness does W. Biltz[9] name his collaborator Werner Fischer[10], the author of this note, as the proposer. Werner Fischer now lives in Freiburg/Breisgau, Germany, and is 99 years old.

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"Whenever I talk with someone, I learn from him"
Gandhi

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Over the last years, I have benefited from the stimulating environment of MDM. Although a relatively small research center, it boasts remarkable researchers and people. I've been learning so much during this time span; as a result, I owe them all something. Simone Cocco for repairing things beyond repair. Antonio Vellei for teaching me the basics – and beyond – of electron beam lithography ("sudo ebl"). Mario Alia for making my clean-room experiments more productive (and entertaining). Olivier Salicio for sharing remarkable moments as my desk neighbor. Grazia Tallarida for AFM/EFM measurements and fruitful discussions. Flavio Volpe for the numerical implementation of the algorithm in eq. 5.1. Roberto Mantovan for fruitful discussion on chalcogenides (and nighttime messages from CERN). Matteo Belli for helpful suggestions on electrical measurements. Andrea Andreozzi and Guido Petretto for being my companions during this PhD course, although on very different tracks. All the other people from MDM – in no special order – for giving me insight and inspiration: Gabriele Congedo, Luca Lamagna, Silvia Vangelista, Roberto Colnaghi, Sabina Spiga, Enrico Prati, Giovanni Mazzeo, Elena Cianci, Marco De Michielis, Alessandro Molle, Gabriele Seguini, Michele Perego, Alberto De Bernardis, Alberto Salinaro, Milka Kutzreba, Alessio Lamperti, Carlo Grazianetti, Davide Rotta, Stefano Paleari, Stefano Brivio, Silvia Baldovino, Francesca Villani, Mara Lanati, Vania Zoccarato, and Anna Grazioli.

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In a long journey, such as this was, sometimes you have to cope with people who thwart you, rather than help. Nevertheless, I have learned something from them too.

Finally, I would like to acknowledge the following Institutions for providing financial support and making it possible for me to keep working in scientific research.

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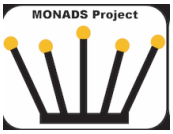

"We decided that when things got too bad we would open a gas station on the desert.
The thought of our gas station seemed to cheer us"
Bruce Merrifield, Nobel Laureate, on his early career at UCLA

List of Publications

- R. Fallica, J.-L. Battaglia, S. Cocco, C. Monguzzi, A. Teren, C. Wiemer, E. Varesi, R. Cecchini, A. Gotti, and M. Fanciulli, "Thermal and Electrical Characterization of Materials for Phase-Change Memory Cell", *J. Chem. Eng. Data* 2009, *54*, 1698–1701, DOI: 10.1021/je800770s
- M. Longo, O. Salicio, C. Wiemer, R. Fallica, A. Molle, M. Fanciulli, C. Giesen, B. Seitzinger, P.K. Baumann, M. Heuken, S. Rushworth, "Growth study of $Ge_xSb_yTe_z$ deposited by MOCVD under nitrogen for non-volatile memory applications", *Journal of Crystal Growth* 310 (2008) 5053–5057. DOI:10.1016/j.jcrysgro.2008.07.054
- M. Longo, R. Fallica, C. Wiemer, O. Salicio, M. Fanciulli, L. Lazzarini, and E. Rotunno "Metal-Organic Chemical Vapor Deposition of Phase Change $Ge_1Sb_2Te_4$ nanowires", submitted for publication (Nanoletters)
- R. Fallica, F. Volpe, M. Longo, C. Wiemer, O. Salicio, A. Abrutis, M. Fanciulli, "Hall characterization of crystalline $Ge_xSb_yTe_z$ thin films", under submission
- A. Vellei, R. Fallica, A. Lamperti, "Spectroscopic Ellipsometry model for optical constants of NiSi formed on Silicon-On-Insulator substrates", submitted for publication (Journal of Applied Physics)

List of conferences

- R. Fallica, J.-L. Battaglia, C. Wiemer, E. Varesi, S. Cocco, M. Fanciulli, “Thermal and electrical characterization of materials for PCM cell”, European Conference on Thermophysical Properties 2008, Pau (France), September 2008, oral presentation

- R. Fallica, C. Wiemer, M. Longo, A. Abrutis, V. Plausinaitiene, E. Varesi, A. Gotti, K. Leitner, M. Fanciulli, R. Bez; International Conference on Amorphous and Nanostructured Chalcogenides (ANC-4), Constanta (Romania), 29 June-3 July 2009, poster on "Mobility and carrier density characterization of crystalline GeTe" [P.31]

- R. Fallica, E. Varesi, L. Fumagalli, S. Grasso, D. Erbetta, S. Spadoni, M. Longo, C. Wiemer, M. Fanciulli, European\Phase Change and Ovonics Symposium (E\PCOS2010), Milano (Italy), September 5th-7th 2010, poster on "Thermal and electrical characterization of N-doped GeTe" [PB8]

- R. Fallica, M. Longo, C. Wiemer, O. Salicio, M. Fanciulli, L. Lazzarini, E. Rotunno, “Electrical characterization of MOCVD-grown chalcogenide nanowires for phase change memory applications”, MRS2011 Spring Meeting, oral presentation

- R. Fallica, M. Longo, C. Wiemer, O. Salicio, M. Fanciulli, L. Lazzarini, E. Rotunno, “Electrical characterization of MOCVD-grown chalcogenide nanowires for phase change memory applications”, E\PCOS 2011, European Symposium on Phase Change and Ovonic Science, September 4th-6th, 2011, Zürich (Switzerland), poster session, Proceedings p.216

- R. Fallica, M. Longo, C. Wiemer, O. Salicio, M. Fanciulli, L. Lazzarini, E. Rotunno, “Electrical characterization of MOCVD-grown chalcogenide nanowires for phase change memory applications”, Leading Edge Embedded NVM Workshop, 17-18 November 2011, Gardanne (France), poster session.

Curriculum Vitae

First name, Surname	Roberto Fallica
Address	via E. Cornalia 19, 20124 Milano (Italy)
Telephone	mobile: +39 347 717 54 47 work: +39 039 603 5938
E-mail	roberto.fallica@mail.polimi.it
Nationality	Italian
Place and Date of birth	Acireale (CT), Italy, 29/06/1979
Gender	Male

Work experience	
Date	June 2007 to present
Employer	Laboratorio MDM (part of Consiglio Nazionale delle Ricerche) in Agrate Brianza (Italy)
Main activities and responsibilities	My main duty is the characterization of the physical properties of thin films of metallic, dielectric and phase-change materials (especially chalcogenide alloys). This includes both experimental activity and data analysis, with a special focus on: a) 4-probe measurement of electrical resistivity (in the van der Pauw configuration) of thin films as a function of temperature; b) the 3 ω technique for the measurement of the thermal conductivity of thin films; c) Hall effect and magnetoresistance of thin films from room temperature to liquid helium (4 K). In addition, I have been directly involved in the development and implementation of new, customized experimental setups to carry out these experiments. My activity includes drafting and disclosing both technical and scientific results by creating internal reports and external publications and participating in conferences.
Education and training	
Date	January 2009 to present
	Ph.D. student at the School of "Nanostructures and Nanotechnology" at the University of Milano-Bicocca (Italy) under the supervision of Prof. Marco Fanciulli. Preparation of a thesis on the characterization of the electronic transport properties of chalcogenide nanostructures for non-volatile memory applications (personal webpage: http://www.nano.unimib.it/php/students.php?id=40)

Date	20th April, 2007
Title of qualification awarded	M.Sc. degree (Laurea) in Electronics Engineering at Politecnico di Milano with final mark of 86/100
Main attended classes	Microelectronics, Solid state physics, Device theory and modelling, Analog and digital electronics, Power electronics, Measurements and instrumentation.
Thesis	"Thermal characterization of phase-change materials by the 3 ω method" carried out at Laboratorio MDM (IMM-CNR) in Agrate Brianza (MB, Italy).
Publications and conferences	R. Fallica, J.-L. Battaglia, S. Cocco, C. Monguzzi, A. Teren, C. Wiemer, E. Varesi, R. Cecchini, A. Gotti, and M. Fanciulli, "Thermal and Electrical Characterization of Materials for Phase-Change Memory Cell", *J. Chem. Eng. Data* 2009, *54*, 1698–1701, DOI: 10.1021/je800770s R. Fallica, J.-L. Battaglia, C. Wiemer, E. Varesi, S. Cocco, M. Fanciulli, "Thermal and electrical characterization of materials for PCM cell" , European Conference on Thermophysical Properties 2008, Pau (France), September 2008, oral presentation R. Fallica, C. Wiemer, M. Longo, A. Abrutis, V. Plausinaitiene, E. Varesi, A. Gotti, K. Leitner, M. Fanciulli, R. Bez; International Conference on Amorphous and Nanostructured Chalcogenides (ANC-4), Constanta (Romania), 29 June - 3 July 2009, poster on "Mobility and carrier density characterization of crystalline GeTe" [P.31]. R. Fallica, E. Varesi, L. Fumagalli, S. Grasso, D. Erbetta, S. Spadoni, M. Longo, C. Wiemer, M. Fanciulli, European\Phase Change and Ovonics Symposium (E\PCOS2010), Milano (Italy), September 5th-7th 2010, poster on "Thermal and electrical characterization of N-doped GeTe" [PB8]. M. Longo, O. Salicio, C. Wiemer, R. Fallica, A. Molle, M. Fanciulli, C. Giesen, B. Seitzinger, P.K. Baumann, M. Heuken, S. Rushworth, "Growth study of GexSbyTez deposited by MOCVD under nitrogen for non-volatile memory applications", Journal of Crystal Growth 310 (2008) 5053–5057. DOI:10.1016/j.jcrysgro.2008.07.054 R. Fallica, M. Longo, C. Wiemer, O. Salicio, M. Fanciulli, L. Lazzarini, E. Rotunno, "Electrical characterization of MOCVD-grown chalcogenide nanowires for phase change memory applications", MRS2011 Spring Meeting, oral presentation R. Fallica, M. Longo, C. Wiemer, O. Salicio, M. Fanciulli, L. Lazzarini, E. Rotunno, "Electrical characterization of MOCVD-grown chalcogenide nanowires for phase change memory applications", E\PCOS 2011, European Symposium on Phase Change and Ovonic Science, September 4th-6th, 2011, Zürich (Switzerland), poster session, Proceedings p.216

	R. Fallica, M. Longo, C. Wiemer, O. Salicio, M. Fanciulli, L. Lazzarini, E. Rotunno, "Electrical characterization of MOCVD-grown chalcogenide nanowires for phase change memory applications", Leading Edge Embedded NVM Workshop, 17-18 November 2011, Gardanne (France), poster session.
Other experiences	May-July 2011 Visiting student at Laboratory of Research on the Structure of Matter, Department of Materials Science and Engineering, University of Pennsylvania, Philadelphia PA (USA), under the supervision of Prof. Ritesh Agarwal
	Aug-Sep 2009 ESONN'09 European School On Nanosciences & Nanotechnologies, Grenoble (France), Session A (49 hour-courses plus practical on MOSFET modelling, characterization, AFM, STM).
	June 2008 – Two weeks experimental activity at Laboratoire TREFLE (Universitè de Bordeaux): thermal conductivity measurements on thin films by photothermal radiometry (PTR).
Personal skills and competences	
Software and Computer skills	Excellent knowledge of Microsoft® Windows® *7*, XP, Vista, and previous operative systems. Good knowledge of Linux and Unix operative systems. Excellent knowledge of the Office/OpenOffice suite programs: Word, Access, Excel, PowerPoint, Outlook. Good knowledge of the MATLAB® software. Good knowledge and experience of National Instruments' LabVIEW™ software. Good knowledge of the programming languages VisualBasic®, C, C++. Good knowledge of COMSOL Multiphysics simulation software.
Languages	
Mother tongue	Italian
Other languages	English – attained internet-based TOEFL in December 2009 with a score of 106/120
	Spanish – good knowledge
Additional information	
	Passed the Italian "Esame di stato per l'abilitazione alla professione di Ingegnere" at Politecnico di Milano. IEEE Graduate Student Member since 01/2010.
Driving licence	Italian "B" license

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