SCUOLA DI DOTTORATO
UNIVERSITÀ DEGLI STUDI DI MILANO-BICOCCA

Department of Physics "Giuseppe Occhialini"

Ph.D. Program in Physics and Astronomy - XXXV cycle
Curriculum in Applied Physics and Electronics

Transceiver Design for Supply-Embedded Communication in Differential Automotive Networks

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Academic Year 2021 - 2022

Abstract

Automotive wire harness has become nowadays a very complex structure as the number of electronic systems and sensors inside a vehicle has increased dramatically. To manage this complexity, and to support the automotive systems of tomorrow, new communication methods need to be investigated.

In this research activity, a Supply-Embedded Communication (SEC) transceiver for differential automotive networks is developed to provide advantages in cost, complexity, and weight. In a Supply-Embedded Communication system, the power supply is merged on the communication bus and hence the number of interconnections is drastically reduced. The proposed approach is intended to be an effective additional physical layer to the Controller Area Network (CAN) which is the most widespread bus in the automotive industry, and hence transmission speed in the order of some Mbps is desired.

Two transmitter topologies based on switching capacitors and their implementation in a first test chip in 180nm CMOS SOI technology are presented. The prototype is validated by communication tests in the laboratory connecting it to a discrete component-based demonstrator receiver board through an unshielded twisted pair cable. A receiver circuit based on StrongArm Latches is designed and integrated into the second version of the prototype to realize a full SEC transceiver. Compared to commercially available solutions, the proposed approach can reach a data transmission rate of 2Mbps making it able to implement high-speed event-driven networks, such as the CAN.

As a side project, a second order curvature compensated bandgap reference circuit is proposed. Voltage references are used in almost every integrated circuit and, one of them is also present in the SEC transceiver prototype to furnish the required bias to the circuit. Although the main project is done in 180nm technology, the side project is developed in 110nm technology for educational purposes. The proposed circuit is validated by simulation in a temperature range from $-40°C$ to $175°C$ in a 6σ process spread. The second order compensation introduces a considerable improvement in performance by reducing the maximum variation from the room temperature to a value lower than $1mV$ in the typical corner.

The motivations and the principle behind this activity are shown in Chapter 1. The transmitter and receiver designs are respectively reported in Chapter 2 and Chapter 3 including layout and simulation results. Chapter 4 shows the top level implementation of the two developed prototypes, while the measurement results are presented in Chapter 5. The proposed bandgap reference circuit is illustrated in Chapter 6. Finally, the conclusions are drawn in Chapter 7.

Abstract

Negli ultimi anni il numero dei sistemi e dei sensori elettronici, utilizzati all'interno degli autoveicoli, è aumentato sensibilmente e, di conseguenza, il loro sistema d'interconnessioni è divenuto uno dei più complessi e critici da progettare. Al fine di gestire tale complessità e di favorire lo sviluppo dell'automobile del futuro, è divenuto quindi necessario studiare nuove soluzioni progettuali.

Nella presente attività di ricerca, viene proposto un ricetrasmettitore Supply-Embedded Communication (SEC) in grado di semplificare il sistema di cablaggio e di ridurre il costo ed il peso dell'autoveicolo. Infatti, nel sistema Supply-Embedded proposto, l'alimentazione è stata integrata sul bus di comunicazione, riducendo notevolmente il numero d'interconnessioni necessario. Il metodo presentato si propone, quindi, come un layer fisico addizionale al Controller Area Network (CAN), il bus attualmente più diffuso nell'industria automotive.

Sono stati realizzati due trasmettitori, basati su capacità di commutazione, ed entrambi sono stati implementati in un test chip in tecnologia 180nm CMOS SOI. Il prototipo è stato validato da test di comunicazione sviluppati in laboratorio, connettendo il chip con un ricevitore a componenti discreti. Un ricevitore basato su StrongArm Latch è stato sviluppato ed integrato nella seconda versione del prototipo, realizzando un ricetrasmettitore SEC completo. Paragonato alle soluzioni già disponibili sul mercato, il metodo proposto consente il raggiungimento di una velocità di trasmissione dati pari a 2Mbps, rendendolo in grado d'implementare reti ad alta velocità come avviene nel bus CAN.

Come progetto secondario, è stato sviluppato un circuito di bandgap reference con compensazione al secondo ordine. I bandgap reference sono presenti ormai in quasi tutti i circuiti integrati, come anche nel ricetrasmettitore SEC oggetto di questo lavoro di tesi, al fine di fornire la necessaria polarizzazione ai circuiti. Per scopi didattici, il progetto secondario è stato realizzato in tecnologia 110nm CMOS SOI, diversamente dal progetto principale. Il circuito proposto è stato validato da simulazioni svolte in un range di temperature da $-40°C$ a $175°C$ in un processo a 6σ. La compensazione al secondo ordine ha consentivo di ottenere una massima variazione dalla temperatura ambiente inferiore ad 1mV nel corner tipico.

Le motivazioni ed il principio alla base del lavoro svolto sono presentati nel Capitolo 1. I design del trasmettitore e del ricevitore sono riportati rispettivamente nel Capitolo 2 e nel Capitolo 3, comprensivi di layout e risultati delle simulazioni. Il Capitolo 4 mostra l'implementazione top level dei due prototipi sviluppati, mentre i risultati delle misure sono illustrati nel Capitolo 5. Il circuito di bandagap reference proposto è riportato nel Capitolo 6 e, infine, nel Capitolo 7 sono tratte le conclusioni.

Contents

Acronyms

BH	Bus High,
BJT	bipolar junction transistor,
BL	Bus Low,
CAN	Controller Area Network,
CMOS	complementary metal-oxide semiconductor,
CTAT	complementary to absolute temperature,
DUT	device under test,
ECUs	electronic control units,
ESD	electro-static discharge,
FPGA	field-programmable gate array,
FS	Floating Switches,
HSS	High-Side Switches,
HV	high voltage,
I/O	input/output,
IC	integrated circuit,
IP	intellectual property,
LED	light emitting diode,
LIN	Local Interconnect Network,
LSS	Low-Side Switches,
LV	low voltage,

MOS	metal-oxide semiconductor,
MV	medium voltage,
NMOS	n-type metal-oxide semiconductor,
PCB	printed circuit board,
PLC	Power-Line Communication,
PMOS	p-type metal-oxide semiconductor,
PRBS	pseudo-random bit stream,
PTAT	proportional to absolute temperature,
QFN	quad-flat no-leads,
RX	receiver,
SEC	Supply-Embedded Communication,
SOI	silicon-on-insulator,
TC	temperature coefficient,
TC1	first test chip,
TC2	second test chip,
TX	transmitter,
URZ	unipolar Return-to-Zero,
VNC	virtual network computing,

CHAPTER 1

Introduction

1.1 Motivation

The automotive industry is living a big transformation as the number of electronic systems and sensors is increasing dramatically. This allows carmakers to improve safety, comfort, and entertainment and to introduce new functions such as Advanced Driver Assistance Systems (ADAS), power-train control, and means for diagnostics. Forecasts on the automotive market suggest that 80% of the innovation in this industry is linked to electronics and that the electronic content growth will rise to 50% by 2030 [1, 2]. As the number of automotive subsystems relying on electronics is increasing, so is the cabling required for their interconnection. Electronic functions, implemented as nodes, are controlled by dedicated electronic control units (ECUs) and are usually connected by a communication bus, the power supply lines, and possibly addressing lines. Since the late 1980s serial communication buses have been used to interconnect the ECUs and signals. Compared to 1-to-1 communication, applying a serial data bus reduces the number of wires by combining the signals on a single wire through time division multiplexing. To handle this level of complexity, many efforts have been done by the automotive industry to standardize the software architectures as well as the communication protocols. Some of the most common Fieldbus technologies used nowadays are the Local Interconnect Network (LIN), the Controller Area Network (CAN), and the FlexRay [3]. LIN is a single-wire, serial network protocol that provides time-triggered communications up to 20 Kbit/s and it is meant for inexpensive communication without reliability or timeliness requirements. CAN is a message-based protocol that provides event-triggered communication at speed of up to 1 Mpbs where each message or data frame is transmitted sequentially. It is the most commonly used Fieldbus thanks to its versatility and relatively high data rate. FlexRay provides time-triggered communication at speeds up to 10 Mbps. It is meant for safety-critical systems, ensuring high data rates and fault tolerance but it is usually more expensive than other Fieldbus.

However, a single modern vehicle can contain up to 150 ECUs, making the wire harness a very complex system that results in high production costs, increased weight of the car,

and extraordinary consumption of raw material [4]. As a consequence, new solutions to drastically reduce the amount of cabling in the near future need to be investigated. In this research topic, a communication approach that merges the power supply on the communication bus is analyzed, since the available spectrum is being unused. This approach, named Supply-Embedded Communication (SEC), is designed to be comparable to CAN since this is the most widespread protocol. A data rate of 2 Mbps is therefore set as a target. Communication methods on the supply lines, known as Power-Line Communication (PLC), are already used in other contexts such as industrial communication, Ethernet, and smart home appliances. However, unlike these applications, the power supply voltage in a car is a DC battery, and furthermore, the compatibility and safety requirements are much more stringent.

The feasibility of PLC systems in an automotive environment has already been proven by commercially available proposals based on a carrier modulation [5–8] but the resulting data rate $\leq 500kbps$ and latency would disable the use in high-speed event-driven applications ($\geq 1Mbps$). Therefore, in this work, a base-band SEC system is examined to realize a CAN protocol with a modified physical layer. The result is a system of n nodes connected to each other only through the communication bus as shown in Fig. 1.1. In this Thesis, the communication bus is referred to as Bus High (BH) and Bus Low (BL) for the analogy with the CAN. Each node must be able to transmit and receive signals on the bus and therefore must include a transmitter (TX) and a receiver (RX). The basic concept consists in injecting defined charges on the transmission line through switching capacitors to obtain signal pulses for communication. Such charge injection principle and some preliminary considerations are detailed in Section 1.2.

This research project was done in collaboration with Andreas Ott. In his Thesis [9], more details on the concept, and the architecture of the test chips including the power supply system, the digital control, and the protection scheme can be found, while this Thesis focuses on transceiver design, layout, simulations, and measurements.

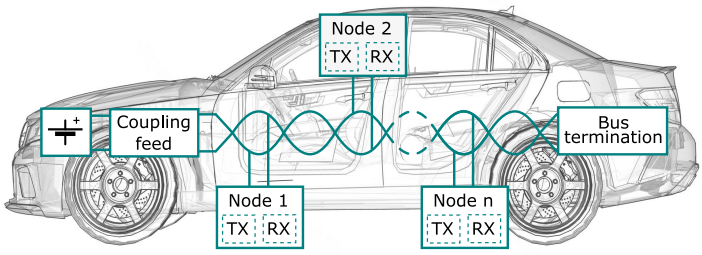

Figure 1.1: Supply-Embedded Communication concept

1.2 Charge Injection Concept

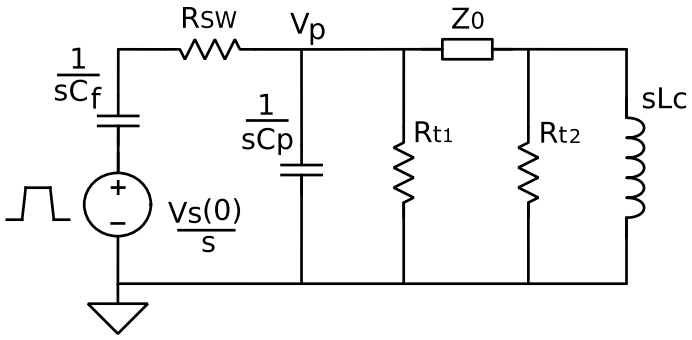

Figure 1.2: Equivalent s-domain model of the charge injection

To understand the principle of charge injection, and to evaluate some design specifications, the discharge phase of a functional switching capacitor C_f was studied. In Fig.1.2 the equivalent s-domain model of a charge injection event is shown. C_f is connected by a switch with finite on-resistance R_{SW} to the transmission line. The line has characteristic impedance $|Z_0|$ and, it is terminated by resistor R_{t1}. The capacitance C_p associated with the physical implementation aspects is also included. In a SEC, since supply and communication are merged on the same line, a coupling feed from the power source is needed to separate it from the communication channel [10]. In the following analysis, the coupling feed is composed of L_c and R_{t2}, and the inductance L_c is assumed to be sufficiently high so that $X_{Lc} >> |Z_0|$ at 10MHz. Assuming that the capacitor is initially charged to the DC supply level $V_s(0)$, the pulse waveform of a discharge event can be evaluated by solving the inverse Laplace transform of the presented scheme:

$$V_p(t) = V_{peak}\left(e^{-\frac{t}{\tau_2}} - e^{-\frac{t}{\tau_1}}\right), \tag{1.1}$$

The peak voltage, the rising (τ_1), and falling (τ_2) time constants are:

$$V_{peak} = \frac{Q_{C_f} R_t}{\kappa} \approx \frac{Q_{C_f} R_t}{C_p R_t + C_f\left(2R_{sw} + R_t\right)} \tag{1.2}$$

$$\tau_{1,2} = \frac{2C_f C_p R_{sw} R_t}{C_p R_t + C_f\left(2R_{sw} + R_t\right) \pm \kappa}. \tag{1.3}$$

with

$$\kappa = \sqrt{\left(C_p R_t + C_f\left(2R_{sw} + R_t\right)\right)^2 - 8\, C_f C_p R_{sw} R_t} \tag{1.4}$$

and $R_t = R_{t1} = R_{t2}$. Simulation results with different sizes of C_f are shown in Fig.1.3 where it was assumed to design a switch with $R_{sw} = 10\Omega$ and, $R_t = |Z_0| = 100\Omega$, $C_p = 10pF$, $L_c = 100uH$, $V_S(0) = 12V$. The resulting τ_2 values are $30.0ns$, $59.5ns$ and $118.0ns$ respectively for $0.5nF$, $1.0nF$ and $2.0nF$.

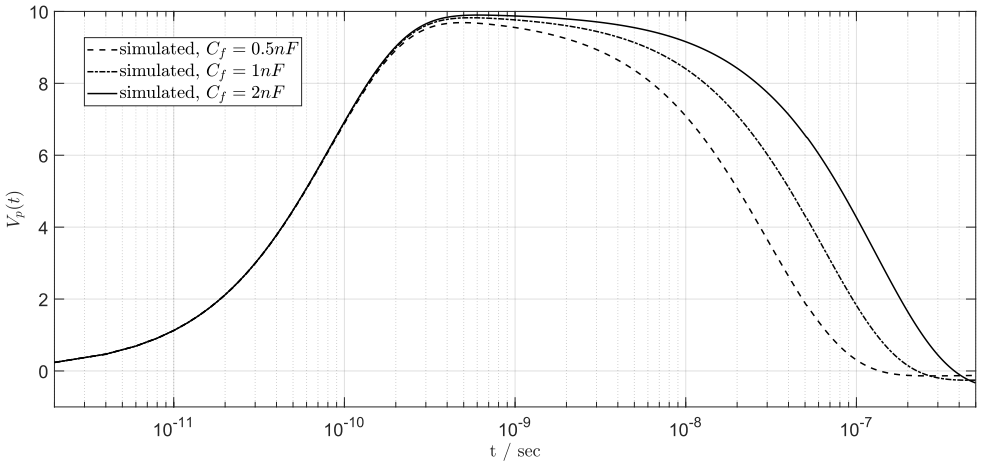

Figure 1.3: Simulation result of a discharge event

To reach a data rate of 2Mbps, it can be deduced that the switching capacitor should be $\leq 2nF$ so that $\tau_2 \approx 0.1$ to $0.15DR^{-1}$ where DR is the data rate. This analysis leads to considering external capacitor C_f in the developed proposal, both for the area occupation and the higher flexibility. More details about the modeling and system specifications are reported in [9].

CHAPTER 2

Transmitter Design

In this chapter two Supply-Embedded Communication transmitter implementations based on switching capacitors are proposed. The first circuit, named H-Bridge topology, is shown in Section 2.1 and it requires 4 switches and 1 external capacitor. The second proposal, named 3-Switches topology and described in Section 2.2, instead requires only 3 switches but 2 external capacitors. Section 2.3 details the implementation and the stand-alone simulations of the needed switches. Finally, Section 2.4 shows the composition of the two transmission circuits and some simulation results.

2.1 H-bridge Transmitter Topology

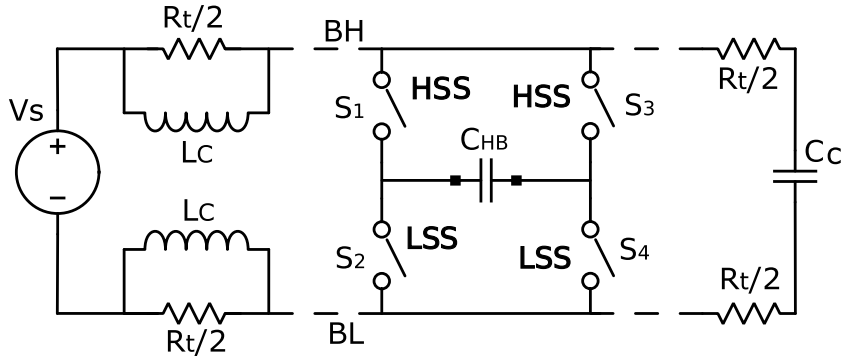

Figure 2.1: H-Bridge TX Topology

The first transmitter topology is the H-Bridge implementation of Fig. 2.1. The supply is applied on the communication bus through the coupling feed composed of $R_t/2$ and L_c. Moreover, the line is terminated by an ac-coupling capacitor (C_c) and two series $R_t/2$ resistors. The circuit consists of a switching capacitor (C_{HB}), which can be connected to the bus through two equal High-Side Switches (HSS), S_1 and S_3, and two equal Low-Side Switches (LSS), S_2 and S_4, which operate in an H-Bridge topology. The circuit commutes among three possible states, as described in Table 2.1, which are alternating at each received data edge. Assuming that C_{HB} is initially discharged, at the first Charge-State

(e.g. Charge 1-4) is it charged to $Q_{CHB} = C_{HB} \times V_S$. As a guard against overlap and unwanted cross currents between the transmission rails, an Open-State is always placed after a charge event, during which the charge in C_{HB} is preserved. In the next step, the second Charge-State (e.g. Charge 2-3) is reconnecting the capacitor to the communication line and is charging it to $-Q_{CHB}$. As illustrated in Fig. 2.2, a drop on the differential bus $B_H - B_L$ occurs at each received data as a result of the charge transferred from the line itself to C_{HB}.

Table 2.1: States of H-bridge Transmitter Topology

State	S_1 , S_4	S_2 , S_3	Description
Open	Open	Open	C_{HB} not connected. Charge is preserved
Charge 1-4	Close	Open	charge accumulated during Charge 2-3 phase is recharged to V_S level
Charge 2-3	Open	Close	charge accumulated during Charge 1-4 phase is recharged to $-V_S$ level

The obtained timing constant (τ_{charge}), and the average current consumption (I_{HB}) can be evaluated as follows:

$$\tau_{charge1-4,2-3} = (R_t/2 + R_{HSS} + R_{LSS}) \times C_{HB} \tag{2.1}$$

$$I_{HB} = 2C_{HB} \times V_S \times DR \tag{2.2}$$

where DR is the data rate, and uniform distribution of '0' and '1' and a costant message stream are supposed. The transmitted signal is unipolar and thus a pre-coding is needed since falling or rising edges of the data signal cannot be distinguished. Hence, for an uncoded data stream applied to the TX, the protocol frame structure needs to be taken into account so that a message header like in [11] can be used to assign the correct data polarity. But the simplest encoding to resolve the ambiguity is to encode the data as a unipolar Return-to-Zero (URZ) stream [12].

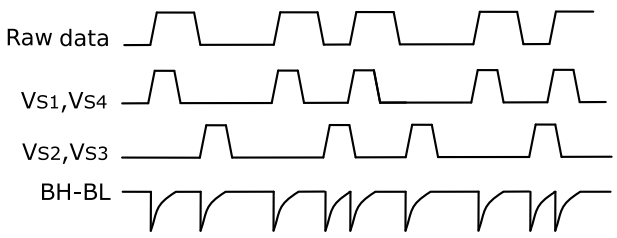

Figure 2.2: Example of data transmission in H-Bridge TX Topology

2.2 3-Switches Transmitter Topology

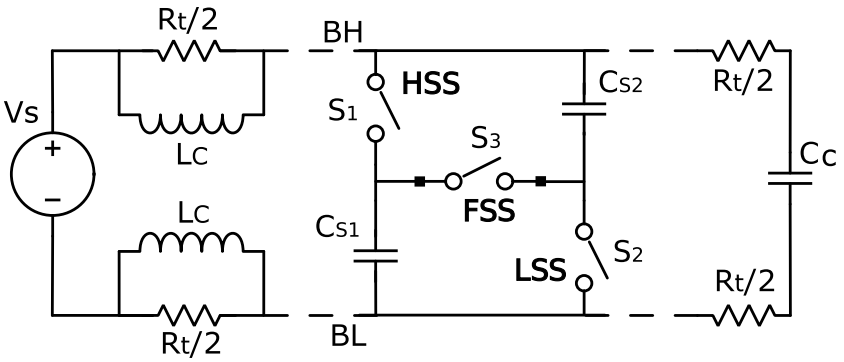

Figure 2.3: 3-Switches TX Topology

The second proposed transmitter topology is the 3-Switches switching capacitor scheme of Fig. 2.3 where two capacitors (C_{S1}, C_{S2}) are charged and discharged according to the 3 possible states described in Table 2.2. During the Charge-State C_{S1} and C_{S2} are charged in parallel through the HSS S_1 and the LSS S_2 to $Q_{CH} = 2C_S \times V_S$, where $C_S = C_{S1} = C_{S2}$. In the next step, the capacitors are discharged in series through the Floating Switches (FS) S_3 to $Q_{DH} = \frac{1}{2}C_S \times V_S$. Similar to the H-Bridge, an Open-State is placed in between to avoid cross currents and during which the charges are preserved. As result, as shown in Fig. 2.4, positive and negative pulses appear on the differential bus and so the data polarity can be recovered directly. Unlike the H-Bridge, the states are not symmetrical and, the charging (τ_{charge}) and discharging ($\tau_{discharge}$) timing constants are not equal:

$$\tau_{charge} = (R_t/2 + (R_{HSS}//R_{LSS})) \times 2C_S \tag{2.3}$$

$$\tau_{discharge} = (R_t/2 + R_{FS}) \times C_S/2 \tag{2.4}$$

The average current consumption (I_{3S}) can be evaluated as

$$I_{3S} = C_S/4 \times V_S \times DR \tag{2.5}$$

and since the charge is partially reused, the consumption is reduced by a factor of 2 compared to the one in the H-Bridge TX. Assuming that the same data rate and the same capacitors size are applied, the current consumption is thus 8-times less than in the previous approach.

Table 2.2: States of 3-Switches Transmitter Topology

State	S_1 , S_2	S_3	Description
Open	Open	Open	C_{S1}, C_{S2} not connected. Charges are preserved
Charge	Close	Open	C_{S1}, C_{S2} are connected in parallel to the bus and charged to V_S
Discharge	Open	Close	C_{S1}, C_{S2} are connected in series and discharged to $V_S/2$

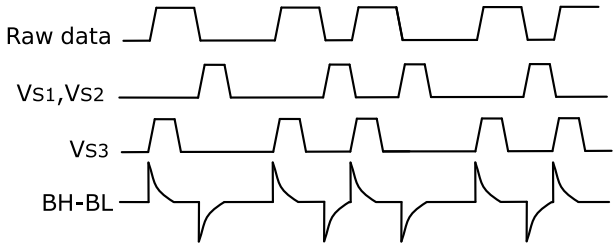

Figure 2.4: Example of data transmission in the 3-Switches TX Topology

2.3 High-Voltage Switches Design for TX circuits

The designs of the transmitters proposed in Fig. 2.1 and Fig. 2.3 require proper switches functions. Efficient low-side switch (LSS, connected to ground), high-side switch (HSS, connected to the power supply), and floating switch (FS, not directly connected to ground or supply), are required. According to equations (2.1),(2.3),(2.4), assuming that switching capacitors of $\approx 1nF$ are used, switches with on-resistance of $\approx 10\Omega$ (and in any case $\leq 30\Omega$) are required to keep the termination resistance dominant and to reach a data rate of 2Mbps. Table 2.3 reports the chosen technology for this project which is an XFAB 180nm silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) technology and it includes high voltage (HV) transistors up to 40V in addition to low voltage (LV) transistors at 1.8V and medium voltage (MV) transistors at 5V [13]. Since the pulses over the communication bus can be up to $2 \times V_S$, where $V_S = 12V$ is the battery voltage, HV devices are required as switches.

The switches are driven by controlled current sources properly designed by using MV transistors. Both the HV and the MV devices have a gate-source voltage range from $-5.5V$ to $5.5V$ which is always ensured to guarantee safe operations even when the pulses appear over the transmission lines. Note that the circuits share a common current master mirror (CM) of $10\mu A$. The resistors used in the following design are poly and high-R poly resistors.

Table 2.3: Selected properties of the wafer process

Process name	XT018
Metalization option	Al, 5 thin, 1 thick (top)
Isolation	BOX, DTI
LV transistors	1.8V
MV transistors	5V
HV transisors	40V
Capacitors	fringe, p-type varactor
Resistors	diffusion, well, poly and high-R poly

2.3.1 Low Side Switch

The LSS is implemented by an HV n-type metal-oxide semiconductor (NMOS) sized with $L = 0.4\mu m$ and $W = 1mm$ to realize a nominal 9Ω on-resistance switch. The full design is shown in Fig. 2.5 where M_{L0} is the LSS device. The source is directly connected to the Bus High (BH) while the drain is connected to the external capacitor pad C_L (i.e. C_{HB} or C_{S2}) through the electro-static discharge (ESD) protection diode D_{L0}.

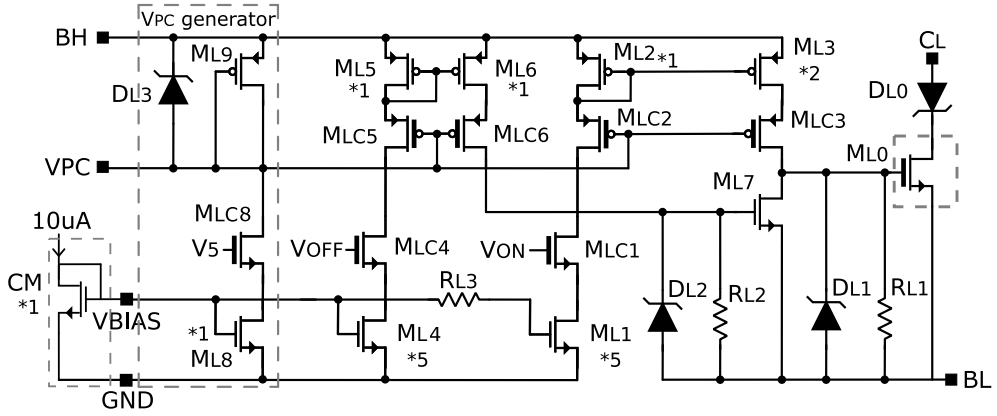

Figure 2.5: LSS schematic

The switch is turned on by the current source referred to ground M_{L1} controlled by the signal V_{ON} applied on the gate of the corresponding cascode HV NMOS M_{LC1}. The generated current is 5 times bigger than the $10\mu A$ master and is doubled again by the p-type metal-oxide semiconductor (PMOS) mirror composed of M_{L2} and M_{L3}. The resulting $100\mu A$ current flows into R_{L1} and pulls up the gate of M_{L0} turning it on with a timing constant given by $R_{L1} \times C_{GSML0}$. C_{GSML0} is estimated to be $\approx 720pF$ in saturation, while R_{L1} can be selected equal to $50k\Omega$ so that $V_{GSML0} = R_{L1} \times I_{ML3} = 5V$ in steady state. Moreover, a stack of diode-connected PMOSs (D_{L1}) is placed as protection clamping the voltage between its terminal, and hence between gate and source of M_{L0}, to $5.5V$.

Similarly, the signal V_{OFF} controls the switching off of the LSS. A $50\mu A$ current is enabled to flow from M_{L4}, through M_{L5} and M_{L6}, to R_{L2} so to turns M_{L7} on. Consequently, the gate of M_{L0} is pushed down to ground and the LSS is turned off. Resistor $R_{L2} = 25k\Omega$ is sized to get $V_{GSML7} = R_{L2} \times I_{L6} = 5V$, while D_{L2} is a stack of diode-connected PMOSs used as protection. Since M_{L7} is a small MV device, its C_{GS} is just a few pF, thus its turn-on timing constant $R_{L2} \times C_{GSML7}$ can be neglected and the LSS turn-off timing constant can be evaluated just as $C_{GSML0} \times (R_{L1}//ron_{ML7}) \approx C_{GSML0} \times ron_{ML7}$.

Finally, note that all the PMOS cascodes are constantly on thanks to the VPC voltage applied to their gates. This is generated by a dedicated block that is shared between all the switches and it is here illustrated. A current tail is provided by M_{L8} and is applied to the diode-connected device M_{L9}. Similarly to the previous ones, D_{L3} is a stack of diode-connected PMOSs and is used as gate-source protection.

Standalone post layout simulations in a 6σ process spread in a temperature range from $-40°C$ to $125°C$ were carried out to evaluate the transition times of the designed switch. Ideal 14V DC voltage and $10\mu A$ current sources were used as well as a load capacitor of $1nF$. The turn-on and turn-off in the typical corner are shown in Fig. 2.6 and are evaluated to be respectively $12.8ns$ and $16.2ns$ by referring to the threshold voltage V_{TH}. In the worst corners, times lengthen and become $28.7ns$ for turning on and $22.5ns$ for turning off.

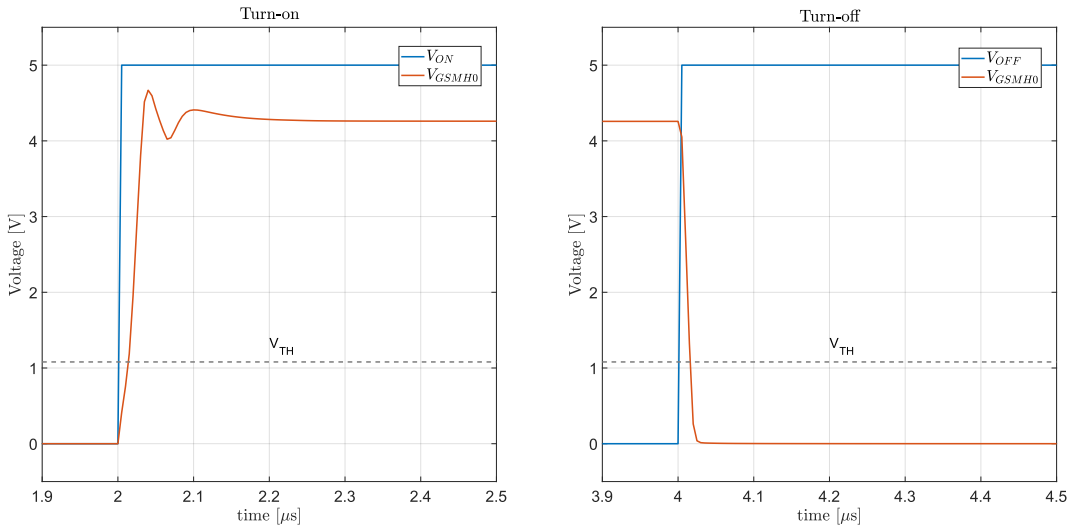

Figure 2.6: LSS turn-on and turn-off times in typical conditions

2.3.2 High Side Switch

Ideally, a perfect matching between the HSS and the LSS is desired to have a perfectly symmetrical structure. One solution to achieve this target can be to use an HV NMOS

also as HSS. To fully charged the load capacitor, a bootstrap circuit is needed. A possible implementation is shown in Fig. 2.8 where M_{B0} is the main switch and the pad C_L (i.e. C_{HB} or C_{S1}) is the connection to the load.

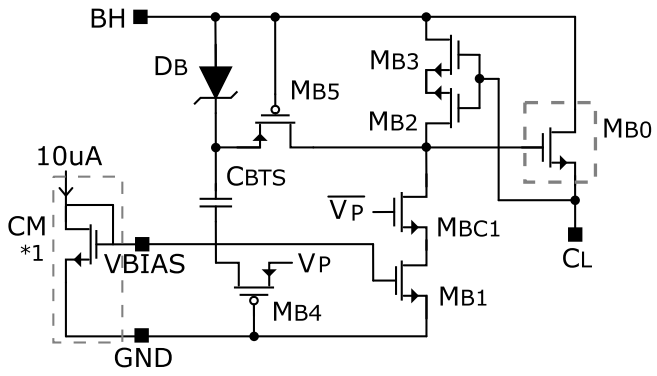

Figure 2.7: HSS bootstrap schematic

Initially, V_P is assumed to be low so that M_{B4} is off, C_{BTS} is charged to the DC value of BH (i.e. V_S), while M_{BC1} is on and a push down current keeps the HSS off. The V_{GS} of M_{B0} is kept below the maximum limit by level shifters M_{B2} and M_{B3}. Once that V_P rises, M_{BC1} is turned off and M_{B4} is turned on. The charge stored in C_{BTS} is shifted up to the bootstrapped voltage $V_{BTS} = V_S + V_P$. Consequently, M_{B5} is turned on and the bootstrapped voltage is transmitted to the gate of M_{B0} turning it on. The diode D_B allows the current to flow only in one direction preventing V_{BTS} to instantly back to V_S and, moreover, it acts as gate-source protection for M_{B5}.

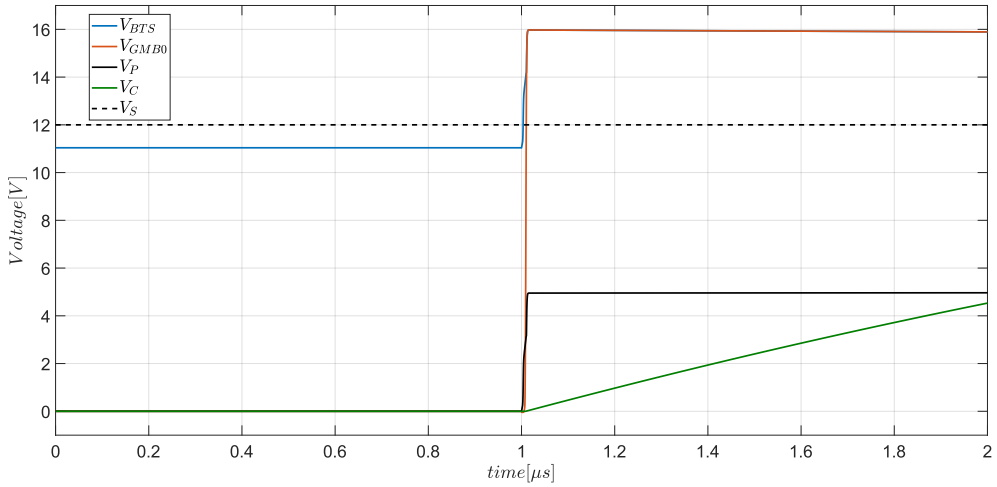

Figure 2.8: HSS bootstrap circuit concept simulation

However, this circuit suffers from some limitations making the implementation difficult:

- assuming the load capacitor is not charged, i.e. $V_L = 0V$, if M_{B0} is switched on by the bootstrap voltage, then its V_{GS} exceeds the maximum value allowed by the technology;
- in case of the HSS does not require to be turned on, but a pulse appears on the transmission bus (this is, for instance, the case of the switch S_3 during the Charge 1-4 phase of Tab.2.1), unwanted turn-on of M_{B5} can happen. An always-off system should be designed to prevent both this event as well as the overlap between on and off states;
- to design a 9Ω device, M_{B0} needs to be a large device, and therefore its C_{GS} is also relevant. Thus, the bootstrap capacitor is estimated to be about $100pF$ to provide sufficient charge and occupies a non-negligible area.

For these reasons it was preferred to develop the HSS in a complementary way to the LSS using an HV PMOS as shown in Fig. 2.9. Due to the lower mobility, to obtain the same nominal on-resistance of 9Ω, M_{H0} is sized around 3 times bigger than the LSS, and thus $L = 0.5\mu m$ and $W = 3mm$. As drawback, its C_{GS} is also 3 times bigger and higher currents are needed to get the same performances as in the LSS. The source is connected to BH while the drain is connected to the external pad through an ESD protection diode.

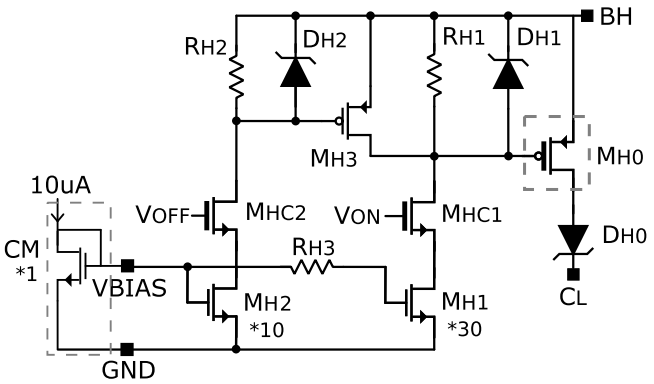

Figure 2.9: HSS schematic

The switch is turned on by a $300\mu A$ pull-down current generated by M_{H1} and enabled by the signal V_{ON} applied on the corresponding cascode device. The current flows into resistor $R_{H1} = 16.5k\Omega$ so that M_{H0} is turned on and $V_{SGMH0} = R_{H1} \times I_{MH1} = 5V$ in steady state. The timing constant is given by $C_{GSMH0} \times R_{H1}$ and, compared to the LSS, a higher current is applied to obtain a similar behavior.

The off state is activated by rising V_{OFF} to apply a $100uA$ pull-down current on the gate of the MV PMOS M_{H3} ($R_{H2} = 50\Omega$). Similar to the LSS, the turn-off constant can be evaluated as $C_{GSMH0} \times (R_{H1}//ron_{MH3}) \approx C_{GSMH0} \times ron_{MH3}$ where the turn-on time of M_{H3} is neglected. Stacks D_{H1} and D_{H2} are also placed to ensure safe operations.

Standalone post layout simulations in the typical corner are shown in Fig. 2.10 for transition times. Simulations were carried out in a temperature range from $-40°C$ to $125°C$ and with an ideal voltage source and current feed. The load capacitor was still supposed equal to $1nF$. Turn-on time is $19.9ns$ in typical conditions and $30.7ns$ in the worst corner. As desired, the result is very similar to the LSS making the structure as symmetric as possible. Turn-off times instead are $3.9ns$ and $4.3ns$ in typical and worst corners respectively.

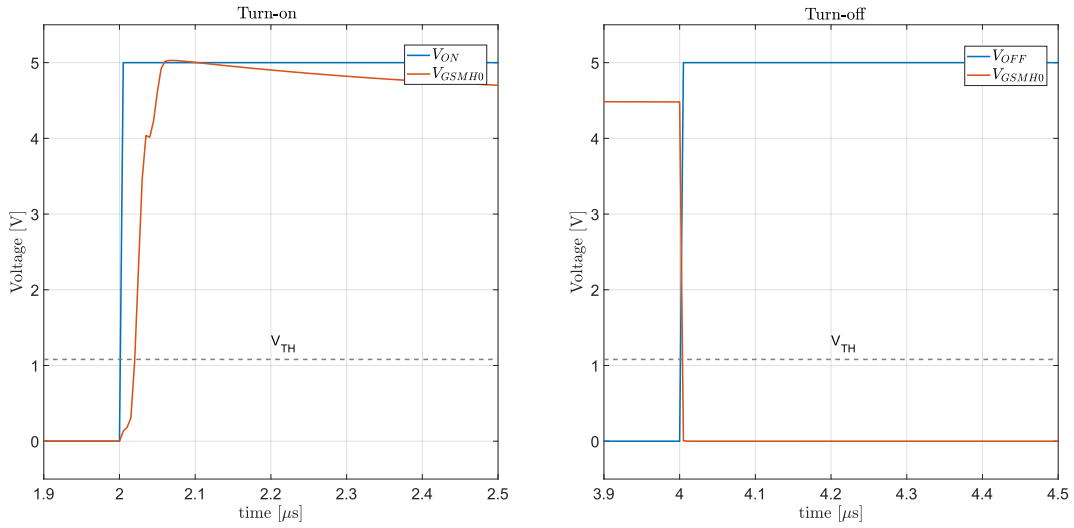

Figure 2.10: HSS turn-on and turn-off times in typical condition

2.3.3 Floating Switch

For the 3-Switches transmitter, a third kind of switch is required. Since it is connected between two floating points, it is called Floating Switch (FS), and it is the most demanding one to design. The schematic is proposed in Fig. 2.11, where the HV NMOS M_{F0} is the FS device. According to Fig. 2.3, its source is connected to the node between C_{S2} and the LSS S_2, which varies between 0 and $V_S/2$, and its drain is connected to the node between C_{S1} and the HSS S_1, which varies between V_S and $V_S/2$. M_{F0} dimensions are $L = 0.4\mu m$ and $W = 1mm$ realizing a nominal 9Ω on-resistance switch.

When $V_{ON} = 5V$, M_{F1} operates as a current source providing a current 5 times bigger than the $10uA$ CM. The generated current passes through the PMOS unity factor

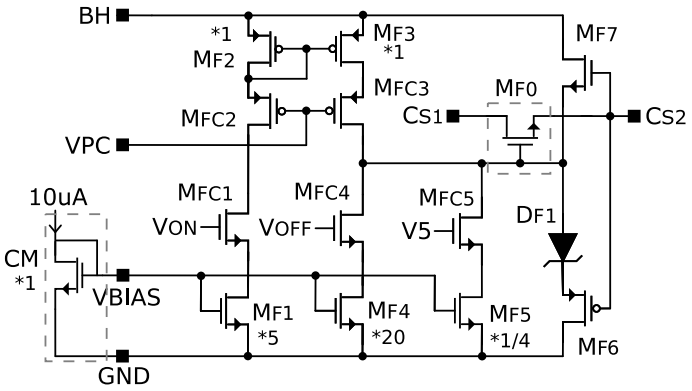

Figure 2.11: FS schematic

current mirror consisting of M_{F2} and M_{F3}, and pulls up the gate of M_{F0} turning the FS on. M_{F6} operates as a source follower and keeps V_{GSMF0} below the upper limit of the technology. A stack of diode-connected PMOSs (D_{F1}) is placed to ensure also a high overdrive: $V_{GSMF0} = V_{SGMF8} + V_{DF1} = 5V$. The turn-on timing constant is dominated by the C_{GSMF0} which is estimated to be around $720pF$ in saturation.

The off branch is enabled when $V_{OFF} = 5V$ so that M_{F4} generates a $200uA$ pull-down current to turn off the switch. The NMOS M_{F7} operates as a source follower and ensures that the V_{GSMF0} is not violating the lower limit of the functional range. In the case of both V_{ON} and V_{OFF} are down, and the 3-Switches TX is not required, a permanent $2.5uA$ pull-down off current is applied by M_{F5} to ensure a no floating gate.

The result of post layout simulations of the turn-on and turn-off are shown in Fig. 2.12

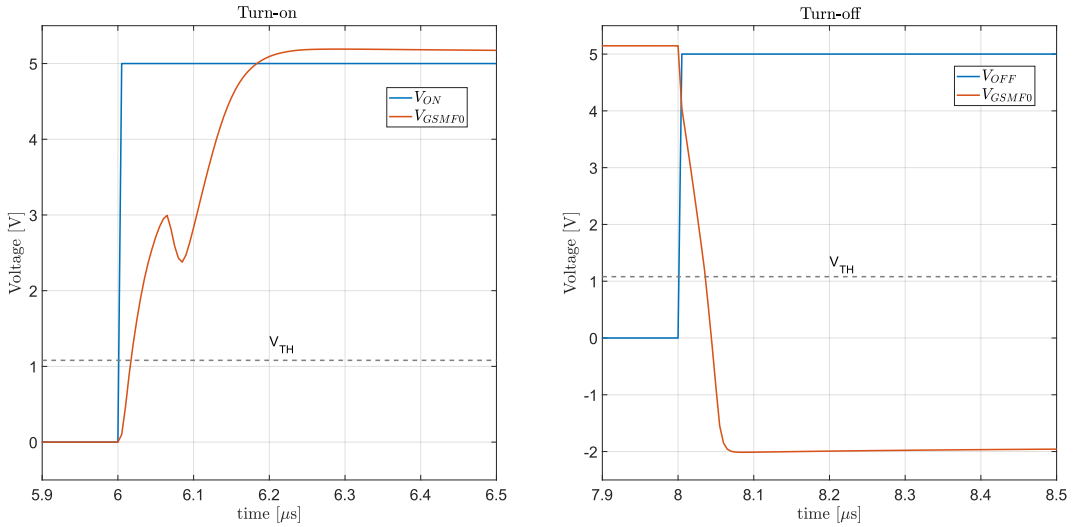

Figure 2.12: FS turn-on and turn-off times in typical condition

where switching capacitors of $1nF$ and ideal sources were used. The typical values are $17.46ns$ and $36.43ns$ respectively, while in the worst corner are $21.7ns$ and $43.4ns$.

2.4 Transmitters Implementation

With the presented switches design, the two transmitter circuits of Fig. 2.1 and Fig. 2.3 can be implemented. The layout views of the H-Bridge topology and the 3-Switches topology are respectively shown in Fig. 2.13 and Fig. 2.14 where the switches are indicated by labels. The size difference between the HSS and the LSS is immediately evident, while the FS has the same size as the LSS even if for practical reasons the single-finger-dimension × number-of-fingers ratio is different. The H-Bridge circuit occupies an area of $434\mu m \times 220\mu m$ while the 3-Switches circuit occupies $315\mu m \times 220\mu m$ and, since it requires one switch less, is about 28% smaller.

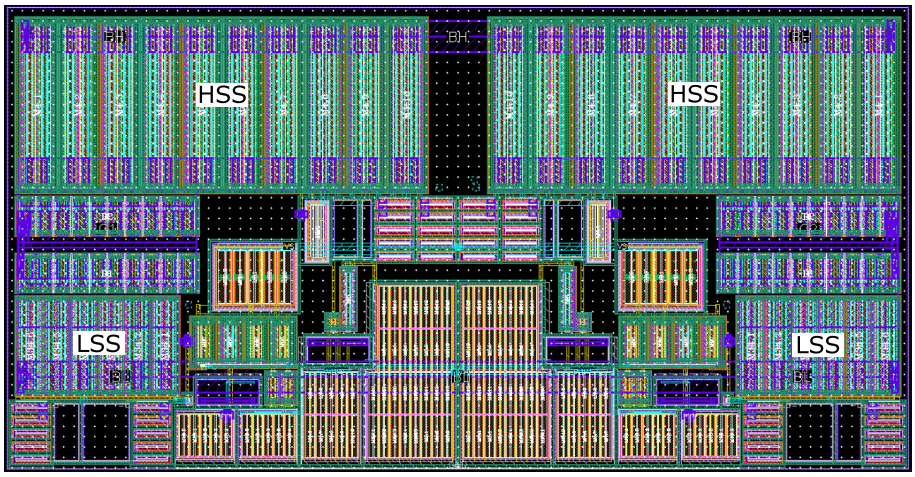

Figure 2.13: Layout view of the H-Bridge transmitter circuit

The designs were simulated in Virtuoso by Cadence in a temperature range from $-40°C$ to $125°C$ over corners in a process spread at 6σ. The H-Bridge topology test bench is shown in Fig. 2.15. The supply source is equal to $14V$, the load capacitor is $0.8nF$, while the coupling system is composed of $R_t = 50\Omega$, and $L_C = 100\mu H$. The control signals for the switches are generated by a Verilog code which implements in a loop the four states of Table 2.1. Each phase has a duration of $500ns$, and so a pulse is expected every $1\mu s$ on the bus. The intermediate open state is placed to avoid overlap between the charging states and hence a fatal short circuit between the lines. Ideal sources are used for the $5V$ supply and the $10\mu A$ biasing current.

The target values (Spec. input) and the obtained schematic and post layout simulation results are reported in Table 2.4. Both the pulse durations over the bus t_{BH}, t_{BL}, and

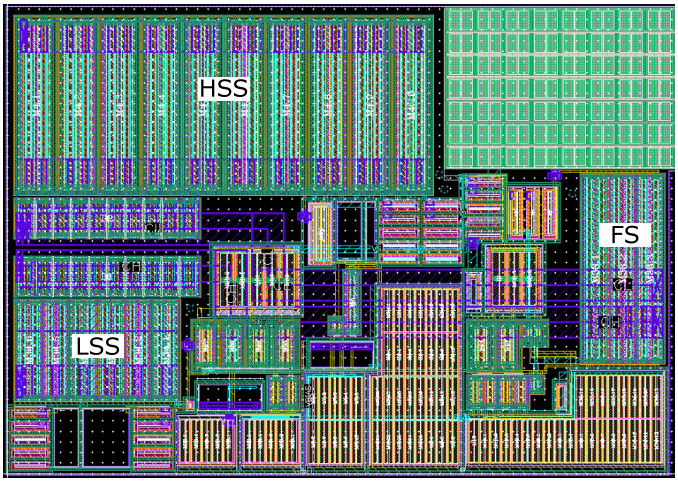

Figure 2.14: Layout view of the 3-Switches transmitter circuit

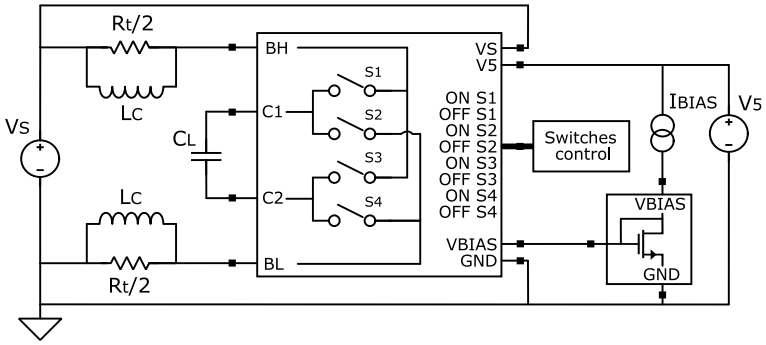

Figure 2.15: Virtuoso test bench for the H-Bridge transmitter

the charging time of the load capacitor t_{CL} are reported, and, even in the worst corner, the goal is satisfied making the proposal valid for the 2Mbps implementation. A target of around 4V is set for the pulse width so to simplify later the receiver system design. A picture of the post layout corner simulation is shown in Fig. 2.16.

Table 2.4: Simulation results of the H-Bridge transmitter

	Spec input	Unit	Schematic Simulation			Post Layout Simulation		
			Min	Typ	Max	Min	Typ	Max
t_{BH}	< 500	ns	217	247	411	224	257	418
t_{BL}	< 500	ns	216	246	410	223	257	417
t_{CL}	< 500	ns	259	296	471	266	307	477
V_{PBH}	4	V	1.5	4.4	6.1	1.5	4.1	5.8
V_{PBL}	4	V	1.4	4.3	6.1	1.4	4.1	5.7

In Fig. 2.17 the 3-Switches solution test bench is reported. The two switching capacitors

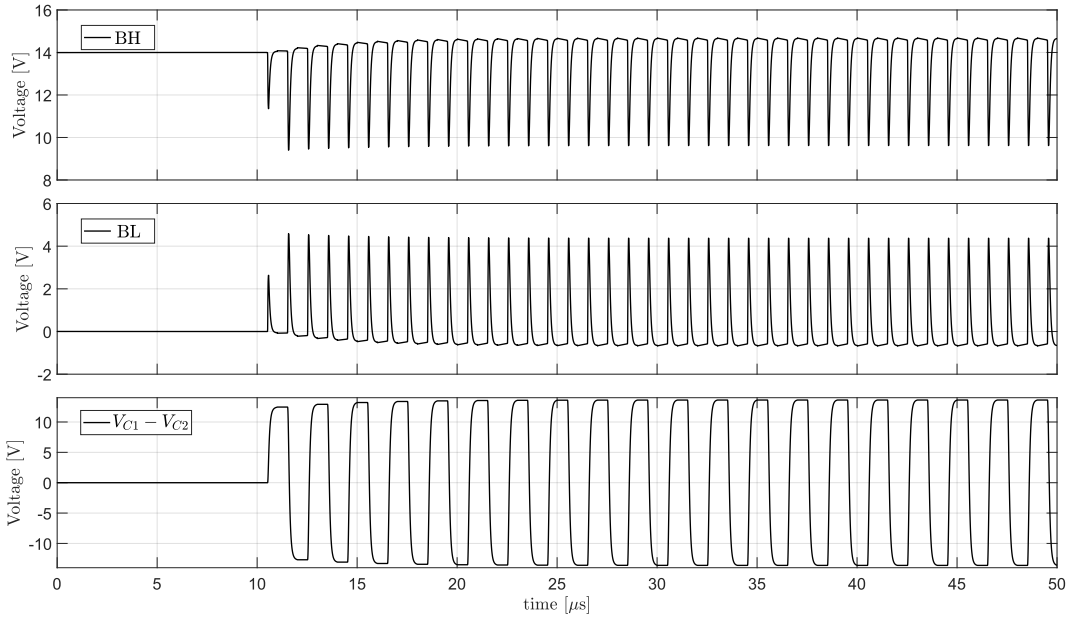

Figure 2.16: Post layout simulation results of the H-Bridge transmitter

C_L and C_H are sized to $0.8nF$ and the same values as before are used for supply and coupling feed. The switches control is implemented in a Verilog code according to Table 2.2 with a phase duration of $500ns$. A picture of the post layout result is shown in Fig. 2.18 while in Table 2.5 are finally reported all the obtained results and the target values. Also in this case the targets are satisfied making the design suitable for the application.

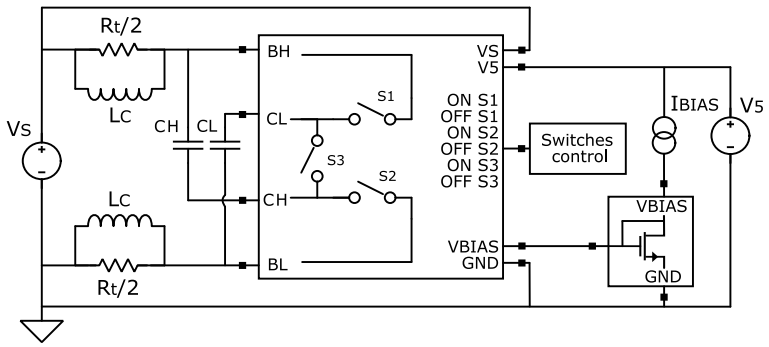

Figure 2.17: Virtuoso test bench for the 3-Switches transmitter

Table 2.5: Simulation results of the 3-Switches transmitter

	Spec input	Unit	Schematic Simulation			Post Layout Simulation		
			Min	Typ	Max	Min	Typ	Max
t_{BH} charge	< 500	ns	307	326	366	311	331	371
t_{BL} charge	< 500	ns	305	323	364	309	329	369
t_{CL} charge	< 500	ns	253	274	311	257	280	315
t_{CH} charge	< 500	ns	253	274	311	257	280	315
V_{PBH} charge	4	V	1.5	2.1	2.3	1.5	2.1	2.3
V_{PBL} charge	4	V	1.4	2.0	2.2	1.4	2.0	2.2
t_{BH} discharge	< 500	ns	187	204	231	198	216	243
t_{BL} discharge	< 500	ns	181	198	225	191	210	237
t_{CL} discharge	< 500	ns	164	182	211	174	193	223
t_{CH} discharge	< 500	ns	156	173	198	167	184	210
V_{PBH} discharge	4	V	2.0	2.4	2.7	1.9	2.2	2.5
V_{PBL} discharge	4	V	2.0	2.4	2.7	1.9	2.2	2.5

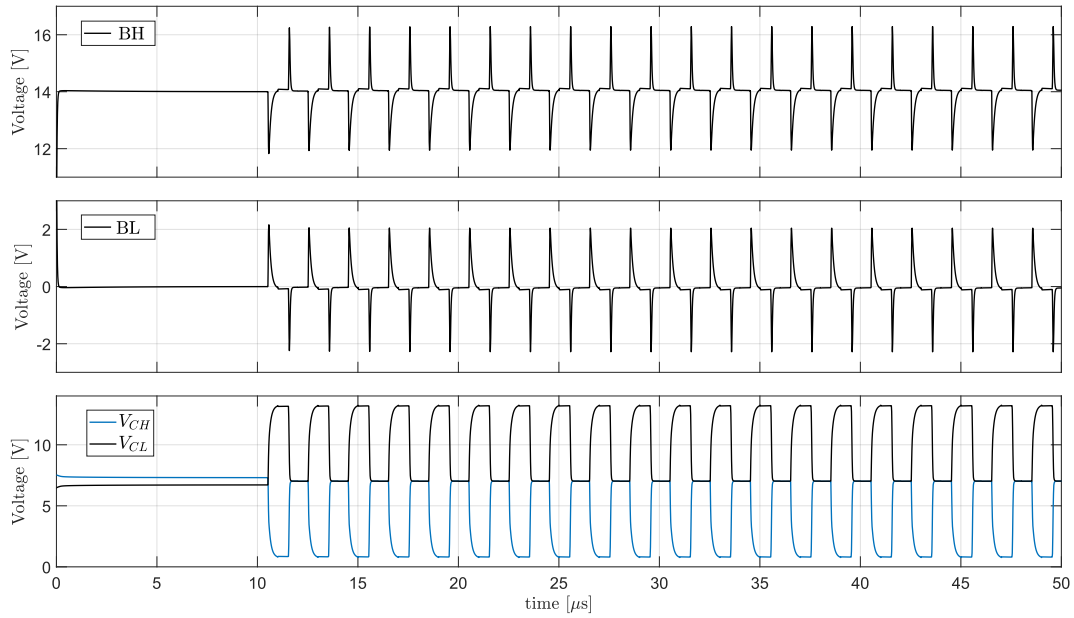

Figure 2.18: Post layout simulation results of the 3-Switches transmitter

CHAPTER 3

Receiver Design

To realize the full Supply-Embedded Communication transceiver, in addition to the transmitter of Section 2, a receiver (RX) needs to be designed. The circuit must operate with both the proposed transmitter topologies and so must be able to detect both unipolar pulses (H-Bridge Transmitter) and bipolar pulses (3-Switches Transmitter). It can be assumed a maximum pulse duration of $500ns$ since the main goal is still to reach a data rate of 2Mbps to replace the CAN bus. Pulses amplitude strongly depends on the size of the switching capacitors. Moreover, other factors affect the pulse amplitude, such as the wire length between the different nodes which can even be bigger than $10m$ and can introduce a significant attenuation. Therefore, a pulse range between $0.5V$ and $6V$ (i.e. $V_S/2$) needs to be considered and a very flexible design is needed to guarantee the correct functionality.

The proposed receiver is based on a StrongArm Latch, to be used as a high sensitivity comparator [14, 15]. The advantages of this circuit are that it does not consume static energy, it directly produces rail-to-rail outputs, and its input-referred offset derives mainly from a differential pair. Furthermore, an imbalance between the two branches of the Latch can be deliberately introduced to control their hysteresis and, therefore, to set detection thresholds [16, 17]. The design is done using the MV devices of the same 180nm CMOS SOI technology used for the TX, and since the communication bus is based on the DC level of the battery (typically 12V) a scaling is needed. This is done by a capacitor divider with a digitally controlled factor which still guarantees high flexibility. A critical point is that the StrongArm Latch is very sensitive to common mode oscillation that can be generated by asymmetry on the communication bus. The transmission circuit itself is also introducing an asymmetry as the high-side and low-side switches are not perfectly equal. A differential buffer is hence placed to provide common mode immunity and make the pulse detection efficient. The complete receiver scheme is finally shown in Fig. 3.1. The second StrongArm Latch is required only in case the 3-Switches Transmitter is used since the transmitted signal is bipolar.

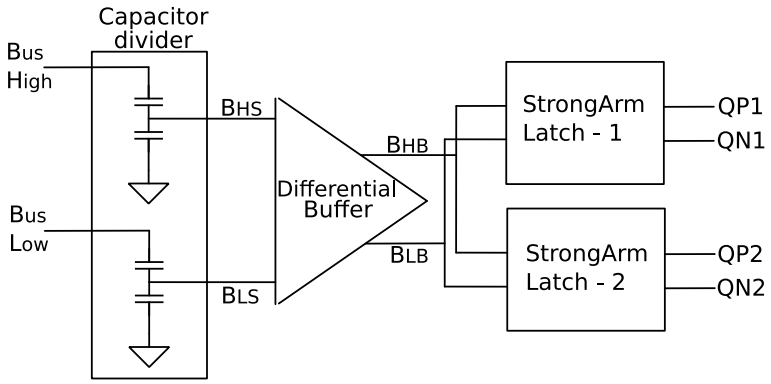

Figure 3.1: Receiver block diagram

3.1 Input Capacitor Divider

Since the communication bus DC level is $\approx 12V$, and the following design is done in a 5V technology, the capacitor divider of Fig. 3.2 is used to scale the input signal, and to ensure safe operations of the receiver. The division is composed of a fixed part given by the HV top fringe capacitance $C_{TOP} = 680fF$, the MV bottom fringe capacitance $C_{BOT} = 2.5pF$, and a variable bottom factor. The variable factor is realized by 4 digitally-controlled additional MV capacitors per side connected by switches, as highlighted in red in Fig. 3.2.

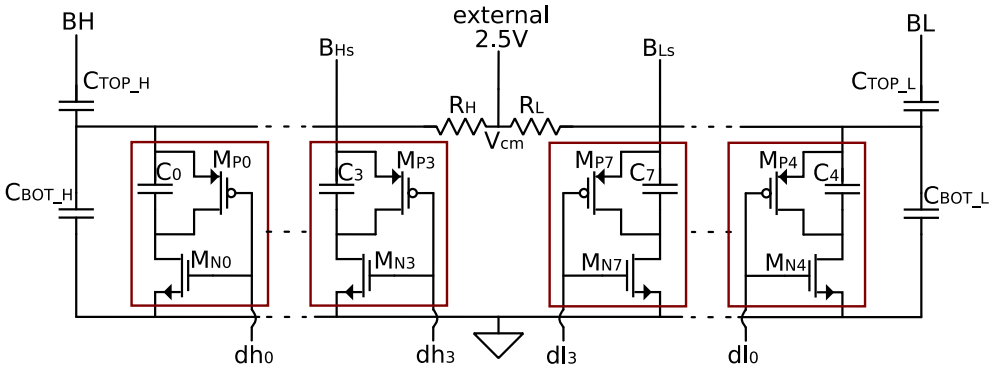

Figure 3.2: Capacitor Divider: 4-bit d_h and d_l set the division of B_H and B_L

The exact capacitance, including the corresponding switches, of a single additional block is evaluated by simulation and results to be $C_{OFF} = 8fF$ in off-state and $C_{ON} = 457.4fF$ in on-state.

The division factor k is then given by the following formula where d is the number of connected elements per side:

$$k = \frac{C_{TOP}}{C_{BOT} + d \times C_{OFF} + (15 - d) \times C_{ON}} \tag{3.1}$$

A comparison of theoretical and simulated k factors is shown in Table 3.1 for some points. A small discrepancy is due to non-idealities and parasitic effects. Capacitors are designed according to the available die size and also to be sufficiently large to avoid unwanted high pass filtering effects. The area occupied by C_{TOP}, C_{BOT}, and the additional bottom capacitors are respectively $950\mu m^2$, $2100\mu m^2$, and $6800\mu m^2$ per each side. The divider outputs are coupled by $R_H = R_L = 1M\Omega$ resistors to a $2.5V$ common mode voltage obtained by an external block (refer to Section 4.2). These resistors are designed to implement $f_c = 49kHz$ high pass cut-off frequency.

Table 3.1: Theoretical k vs simulated k

no. of connected elements	0	3	6	9	12	15
theoretical k	4.0	6.0	8.1	10.1	12.1	14.1
simulated k	5.2	7.1	9.1	11.0	12.9	14.9

3.2 Differential Buffer

The common mode immunity is ensured by the resistively degenerated differential pair with split tail current source of Fig. 3.3.

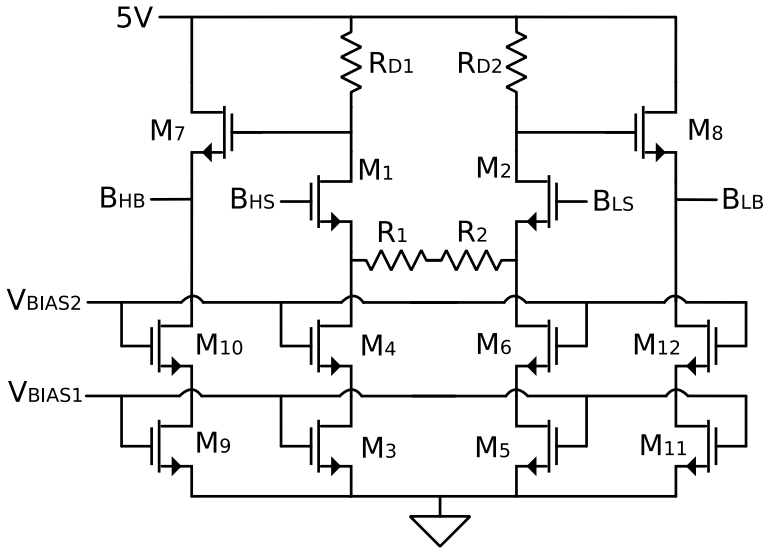

Figure 3.3: Differential pair with native NMOS input

To extend the input voltage range as much as possible, native NMOS are used as input devices. The absence of a p-well in these metal-oxide semiconductor (MOS) transistors ensures a nearly zero threshold voltage, which is needed in this case. The extrapolated threshold voltage V_{th} is $-0.16V$. Resistors R_{D1} and R_{D2} are equal to $100k\Omega$ and are designed with $W = 900nm$ and $L = 320\mu m$ to offer a good matching parameter, which, for this technology, results to be 0.092σ. A wide swing cascode current mirror is used to increase signal swing and reduce the dependency on the input common mode level. Each current tail is $10\mu A$ and the common mode output of the differential pair is then given by $V_{DD} - (R_D \times I_{TAIL}) = 4V$. This level is also the upper limit of the input signal since it must be ensured that M_1 and M_2 operate in saturation, and, therefore, that the condition $V_{GD} < V_{TH}$ is satisfied. Since the maximum V_{GS} allowed by the technology is $5.5V$, M_7 and M_8 are used to shift the common mode level to $3V$, which guarantees that no violation appears at Latches input devices when positive pulses are transmitted. It must also be ensured that this level is not too close to V_{TH}, otherwise, negative pulses can turn off latches input MOS, and alter the normal functioning. The differential gain of the designed buffer over the used input range is shown in Fig.3.4. The gain variation vs. common mode input level is shown on the left side of Fig. 3.6 for signal frequencies of $1MHz$ and $10MHz$. The minimum gain is around $-2.5dB$ and since this corresponds to the typical input common mode level ($\approx 2.5V$), the applicable common mode variations do not lead to a signal reduction below the detection threshold. Moreover, in Fig. 3.5, a Montecarlo mismatch simulation on 500 points shows that the designed buffer has a good common mode rejection up to $10MHz$. The histogram obtained by the Montecarlo simulations at $1MHz$ is presented in Fig. 3.6. The mean value is $-61.4dB$, the maximum is $-45.43dB$, and the standard deviation is 7.776.

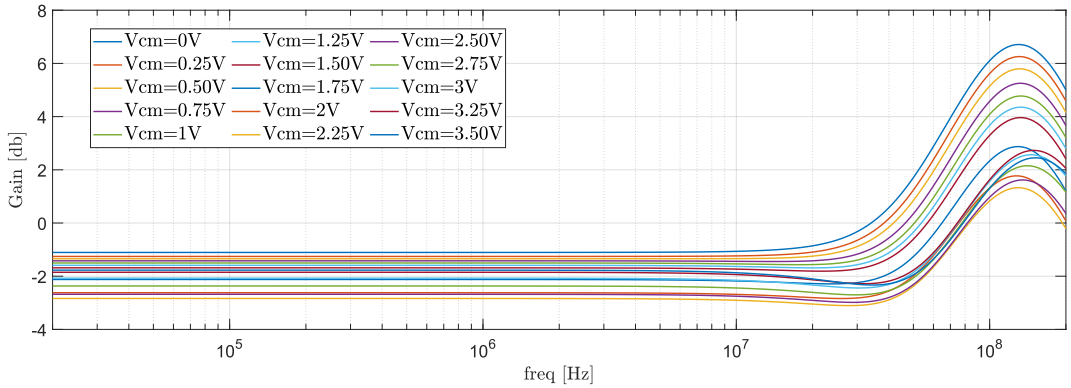

Figure 3.4: Differential gain of the proposed buffer

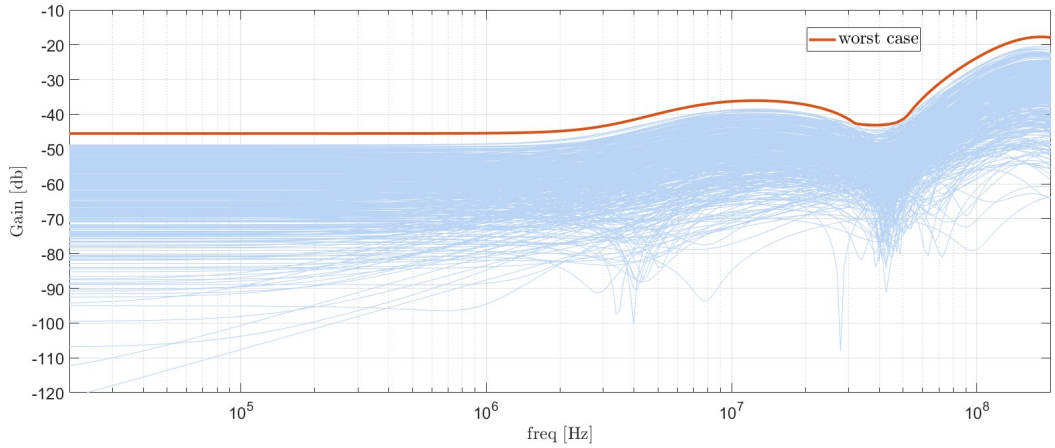

Figure 3.5: Common-mode gain of the proposed buffer

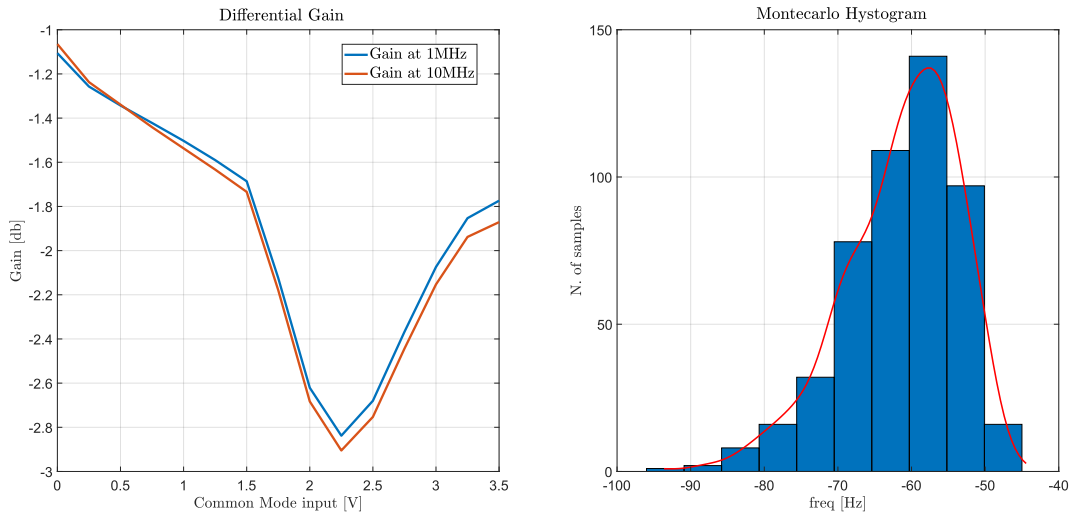

Figure 3.6: Differential gain variation at 1MHz and 10MHz over the input range, and Common-mode Montecarlo histogram at 1MHz on 500 mismatch points

3.3 Strong-Arm Latch

The core of the receiver is composed of two StrongArm Latches with tunable hysteresis. The circuit is shown in Fig. 3.7.

At $clock = 1$, the input PMOS M_1 and M_2 are off. The nodes P, Q, Q_P, and Q_N are grounded since NMOS M_7, M_8, M_9, and M_{10} are on. Whit the negative edge of the clock, M_1 and M_2 turn-on, and the levels in P and Q start to increase. When they reach V_{THn}, M_3 and M_4 turn-on and the two output levels start to increase too. The first output reaching V_{THn} will activate the cross-connected NMOSs (i.e. M_5 or M_6), which will pull the other output to ground while the first one is free to reach V_5.

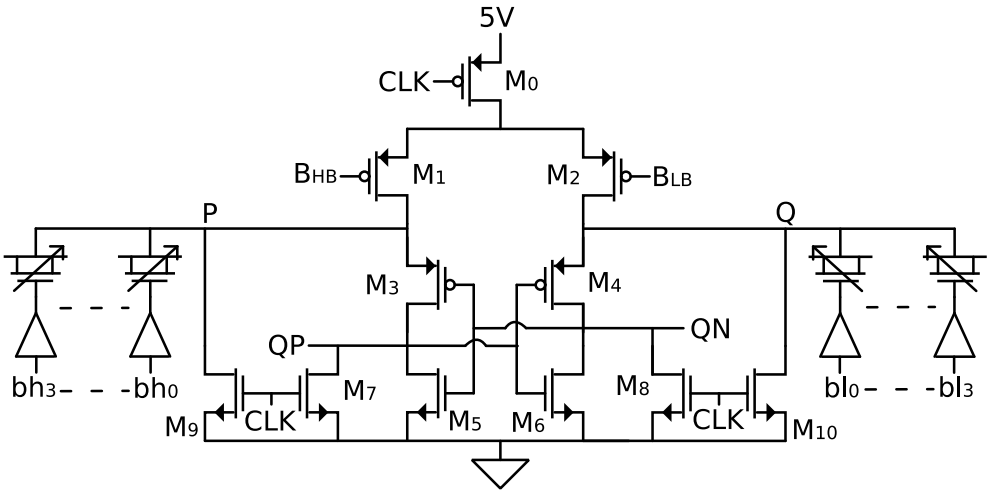

Figure 3.7: StrongArm Latch with tunable hysteresis - MOS varactor are inserted in nodes P and Q by 4-bit per side b_h and b_l

The Latch must be sized to obtain the best trade-off between power consumption, delay, and input-referred noise. Large $M_{1,2}$ and thin $M_{3,4}$ ensure low delay. Large devices provide lower input-referred noise but come with a higher power consumption [18]. The chosen sizes, which correspond to the best compromise, are $w_{M1,2} = 15\mu m$ and $w_{M3,4} = 2\mu m$. Fig. 3.8 shows a speed comparison sweeping $w_{M1,2}$ and $w_{M3,4}$ from $2\mu m$ to $20\mu m$. Quick discharge of nodes P and Q is given by selecting $w_{M9,10} = 2\mu m$.

Inserting a charge imbalance at nodes P and Q allows control of the hysteresis, and thus sets detection thresholds. The imbalance is realized by digitally-controlled MOS varactors, sized to furnish the best ratio between two biasing points. Sizing needs to be done carefully since it degenerates the latch timing performances. Fig. 3.8 shows the obtained capacitance value of a single MOS varactor designed with $W = 2\mu m$ and $L = 6\mu m$. The biasing point is swept from -5V to 5V and a ratio of 3 is reachable using 0V and 5V.

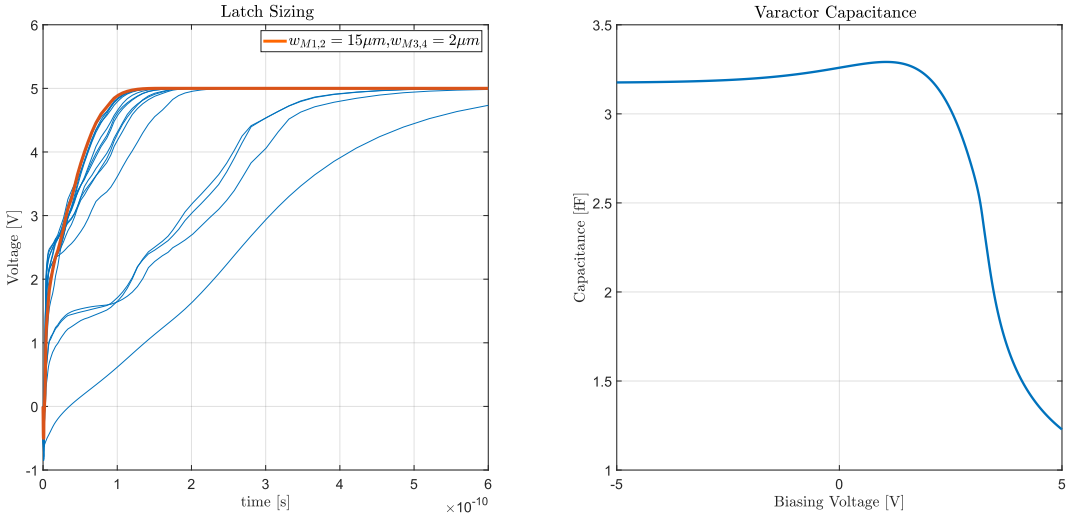

Figure 3.8: StrongArm Latch sizing, and capacitance offered by a MOS varactor

3.4 Receiver Top Level

In addition to the presented schemes, an output stage is added to the capacitor divider. This consist of 5 switches disposed as in Fig. 3.10 and it is intended for use in debugging to compare the common mode voltage V_{CM} with the common output signal (non-differential). Therefore, 5 additional control bits are needed to implement the states described in Table 3.2. The switches SW_3 and SW_4 are redundant but are both placed for symmetry reasons.

Table 3.2: Capacitor divider output stage configuration

State	Closed	Open
Normal operation	SW_1 , SW_2	SW_0 , SW_3 , SW_4
Common-mode	SW_0 , SW_1 , SW_4	SW_2 , SW_3
Common-mode	SW_0 , SW_2 , SW_3	SW_1 , SW_4

The proposed circuit, implemented in the layout of Fig. 3.9, was validated by post layout simulation with the setup of Fig. 3.11. The total area occupied by the circuit is $50000\mu m^2$. The supply feed, transmitter, receiver, and bus termination are connected through a $2m$ model fitting of an unshielded twisted pair cable, which is a multi-segmented RGLC-model. The line impedance Z_N, as reported in [9], is assumed to be 50Ω.

In Fig. 3.12 the 3-Switches Transmitter with $1nF$ switching capacitors is used to transmit at a data rate of 2Mbps. In Table 3.3 the amplitudes of the pulses at different stages of the proposed receiver are reported. The divider is configured with $dh = dl = 6$ additional elements connected and the resulting division factor k is around 9 as expected from Table

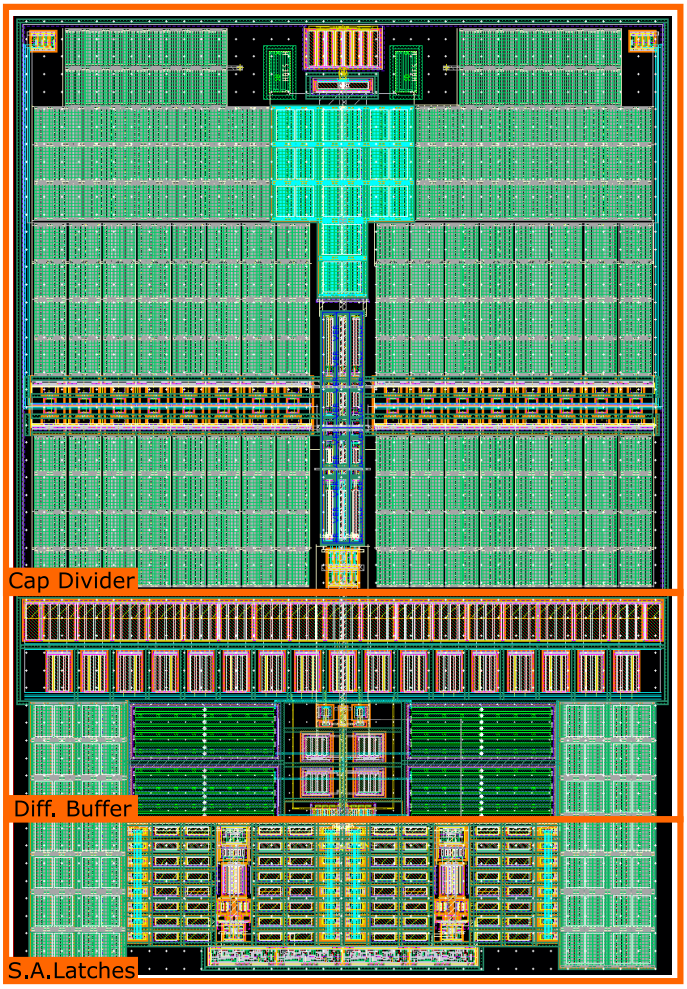

Figure 3.9: Full receiver layout

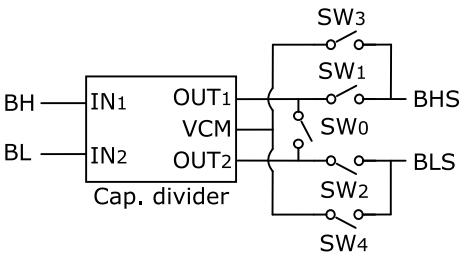

Figure 3.10: Capacitor divider output stage

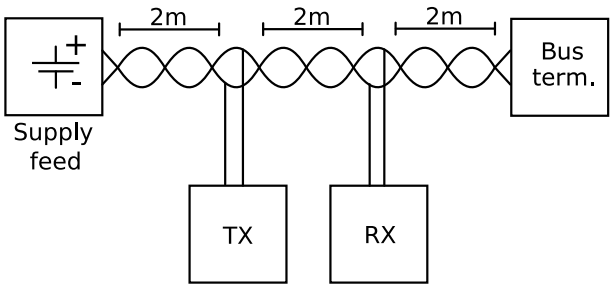

Figure 3.11: Receiver simulation setup

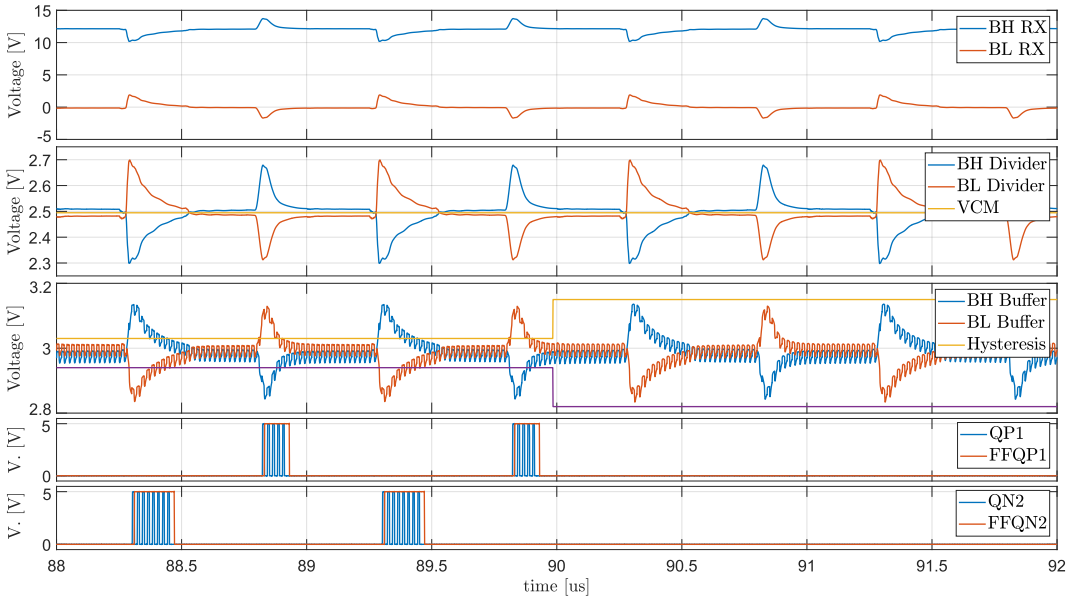

Figure 3.12: Receiver simulation result

3.1. The buffer is filtering the signal to the Latches and it provides a $2.98V$ common mode voltage. Due to its differential gain, it is also providing attenuation of about $20-25\%$.

By the use of 4 bits per side, there are 256 possible combinations of imbalance in the designed StrongArm Latch. The range of possible levels is shown in Fig. 3.13 where the number of varactors biased with 0V is kept to 0 on one side (i.e. *bh* or *bl*) and is swept from 0 to 15 on the other. The resulting minimum is $15mV$ while the maximum is $225mV$.

To detect both positive and negative pulses, in Fig. 3.12 the hysteresis is set inversely

Table 3.3: Simulation results: divider and buffer outputs

State	BH	BL	BHS	BLS	BHB	BLB
Charge	-1.87	1.91	-0.200	0.208	0.150	-0.150
Discharge	1.78	-1.77	0.192	-0.189	-0.150	0.150

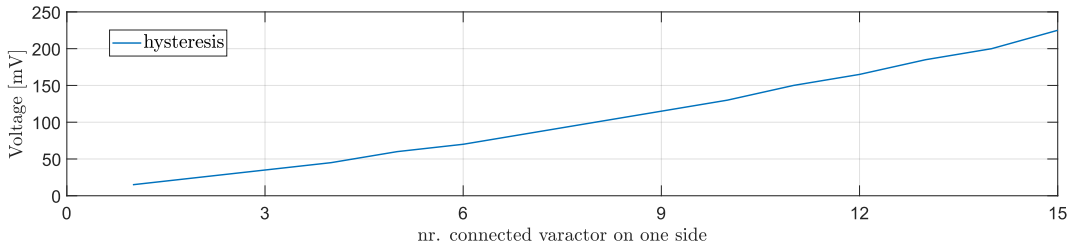

Figure 3.13: Achievable levels of hysteresis

for the two latches, which means that $bh_{LATCH1} = bl_{LATCH2} = h$ and $bl_{LATCH1} = bh_{LATCH2} = 0$. An external $50MHz$ clock is applied, and flip-flops are placed downstream of the outputs to reconstruct the received signal. In the first half of the simulation, the pulses are detected because the hysteresis is set to $25mV$. At $90\mu s$ the threshold is raised to $160mV$, which is higher than the received pulses, and so no output variation occurs. The effect of the imbalance obtained by the increasing of capacitances at node P is shown in Fig. 3.14 where the Latch inputs are set as $B_{HB} = V_{CM} - V_D$, $B_{LB} = V_{CM} + V_D$. In the case of high hysteresis, node P does not become faster than node Q even in the presence of the pulse, and therefore the output is not triggering.

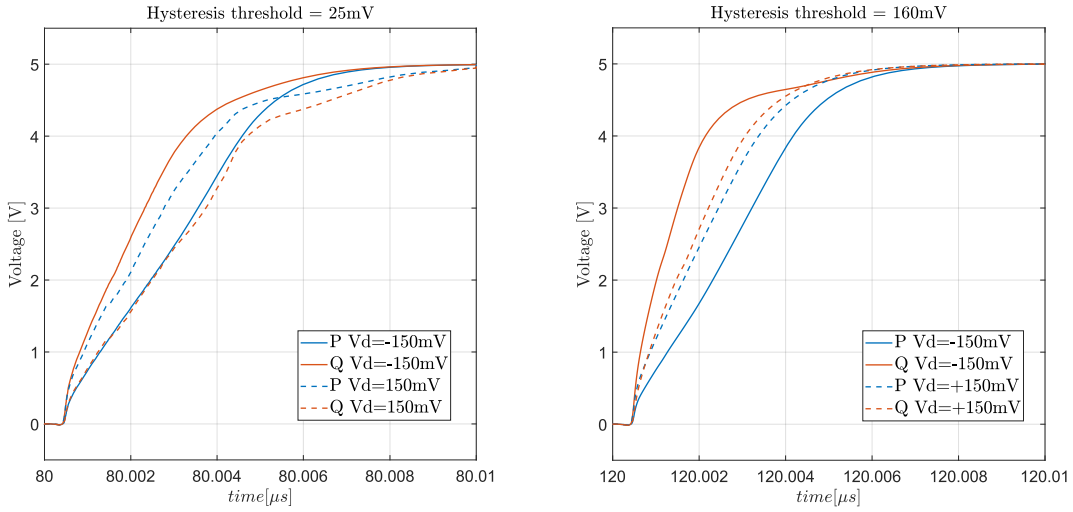

Figure 3.14: Hysteresis set used in simulation

CHAPTER 4

Test Chips Implementation

Two prototypes were developed to validate the proposal of this work in the laboratory. The first test chip (TC1) includes only the transmitter part and was developed to verify the validity of the Supply-Embedded Communication concept in an intermediate step. The second test chip (TC2) was designed following the successful tests carried out on the TC1, and it implements the full transceiver since it includes also the receiver circuit. To simplify the work, the first prototype was designed taking into account the possible future developments: a sufficiently large empty space was intentionally left to insert the receiving circuit, and not all available pins were used. The chips have the same basic architecture and are packaged in a 24-pin quad-flat no-leads (QFN) package, although the TC1 only uses 20 pins. In this chapter, first, the TC1 architecture is described in detail in Section 4.1, and then the design extension to realize the complete transceiver in TC2 is shown in Section 4.2.

4.1 Test Chip 1

The first test chip implements only the transmission function, and both the H-Bridge and the 3-Switches topologies are included in the prototype since they offer different advantages interesting to analyze. An appropriate driving system is necessary to avoid the simultaneous function of the two circuits and to turn the switches on and off properly. Moreover, a block that generates the required supply voltages and currents, and a protection system are needed. The top level block diagram of TC1 is shown in Fig. 4.1 where 4 main structures can be distinguished: the transmission block, the supply system, the digital control, and the padring interface.

- Transmitter Block
  The two transmitter circuits described in Section 2, are connected in parallel on the transmission bus as shown in Fig. 4.2 so as not to influence each other. For each implementation, the control signals are passed through a pre-driver. Such pre-drivers have an enable signal which is inverted for the two circuits (i.e. SELN = !SELP) so that they can never operate simultaneously.

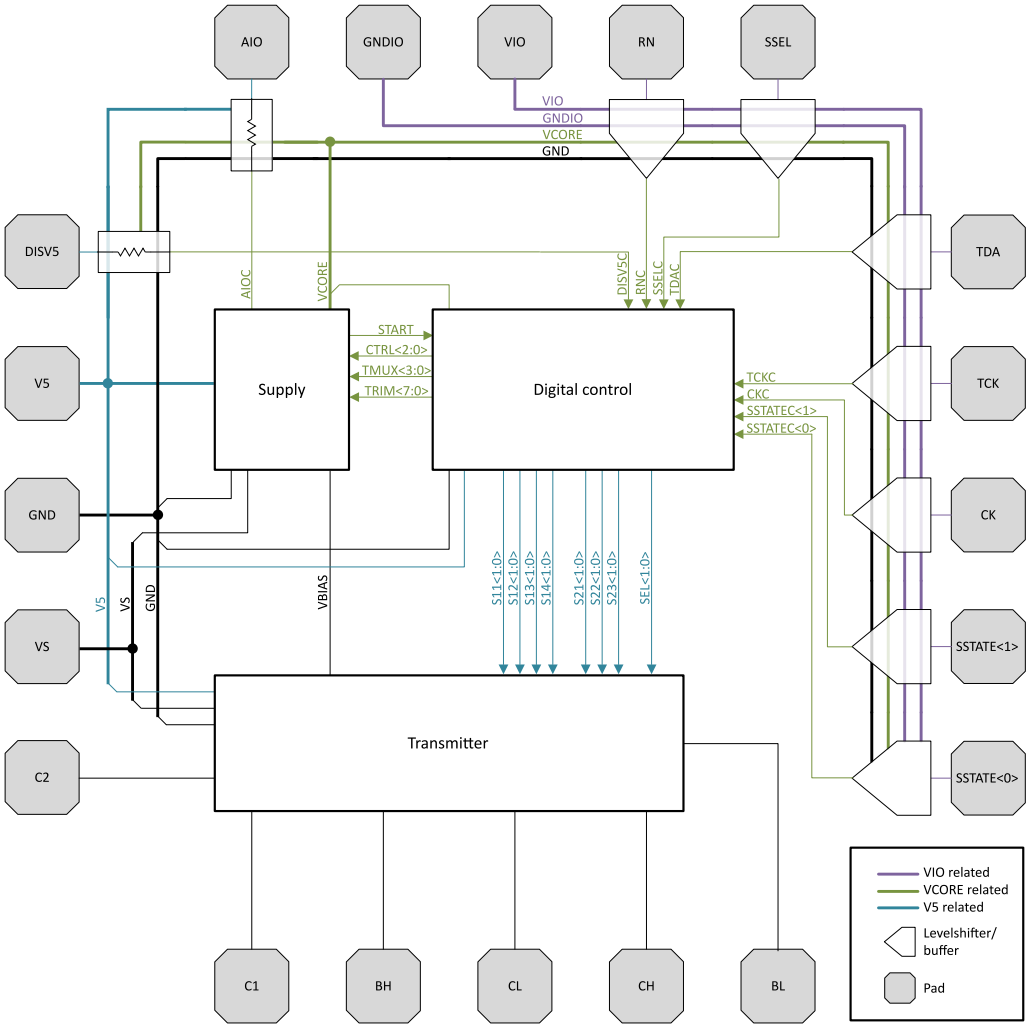

Figure 4.1: Top level block diagram of the TC1

- Supply System

  To operate properly, the switches need, besides the main power supply and the control infrastructure, a $5V$ voltage, and a biasing current. Moreover, also the digital control and the padring need to be supplied properly. Thus, inside the chip coexist different supply voltage levels which can be distinguished by the color code used in Fig. 4.1. The supply system, detailed in [9], is composed of available intellectual property (IP) subcircuits such as a $5V$ regulator and a bandgap reference circuit, and takes the external battery voltage V_S as input to generate the internal sources. The $5V$ voltage, indicated in blue in Fig. 4.1, is particularly critical as the switch control signals are based on it. However, the maximum gate-source interface voltage for the MV and HV devices, and the maximum drain-source voltage of the MV devices,

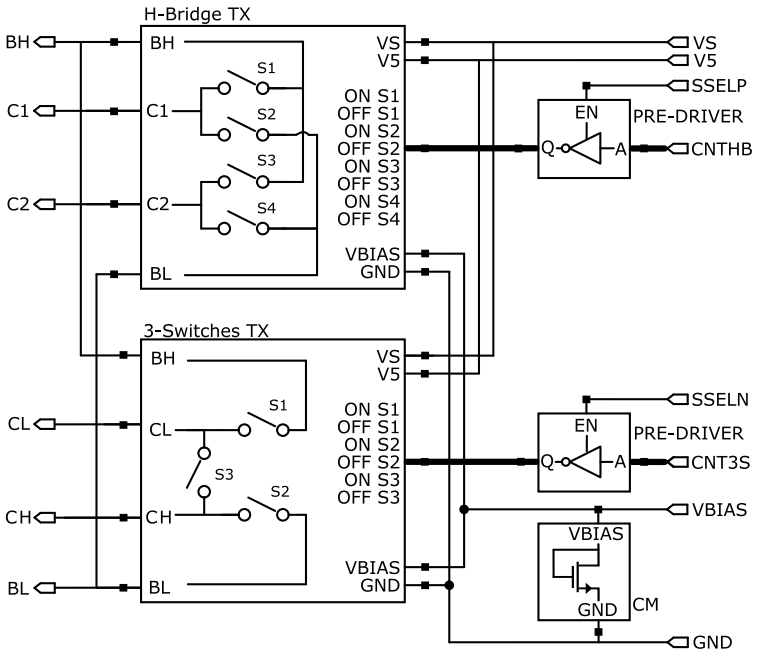

Figure 4.2: Transmitter block inside the TC1

in this technology is $5.5V$ making the margin of error of the $5V$ generation quite small. Both the internal regulator and the bandgap reference circuit have an internal 4-bit trimmer that makes their settings flexible so that any post-production errors or process variations can be easily adjusted within a certain range. The setting is managed by a 8-bit signal $TRIM < 7 : 0 >$ applied through the digital control. As an additional option, it is also included the possibility to use an external $5V$ source and bypass the internal regulator. Indeed, 3-bits from the digital and named $CTRL < 2 : 0 >$ are dedicated to respectively enabling the transmitter bias current, the $5V$ regulator bias current, and the $5V$ regulator operation. As illustrated in green in Fig. 4.1, an additional voltage called V_{CORE} is also generated by the supply system. This voltage has a typical value of $3.8V$ and it is dedicated to supplying all the parts of the TC1 that are not dedicated to the transmission itself, as the digital control. Finally, a $5\mu A$ current (named $IPD5U$ and illustrated as V_{BIAS} in Fig. 4.1) is generated and injected into the Current Master mirror (CM) of the transmitter which will double it to $10\mu A$ to feed the switches as explained in Section 2. The pin AIO is dedicated to the supply debugging. Through the 4-bit $TMUX < 3 : 0 >$ it is possible to set an internal multiplexer that outputs 4 possible values as shown in Table 4.1 which indicates the correct functionality.

Table 4.1: Test signal mux to *AIOC*

Muxer input	Signal to *AIOC*
TMUX<3>	VBIAS
TMUX<2>	VCORE
TMUX<1>	VBG
TMUX<0>	IPD5U

- Padring Interface
  To protect the test chip from electrostatic discharge, a dedicated protection scheme is required. The design is particularly complex for the pins connected to the bus and to the switching capacitors since the voltage level in these nodes can reach values higher than V_S or lower than $0V$. Furthermore, in order to operate correctly, the transmission circuit needs to draw currents directly from the bus, and therefore the connection through the pins must be done properly so as not to affect the operations. An external power supply, VIO and $GNDIO$ indicated in purple in Fig. 4.1, is dedicated to the input/output (I/O) interfaces. Implementation details of such interface and advanced simulations are reported in [9].
- Digital Control
  The digital control block is realized by a synthesis of a Verilog code and it takes some external inputs to generate the needed internal control signals. The first task performed by this block is to manage the data transmission. First, the circuit topology is selected through the pin $SSEL$, then the switch states are set by means of the two pins $SSTATE < 1 : 0 >$ which implement all the possible working configurations as shown in Table 4.2. An external clock is applied via the dedicated pin (CK) to synchronize the $SSTATE$ signals. The mode in which both signals $SSTATE$ are high is called "Configuration Mode" and it is used to set the parameters of the supply system. A shift register of 16-bit length is transmitted through the TDA pin and the test clock TCK to generate the controls for the $5V$ regulator trimmer, the bandgap trimmer, the multiplexer input, and the enables of the supply system. Note that an additional pin is dedicated to disabling the $5V$ regulator in case an external source wants to be used. The 16-bit stream required to set all the parameters of the TC1 is summarized in Fig. 4.3. Even if the digital control block is supplied by the V_{CORE} voltage, to provide high overdrive and speed up the switches transitions, the switches control signals are shifted to the $5V$ domain, and hence are indicated in blue in Fig. 4.1. The pin RN is dedicated to the reset. The full Verilog code is reported in [9].

Table 4.2: State control

SSEL	STATE<1:0>	Mode
0	00	off state
	01	Charge 1-4
	10	Charge 2-3
	11	Config. mode
1	00	off state
	01	Charge
	10	Discharge
	11	Config. mode

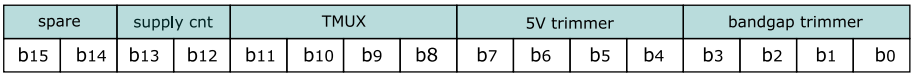

Figure 4.3: Control bit stream for the TC1

The top level layout of the TC1 is shown in Fig. 4.4. The area occupied by the transmission block including the Current Master mirror is $0.18mm^2$, the area occupied by the supply system is $0.12mm^2$, and the one occupied by the digital block is $7000\mu m^2$. Stack of a MV PMOS accumulation mode varactor and fringe capacitor from metal 1 to 5 implements decoupling capacitor of $350pF$ and $210pF$ respectively to the V_5 and V_{CORE} voltages and take an area of $0.23mm^2$. The layout included 5 metal layers plus the thick top metal which is dedicated to the main connection and is clearly visible in the 2000x microscope picture of Fig. 4.5. Empty areas were filled with dummy patterns for the planar process so that only the elements on the top metal are visible. A large empty space in top right region was intentionally left for inserting the receiver circuit later.

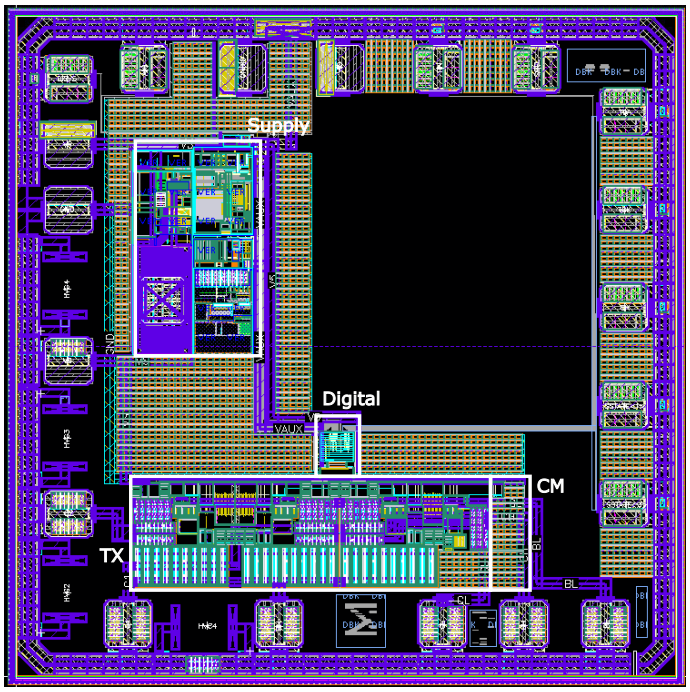

Figure 4.4: Top level layout of the TC1

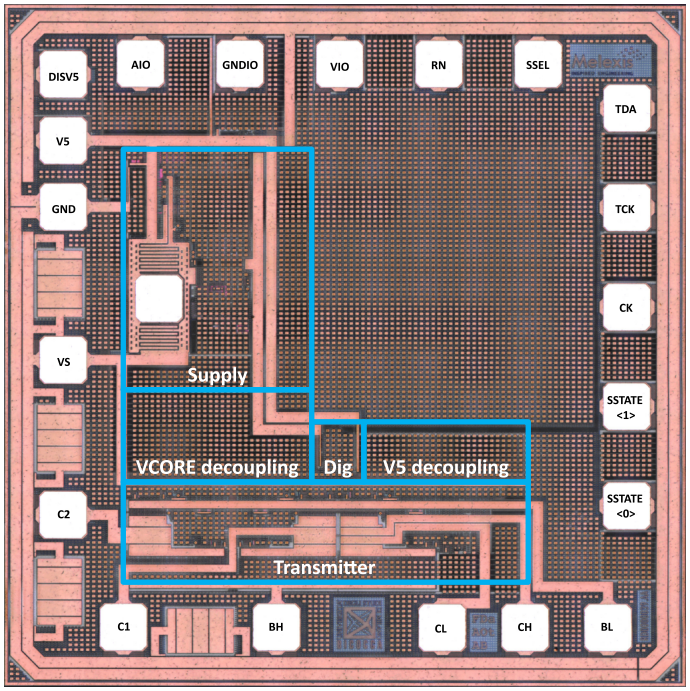

Figure 4.5: TC1 2000x micrograph picture

4.2 Test Chip 2

Since no problems come out from the tests performed on TC1 (refer to Section 5), the design could be extended to TC2 to include the RX circuit as well. The resulting top level block diagram is shown in Fig. 4.7 similar to TC1. Three additional pins are required: two for the received outputs ($RXO1$ and $RXO2$) and one for the received clock ($RXCK$). Only two of the four outputs of the Latches are taken out (one per Latch) as the received signal can be reconstructed by means of simple digital post-processing of these. Besides the $V5$, the receiver circuit needs two $5\mu A$ biasing currents for the differential buffer and a common-mode voltage reference for the capacitor divider. This can be obtained by a simple level-shifting of the V_{CORE} as illustrated in Fig. 4.6. A third $5\mu A$ biasing current is then required. These are obtained similarly to the transmitter bias by a simple extension of the supply system and are named respectively V_{BIASRX}, $V_{BIASRXC}$, and $V_{BIASRXDIV}$.

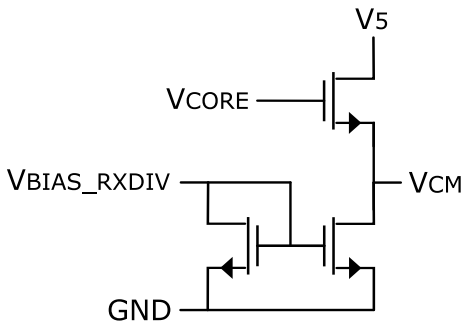

Figure 4.6: Generation of the V_{CM} voltage by level-shifting of the V_{CORE}

The digital control block must also be extended according to the new requirements. In particular, 8-bits are needed to set the input division factor, 8-bits to set the hysteresis of Latch 1, 8-bits to set the hysteresis of Latch 2, 5-bits to set the output stage of the divider (and hence the receiver operation mode), and 1 bit to enable the RX itself. The extended bit stream of 64-bits is reported in Fig. 4.8. In addition, 2-bits ($enDOUT/OD$) were introduced to set the output states of the RX pads [9]. The new top level layout is shown in Fig. 4.9. The area occupied by the RX block is $50000\mu m^2$, and an additional $11700\mu m^2$ is occupied by a $37pF$ decoupling capacitor for the internal common mode voltage implemented by a stack of a MV PMOS accumulation mode varactor and fringe capacitor from metal 1 to 3. The digital size was extended to $20000\mu m^2$ while no relevant increase happen in the supply system. The shapes of the decoupling capacitor of V_5 and V_{CORE} were slightly modified according to the available spaces but no relevant changes in the size was done. Finally, a micrograph of the silicon is shown in Fig. 4.10.

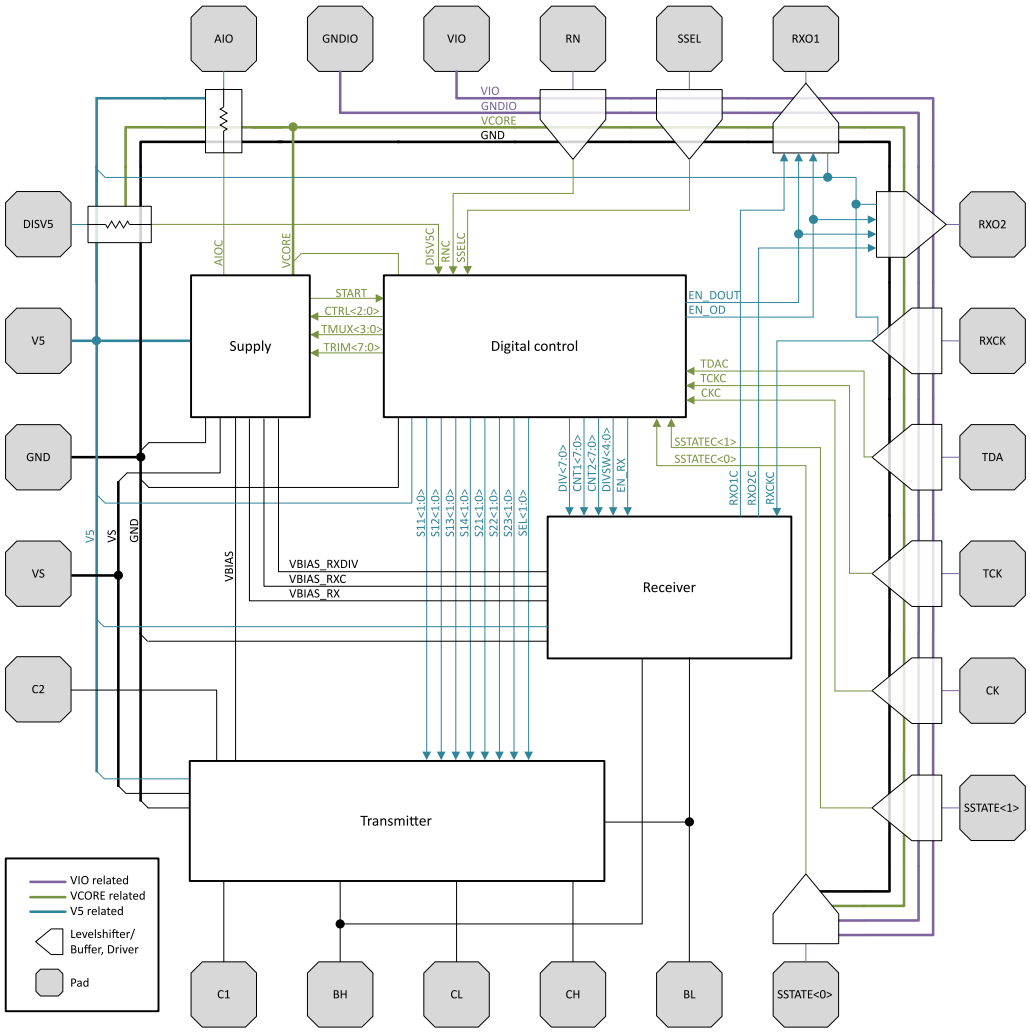

Figure 4.7: Top level block diagram of the TC2

spare								en RX	en DOUT/OD		RX divider output stage				
b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
CNT1 - hysteresis control latch1								CNT2 - hysteresis control latch2							
b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
spare								DIVD - RX input divider							
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
spare		supply cnt		TMUX				5V trimmer				bandgap trimmer			
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Figure 4.8: Control bit stream for the TC2

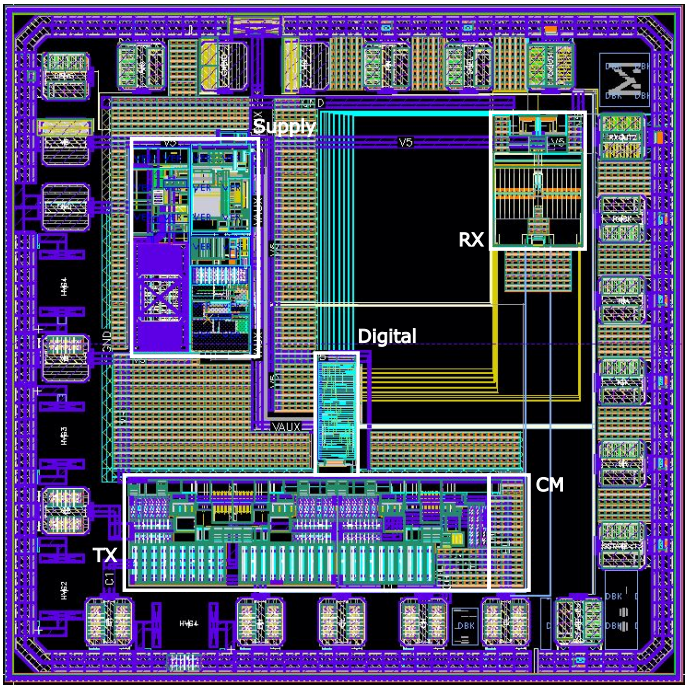

Figure 4.9: Top level layout of the TC2

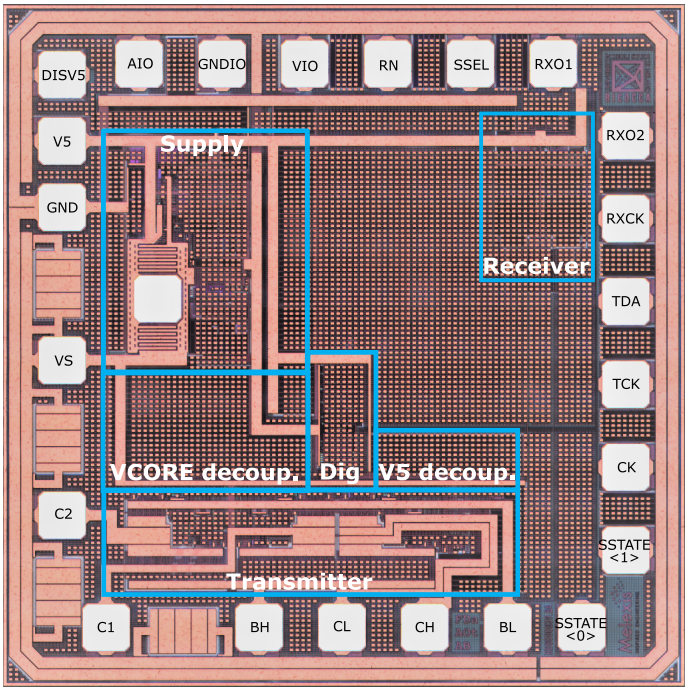

Figure 4.10: TC2 micrograph picture

CHAPTER 5

Measurement and Validation Results

The TC1 was taped out and tested in the laboratory in September 2021. In addition to a testing printed circuit board (PCB) containing the chip and the components necessary for its operation, the standard laboratory instrumentation, and an external source to generate the control signals were required. In the carried out tests, a Raspberry PI was used for the static measurements (supply and other fundamental parameters tests), while a field-programmable gate array (FPGA) was used for the dynamic measurements (data transmission between two nodes tests).

In Section 5.2 the TC2 is validated by advanced post-layout simulations between two nodes. Moreover, the implementation is verified by measurements on the silicon which show the correct operation of the transceiver and the setting of its parameters.

5.1 Test Chip 1 Validation

In order to test the TC1, a testing PCB was designed in Altium Designer. As shown in the schematic of Fig. 5.1, just a few external to the chip components are needed. For the switching capacitors C_F, C_L, and C_H a 1206 footprint was chosen, and devices with a DC voltage rating higher than $20V$ should be applied. A double option between standard inductors (L_1 and L_2) and a common mode choke (L_3) is provided for the supply coupling. Connector J_4 acts as an interface between the FPGA/microcontroller board and the test chip, while the transmission bus can be connected on J_3. Finally, some external decoupling capacitors can be inserted for V_S and V_5. The designed PCB is a 2 layer board where the bottom is dedicated to the ground plane while the top layer is reserved for the net interconnections. Four vias are provided under the chip to help heat dissipation. The resulting populated board is shown in Fig. 5.2.

As a preliminary stage, static tests were performed to verify the proper function of the power supply and to ensure the absence of internal short circuits and any other possible fatal errors. Then communication tests between two nodes have been carried out. Since the TC1 implements only the transmission function, the discrete component breadboard developed in [9] was used as a receiver.

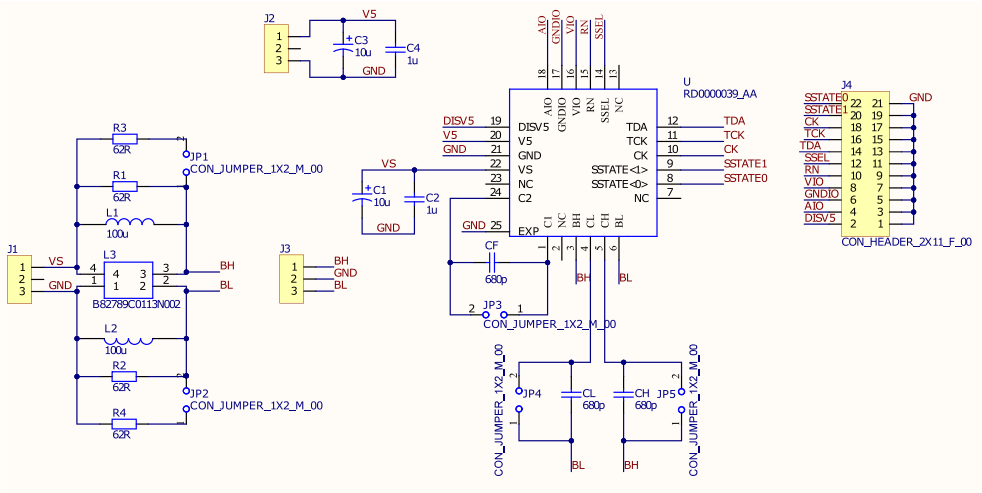

Figure 5.1: Schematic of the PCB for testing designed for the TC1

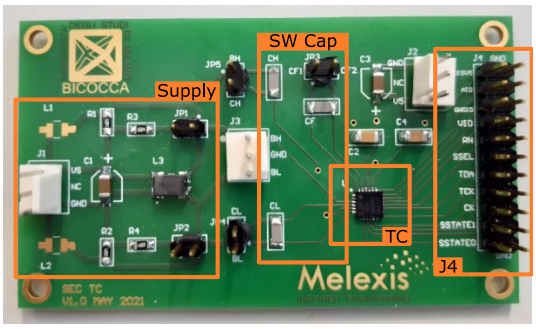

Figure 5.2: Picture of the PCB for testing designed for the TC1

The demonstrator board composed of off-the-shelf components shown in Fig. 5.3 is composed of the following blocks:

- Local supply: provides the necessary internal voltages starting from a $5V$ micro-usb power supply;
- Transmitter: implements the H-Bridge and 3-Switches topologies of Section 2 through an ADG5413 [19] by Analog Devices that contains four independent single-pole/single-throw (SPST) with a nominal on-resistance $\leq 10\Omega$;
- Receiver: consists of a 4GHz LNA LTC6268-10 [20] coupled to the transmission line and which acts as a high-speed differential amplifier whose single-ended output is compared to a generated low and high thresholds by two low voltage differential signaling (LVDS) comparators;
- Analog-to-digital converter (A/D) to convert the received signal from the analog to the digital domain.

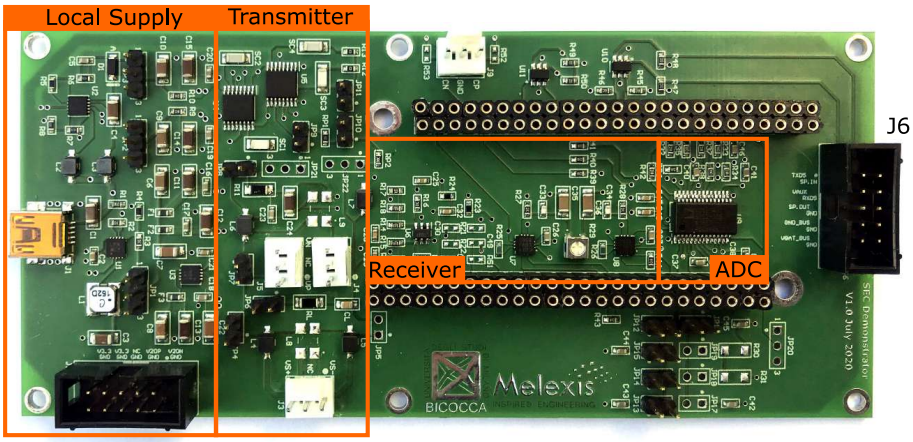

Figure 5.3: PCB Demonstrator

An FPGA can be connected to the demonstrator to manage the control for both master and slave configuration. The design was made for fitting a TE0725 FPGA from Trenz on top of the PCB. In this work, a can-like protocol named Melexis Light Bus (MeLiBu) [21] is used as a protocol layer and so a UART/CAN interface bridge can be connected to connector J_6 so as to make the received signal and clock available.

5.1.1 Static Measurements TC1

By static measurements are meant all the preliminary measurements made before testing the data transmission itself. These basic measures are needed to verify the correct functionality of the power supply system and the absence of fatal errors. For these tests, a Keithley 2602B Source Meter [22] was used. It provides two completely isolated channels (CH-A and CH-B) of wide dynamic source and measures within the same footprint. Each 40W channel provides a 6½-digit precision resolution source and measures from $10A$ pulse to $0.1fA$ and $200V$ to $100nV$ at less than $100\mu s$ pulse width and within 0.1% of settled value. It also supports the PyVISA package which is a Python package that enables the user to control all kinds of measurement devices independently of the interface (e.g. GPIB, RS232, USB, Ethernet). To take full advantage of this feature and to automatize the measurement process as much as possible in order to reduce the possibility of errors, a Raspberry PI3 was chosen to generate the control signals since it also supports Python coding [23]. The Rasberry PI3 can be connected to the connector J_4 of the testing PCB as shown in Table 5.1 and according to the pinout shown in Fig. 5.4.

As illustrated in the setup of Fig. 5.5, both the Raspberry PI3 and the Keithley 2602B were connected over the ethernet, and through a PC and a virtual network computing (VNC) software some Python codes could be loaded into the Raspberry to both set the TC1 parameters and the source meter instructions. A Python package has been written to

Table 5.1: Raspberry PI3 pinout assignment

PCB J_4 PIN	Raspb. PI3 PIN	Function
VIO	17	3.3V PWR
GNDIO	39	GND
DISV5	39	GND
GNDIO	39	GND
RN	11	GPIO17
SSEL	12	GPIO18
SSTATE1	26	GPIO7
SSTATE0	24	GPIO8
CK	23	GPIO11
TCK	13	GPIO27
TDA	15	GPIO22

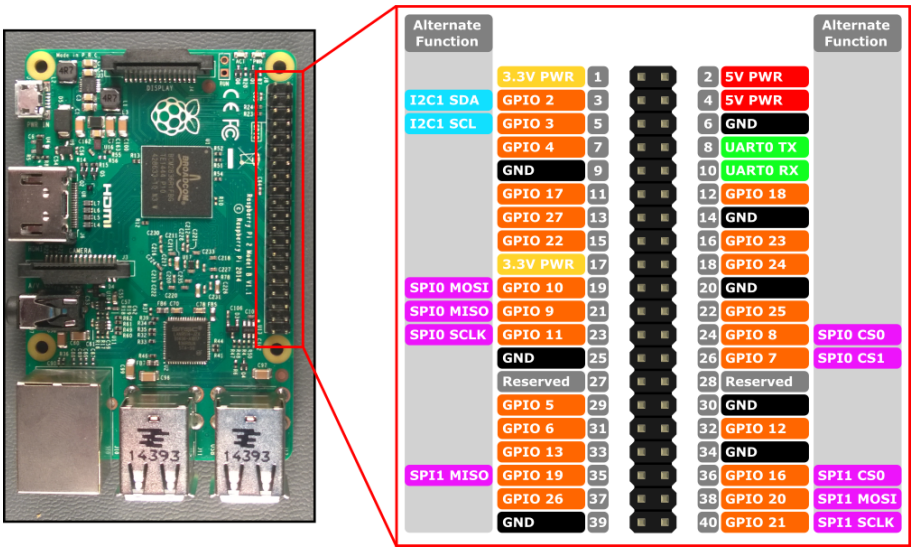

Figure 5.4: Raspberry PI3 pinout

implement the functions necessary to drive the test chip such as:

- INIT(RNpin, SSELpin, SSTATE1pin, SSTATE0pin, CKpin, TCKpin, TDApin) #initialization and pin assignment
- RES(RNpin, ckdelay) #reset
- SEL(SSEL, solution) #selection of TX topology
- STA(SSTATE1, SSTATE0, CK, state, ckdelay) #set SSTATE<1:0>
- TM(TCK, TDA, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay) #set TM shift register

The complete Python sripts of these functions is reported in Appendix A.1.

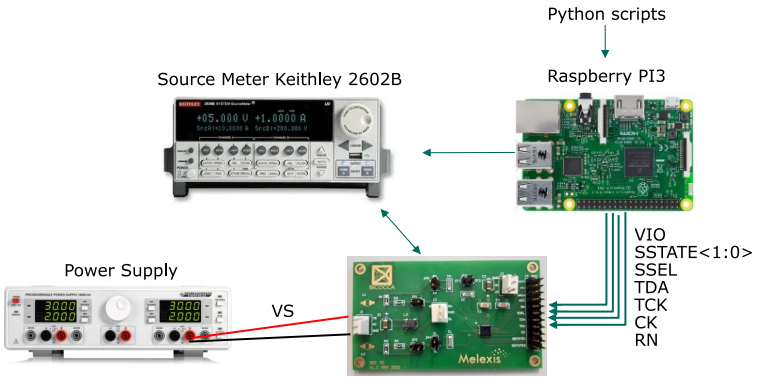

Figure 5.5: TC1 static measurements laboratory setup

Static measurements on 7 samples of TC1 were carried out. The first tests were carried out to measure the voltage $V5$ and some power supply parameters available through the AIO pin: V_{BIAS}, V_{CORE}, $IPD5U$. The measurement process was performed in an automatized way using Python scripts: the Raspberry PI3 switched the internal trimmers to all possible values (from 0 to 15), while the two channels of the source meter were connected on $V5$ and AIO to perform the measures. Details of the Python code are reported in Appendix A.2. Fig 5.6 shows the colormap of all the possible values of $V5$ obtained on the first device under test (DUT). In the default trimmers setting ($T_{V5} = 7$ and $T_{BG} = 0$) the expected value is $5.00V$ and the measured one is $5.05V$ which is really close.

Table 5.2 shows the values of $V5$ obtained for the 7 DUTs in the default trimmers setting, expected $5.5V$ setting, expected $4.5V$ setting, and the maximum and minimum measured values.

Table 5.2: Measured $5V$ over the possible settings

	V5					
	DEF	5.5V	4.5V	MAX	MIN	UNIT
DUT_1	5.05	5.55	4.52	5.70	4.48	V
DUT_2	5.00	5.50	4.48	5.64	4.44	V
DUT_3	5.02	5.51	4.50	5.66	4.46	V
DUT_4	5.01	5.51	4.49	5.66	4.45	V
DUT_5	4.98	5.47	4.46	5.61	4.42	V
DUT_6	5.02	5.53	4.50	5.67	4.46	V
DUT_7	5.09	5.54	4.55	5.68	4.47	V

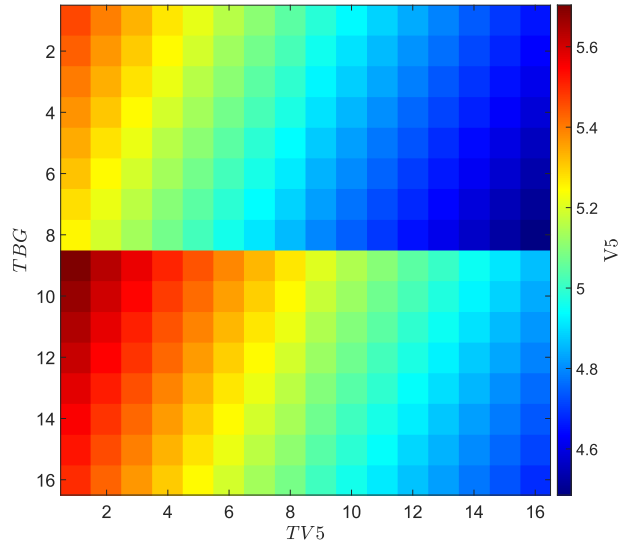

Figure 5.6: All $V5$ values measured on DUT-1

Similarly, by simply changing the value of $TMUX$, and therefore the output available on the AIO pin, the values of V_{BIAS}, V_{CORE} and $IPD5U$ were measured for all the possible trimmers configurations. The results are reported respectively in Table 5.3 and Table 5.4 for the dafault $V5$ setting, expected $5.5V$, and expected $4.5V$. The obtained results show that the measured values are perfectly in line with the expectations and that there are also no relevant differences between the 7 devices under analysis.

Table 5.3: Measured V_{CORE} and V_{BIAS} over the possible settings

	VBIAS			VCORE			
	DEF	5.5V	4.5V	DEF	5.5V	4.5V	UNIT
DUT_1	0.82	0.82	0.82	3.66	3.66	3.67	V
DUT_2	0.82	0.82	0.82	3.70	3.70	3.70	V
DUT_3	0.81	0.81	0.81	3.74	3.74	3.74	V
DUT_4	0.82	0.82	0.82	3.66	3.66	3.66	V
DUT_5	0.82	0.82	0.82	3.67	3.67	3.67	V
DUT_6	0.82	0.82	0.82	3.68	3.68	3.68	V
DUT_7	0.82	0.82	0.82	3.70	3.70	3.70	V

As a next step, the leakage current in each switch was measured. Through the source meter channels, a voltage equal to V_S was applied between the drain and source of the switch under examination and the flowing current was measured. The Python code used for the 3-Switches transmitter is reported in Appendix A.3 and can be applied similarly to the H-Bridge transmitter. The obtained leakage currents, reported in Table 5.5 and Table

Table 5.4: Measured IPD5U over the possible settings

IPD5U				
	DEF	5.5V	4.5V	UNIT
DUT_1	4.70	4.70	4.70	μA
DUT_2	4.89	4.89	4.89	μA
DUT_3	4.78	4.78	4.78	μA
DUT_4	4.68	4.68	4.68	μA
DUT_5	4.96	4.96	4.96	μA
DUT_6	4.66	4.68	4.68	μA
DUT_7	4.68	4.68	4.68	μA

5.6, are in most cases in the order of few pico-amperes, and in any case never higher than a few nano-amperes.

Table 5.5: Leakage currents in the H-Bridge transmitter

	HSS			LSS			
	DEF	5.5V	4.5V	DEF	5.5V	4.5V	UNIT
DUT_1	-13858	201	156	28	97	100	pA
DUT_2	-17095	255	119	15	96	96	pA
DUT_3	16428	227	209	251	70	82	pA
DUT_4	20069	285	-45	241	78	90	pA
DUT_5	10911	250	103	37	75	72	pA
DUT_6	-12238	202	-127	67	86	110	pA
DUT_7	18246	177	274	88	115	111	pA

Table 5.6: Leakage currents in the 3-Switches transmitter

	HSS			LSS			FS			
	DEF	5.5V	4.5V	DEF	5.5V	4.5V	DEF	5.5V	4.5V	UNIT
DUT_1	8971	-565	-507	218	26	15	-55	-66	-38	pA
DUT_2	-9440	-939	-859	30	24	18	-76	-75	-71	pA
DUT_3	-14604	-528	-723	205	32	27	-66	-66	-76	pA
DUT_4	17866	-981	-914	34	34	44	-68	-77	-78	pA
DUT_5	13398	-1094	-1013	221	23	12	-67	-48	-74	pA
DUT_6	12311	-710	-582	36	36	28	-109	-115	-124	pA
DUT_7	-12813	-990	-985	250	54	58	-85	-77	-86	pA

Finally, the on-resistances of each switch were measured. However, only for the FS it was possible to execute the measure directly since the drain and source terminals are accessible externally through the CH and CL pins. For the HSS and the LSS, indeed, as shown in

Fig. 2.9 and Fig. 2.5 respectively, the ESD protection diodes are present between the drain terminal and the external pin, making the direct measure not possible. Measures were performed by injecting a current, e.g. from $50m$ to $60mA$, and measuring the voltage in 100 points per switch. The on-resistance is then evaluated by applying Ohm's law $R = V/I$. The full Python code used for the 3-Switches transmitter is also reported in Appendix A.4 and can be applied also to the H-Bridge transmitter. As reported in Table 5.7 and Table 5.8, the FS exhibits a r_{on} of about 10Ω which, considering process variations and parasitic elements introduced by pads and connections, is very close to the expected value of 9Ω. In both the transmitter topologies, the measured values for the HSS switches have an average value of about 16Ω while the LSS has an average value of about 25Ω. Comparing the obtained results with analogous simulations including the series diodes, it can be concluded that the results are reasonable. There are no relevant differences between the 7 tested DUTs.

Table 5.7: Switches on-resistance in the H-Bridge transmitter

	HSS			LSS			
	DEF	5.5V	4.5V	DEF	5.5V	4.5V	UNIT
DUT_1	15.68	16.71	16.02	23.91	25.19	24.41	Ω
DUT_2	15.39	16.39	15.69	21.88	23.07	22.28	Ω
DUT_3	16.78	16.87	16.22	28.25	28.22	27.46	Ω
DUT_4	15.4	16.42	16.1	19.87	21.01	20.71	Ω
DUT_5	16.9	16.91	16.15	26.23	26.19	25.29	Ω
DUT_6	16.64	15.95	15.91	21.91	21.05	21.08	Ω
DUT_7	16.63	16.82	16.08	23.23	23.41	22.59	Ω

Table 5.8: Switches on-resistance in the 3-Switches transmitter

	HSS			LSS			FS			
	DEF	5.5V	4.5V	DEF	5.5V	4.5V	DEF	5.5V	4.5V	UNIT
DUT_1	16.26	16.04	15.83	24.93	24.61	24.12	10.70	10.68	10.70	Ω
DUT_2	15.62	16.69	16.12	22.64	23.92	23.32	10.40	10.43	10.43	Ω
DUT_3	16.15	17.18	16.69	27.97	29.41	28.86	10.95	10.95	10.97	Ω
DUT_4	15.64	16.58	16.10	20.24	21.28	20.80	10.01	10.05	10.03	Ω
DUT_5	17.06	16.97	16.52	26.89	26.68	26.20	10.79	10.73	10.76	Ω
DUT_6	17.00	16.45	17.05	22.60	21.89	22.72	10.17	10.18	10.19	Ω
DUT_7	16.00	16.92	16.43	22.95	24.04	23.53	10.38	10.37	10.40	Ω

5.1.2 Dynamic Measurements TC1

Data transmission tests between two nodes were carried out using the TC1. Since the Raspberry PI3 does not include a real time clock, an FPGA TE0725 from Trenz [24] that hosts a Xilinx Artix-7 XC7A100T [25] was used. Since the TC1 implements only the transmitter function, the discrete component breadboard was used as a receiver. The block diagram of the laboratory setup is shown in Fig. 5.7, while in Fig. 5.8 a real picture of the same setup is reported.

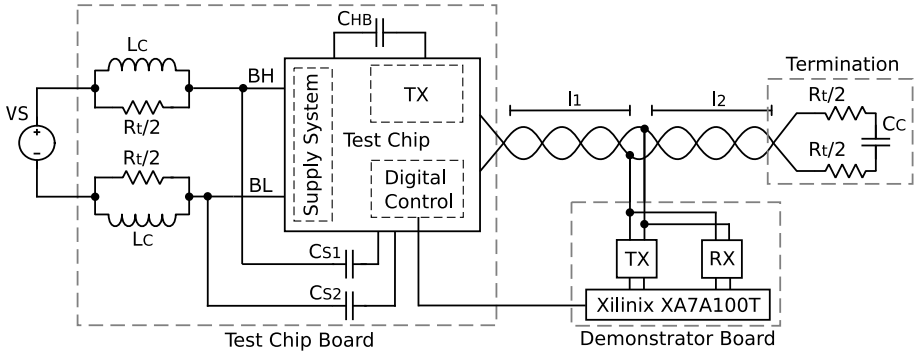

Figure 5.7: Block diagram of the data transmission measurement setup

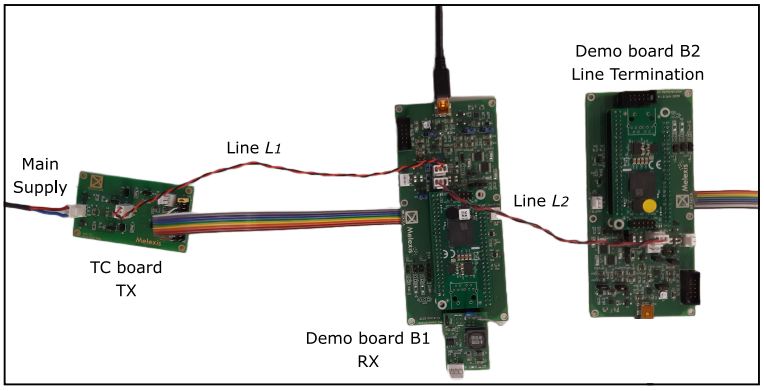

Figure 5.8: Picture of the data transmission measurement setup

The Test Chip Board, powered by a standard bench power supply, is connected via a twisted pair cable of length l_1 to the first breadboard ($B1$) which acts as a receiver. Another segment of twisted pair cable of length l_2 connects $B1$ to a second breadboard ($B2$) which is not supplied and acts just as a line termination of 50Ω. The FPGA is mounted on $B1$ and, moreover, it is connected to the TC1 board through a dedicated cable so that it is both driving the transmission and managing the reception of the signal. A digital circuit

handled as a configuration file that can be uploaded to the FPGA is implemented for the testing. The circuit takes the outputs from the receiver, synchronizes them with the FPGA master clock which has a frequency of $100Mhz$ and through a decoder extracts the data signal using a coding scheme. For the 3-switches transmitter the coding is immediate as the signal has both negative and positive pulses. For the H-bridge it is possible to implement either a direct coding or a URZ code as summarized in Table 5.9.

Table 5.9: Coding schemes

TX Topology	Coding
H-Bridge TX	Direct coding
	Unipolar return-to-zero code (RZ)
3-Switches TX	Simple coding

The received and transmitted data streams are then compared and in case the error counter overflows, an error flag is set which is visualized by a light emitting diode (LED) located on the FPGA board. In the TC1 board, $100\mu H$ surface mounted inductors and 50Ω resistors were used to populate L_1, L_2, R_1, and R_2, while L_3 was left un-populated. The default settings for the supply system were used as it was verified that the values generated under these conditions are as expected. The data transmission is regulated by a 9-bit pseudo-random bit stream (PRBS) generator. The received data stream and the recovered clock are available at the outputs of the UART/CAN interface.

The first communication tests were carried out using $820pF$ switching capacitors so that, by using equations 2.1, 2.3, and 2.4, a data rate of 2Mbps is achievable for both the H-Bridge and the 3-Switches:

$$\tau_{charge1-4,2-3} = (R_t/2 + R_{HSS} + R_{LSS}) \times C_{HB} = 63ns \tag{5.1}$$

$$\tau_{charge} = (R_t/2 + (R_{HSS}//R_{LSS})) \times 2C_S = 105ns \tag{5.2}$$

$$\tau_{discharge} = (R_t/2 + R_{FS}) \times C_S/2 = 28ns \tag{5.3}$$

Three different combinations of twisted pair cables length l_1 and l_2 were tested: $l_1 = l_2 = 0.25m$, $l_1 = 6.00m, l_2 = 0.25m$, and $l_1 = 0.25m, l_2 = 6.00m$. Fig. 5.9 and Fig. 5.10 show the differential bus measured at the RX node (therefore at a distance l_1 from the TX), the received data, and the received clock when $l_1 = 6.00m$ and $l_2 = 0.25m$ are used. A URZ coding was applied for the H-Bridge transmitter.

Table 5.10 and Table 5.11 report the amplitudes of the measured peaks at the RX and termination nodes, and the capacitor charging times for the H-Bridge and the 3-Switches topologies respectively. The attenuation introduced by the $6.00m$ cable is evident even if it

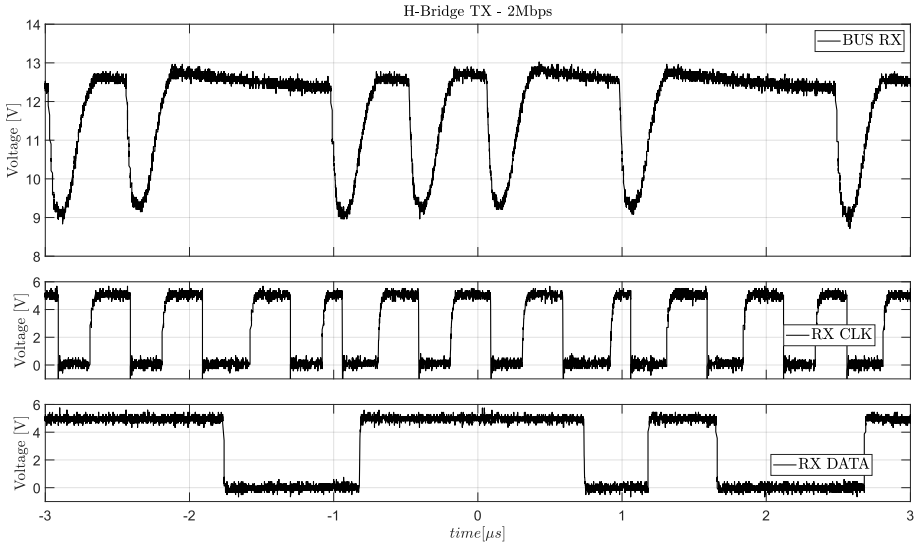

Figure 5.9: H-Bridge TX: Data transmission measurement result with switching capacitors of 820pF, cable lenghts of $l_1 = 6.00m$ and $l_2 = 0.25m$

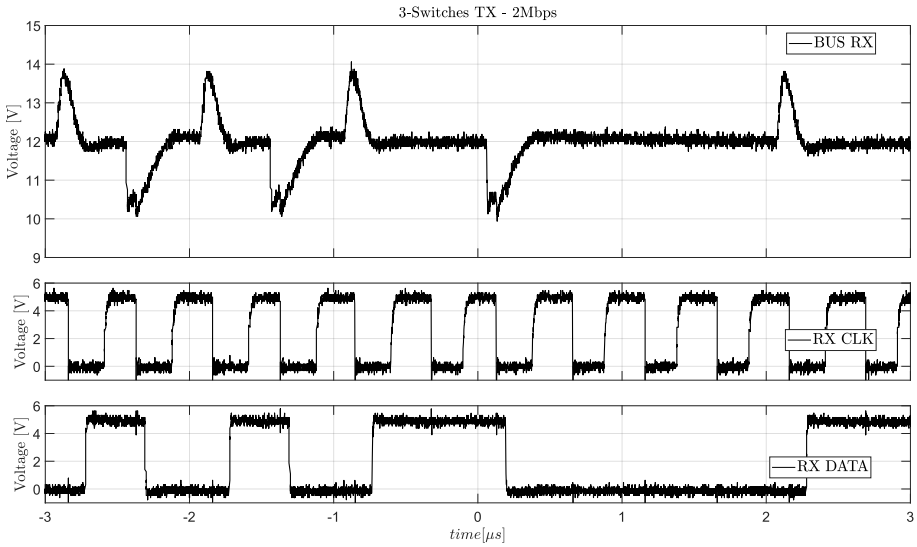

Figure 5.10: 3-Switches TX: Data transmission measurement result with switching capacitors of 820pF, cable lenghts of $l_1 = 6.00m$ and $l_2 = 0.25m$

is still not critical as the pulse amplitude is higher than $1V$. The charging time can be estimated by the curves measured by an oscilloscope to the switching capacitor terminals as illustrated in Fig. 5.11. The difference in CH and CL during the charge state is due to the asymmetry introduced by the HSS and the LSS in the parallel charge. The obtained results match with the expectation from the theoretical assumption, considering that the capacitors are not completely discharged to ground in the 3-Switches approach.

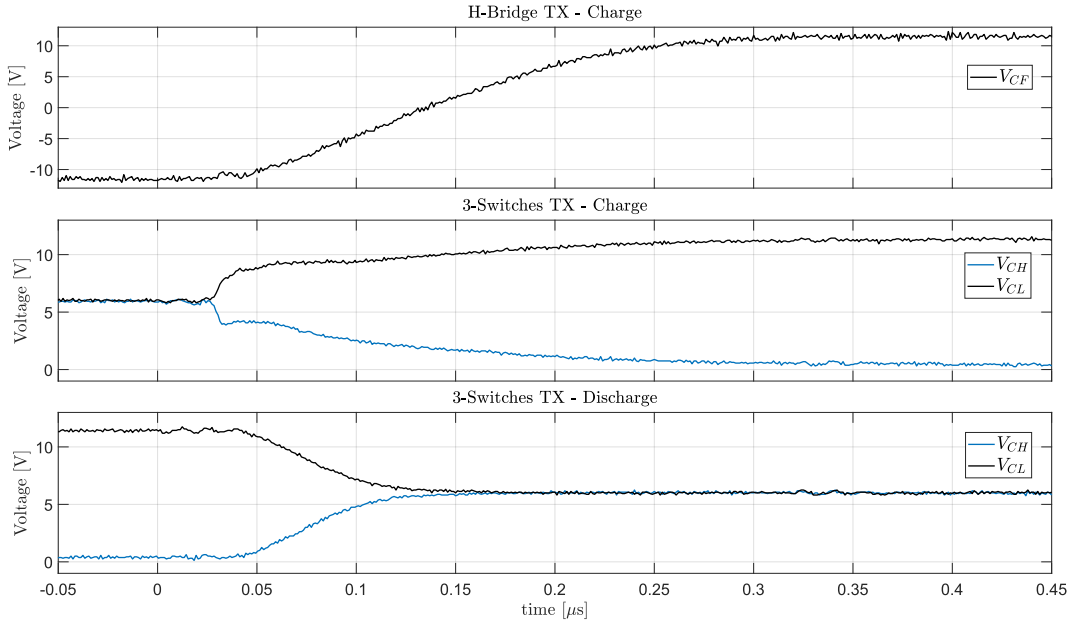

Figure 5.11: Measured voltages across switching capacitors

Table 5.10: Result of H-Bridge TX with $820pF$ switching capacitors

		l1=0.25m l2=0.25m	l1=6.00m l2=0.25m	l1=0.25m l2=6.00m
$\Delta V[V]$	Charge	3.29	2.85	4.35
$4\tau[ns]$	Charge	240	251	246

Table 5.11: Result of 3-Switches TX with $820pF$ switching capacitors

		l1=0.25m l2=0.25m	l1=6.00m l2=0.25m	l1=0.25m l2=6.00m
$\Delta V[V]$	Charge	2.88	2.13	3.38
$4\tau[ns]$	Charge	211	254	203
$\Delta V[V]$	Discharge	2.5	1.81	2.81
$4\tau[ns]$	Discharge	96	95	94

Further tests for purely investigative purposes were carried out with capacitor values of $330pF$ and $180pF$ which would theoretically allow reaching data rates of 5Mbps and 10Mbps respectively. The results obtained with the $330pF$ are shown in Fig. 5.12 and Fig. 5.13, while the resulting values are reported in Table 5.12 and Table 5.14. Finally, results for the $180pF$ are reported in Table 5.13 and Table 5.15 however, the proposed design is done for a 2Mbps target and hence it does not foresee such high data rates where parameters like the switches transition times and the parasitic effects along the line start giving a significant contribution and more effort should be spent.

Table 5.12: Result of H-Bridge TX with $330pF$ switching capacitors

		l1=0.25m l2=0.25m	l1=6.00m l2=0.25m	l1=0.25m l2=6.00m
$\Delta V[V]$	Charge	3.16	2.6	4.04
$4\tau[ns]$	Charge	120	124	125

Table 5.13: Result of H-Bridge TX with $180pF$ switching capacitors

		l1=0.25m l2=0.25m	l1=6.00m l2=0.25m	l1=0.25m l2=6.00m
$\Delta V[V]$	Charge	2.75	2.19	3.14
$4\tau[ns]$	Charge	81	91	83

Table 5.14: Result of 3-Switches TX with $330pF$ switching capacitors

		l1=0.25m l2=0.25m	l1=6.00m l2=0.25m	l1=0.25m l2=6.00m
$\Delta V[V]$	Charge	2.63	1.59	2.88
$4\tau[ns]$	Charge	97	140	114
$\Delta V[V]$	Discharge	1.31	1.03	1.56
$4\tau[ns]$	Discharge	72	72	70

Table 5.15: Result of 3-Switches TX with $180pF$ switching capacitors

		l1=0.25m l2=0.25m	l1=6.00m l2=0.25m	l1=0.25m l2=6.00m
$\Delta V[V]$	Charge	2.16	1.44	2.44
$4\tau[ns]$	Charge	55	96	78
$\Delta V[V]$	Discharge	0.78	0.59	0.97
$4\tau[ns]$	Discharge	65	59	60

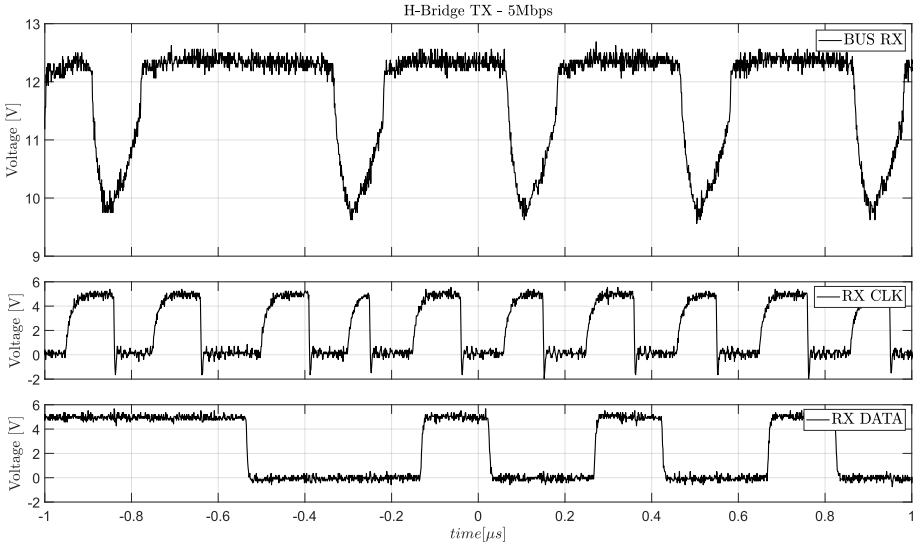

Figure 5.12: H-Bridge TX: Data transmission measurement result with switching capacitors of $330pF$ and cable lenghts of $l_1 = l_2 = 0.25m$

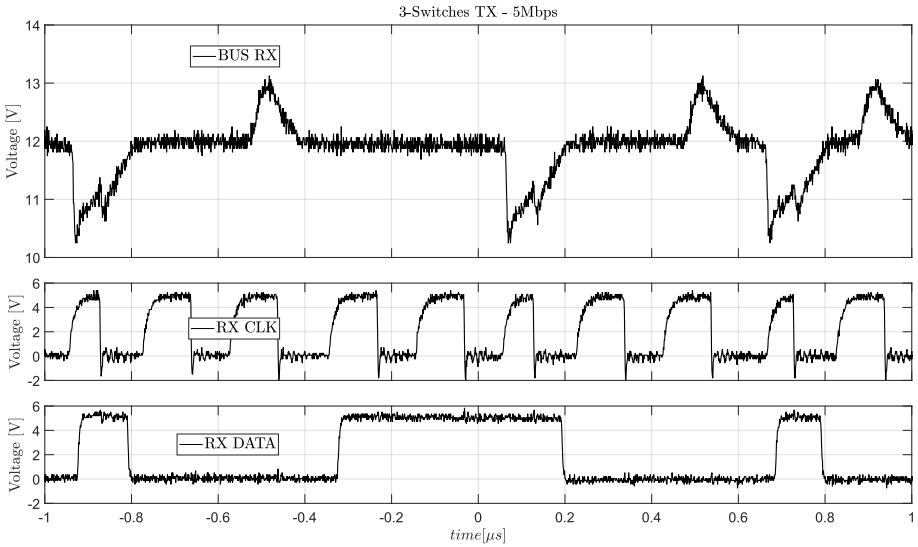

Figure 5.13: 3-Switches TX: Data transmission measurement result with switching capacitors of $330pF$ and cable lenghts of $l_1 = l_2 = 0.25m$

5.2 Test Chip 2 Validation

The TC2 is first validated by advanced post layout top level simulations by using the simulation setup of Fig. 5.14, which is composed of two transceivers connected to each other via a $1m$ reliable RGLC-model of a twisted pair cable to emulate a real automotive environment. The first TC2 (TC-T) is configured as a transmitter, therefore its RX is not activated, while the second TC2 (TC-R) works only as a receiver. The configuration settings and the stimulus are generated via a Verilog code.

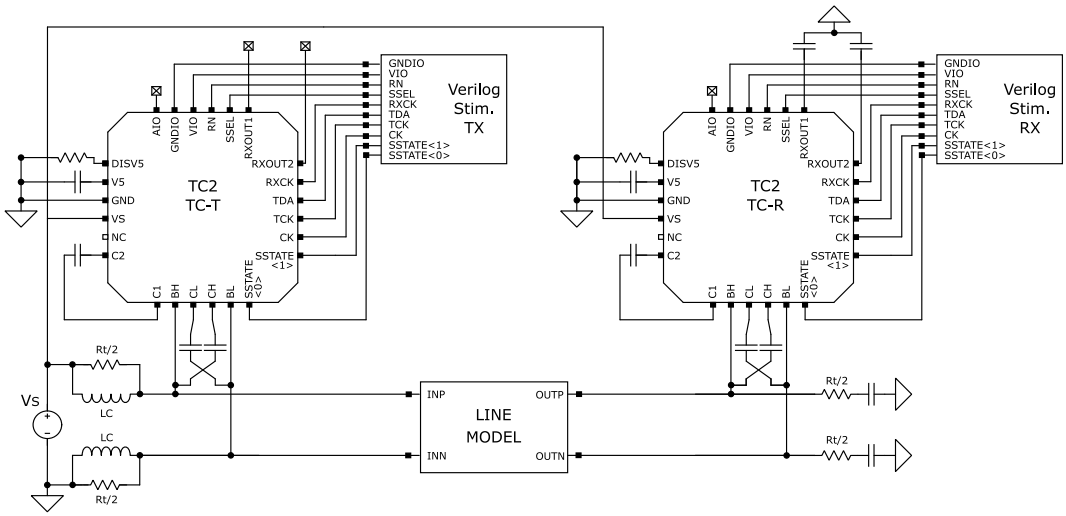

Figure 5.14: Setup of the top Level Virtuoso test bench for the TC2

After an initial reset, and after having waited a sufficient time to stabilize the power supplies, the RX function is enabled in the TC-R and the tunable parameters are set. The input division is set to 7.1 for both BH and BL which means, according to Fig. 4.3 DIVD set to 0x33. The hysteresis is set to $\approx 150mV$ for the right arm of the StrongArm Latch-1 and the left arm of the StrongArm Latch-2 while is kept to 0 for the other 2 branches so that one Latch can detect positive pulses while the other can detect the negative (CNT1 set to 0x0B and CNT2 set to 0xB0). An external 20MHz RX clock is generated in Verilog. In the real implementation, a clock of 50MHz is expected to be usually present in a node, but a lower value was chosen to speed up the simulation. Subsequently, the $SSTATE < 1 : 0 >$ of the TC-T are toggled according to a 2Mbps clock, and so it starts transmitting data. Initially, the $SSEL$ signal is set to 0 and thus the H-Bridge Topology is selected. In Fig. 5.15 the simulation results show that tha StrongArm Latch 2 is detecting all the negative pulses correctly while the Latch 1 can be negleted in this case since the signal is unipolar. At $188\mu s$ the $SSEL$ signal is switched to 1 and, after a few μs, a new data sequence is transmitted via 3-Switches TX, so both the receiver outputs are needed now. As illustrated

in Fig. 5.15 all the pulses in both directions are detected successfully and the signal can be easily reconstructed.

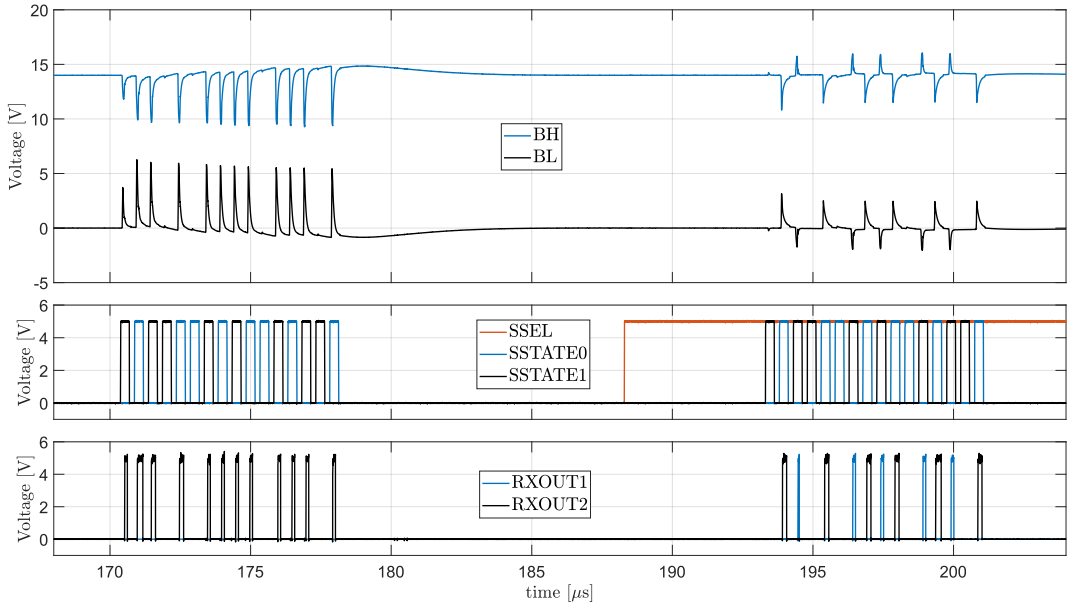

Figure 5.15: Top level post layout simulation of the TC2

The design was then validated in the laboratory. A new PCB for testing, illustrated in Fig. 5.16, was designed similarly to the one in Fig. 5.2. The interface connector J_4 was extended, and an RC path and a SMB connector were added to eventually perform Direct Power Injection (DPI) tests as described in [9]. A $100\mu H$ coupled inductor acting in differential mode was placed as input supply feed and $820pF$ switching capacitors were chosen to still ensure 2Mbps data rate.

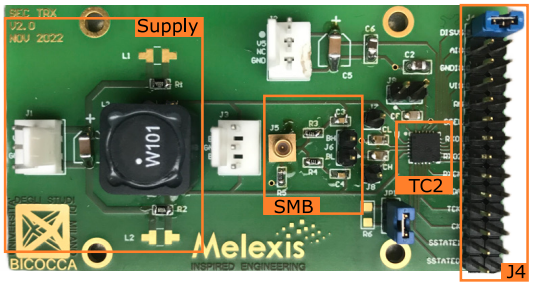

Figure 5.16: Picture of the PCB for testing designed for the TC2

Quasi-static parameters (enables, supply system settings, RX parameters, transmitter topology selection) were controlled via Raspberry PI3 by extending the previous Python

package as reported in Appendix A.5, while the communication was delegated to the TE0725 FPGA, which also provided a $50MHz$ clock to the receiver. A single node with both TX and RX functions enabled was tested and, as conseguence, higher pulses than in the previous cases were detected. In Fig. 5.17 the H-Bridge TX is used to transmit, and the RX is configured with the maximum divison factor (DIVD = 0xFF) and an hysteresis of around 80mV (CNT1 = 0x0B and CNT2 = 0xB0). The pulses are reduced to $\approx 1.2V$ and therefore are detected by the RXOUT2, while RXOUT1 is quiet. In Fig. 5.18 the 3-Switches TX is selected and since the pulses are around 3 times smaller, the RX is set with the minimum division factor (DIVD = 0x00) to get a similar value as before. The hysteresis is still set to 80mV and hence the pulses are correctly detected.

In the three plots in Fig. 5.19 the dividing factor was fixed to the maximum value (DIVD = 0xFF), while the hysteresis was varied between $100mV$, $115mV$ and $130mV$ (CNT1 = 0x08, 0x09, 0x0A and CNT2 = 0x80, 0x90, 0xA0 respectively). Due to the not perfect symmetry, the pulses in the charge phase measure about $2.0V$, while those in the discharge phase measure about $2.2V$. Assuming that the dividing factor is exactly as expected from the post-layout simulation and thus around 14.9 according to Table 3.1, the pulses are scaled to about $130mV$ and $145mV$ respectively. With the first hysteresis value, all pulses are detected correctly. With the next setting, only the pulses during the discharge are detected due to the slightly higher value, while with the hysteresis set to $130mV$, no pulses are detected at all. Recalling that, as explained in Chapter 3, the differential buffer introduces an additional attenuation of 20% - 25%, it can be concluded that the results obtained are extremely close to the expectations.

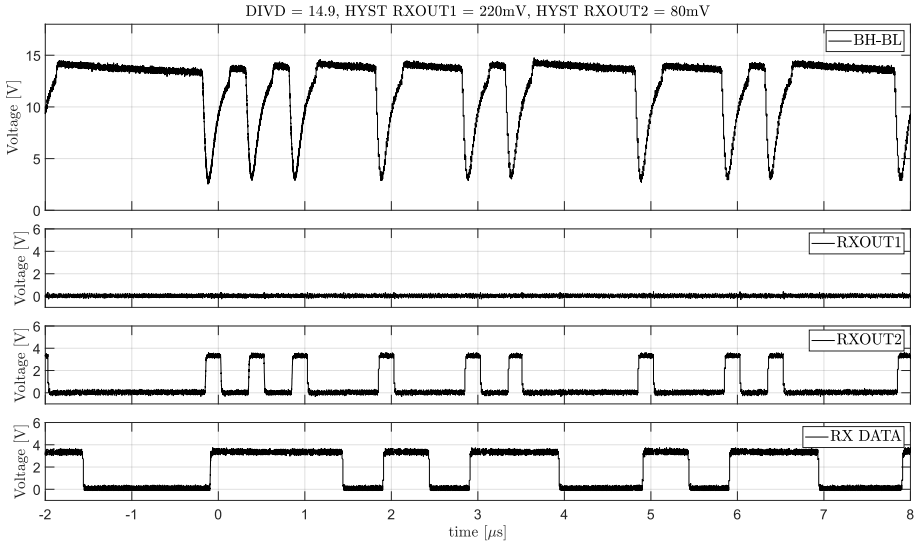

Figure 5.17: TC2 single node test with H-Bridge TX

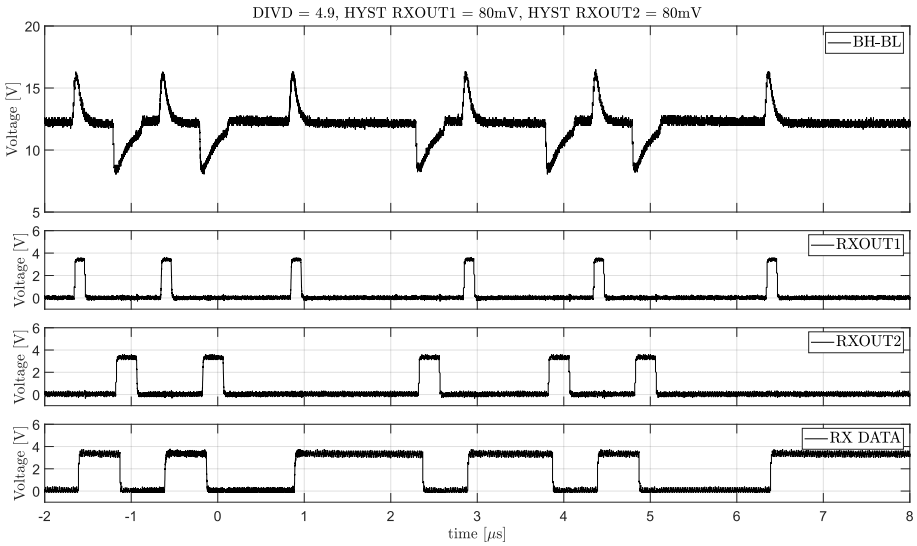

Figure 5.18: TC2 single node test with 3-Switches TX

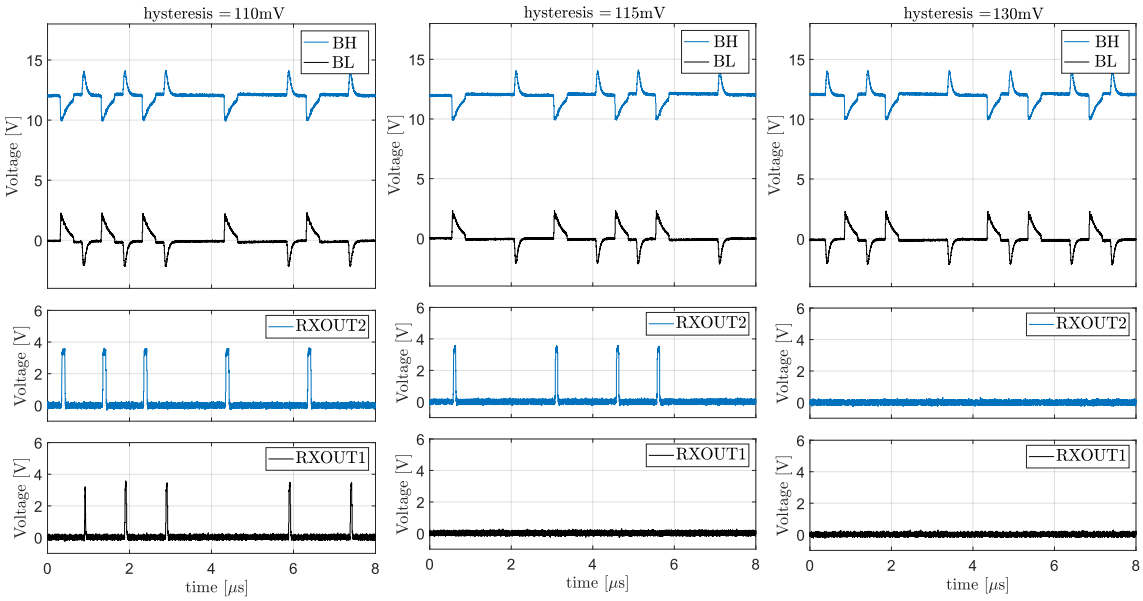

Figure 5.19: TC2 single node test with different hysteresis settings

CHAPTER 6

Bandgap Reference Circuit with 2nd Order Curvature Compensation

As a side project, a Bandgap Reference circuit with second order curvature compensation was designed in a 110nm CMOS SOI technology. The activity aimed to obtain a circuit capable of providing a voltage of about $1.1 \sim 1.2V$ with a variation as small as possible in a temperature range from $-40°C$ to $175°C$. In Section 6.1 a brief history and introduction to the bandgap circuit are presented. The circuit design is proposed in Section 6.2 and is validated in Section 6.3 by simulations.

6.1 Introduction

With the beginning of integrated electronic production in the 1950s, the need for precise integrated voltage references came out. A Bandgap Reference is a circuit capable of producing a stable and constant voltage independent of power fluctuations, temperature variations, and load swings. Nowadays, voltage references are used in almost every modern integrated circuit (IC) design as in A/D and D/A converters, voltage regulators, and measurement systems, and so they are one of the most important blocks to design. Temperature independence in electronics can usually be obtained by combining two different effects with opposite temperature coefficient (TC). It is well known that the voltage across a forward-biased diode, and hence the base-emitter voltage of a bipolar junction transistor (BJT), has a negative TC [26]. Indeed, for a constant collector current,

$$\frac{\delta V_{BE}}{\delta T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \tag{6.1}$$

where T is the absolute temperature, $m \approx -3/2$, $V_T = kT/q$ is the thermal voltage, and E_g is the bandgap energy.

In 1964 Hilbibier of Fairchild Semiconductor noticed that two diode stacks biased with different currents generate a voltage with positive TC [27]. According to Fig. 6.1, the obtained difference

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T ln(nI_0/I_S) - V_T ln(I_0/I_S) = V_T ln(n) \tag{6.2}$$

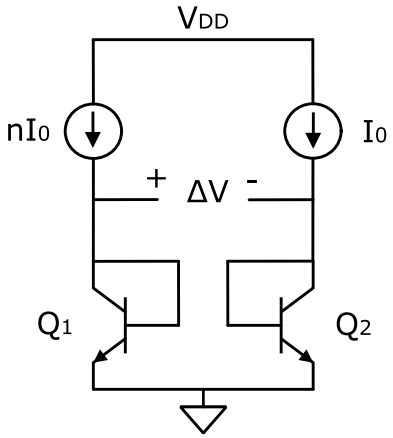

Figure 6.1: Positive TC voltage across two diode

has a positive TC, and so can be added to a V_{BE} to get a temperature independent voltage. The same result can be obtained by injecting equal currents in bipolar devices of different sizes, i.e. $Q_1 = nQ_2$. Later, in 1971, Widlar developed the circuit of Fig. 6.2, which is the first Bandgap Reference based on that concept [28, 29]. The circuit sum the proportional to absolute temperature (PTAT) voltage $V_{PTAT} = (R_2/R_3)\Delta V_{BE}$ and the complementary to absolute temperature (CTAT) voltage V_{BE3} across the forward-biased base-emitter diode Q_3.

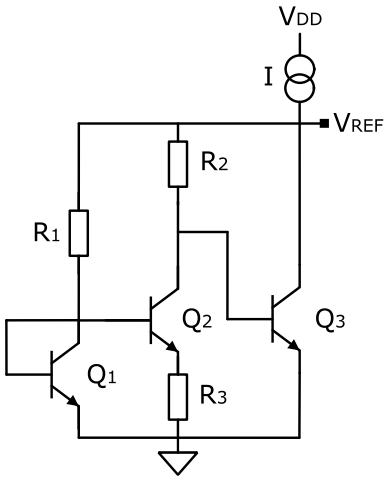

Figure 6.2: Widlar Bandgap Reference

Many other circuits were proposed in the following years to improve Bandgap Reference performances [30–32]. For a BJT with typical current densities $V_{BE} = V_T ln(I_C/I_S) \approx$

$750mV$ at room temperature, yielding a TC of about -1.5 mV/K. To compensate for such value, the n factor of Eq. 6.18 needs to be extraordinarily big making the real implementation not feasible. This issue can be solved by amplifying the PTAT term before it is added to the CTAT as in the circuit of Fig. 6.3 proposed by Kujik in 1973 [32]. Thanks to the non-inverting amplifier A, the output voltage can be written as:

$$V_{BG} = V_{BE1} + \Delta V_{BE}\frac{R_2}{R_1} \tag{6.3}$$

$$= V_{BE1} + V_T ln(n)\frac{R_2}{R_1} \tag{6.4}$$

and the ratio of resistors R_2 and R_1 can be used to reduce n to a reasonable value (e.g. $8 \sim 16$).

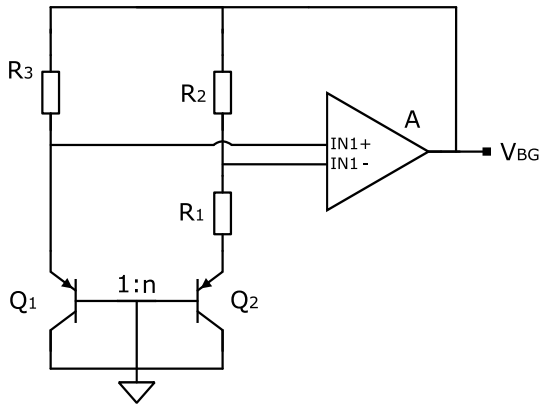

Figure 6.3: Kujik Bandgap Reference

However, a circuit like this, which implements a first order temperature compensation, has a strong limitation due to the nonlinear TC in the base-emitter voltage of the bipolar junction transistor [33, 34]. In modern applications where temperature coefficients lower than 20 ppm/K are required, to overcome this limitation, a variety of multi order temperature compensation methods have been developed, such as resistor ratio based [35], and generating a nonlinear current to compensate the non-linear V_{BE} of BJT [36–39].

6.2 Proposed 2nd order compensated Bandgap Reference

A Bandgap Reference Circuit with second order curvature compensation is presented in Fig. 6.4. The basic network is similar to the one of Fig. 6.3 proposed by Kujik, except that trimmer resistor R_4 is added as in [40]. The second-order compensation is performed by

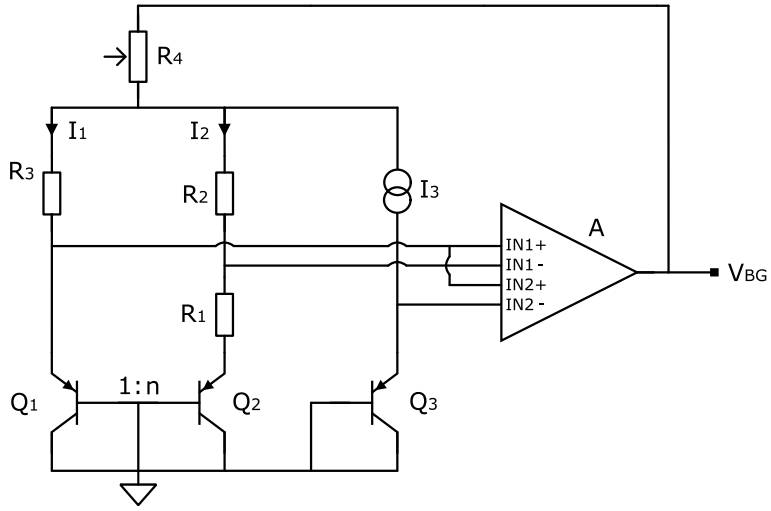

Figure 6.4: Proposed Bandgap Reference

comparing the V_{BE1} of bipolar Q_1 polarized with the PTAT current $I_{PTAT} = \Delta V_{BE12}/R_1$ and the V_{BE3} of bipolar Q_3 polarized with a CTAT current. The CTAT current can be obtained in many ways, e.g. by applying across a resistor a CTAT voltage as V_{BE} [37], or V_{BG} itself [38]. This mean that the operational amplifier A now has two input stages: the first input stage is dedicated to first order compensation as in almost every previously presented design, while the second stage is dedicated to additional compensation. The output voltage of the proposed circuit can therefore be written as

$$V_{BG} = [gm_1(V_{1+} - V_{1-}) + gm_2((V_{2+} - V_{2-})]r_{out} \tag{6.5}$$

where r_{out} is the output resistance of the operational amplifier, g_{m1} and g_{m2} are the transconductances of the first and second input stages respectively. According to Fig. 6.4, the inputs of the amplifier can be written as

$$V_{1+} = V_{BE1} \tag{6.6}$$

$$V_{1-} = V_{BE2} + I_2 R_1 + V_{OS} \tag{6.7}$$

$$V_{2+} = V_{BE1} \tag{6.8}$$

$$V_{2-} = V_{BE3} \tag{6.9}$$

and the Eq. 6.5 can be rewritten as

$$V_{BG} = [(V_{BE1} - V_{BE2} - I_2R_1 - V_{OS}) + \frac{gm_2}{gm_1}(V_{BE1} - V_{BE3})]A_1 \tag{6.10}$$

where $A_1 = g_{m1}r_{out}$. Voltages across the resistors are given by the following expressions:

$$V_{BG} = (I_1 + I_2)R_4 + I_1R_3 + V_{BE1} \tag{6.11}$$

$$V_{BG} = (I_1 + I_2)R_4 + I_2(R_1 + R_2) + V_{BE2} \tag{6.12}$$

and the currents I_1 and I_2 in the two branches of the Bandgap network can be found:

$$I_1 = \frac{V_{BG} - V_{BE2} - I_2(R_1 + R_2 + R_4)}{R_4} \tag{6.13}$$

$$I_2 = \frac{V_{BG}R_3 + R_4(V_{BE1} + V_{BE2}) - R_3V_{BE2}}{F} \tag{6.14}$$

where F is a proportional factor given by

$$F = R_1R_4 + R_2R_4 + R_1R_3 + R_2R_3 + R_3R_4 \tag{6.15}$$

Finally, Eq. 6.10 can be rewritten highlighting the compensation factors the for first and second order compensations:

$$\begin{aligned} V_{BG} = \frac{A_1}{1 + \frac{A_1R_1R_3}{F}}[V_{BE1}(1 - \frac{R_1R_4}{F}) - V_{BE2}(1 - \frac{R_1(R_3 + R_4)}{F}) - V_{OS} \\ + \frac{gm_2}{gm_1}(V_{BE1} - V_{BE3})] \end{aligned} \tag{6.16}$$

The first order compensation is already well known [40] while the second part depends on ΔV_{BE13} and the ratio g_{m2}/g_{m1}. Assuming that Q_1 and Q_3 have the same size, and hence the same I_S, the term ΔV_{BE13} merely depends on the ratio of the emitter currents:

$$\Delta V_{BE13} = V_{BE1} - V_{BE3} = V_T ln(I_1/I_S) - V_T ln(I_3/I_S) = V_T ln(I_1/I_3) \tag{6.17}$$

If the input devices of the two input stages of the operational amplifier A operate in saturation, $g_m = \sqrt{\mu C_{OX} 2 I_D \frac{W}{L}}$, and assuming a relation between device sizes and current

tails respectively $W_1 = NW_2$ and $I_{D1} = MI_{D2}$, the term g_{m2}/g_{m1} can be written as:

$$\frac{g_{m2}}{g_{m1}} = \frac{\sqrt{\mu C_{OX} 2 I_{D2} \frac{W_2}{L_2}}}{\sqrt{\mu C_{OX} 2 I_{D1} \frac{W_1}{L_1}}} = \frac{1}{\sqrt{NM}}. \tag{6.18}$$

On the other hand, if these devices are operating in sub-threshold, $g_m \approx 2I_D/(V_{GS} - V_{TH})$ and hence $g_{m2}/g_{m1} = 1/N$.

6.3 Simulation Results

The equations derived in the previous section were implemented in a mathematical model used to find the best trade-off between the parameters. According to the obtained result, the circuit of Fig. 6.4 was implemented in Cadence Virtuoso in a 110nm CMOS SOI technology.

For the circuit of Fig. 6.3, which realizes only the first order compensation, the best sizing of the resistors network was found to be $R_1 = 19.5k\Omega$, $R_2 = R_3 = 56k\Omega$, $R_4 = 68k\Omega$ while the ratio between Q_1 and Q_2 was selected equal to 8. The results over a temperature range from $-40°C$ to $175°C$ of the mathematical model and the real circuit simulation in typical corner are shown in Fig. 6.5. The maximum variation from the room temperature value is $3.1mV$ for the circuit simulation, and $4.2mV$ for the theoretical model.

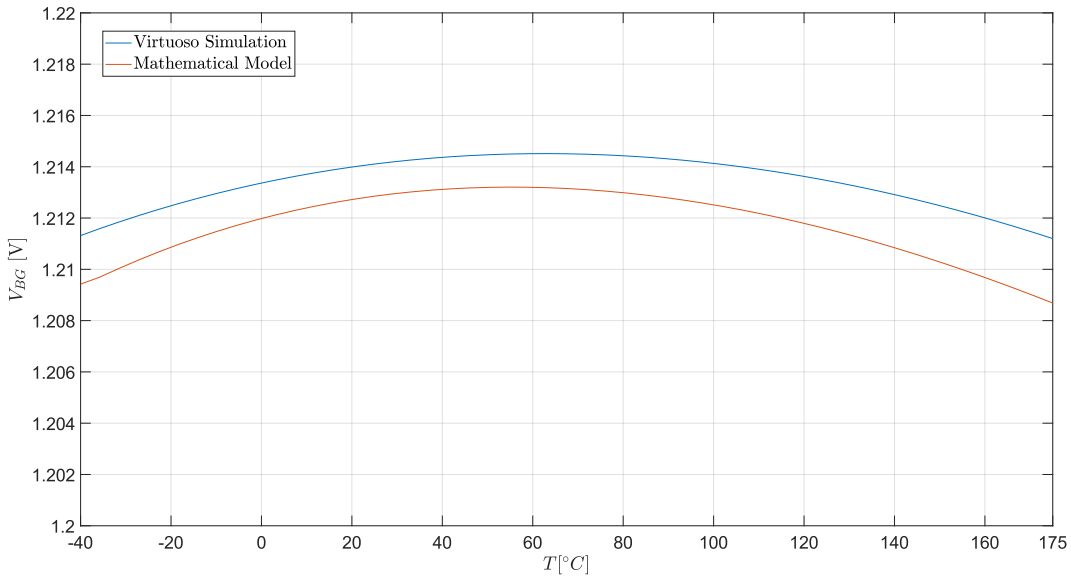

Figure 6.5: Comparison between the mathematical model and the schematic simulation for the 1st order compensation design

When the second order compensation is introduced, many parameters start playing a role and obtaining a good matching between the mathematical model and the Virtuoso simulation becomes quite challenging. Indeed, some ideal assumptions were considered to derive equations:

- the operational amplifier gain was assumed $\rightarrow \infty$;
- the currents I_1 and I_2 were supposed equal, while in reality the mismatch and the non-ideality of the amplifier made them slightly different;

Moreover, it turned out that the modeling of some technological parameters (e.g. the BJT saturation current I_S) greatly influences the accuracy of the equations and therefore a great effort should be spent for a good result. For these reason, although the model is still useful as a starting point, parameter simulations need to be run to find the best circuit sizing.

In Fig. 6.6 the comparison between the mathematical model and the Virtuoso simulation is reported. The resistive network is sized with $R_1 = 27.4k\Omega$, $R_2 = R_3 = 60.1k\Omega$, $R_4 = 76k\Omega$. The current I_3 in Q_3 is equal to $900nA$, while $I_1 = I_2 = 3\mu A$. Finally, the ratio g_{m2}/g_{m1} is chosen equal to 1/15 with devices operating in sub-threshold. Both curves show a change in the slope as typical for second-order compensated bandgap, but precise matching is not achieved. The proposed design shows a DC value of around $1.165V$ and has a deviation from maximum to minimum value of just $730\mu V$.

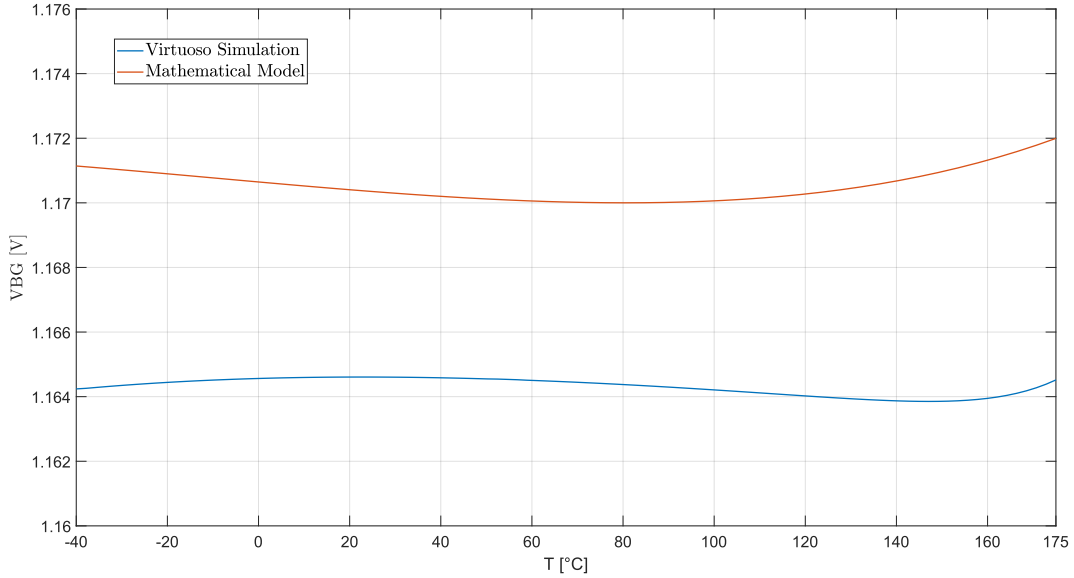

Figure 6.6: Comparison between the mathematical model and the schematic simulation for the 2nd order compensation design

A corner simulation plus R_4 trimming in a 6σ process spread from $-40°C$ to $175°C$ is shown in Fig. 6.7. Resistor R_4 is swept from $68k\Omega$ to $83k\Omega$ by the use of 4-bits. The maximum variation from the room temperature in the range from $0°C$ to $125°C$ is lower than $1mV$ in all corner except corner 6 where is $2.5mV$ as shown in Table 6.1. The maximum variation in the full temperature range is lower than $1.75mV$ in most of the corners making exception for corner 6, 13 and 14. Corner 6 can be easily adjusted to $< 1.75mV$ too by extending the trimming range to lower value ($65k\Omega$), while corner 13 and corner 14 show a slight divergence of the curve at very low temperature ($< -20°C$) which does not depend on the sizing of the network but on the polarization of the circuit itself, which should therefore be revised.

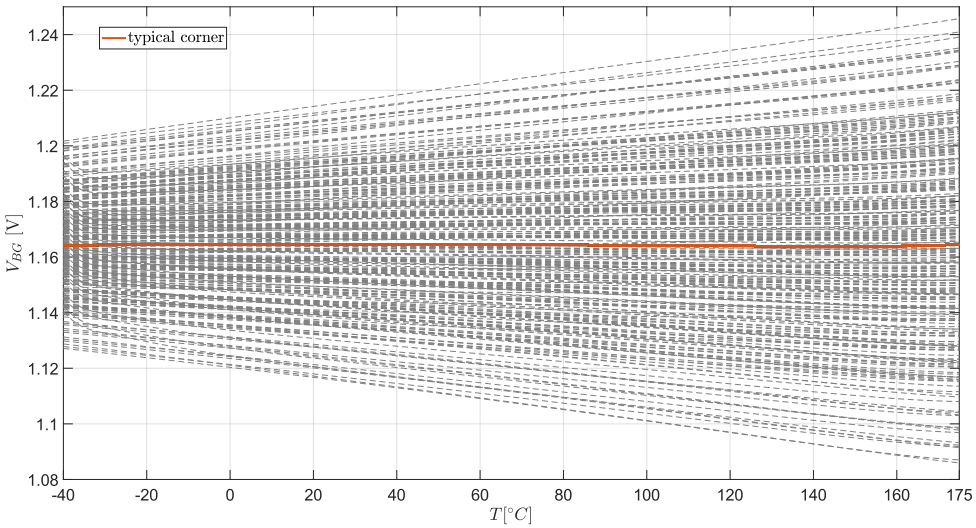

Figure 6.7: Corners simulation of the proposed circuit

Table 6.1: Bandgap simulation with the best trimming setting for each corner

Corner	$V_{MAX} - V_{T0}$ [0:125]$°C$ [mV]	$V_{MAX} - V_{T0}$ [0:175]$°C$ [mV]	Corner	$V_{MAX} - V_{T0}$ [0:125]$°C$ [mV]	$V_{MAX} - V_{T0}$ [0:175]$°C$ [mV]
1	0.24	0.28	9	0.16	1.28
2	0.26	0.41	10	0.28	1.41
3	0.03	0.71	11	0.23	1.06
4	0.15	0.80	12	0.37	1.75
5	0.08	0.83	13	0.14	4.70
6	2.53	4.50	14	0.23	5.02
7	0.48	0.69	15	0.24	1.36
8	0.17	1.33	16	0.56	1.25

CHAPTER 7

Conclusion

In this work, the design of a Supple-Embedded Communication transceiver for differential automotive networks was proposed. Two different transmitter circuits based on switching capacitors were analyzed. The H-Bridge topology requires fewer external components (1 switching capacitor) than the 3-Switches topology (2 switching capacitors), but its current consumption is 8-times higher. Moreover, it occupies an area 1.4 times bigger than the 3-Switches implementation and a coding scheme is required to reconstruct the transmitted signal. A test chip was realized to validate the proposed implementations and was successfully tested in the laboratory by connecting it to a discrete component demonstrator receiver board. A data rate of 2Mbps was reached and, furthermore, operations up to 5Mbps and 10Mbps have been theoretically proven. A receiver based on StrongArm Latches was proposed and implemented in a second test chip to realize a full Supply-Embedded Communication transceiver. The circuit includes many tunable parameters that make the design very flexible. The chip was validated by top level post layout simulations in a real automotive environment model and by laboratory measurements which showed a good matching with the simulations. The use in real applications must be tested in the near future to actually provide benefits in the automotive wiring harness.

As a side project, a second order curvature compensated bandgap reference circuit was designed. The circuit exhibited a maximum deviation from the value at room temperature of just $730\mu V$ in the typical corner and has been tested over corners with good results. A mathematical model has been proposed but better modeling of some parameters is required for a perfect matching with the circuit simulations. The validity of the proposal will be verified by a test chip in the close future.

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List of Figures

List of Tables

A Appendix Python Scripts

A.1 Supply-Embedded Communication Package

```
import RPi.GPIO as GPIO
import time
GPIO.setmode(GPIO.BCM)
GPIO.setwarnings(False)

def INIT(RN, SSEL, SSTATE1, SSTATE0, CK, TCK, TDA):
    GPIO.setup(RN, GPIO.OUT)
    GPIO.output(RN, GPIO.LOW)
    GPIO.setup(SSEL, GPIO.OUT)
    GPIO.output(SSEL, GPIO.LOW)
    GPIO.setup(SSTATE1, GPIO.OUT)
    GPIO.output(SSTATE1, GPIO.LOW)
    GPIO.setup(SSTATE0, GPIO.OUT)
    GPIO.output(SSTATE0, GPIO.LOW)
    GPIO.setup(CK, GPIO.OUT)
    GPIO.output(CK, GPIO.LOW)
    GPIO.setup(TCK, GPIO.OUT)
    GPIO.output(TCK, GPIO.LOW)
    GPIO.setup(TDA, GPIO.OUT)
    GPIO.output(TDA, GPIO.LOW)
    # TM reg defaults:
    en_pd = 0
    en_pu = 1
    tmux = 0
    tv5 = 7
    tbg = 0
    tmwrite = 0
    return[en_pd, en_pu, tmux, tv5, tbg, tmwrite]

def RES(RN, ckdelay):
    print("# issue reset ... ")
    GPIO.output(RN, GPIO.LOW)
    time.sleep(ckdelay)
    GPIO.output(RN, GPIO.HIGH)
    tmux = 0
    tbg = 0
    tv5 = 7
```

```
38      en_pu = 1
39      en_pd = 0
40      tmwrite = 0
41
42  def SEL(SSEL, solution):
43      print('# set SSEL to ',solution)
44      if solution == 0:
45          GPIO.output(SSEL, GPIO.LOW)
46      else:
47          GPIO.output(SSEL, GPIO.HIGH)
48
49  def STA(SSTATE1, SSTATE0, CK, state, ckdelay):
50      print('# set SSTATE to ',state)
51      GPIO.output(CK, GPIO.LOW)
52      if state == 3:
53          GPIO.output(SSTATE1, GPIO.HIGH)
54          GPIO.output(SSTATE0, GPIO.HIGH)
55          tmwrite = 1 # allows writing tmreg
56      elif state == 2:
57          GPIO.output(SSTATE1, GPIO.HIGH)
58          GPIO.output(SSTATE0, GPIO.LOW)
59          tmwrite = 0 # disables writing tmreg
60      elif state == 1:
61          GPIO.output(SSTATE1, GPIO.LOW)
62          GPIO.output(SSTATE0, GPIO.HIGH)
63          tmwrite = 0 # disables writing tmreg
64      else:
65          GPIO.output(SSTATE1, GPIO.LOW)
66          GPIO.output(SSTATE0, GPIO.LOW)
67          tmwrite = 0 # disables writing tmreg
68      # CK Pulse
69      time.sleep(ckdelay)
70      GPIO.output(CK, GPIO.HIGH)
71      time.sleep(ckdelay)
72      GPIO.output(CK, GPIO.LOW)
73      return(tmwrite)
74
75  def TM(TCK, TDA, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay):
76      if tmwrite == 1:
77          tmreg = bin(en_pd*2**13 + en_pu*2**12 + tmux*2**8 + tv5*2**4 +tbg)[2:].zfill(16)
78          GPIO.output(TCK, GPIO.LOW)
79          GPIO.output(TDA, GPIO.LOW)
80          time.sleep(tckdelay)
81          print("# send TMREG ",tmreg)
82          for i in range (0,16):
```

```
83                 if tmreg[15-i] == '1':
84                     GPIO.output(TDA, GPIO.HIGH)
85                 else:
86                     GPIO.output(TDA, GPIO.LOW)
87                 time.sleep(tckdelay)
88                 GPIO.output(TCK, GPIO.HIGH)
89                 time.sleep(tckdelay)
90                 GPIO.output(TCK, GPIO.LOW)
91             GPIO.output(TDA, GPIO.LOW)
92             time.sleep(tckdelay)
93         else:
94             print("# Cannot write TM, PLEASE set SSTATE to 3 before !!!")
```

A.2 Supply parameters test

```
1  import SECpkg as PKG
2  import pyvisa as visa
3  import time
4  import numpy as np
5  import csv
6  import os
7
8  # GPIOs assignment & defaults:
9  RN=17       # J8_11 (GPIO17)
10 SSEL=18     # J8_12 (GPIO18)
11 SSTATE1=7   # J8_26 (GPIO7)
12 SSTATE0=8   # J8_24 (GPIO8)
13 CK=11       # J8_23 (GPIO11)
14 TCK=27      # J8_13 (GPIO27)
15 TDA=22      # J8_15 (GPIO22)
16 [en_pd,en_pu,tmux,tv5,tbg,tmwrite]=PKG.INIT(RN,SSEL,SSTATE1,SSTATE0,CK,TCK,TDA)
17
18 ckdelay = 0.0001       # clock delay
19 tckdelay = 0.0001      # test clock delay
20 tdelay = 1             # delay between measurements
21 mes = 0                # enable measurements
22 v = np.zeros((16,17)) # matrix to store measurements on channelA
23 w = np.zeros((16,17)) # matrix to store measurements on channelB
24 x = np.zeros(17)       # vector to store tv5 value
25
26 PKG.RES(RN,0.05)      # initial reset
27
28 rm = visa.ResourceManager('@py') # Use the pyvisa-py backend
29 address = "TCPIP0::10.49.41.51::inst0::INSTR" # Keithley DAQ6510 IP address TCP/IP string
30 sm = rm.open_resource(address)
```

```
31 sm.write("reset()") # sm initial reset
32
33 while (mes==0): # Start operation
34     print("Insert test board number:") # insert csv file name
35     tcn = input("cmd>>")
36     name = "SupplySystem1_TB"+tcn
37
38     # Set sm CHA as DC-V source, set I/V limits, I_OUT=0, tunr output ON
39     sm.write("smua.source.func = smua.OUTPUT_DCAMPS")
40     sm.write("smua.source.limitv = 3")
41     sm.write("smua.source.limiti = 0.000001")
42     sm.write("smua.source.leveli = 0")
43     sm.write("smua.source.output = smua.OUTPUT_ON")
44     # Set sm CHB as DC-V source, set I/V limits, I_OUT=0, tunr output ON
45     sm.write("smub.source.func = smub.OUTPUT_DCAMPS")
46     sm.write("smub.source.limitv = 6")
47     sm.write("smub.source.limiti = 0.000001")
48     sm.write("smub.source.leveli = 0")
49     sm.write("smub.source.output = smub.OUTPUT_ON")
50
51     tmux=4 # Set tmux=4 to measure the desired output on AIO
52     tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 3, ckdelay) # Enter STA=3 for TC config. mode
53     time.sleep(tdelay)
54     PKG.TM(TCK, TDA, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay) # Set TDA
55     time.sleep(tdelay)
56     tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 0, ckdelay) # Back to STA=0
57     print("Measuring bandgap voltage..")
58     time.sleep(tdelay)
59
60     # Use two for-cycles to trim TBG and TV5 from 0 to 15
61     for i in range(0,16):
62         tbg=i # Set TBG=i
63         tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 3, ckdelay) # Enter STA=3 for TC config. mode
64         time.sleep(tdelay)
65         PKG.TM(TCK, TDA, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay) # Set TDA
66         time.sleep(tdelay)
67         tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 0, ckdelay) # Back to STA=0
68         print("TBG set to",i)
69         time.sleep(tdelay)
70         v[i,0]=i
71         w[i,0]=i
72         for j in range (0,16):
73             tv5=j # Set TV5=j
74             tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 3, ckdelay) # Enter STA=3 for TC config.
mode
```

```
75              time.sleep(tdelay)
76              PKG.TM(TCK, TDA, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay) # Set TDA
77              time.sleep(tdelay)
78              tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 0, ckdelay) # Back to STA=0
79              print("TV5 set to",j)
80              x[j+1]=j
81              # Measure VBG and V5, printing values and store in matrix
82              sm.write("print(smua.measure.v())")
83              valuea=sm.read()
84              print("Measured value on channel A = ",valuea)
85              sm.write("print(smub.measure.v())")
86              valueb=sm.read()
87              print("Measured value on channel B= ",valueb)
88              v[i,j+1]=valuea
89              w[i,j+1]=valueb
90              time.sleep(tdelay)
91
92          if i==15 and j==15: # Complete the operation and save in csv
93              mes=1
94              with open('temp.csv','w') as f: # Build csv output file
95                  writer = csv.writer(f)
96                  header1 = ['AIO']
97                  header2 = ['V5']
98                  writer.writerow(header1)
99                  writer.writerow(x)
100                 for n in range(0,16):
101                     writer.writerow(v[n,:])
102                 writer.writerow(header2)
103                 writer.writerow(x)
104                 for m in range(0,16):
105                     writer.writerow(w[m,:])
106             os.rename('temp.csv',name +'.csv')
```

A.3 Switches leakage current

```
1  import SECpkg as PKG
2  import pyvisa as visa
3  import time
4  import numpy as np
5  import csv
6  import os
7
8  # GPIOs assignment & defaults:
9  RN=17       # J8_11 (GPIO17)
10 SSEL=18     # J8_12 (GPIO18)
```

```
SSTATE1=7   # J8_26 (GPIO7)
SSTATE0=8   # J8_24 (GPIO8)
CK=11       # J8_23 (GPIO11)
TCK=27      # J8_13 (GPIO27)
TDA=22      # J8_15 (GPIO22)
[en_pd,en_pu,tmux,tv5,tbg,tmwrite]=PKG.INIT(RN,SSEL,SSTATE1,SSTATE0,CK,TCK,TDA)

ckdelay = 0.0001        # clock delay
tckdelay = 0.0001       # test clock delay
tdelay = 1              # delay between measurements
mes = 0                 # enable measurements
v = np.zeros((3,8))     # matrix to store measurements

PKG.RES(RN,0.05)        # initial reset

rm = visa.ResourceManager('@py') # Use the pyvisa-py backend
address = "TCPIP0::10.49.41.51::inst0::INSTR" # Keithley DAQ6510 IP address TCP/IP string
sm = rm.open_resource(address)
sm.write("reset()") # sm initial reset

while (mes==0): # Start operation
    print("Insert test board number:") # insert csv file name
    tcn = input("cmd>>")
    name = "LeakageS2_TB"+tcn

    for i in range(0,3):
        if i==1: # Setting for V5 MAX
            tbg=13
            tv5=0
            tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 3, ckdelay) # STA=3
            time.sleep(tdelay)
            PKG.TM(TCK, TDA, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay) # set TDA
            time.sleep(tdelay)
            tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 0, ckdelay) # STA=0
            time.sleep(1)
        elif i==2: #V Setting for V5 MIN
            tbg=7
            tv5=14
            tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 3, ckdelay) # STA=3
            time.sleep(tdelay)
            PKG.TM(TCK, TDA, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay) # set TDA
            time.sleep(tdelay)
            tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 0, ckdelay) # STA=0
            time.sleep(1)

```

```
56          # Leakage HSS on CHA: set CHA as Voltage Source
57          sm.write("smua.source.func = smua.OUTPUT_DCVOLTS")
58          sm.write("smua.source.limitv = 12")
59          sm.write("smua.source.limiti = 0.001")
60          sm.write("smua.source.levelv = 12")
61          sm.write("smua.source.output = smua.OUTPUT_ON")
62
63          time.sleep(tdelay)
64          sm.write("print(smua.measure.v())")
65          valuea=sm.read()
66          v[i,0] = valuea
67          time.sleep(20)
68          sm.write("print(smua.measure.i())")
69          valuea=sm.read()
70          v[i,1] = valuea
71          time.sleep(5)
72          sm.write("reset()") # sm reset
73          time.sleep(5)
74
75          # Leakage LSS on CHB: set CHB as Voltage Source
76          sm.write("smub.source.func = smub.OUTPUT_DCVOLTS")
77          sm.write("smub.source.limitv = 12")
78          sm.write("smub.source.limiti = 0.001")
79          sm.write("smub.source.levelv = 12")
80          sm.write("smub.source.output = smub.OUTPUT_ON")
81
82          sm.write("print(smub.measure.v())")
83          valueb=sm.read()
84          v[i,2] = valueb
85          time.sleep(20)
86          sm.write("print(smub.measure.i())")
87          valueb=sm.read()
88          v[i,3] = valueb
89          time.sleep(5)
90          sm.write("reset()") # sm reset
91          time.sleep(5)
92
93          # Leakage FS: Set CHA and CHB as Voltage Sources
94          sm.write("smua.source.func = smua.OUTPUT_DCVOLTS")
95          sm.write("smua.source.limitv = 0.01")
96          sm.write("smua.source.limiti = 0.001")
97          sm.write("smua.source.levelv = 0")
98          sm.write("smua.source.output = smua.OUTPUT_ON")
99          sm.write("smub.source.func = smub.OUTPUT_DCVOLTS")
100         sm.write("smub.source.limitv = 0.01")
```

```
101             sm.write("smub.source.limiti = 0.001")
102             sm.write("smub.source.levelv = 0")
103             sm.write("smub.source.output = smub.OUTPUT_ON")
104 
105             time.sleep(tdelay)
106             sm.write("print(smua.measure.v())")
107             valuea=sm.read()
108             v[i,4] = valuea
109             sm.write("print(smub.measure.v())")
110             valueb=sm.read()
111             v[i,5] = valueb
112             time.sleep(20)
113             sm.write("print(smua.measure.i())")
114             valuea=sm.read()
115             v[i,6] = valuea
116             sm.write("print(smub.measure.i())")
117             valueb=sm.read()
118             v[i,7] = valueb
119 
120     # Complete the operation and save in csv
121     with open('temp.csv','w') as f:
122             writer = csv.writer(f)
123             header1 = ['Leakage SOL2 with V5typ']
124             header2 = ['Leakage SOL2 with V5max']
125             header3 = ['Leakage SOL2 with V5min']
126             header = ['Vds_HSS','Ileakage_HSS','Vds_LSS','Ileakage_LSS','VBH-Vd_FS','Vs_FS-VBL','
    Ileakage_FS','Ileakage_FS']
127             writer.writerow(header1)
128             writer.writerow(header)
129             writer.writerow(v[0,:])
130             writer.writerow(header2)
131             writer.writerow(header)
132             writer.writerow(v[1,:])
133             writer.writerow(header3)
134             writer.writerow(header)
135             writer.writerow(v[2,:])
136             print("Measure completed")
137             os.rename('temp.csv',name +'.csv')
138     mes=1
```

A.4 Switches on-resistance

Floating Switch

```
1 import SECpkg as PKG
2 import pyvisa as visa
```

```
3  import time
4  import numpy as np
5  import csv
6  import os
7  # GPIOs assignment & defaults:
8  RN=17       # J8_11 (GPIO17)
9  SSEL=18     # J8_12 (GPIO18)
10 SSTATE1=7   # J8_26 (GPIO7)
11 SSTATE0=8   # J8_24 (GPIO8)
12 CK=11       # J8_23 (GPIO11)
13 TCK=27      # J8_13 (GPIO27)
14 TDA=22      # J8_15 (GPIO22)
15 [en_pd,en_pu,tmux,tv5,tbg,tmwrite]=PKG.INIT(RN,SSEL,SSTATE1,SSTATE0,CK,TCK,TDA)
16
17 ckdelay = 0.0001       # clock delay
18 tckdelay = 0.0001      # test clock delay
19 tdelay = 1              # delay between measurements
20 mes = 0                 # enable measurements
21
22 ni = 6
23 nv = 7
24 istart = 0
25 istop = 0.05
26 vstart = 0
27 vstop = 12
28 newv = vstart
29 newi = istart
30 istep = (istop-istart)/(ni-1)
31 vstep = (vstop-vstart)/(nv-1)
32 bias = np.zeros((nv,1))
33 v = np.zeros((ni*nv,3))
34
35 PKG.RES(RN,0.05) # initial reset
36
37 rm = visa.ResourceManager('@py') # Use the pyvisa-py backend
38 address = "TCPIP0::10.49.41.51::inst0::INSTR" # Keithley DAQ6510 IP address TCP/IP string
39 sm = rm.open_resource(address)
40 sm.write("reset()") # sm initial reset
41
42 while (mes==0): # Start operation
43     print("Insert test board number:") # insert csv file name
44     tcn = input("cmd>>")
45     name = "onResS2_FS_V5typ_TB"+tcn
46
47     PKG.SEL(SSEL, 1) # Set SEL=1
```

```
48      time.sleep(tdelay)
49      tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 2, ckdelay) # STA=2
50      time.sleep(tdelay)
51
52      # Set CHB as Voltage Source
53      sm.write("smub.source.func = smub.OUTPUT_DCVOLTS")
54      sm.write("smub.source.limitv = ",str(vstop))
55      sm.write("smub.source.limiti = 0.05")
56      sm.write("smub.source.levelv = ",str(vstart))
57      sm.write("smub.source.output = smub.OUTPUT_ON")
58      time.sleep(tdelay)
59      # Set CHA as Current Source
60      sm.write("smua.source.func = smua.OUTPUT_DCAMPS")
61      sm.write("smua.source.limitv = 12")
62      sm.write("smua.source.limiti = ",str(istop))
63      sm.write("smua.source.leveli = ",str(istart))
64      sm.write("smua.source.output = smua.OUTPUT_ON")
65      time.sleep(tdelay)
66
67      for j in range(0,nv):
68          bias[j,0] = newv
69          for i in range(0,ni):
70              sm.write("print(smua.measure.i())")
71              valuea=sm.read()
72              v[(i+(ni*j)),0] = valuea
73              time.sleep(tdelay)
74              sm.write("print(smua.measure.v())")
75              valuea=sm.read()
76              v[(i+(ni*j)),1] = valuea
77              time.sleep(tdelay)
78              if i>0:
79                  v[(i+(ni*j)),2] = v[(i+(ni*j)),1]/v[(i+(ni*j)),0]
80              newi = newi + istep
81              if (newi <= istop):
82                  sm.write("smua.source.leveli = ",str(newi))
83              else:
84                  time.sleep(tdelay)
85                  newi = istart
86                  sm.write("smua.source.leveli = ",str(istart))
87              time.sleep(tdelay)
88          newv = newv + vstep
89          time.sleep(tdelay)
90          if (newv <= vstop):
91              sm.write("smub.source.levelv = ",str(newv))
92              time.sleep(tdelay)
```

```
93
94      if  i==ni-1 and j==nv-1:
95          mes=1
96          print(v)
97          with open('temp.csv','w') as  f:
98                  writer  = csv.writer(f)
99                  header1 = ['on resistance  Sol2 with 5Vtyp']
100                 header = ['I_FS','V_FS','Ron']
101                 header2 = ['BIAS:']
102                 writer.writerow(header1)
103                 for  n in  range(0,nv):
104                     writer.writerow(header2)
105                     writer.writerow(bias[n ,:])
106                     writer.writerow(header)
107                     for  m in range((ni*n),((ni*n)+ni)):
108                         writer.writerow(v[m,:])
109         print("Measure completed")
110         os.rename('temp.csv',name +'.csv')
```

High-side switch and Low-side switch

```
1  import SECpkg as PKG
2  import pyvisa as visa
3  import time
4  import numpy as np
5  import csv
6  import os
7  # GPIOs assignment & defaults:
8  RN=17       # J8_11 (GPIO17)
9  SSEL=18     # J8_12 (GPIO18)
10 SSTATE1=7   # J8_26 (GPIO7)
11 SSTATE0=8   # J8_24 (GPIO8)
12 CK=11       # J8_23 (GPIO11)
13 TCK=27      # J8_13 (GPIO27)
14 TDA=22      # J8_15 (GPIO22)
15 [en_pd,en_pu,tmux,tv5,tbg,tmwrite]=PKG.INIT(RN,SSEL,SSTATE1,SSTATE0,CK,TCK,TDA)
16
17 ckdelay = 0.0001       # clock delay
18 tckdelay = 0.0001      # test clock delay
19 tdelay = 1              # delay between measurements
20 mes = 0                 # enable measurements
21
22 points = 101 # Number of sweeping points
23 start = 0.05 # Starting value
24 stop = 0.06 # Ending value
25 step = (stop-start)/(points-1) # Step size
```

```
26 newlv = start # Sweeping variable
27 v = np.zeros((points,8)) # Matrix to store measurements
28
29 PKG.RES(RN,0.05) # initial reset
30
31 rm = visa.ResourceManager('@py') # Use the pyvisa-py backend
32 address = "TCPIP0::10.49.41.51::inst0::INSTR" # Keithley DAQ6510 IP address TCP/IP string
33 sm = rm.open_resource(address)
34 sm.write("reset()") # sm initial reset
35
36 while (mes==0): # Start operation
37     print("Insert test board number:") # insert csv file name
38     tcn = input("cmd>>")
39     name = "onResS2_HSSLSS_V5typ_TB"+tcn
40
41     PKG.SEL(SSEL, 1) # Set SEL=1
42     time.sleep(tdelay)
43     tmwrite=PKG.STA(SSTATE1, SSTATE0, CK, 1, ckdelay) # STA=1
44     time.sleep(tdelay)
45
46     # Set CHA as Current source
47     sm.write("smua.source.func = smua.OUTPUT_DCAMPS")
48     sm.write("smua.source.limitv = 12")
49     sm.write("smua.source.limiti = ",str(stop))
50     sm.write("smua.source.leveli = ",str(start))
51     sm.write("smua.source.output = smua.OUTPUT_ON")
52     # Set CHB as Current source
53     sm.write("smub.source.func = smub.OUTPUT_DCAMPS")
54     sm.write("smub.source.limitv = 12")
55     sm.write("smub.source.limiti = ",str(stop))
56     sm.write("smub.source.leveli = ",str(start))
57     sm.write("smub.source.output = smub.OUTPUT_ON")
58     time.sleep(tdelay)
59
60     # Sweep I
61     for i in range(0,points):
62         print("step",i)
63         print("current level :",newlv)
64         newlv = newlv + step
65         print("Next current level :",newlv)
66         sm.write("print(smua.measure.i())")
67         valuea=sm.read()
68         v[i,0] = valuea
69         sm.write("print(smub.measure.i())")
70         valueb=sm.read()
```

```
71          v[i,4] = valueb
72          time.sleep(tdelay)
73          sm.write("print(smua.measure.v())")
74          valuea=sm.read()
75          print("Measured value on channel A = ",valuea)
76          v[i,1] = valuea
77          v[i,2] = v[i,1]/v[i,0]
78          sm.write("print(smub.measure.v())")
79          valueb=sm.read()
80          print("Measured value on channel B = ",valueb)
81          v[i,5] = valueb
82          v[i,6] = v[i,5]/v[i,4]
83          if i>0:
84              v[i,3] = (v[i,1]-v[i-1,1])/(v[i,0]-v[i-1,0])
85              v[i,7] = (v[i,5]-v[i-1,5])/(v[i,4]-v[i-1,4])
86          time.sleep(tdelay)
87          sm.write("smua.source.leveli = ",str(newlv))
88          sm.write("smub.source.leveli = ",str(newlv))
89          time.sleep(mdelay)
90
91      if i==points-1:
92          mes=1
93          with open('temp.csv','w') as f:
94                  writer = csv.writer(f)
95                  header1 = ['on resistance Sol2 with 5Vtyp']
96                  header = ['I_HSS','V_HSS','R_HSS','Rdiff_HSS','I_LSS','V_LSS','R_LSS','
Rdiff_LSS']
97                  writer.writerow(header1)
98                  writer.writerow(header)
99                  for n in range(0,points):
100                     writer.writerow(v[n,:])
101         print("Measure completed")
102         os.rename('temp.csv',name +'.csv')
```

A.5 Supply-Embedded Communication Package Extended for TC2

```
1  import RPi.GPIO as GPIO
2  import time
3
4  GPIO.setmode(GPIO.BCM)
5  GPIO.setwarnings(False)
6
7  def INIT(RN, SSEL, SSELF, SSTATE1, SSTATE0, CK, TCK, TDA, EN_TEST):
8      GPIO.setup(RN, GPIO.OUT)
9      GPIO.output(RN, GPIO.LOW)
```

```
10      GPIO.setup(SSEL, GPIO.OUT)
11      GPIO.output(SSEL, GPIO.LOW)
12      GPIO.setup(SSELF, GPIO.OUT)
13      GPIO.output(SSELF, GPIO.LOW)
14      GPIO.setup(SSTATE1, GPIO.OUT)
15      GPIO.output(SSTATE1, GPIO.LOW)
16      GPIO.setup(SSTATE0, GPIO.OUT)
17      GPIO.output(SSTATE0, GPIO.LOW)
18      GPIO.setup(CK, GPIO.OUT)
19      GPIO.output(CK, GPIO.LOW)
20      GPIO.setup(TCK, GPIO.OUT)
21      GPIO.output(TCK, GPIO.LOW)
22      GPIO.setup(TDA, GPIO.OUT)
23      GPIO.output(TDA, GPIO.LOW)
24      GPIO.setup(EN_TEST, GPIO.OUT)
25      GPIO.output(EN_TEST, GPIO.LOW)
26
27      # TM reg defaults:
28      en_rx = 0
29      en_dout = 0
30      en_od = 0
31      rxmode = 6
32      hystl1_h = 0
33      hystl1_l = 0
34      hystl2_h = 0
35      hystl2_l = 0
36      rxdiv_h = 0
37      rxdiv_l = 0
38      en_pd = 0
39      en_pu = 1
40      tmux = 0
41      tv5 = 7
42      tbg = 0
43      tmwrite = 0
44      en_tx = 1
45      return[en_rx, en_dout, en_od, rxmode, hystl1_h, hystl1_l, hystl2_h, hystl2_l, rxdiv_h, rxdiv_l,
    en_pd, en_pu, tmux, tv5, tbg, tmwrite, en_tx]
46
47  def RES(RN, ckdelay):
48      print("# issue reset  ... ")
49      GPIO.output(RN, GPIO.LOW)
50      time.sleep(ckdelay)
51      GPIO.output(RN, GPIO.HIGH)
52      en_rx = 0
53      en_dout = 0
```

```
54      en_od = 0
55      rxmode = 6
56      hystl1_h = 0
57      hystl1_l = 0
58      hystl2_h = 0
59      hystl2_l = 0
60      rxdiv_h = 0
61      rxdiv_l = 0
62      tmux = 0
63      tbg = 0
64      tv5 = 7
65      en_pu = 1
66      en_pd = 0
67      tmwrite = 0
68      en_tx = 1
69
70  def SEL(SSEL, SSELF, solution):
71      print('# set SSEL to ',solution)
72      if  solution  == 0:
73          GPIO.output(SSEL, GPIO.LOW)
74          GPIO.output(SSELF, GPIO.LOW)
75      else:
76          GPIO.output(SSEL, GPIO.HIGH)
77          GPIO.output(SSELF, GPIO.HIGH)
78
79  def STA(SSTATE1, SSTATE0, CK, state, ckdelay):
80      print('# set SSTATE to ',state)
81      GPIO.output(CK, GPIO.LOW)
82      if  state  == 3:
83          GPIO.output(SSTATE1, GPIO.HIGH)
84          GPIO.output(SSTATE0, GPIO.HIGH)
85          tmwrite = 1 # allows writing tmreg
86      elif  state  == 2:
87          GPIO.output(SSTATE1, GPIO.HIGH)
88          GPIO.output(SSTATE0, GPIO.LOW)
89          tmwrite = 0 # disables writing tmreg
90      elif  state  == 1:
91          GPIO.output(SSTATE1, GPIO.LOW)
92          GPIO.output(SSTATE0, GPIO.HIGH)
93          tmwrite = 0 # disables writing tmreg
94      else:
95          GPIO.output(SSTATE1, GPIO.LOW)
96          GPIO.output(SSTATE0, GPIO.LOW)
97          tmwrite = 0 # disables writing tmreg
98      # CK Pulse
```

```
99      time.sleep(ckdelay)
100     GPIO.output(CK, GPIO.HIGH)
101     time.sleep(ckdelay)
102     GPIO.output(CK, GPIO.LOW)
103     return(tmwrite)
104
105 def TM(TCK, TDA, en_rx, en_dout, en_od, rxmode, hystl1_h, hystl1_l, hystl2_h, hystl2_l, rxdiv_h,
     rxdiv_l, en_pd, en_pu, tmux, tv5, tbg, tmwrite, tckdelay):
106     if tmwrite == 1:
107         tmreg = bin(en_rx*2**55 + en_dout*2**54 + en_od*2**53 + rxmode*2**48 + hystl1_h
    *2**44 + hystl1_l*2**40 + hystl2_h*2**36 + hystl2_l*2**32 + rxdiv_h*2**20 + rxdiv_l*2**16 +
    en_pd*2**13 + en_pu*2**12 + tmux*2**8 + tv5*2**4 +tbg)[2:].zfill(64)
108         GPIO.output(TCK, GPIO.LOW)
109         GPIO.output(TDA, GPIO.LOW)
110         time.sleep(tckdelay)
111         print("# send TMREG ",tmreg)
112         for i in range (0,64):
113             if tmreg[63-i] == '1':
114                 GPIO.output(TDA, GPIO.HIGH)
115             else:
116                 GPIO.output(TDA, GPIO.LOW)
117             time.sleep(tckdelay)
118             GPIO.output(TCK, GPIO.HIGH)
119             time.sleep(tckdelay)
120             GPIO.output(TCK, GPIO.LOW)
121         GPIO.output(TDA, GPIO.LOW)
122         time.sleep(tckdelay)
123     else:
124         print("# Cannot write TM, PLEASE set SSTATE to 3 before !!!")
125
126 def ENT(EN_TEST, en_tx):
127     if en_tx == 0:
128         GPIO.output(EN_TEST, GPIO.HIGH)
129     else:
130         GPIO.output(EN_TEST, GPIO.LOW)
```

Publications

Paper

[1] F. D'Aniello, A. Ott, and A. Baschirotto. 'Supply Line Embedded Communication in Automotive Sensor / Actuator Networks'. In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)* (2021), pp. 7–11.

[2] F. D'Aniello, A. Ott, and A. Baschirotto. '2-Mbps Power-Line Communication Transmitter Based on Switched Capacitors for Automotive Networks'. In: *Electronics* 11.22 (2022), p. 3651.

[3] F. D'Aniello, A. Ott, and A. Baschirotto. 'StrongArm-Latch-Based Receiver for Supply Line Embedded Communication'. In: *PRIME 2022 - 17th International Conference on Ph.D Research in Microelectronics and Electronics, Proceedings* (2022), pp. 321–324.

[4] A. Ott, F. D'Aniello, and A. Baschirotto. 'A Switched Capacitor Approach for Power Line Communication in Differential Networks'. In: *PRIME 2022 - 17th International Conference on Ph.D Research in Microelectronics and Electronics, Proceedings* 1 (2022), pp. 317–320.

Patents

[1] A. Ott, F. D'Aniello, A. Baschirotto, and T. Freitag. 'Transmitter For Power Line Communication'. EP3982513B1. 2022.

[2] A. Ott, F. D'Aniello, A. Baschirotto, and T. Freitag. 'Transmitter For Power Line Communication'. CN114401028A. 2022.

[3] A. Ott, F. D'Aniello, A. Baschirotto, and T. Freitag. 'Transmitter For Power Line Communication'. US 11,522,677 B2. 2023.

Acknowledgments

I would like to express my deep gratitude to Prof. Andrea Baschirotto for giving me the opportunity to join the Ph.D. in his group and for guiding me during these years. I also would like to thank all the people of the Microelectronic Group for the unforgettable time spent together in Milan and during conferences.

A special thanks to my mentor and friend Andreas Ott who was always available to help me when I needed it and made it possible to achieve the results of this thesis.

I also would like to acknowledge Melexis and all its people who supported this activity, especially Dirk Nuernbergk for his contribution and his patience.

Major thanks to my best friends, Valerio whom I can always count on for advice, and Stefano, Matteo, Fabrizio, and Raffaele for always being by my side despite the distance.

Finally, thanks to the most important people in my life, my family for always believing and constantly encouraging me, and Marcella for being the love of my life.