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Large increase of the thermoelectric power factor in multi-barrier nanodevices

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ABSTRACT

Improving the power factor (PF) of thermoelectric materials, crucial for enhancing the power output of thermoelectric generators, is challenging due to the adverse interdependence of the Seebeck coefficient and the electrical conductivity on carrier density. We introduce a novel strategy employing energy filtering via built-in potential barriers to alleviate this dependency, significantly enhancing the PF. Utilizing electron-beam lithography, we developed a Si-based nanodevice featuring a multiple well/barrier design. Measurements yielded a PF of 11 mW m^{-1} K^{-2}, more than doubling the optimal PF achievable in bulk silicon. Experimental findings align well with theoretical models, affirming the efficacy of the approach. Leveraging established silicon technologies in device fabrication unveils pathways for on-chip micro-energy harvesters and localized Peltier coolers. Moreover, the results validate a material-agnostic energy filtering model, guiding the creation of PF-enhanced devices across various thermoelectric materials.

Thermoelectric Devices (TEDs) have great potential for both direct heat scavenging and heat pumping (thermoelectric cooling). The efficiency of TEDs is quantified by the dimensionless Figure of Merit of the constituent thermoelectric (TE) material $ZT = \frac{S^2\sigma}{\kappa}T$ [1,2], where S is the Seebeck coefficient, σ the electrical conductivity, κ the thermal conductivity and T is the absolute temperature. A good thermoelectric material should have a low κ and a high power factor PF= $S^2\sigma$. Over the last two decades, the introduction of nanotechnology and advancements in the control of defects, nanoinclusions, nanoscale features and interfaces in TE materials, allowed for reductions in thermal conductivity by enhancing phonon scattering with minimal effect on the PF, leading ZT to values beyond 2 [3]. The power factor, however, proved more difficult to increase. The reason is the well-known adverse interdependence of S and σ on carrier density. Several concepts, however, have emerged over the last years, leading to enhanced PFs in specific materials. These include energy filtering of cold electrons using potential energy barriers [4], resonant levels [5], high defect levels in semi-metallic materials [6,7], and highly asymmetric energy transport in low bandgap materials and even metals [8]. However, in contrast to phonon transport engineering which is more widely applicable to TE materials, some of these PF methods are only applicable to specific classes of materials. Beyond high ZT and PF, a wider use of thermoelectricity calls for largely available, low-cost, technologically mature, and

stable TE materials. Single-crystalline silicon is an excellent candidate as of its PF, which could reach values of around 4–5 mW m^{-1} K^{-2} at room temperature [9], competing with the best TE materials. Bulk Si, however, has a very large κ = 148 W m^{-1}K^{-1} that reduces its ZT to a meager 0.01 at room temperature. Several research groups [10–15] demonstrated drastic reduction of κ in many nanostructures due to undergoing strong phonon scattering. Values smaller than 2 W m^{-1}K^{-1} were measured in rough silicon nanowires [16–19], while a reduced thermal conductivity down to the amorphous limit has also been measured in holey silicon membranes [20–22].

Along with a reduced κ, the PF in silicon can be further increased by implementing energy filtering. Prior theoretical studies showed that energy filtering produced by an energy multi-barrier structure under ultra-high doping conditions and clean-from-dopant barriers is a very effective approach in enhancing the PF, which can ultimately lead to over an order of magnitude improvements [23,24]. Experimentally, a PF enhancement has been observed controlling nanowire interfaces [25]. A significant increase of the PF has been also observed in thin films of highly boron doped *p*-type nano-crystalline Si, subjected to a thermal treatment in a non-oxidizing atmosphere (annealing) [26–30]. This increase was attributed to the precipitation at grain boundaries of dopants exceeding the solubility threshold [27,

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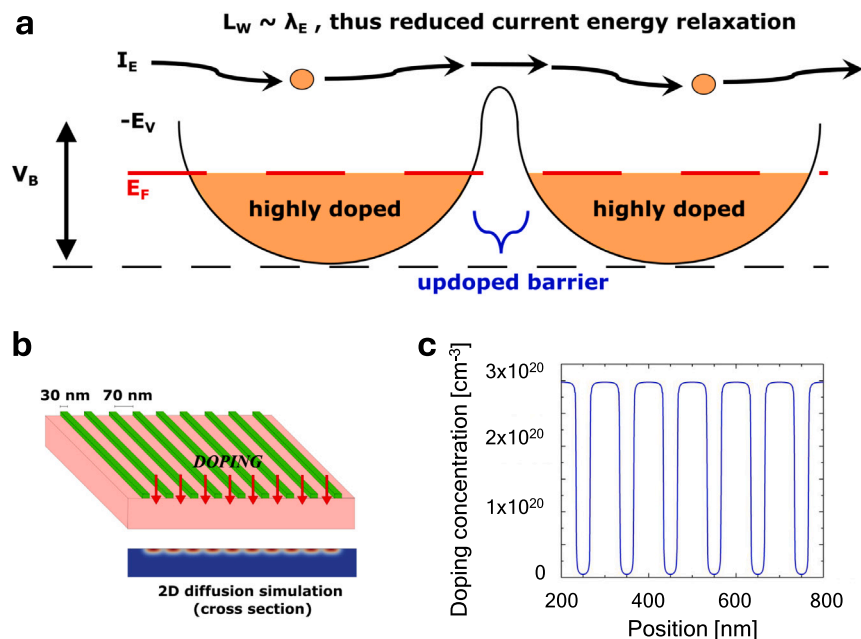
Fig. 1. Panel (a): The energy filtering concept envisioned. A potential well/barrier structure is formed under alternation of high doping and undoped (or lightly doped) regions. The Fermi level, E_F, resides into the bands, providing high conductivity wells. The barriers provide energy filtering and high Seebeck coefficients, S. The size of the wells must be of the order of the carriers energy relaxation length. The undoped barrier regions allow for high carrier mobility, thus mitigating the reduction in conductivity that they cause. Panel (b): sketch of the selective doping process of silicon implemented in this work, to induce the potential well/barrier structure required for an effective energy filtering. Nanometric oxide strip, precisely defined by e-beam lithography and etching, are used to mask the boron diffusion in silicon, in order to fabricate a planar selective p^+/p doping that generates a multi-barrier structure by electrostatic modulation of the valence and the conduction band (each barrier/well is similar to that of Panel a). Panel (c) shows a simulated doping profile along the propagation direction. The profile is taken at a depth of 5 nm. See the "supplementary information" for the detail of the simulation.

29,31], generating energy barriers at the grain boundaries that filter out 'cold' carriers, leading to an increase in S. At the same time, mobile (non-filtered) holes with higher kinetic energy (and thus larger mobility) compensate for the reduced carrier density, allowing for high σ. Experimentally, PFs up to 35 mW m^{-1}K^{-2} could be reached in nanocrystalline p-type thin Si films [27], a factor of around 7× compared to the optimal bulk material. Many other reports over the years have discussed the beneficial effect of energy filtering on the power factor [32–37], however, in most other experimental cases the improvements were modest, as despite increases in the Seebeck coefficient the conductivity was strongly reduced as well. In this work, we have implemented energy filtering under controlled conditions, following suggestions from our prior theoretical work, which specifies the recipe to be followed for optimal energy filtering. This includes the sizes of the wells and barriers and the doping level [23,24]. We have designed, fabricated and characterized an on-chip p–type silicon device with an induced modulation band profile achieved by selective doping, aiming at implementing the energy filtering concept as described in Ref. [23]. A planar energy multi-barrier structure made of a large number of alternated heavily-doped/low-doped regions was fabricated, such that the conduction/valence band modulation resulted in narrow barriers (of 20–30 nm) in the low-doped regions, and larger wells (70 nm) in the heavily-doped regions. Thus, we experimentally confirm the theoretical predictions about the benefits of the multi-barrier energy filtering on a well-controlled and precisely designed structure, with a 2× increase in the PF compared to optimized bulk Si.

1. Device design, fabrication and characterization

The device consists of a series of built-in potential barriers, which prevent the low-energy ('cold') carriers from flowing, while allowing the high-energy ('hot') carriers to propagate. This results in an increased Seebeck coefficient S, because only carriers with energies above the barrier heights and well above the Fermi level can propagate (Fig. 1(a)). In addition, these high energy carriers have high mobility

which benefits the electrical conductivity (especially in the vicinity of the undoped/lightly-doped device regions) [23]. The implementation exploits standard silicon technology steps, combined with high resolution lithography, to achieve a planar selective p^+/p alternating doping which generates the multi-barrier structure by electrostatic modulation of the conduction and valence bands in the direction of the carrier propagation. The alternated doping has been fabricated in a top silicon layer of a Silicon-On-Insulator (SOI) wafer, 260 nm thick, with a very low initial doping concentration (resistivity 10 Ωcm). In our case-study, boron (p-type) has been used, but alternatively, n^+/n could have been used for electron conduction in a symmetric fashion. Oxide nanostrips, 30 nm wide and with a pitch of 100 nm (i.e. 1D grating, with potential well width of 70 nm), have been fabricated and have been used as a mask for the boron thermal diffusion (see the schematic of the oxide mask shown in Fig. 1(b)). Although diffusion is an isotropic process, under-the-mask diffusion marginally impacts Si doping within a depth of the order of boron diffusion length ($\approx$ 220 nm) due to the large solubility of boron into the oxide [38], which acts as a boron getter. Therefore, the doping concentration shows a strong variation in the lateral direction (see the diffusion simulation shown in Fig. 1(b) and the simulated doping profile in Fig. 1(c)). Additional details about the diffusion model are reported in the Supplemental Information. The design of the device is completed by an integrated heater, to provide a temperature gradient, and by two temperature sensors. Two voltage contacts, at the ends of the multi-barrier structure, are used for the measurement of both the two-contact electrical conductivity (whit the heater off) and of the Seebeck voltage. SEM images of a typical device are shown in Fig. 2(a,b,c). Details of the fabrication and of the measurement procedure are reported in the "Methods" section.

The electrical contacts and the two temperature sensors at the ends of the multi-barrier structures are exactly aligned (see the SEM images and the scheme of Fig. 2(d)), in such a way that the temperature difference is measured at the same distance of the voltage drop (Seebeck voltage). This is a specific requirement for the precise measurement of the Seebeck voltage. However, this design allows only a two-contact
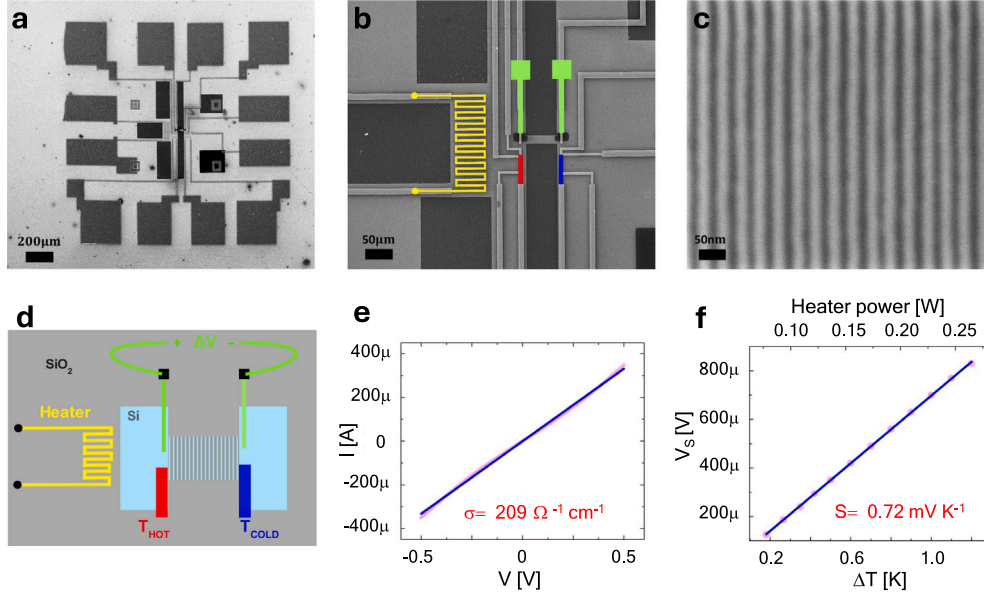
Fig. 2. Panel (a), (b) and (c): composition of SEM images of a typical fabricated device. Panel (b) shows the metal heater (yellow), the two termoresistors (in red that for T_H, in blue that for T_C), and the two contacts for the measurement of the Seebeck voltage drop (green). Panel (c) is an enlargement of the oxide nanostrips forming the grating area (active part of the device). Panel (d) shows a sketch of the device. Panel (e) and (f) are electrical measurements of the device, respectively an IV characteristic with the heater off (e) and the Seebeck voltage as a function of temperature drop (f) for different values of heating power.

configuration for the measurement of the electrical resistance, which will be therefore affected by the contact resistances.

Measurements of conductivity and Seebeck coefficient were repeated on several devices, fabricated in different fabrication runs, with the same process parameters. Current–voltage characteristics are linear and let measure the resistance of the 1D grid (Fig. 2(e)), and hence of the electrical conductivity that accounted to (209 ± 33) Ω^{-1} cm^{-1}. This is a high value (even if underestimated because measured with a two contact configuration) due to the increasing of the doping concentration by diffusion. To be noted that, based on diffusion simulation shown in Fig. 1(b), the doping concentration is increased to ultra-high values in a layer of thickness roughly 1/5 of the total top silicon layer, where the wells/barriers form. The well/barrier structure is lost deeper into the channel depth, where lateral diffusion leads to uniform doping of reduced level. This region would still be conducting at some degree, but the thermoelectric performance in the top well/barrier layer dominates and dictates the larger than bulk PF increase we measure. The Seebeck coefficient is achieved by fitting the Seebeck voltage measured as a function of the temperature drop (Fig. 2(f)): it resulted to $S = 0.72 \pm 0.02$ mV/K. The power factor is then computed to be 11 ± 2 mW m^{-1} K^{-2}. Compared to the power factor of uniformly doped p-type bulk silicon at optimal doping concentrations (≈ 4–5 mW/(m K^2)) [9], the PF of the multi-barrier device is more than doubled. Note that this is a prudential value, due to the underestimation of the electrical conductivity.

2. Energy filtering model: Comparison to experiment

In what follows, we will show that the experimental results validate the energy filtering model of the charge carrier transport, based on the Boltzmann transport theory. We first computed the mobility of bulk p-type Si versus doping density using the band structure of the Si valence band for calibration purposes [23] (see also the section Methods and SI). For the calculation of the Seebeck coefficient S_{total} we consider the contribution of both the diffusive S_d and the phonon drag S_{pd} components, which is significant in Si even at room temperature due to the long acoustic phonon Mean Free Paths (MFPs) [39,40]. These two components are affected differently by the p^+/p well/barrier structure: S_d senses the potential barriers, whereas S_{pd} depends on the variation

of the doping density between wells and barriers (see the methods section for the details of the calculation).

For the multi-barrier structure, at first we estimate the shape of the band along the transport direction which will determine the potential of the well and height of the barrier. We solved the 1D Poisson equation considering abrupt p^+/p variations in the doping profile. Fig. 3(a) shows a simulated band profile achieved with 70 nm wide heavily doped regions at $p^+ = 2 \times 10^{20}$ cm^{-3}, and 30 nm wide undoped regions. These numbers are based on geometrical features of the oxide mask (see Fig. 1(b)) and on the boron diffusion profile, assuming undoped regions underneath the oxide. Note that although the carriers are holes, we use positive increasing energies for convenience (the actual valence band profile would be reverted). The two important parameters that determine the level of energy filtering are: (1) the Fermi level position with respect to the bottom of the well potential, E_F ($E_F - E_{V \text{ (well)}}$), which turns out to be 0.14 eV as shown in Fig. 3(a); and (2) the energy barrier height V_B, again from the bottom of the well potential, which is turns out to be 0.25 eV in the p^+/p junction we considered, making the effective barrier height that the carriers around the Fermi level experience to be 0.11 eV. The overall electrical conductivity and Seebeck coefficient are both computed as a series combination of their values in the different regions of the channel. To mimic the experimental structure, where the doping is not abruptly changing between the barrier and well, we also consider an intermediate region. Correspondingly we approximate the barrier profile of Fig. 3(a) with a linear piecewise function (see Fig. 3(b)): the well (W, $L_W = 70$ nm), the barrier (B, $L_B = 10$ nm) and an intermediate transition region (I, $L_I = 20$ nm) where the potential changes gradually from the well to the barrier levels.

Figs. 3(c–e) show the computed thermoelectric parameters: electrical conductivity σ, Seebeck coefficient S, and power factor $S^2\sigma$, respectively. The black lines show the values for p-type bulk Si (no barriers), as a function of the Fermi level E_F, i.e. translated one-to-one as a function of the uniform doping concentration. As expected, the bulk power factor peaks at around PF$_{\text{bulk}} = 5$ mW m^{-1} k^{-2} for $E_f = 0.11$ eV, that corresponds to an uniform doping concentration $p^+ = 10^{20}$ cm^{-3}, in agreement with the available experimental data [9]. For the multi-barrier structure, we simulated slightly different cases to account for uncertainties in the geometry, doping levels, doping profile,
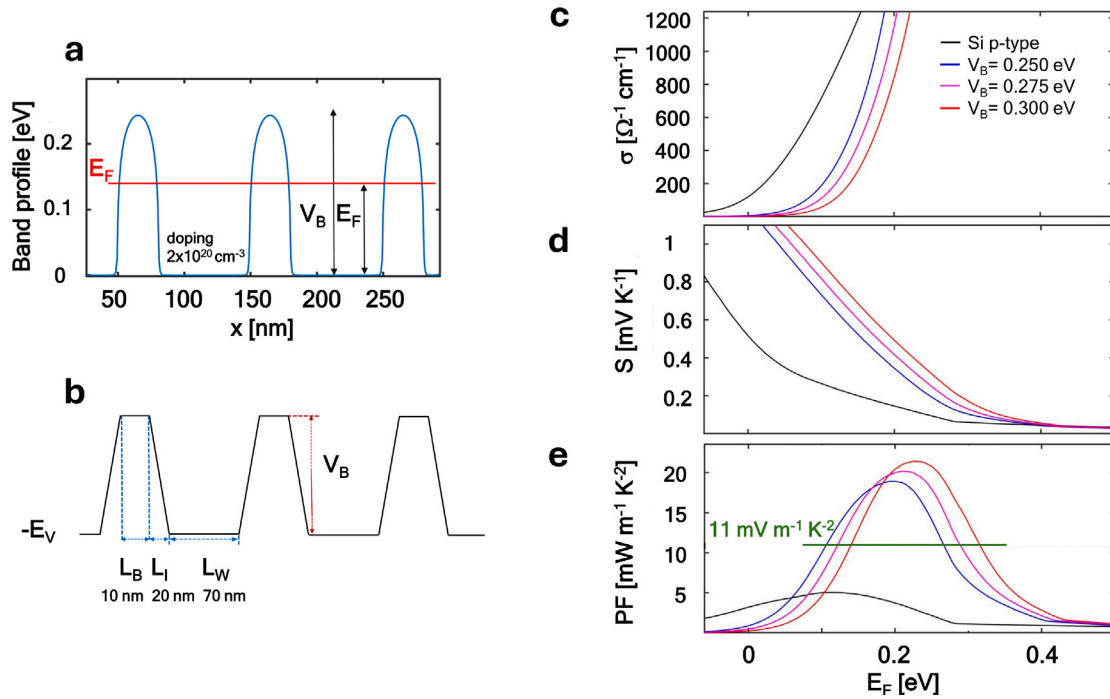
Fig. 3. Panel (a) shows the Poisson equation solution of the band profile in the well/barrier structure of size 70 nm/30 nm and p^+p 2×10^{20} cm^{-3} well doping density. The simplified band profile schematic (linear piecewise) used in the transport model is shown in Panel (b). Panels (c), (d) and (e) show the simulated TE coefficients: (c) electrical conductivity, (d) Seebeck coefficient, and (e) power factor versus the Fermi level position, E_F. The black lines show the single crystal p-type Si (bulk Si) calculated result. The blue, magenta and red lines show the well/barrier structure using $V_B = 0.25$, 0.275, and 0.3 eV.

and uncertainties that arise from the 1D model treatment versus the measurements on a structure with a 2D doping distribution. The three colored curves of Fig. 3 (c–e) show the thermoelectric parameters for three different values of the barrier height V_B (0.25, 0.275 and 0.3 eV), as a function of E_F. With the potential barriers, the transport is shifted at higher energies, resulting in a large increase of the Seebeck coefficient.

The electrical conductivity is instead reduced with respect to pristine bulk. However, even if not finally reaching the bulk value, the electrical conductivity rapidly increases for higher values of E_F (higher doping values). Retaining high electrical conductivities at high Seebeck coefficients is the key point that allows achieving high power factors. The electrical conductivity is rapidly recovering with E_F increasing because: (i) the mobile carriers in this material are primarily hot carriers of high mobility, as they travel at elevated energies above V_B at which ionized impurity scattering is weak, and (ii) they encounter a significant volume in the material with zero or reduced doping density (barrier and intermediate regions) where they experience the higher phonon-limited mobility. The blue line in the simulations refers to the nominal $V_B = 0.25$ eV, achieved with the band profile of Fig. 3(a). In this case, at the position of $E_F = 0.14$ eV, the Seebeck coefficient is smaller that the measured value, while the electrical conductivity is higher. The purple lines refers to $V_B = 0.275$ eV, and move one step closer to the experimental values at the set Fermi level. Finally, the red lines are simulations for $V_B = 0.3$ eV, and achieve the experimental values of $S = 0.72$ mV/K and $\sigma = 209$ Ω^{-1}cm^{-1} at the required (by the doping density through Poisson) $E_f = 0.14$ eV, resulting in PF of $PF = 11$ mW/mK^2.

The values V_B=0.25-0.275–0.3 eV have been considered to cover uncertainties in the model. Although the model predicts that the PF will increase monotonically with V_B and E_F, placed in its vicinity, in practice: (i) it is unrealistic to achieve doping concentration above 10^{20} cm^{-3}, to further raise E_F; (ii) the PF peak region happens in a narrow concentration interval, very difficult to control in particular for high doping concentrations, and (iii) additional quantum mechanical effects between the large energy discontinuities of the well/barrier interface

could introduce larger resistances and degrade performance. Despite the simple 1D Poisson/ 1D series resistance model and the overall uncertainties, we are able at first order to explain why and how the power factor can increase substantially in such multi-barrier devices with reasonable consistency between the approximated underlying potential profile and Fermi level. As described in the previous section, the experimental conductivity contains contact effects, thus the internal transport properties of the device and the PF would be even higher. In fact, our model predicts that the performance potential of this multi-barrier design can be even much higher, allowing for PF values beyond $PF = 20$ mW/mK^2, 5-times the value of the pristine material, achieved at slightly different Fermi level positions from what we believe our fabricated structure has.

3. Conclusions

In this work we designed and developed a fabrication process for an on-chip p−type Si-based thermoelectric device that exploits the concept of energy filtering for an enhanced PF. At first, our technique can be implemented in on-chip silicon devices for scavenging, microharvesting and localized cooling. Much more than that, using a well defined and not random structure, our work validates the concept of energy filtering as a universal tool to enhance the thermoelectric power factor of a material in a controllable way. Using silicon, we obtained an improvement of the PF by more than 2× compared to the optimal bulk value. We factually report a power factor of 11 mW m^{-1}K^{-2} at room temperature. This is a prudential value, because the resistance of the multi-barrier structure is measured in two-contact configuration, hence it is engraved by the contact resistance, while the actual internal performance of our structure would be even higher. Additionally, our calculation suggests that the power factor can be higher depending on further Fermi Energy and barrier height adjustments, with values in excess of 20 mW m^{-1}K^{-2} predicted. Future work would be focused on the optimization of the potential profile, the underlying doping and the position of the Fermi level, leading to even larger
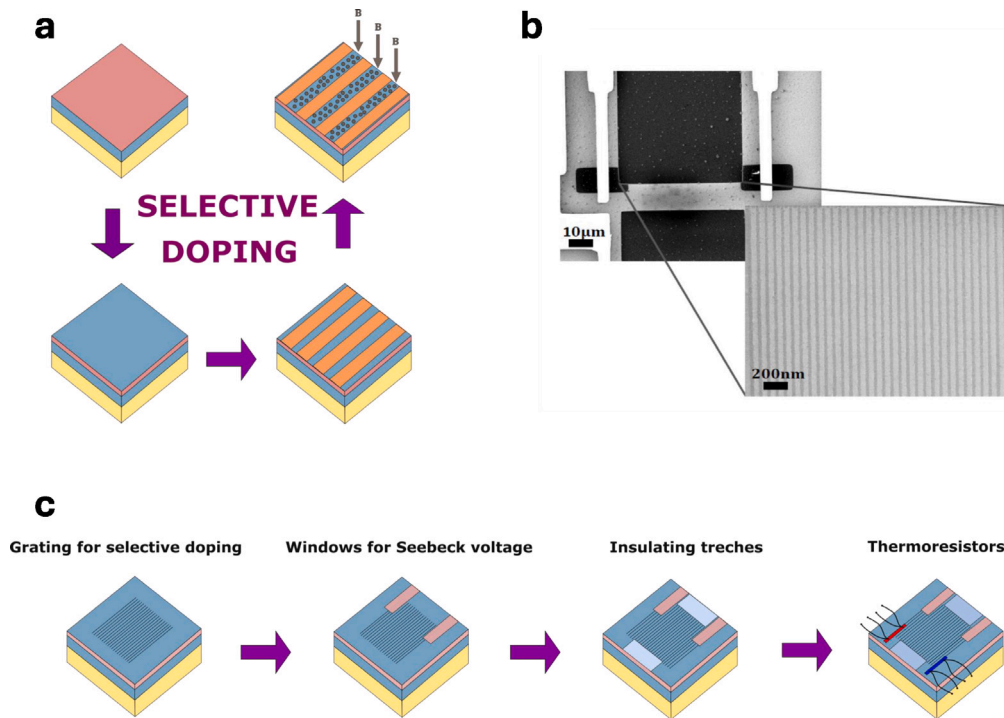
Fig. 4. Sketches of the fabrication process, and SEM photos of a fabricated device. The grating is achieved by e-beam lithography and BHF etching in the top oxide layer (Panel (a)). This grating (oxide strips) is used for selective Boron diffusion in silicon. Panel (b) shows SEM images of the active part, including the contacts through oxide windows at the ends of the multi-barrier structures. The inset shows an enlargement of the oxide nanostrips used for the selective doping. The device is completed of metal heater, temperature sensors and contacts for voltage measurement, achieved by standard IC processing (Panel (c)).

power factors, as predicted by the theoretical results. We note that the devices developed for this experiment are suitable to measure the power factor. Instead, different designs and fabrication methodologies would be needed for the measurement of the thermal conductivity. Since values of κ smaller than 2 W m^{-1}K^{-1} have been achieved in rough silicon nanowires [18,19,41] with engineered (reduced) phonon conduction, in 1D multi-barrier systems one might expect figures of merit exceeding $ZT = 1.5$ at room temperature. The fabrication process we used is based on advanced lithography and selective doping, which are standard methods in silicon technology. Thus, our results could pave the way to industrial fabrication of on-chip thermoelectric devices with remarkably improved figures of merit. In this regard, this multi-barrier technique calls for further improvement and optimization, e.g. by combining it with 1D or 2D nanostructuring for the reduction of the thermal conductivity. We finally remark that, beyond the device performance, our study validates the specific energy filtering design we implement as an effective, material-agnostic strategy for enhancing the PF of any thermoelectric material subject to the ability to create alternate potential barriers. As for example, the same concepts can be applied to randomly distributed particles, including multiple domains, each with its own attribute, and considering the statistic distribution of parameters. Thus, this approach offers a portable solution to boost thermoelectric efficiency, extending its potential for applications in heat scavenging and localized cooling.

4. Methods

Device fabrication. Fig. 4 shows sketches of the fabrication process, and SEM images of a typical device. The device is fabricated on a Silicon-On-Insulator (SOI) wafer with a top silicon layer (device layer) 260 nm thick, buried oxide layer 2 μm thick and silicon handler layer 500 μm thick. The fabrication process of the device follows a top-down approach, and it is based on Electron Beam Lithography (EBL) which allows for high resolution and fast prototyping. Processes based on the same principles can be developed in an industrial environment

exploiting advanced (deep-UV) lithography. Five lithographic steps are required for the fabrication of the device. Standard PMMA resist (molecular weight 996 k (kmw)) is used for all the lithographic steps, 1.5% in anisole for the grating (high resolution), 6% in anisole for the other steps. At first, a thermal oxide layer 25 nm thick is grown on the top silicon layer. The **first** lithographic step is used for the definition of markers. The **second**, high resolution, lithographic step (see Fig. 4(a)) is used to define the multi-barrier structure in the resist layer (PMMA 996 kmw, 1.5% in anisole), then transferred to the top SiO$_2$ layer by a calibrated BHF etching. After resist stripping, the grating into the oxide layer (see the SEM image of Fig. 2(b)) is used as a mask for Boron predeposition (900 °C, 10 min) using a solid source in a tubular furnace. A drive-in step has then been performed in a Rapid Thermal Annealer at 1150 °C, 5 min in oxidizing atmosphere to prevent dopant out-diffusion. The **third** lithographic step (not shown in the sketches of Fig. 4) allows for the removal of the silicon top layer around the multibarrier structures, as shown in the main SEM image of Fig. 4(b); Si has a very high thermal conductivity, hence its removal all around the mutibarrier region increases the precision of temperature measurements. The **fourth** lithographic step is used for opening windows through the top SiO$_2$ oxide layer at the ends of the multi-barrier structure. These through-the-oxide windows allow for the measurement of the Seebeck voltage and of the electrical conductivity. The **fifth** lithographic step is used to define metal tracks (thickness 80 nm of Gold on 15 nm of Chrome to enhance adhesion), by metal thermal evaporation and lift-off. In this step we define the metal heater, the two temperature sensors (resistors with a four-contact configuration) and the contacts for Seebeck voltage and electrical conductivity measurement.

Characterization The heater and the two metal thermoresistors were used to determine the Seebeck coefficient. To be noted that the two thermoresistors are placed exactly at the extremities of the grating, in correspondence with the Seebeck contacts (same distance from the heater). Hence, the difference of temperature upon heating, evaluated
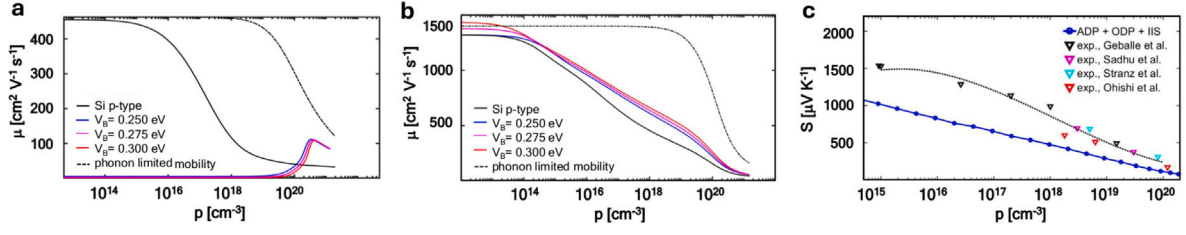
Fig. 5. Panel (a): (black-solid) the mobility of the uniformly doped *p*-type silicon versus doping concentration. The black-dotted line shows the phonon limited mobility. The colored lines show the mobility of well/barrier structures, for three values of the barrier height (0.25, 0.275 and 0.3 eV). Panel (b): the mobility of carriers with energies higher than the barrier height V_B is reported as a function of the doping concentration. Panel (c): the Seebeck coefficient versus density for uniformly doped $p-type$ Si from literature experiments (data points and dashed-black line), compared to the calculated diffusive part of the Seebeck coefficient (blue line). The difference gives the phonon drag contribution S_{pd} as a function of the doping concentration. The experimental data in (c) are taken from the works of Geballe and co.[42], Sadhu and co.[43], Stranz and co.[44], Oishi and co.[45].

by the variation of their resistances (measured in a four-contact configuration), is proportional to the temperature drop between the electrical contacts, and can be then used to obtain the Seebeck coefficient. The Temperature Coefficient of Resistance (TCR) α was determined using external macroscopic heaters. Its value $\alpha = 0.0022$ K^{-1} is comparable to that largely reported in the literature. The variation of resistance of the two thermoresistor, i.e. the temperatures at the ends of the multibarrier, has been recorded together with the Seebeck voltage for several values of the heating power. The Seebeck coefficient is achieved by a linear fit of the Seebeck voltage as a function of the temperature drop, as shown in Fig. 2(f). The resistance of the multibarrier structure is achieved by a linear fit of the IV characteristic recorded between the same contacts used for Seebeck measurement, with the heater off. The conductivity is then evaluated taking into account the measured resistance and the geometrical factors measured by SEM imaging.

Electrical transport model. First, the mobility of bulk *p*-type Si versus dopant density was computed using the band structure of Si valence band, including the heavy hole, light hole and split off bands [23]. Using the appropriate phonon mean-free paths (MFPs) to match the *p*-type Si low-field low-density mobility (450 cm^{2}V^{-1}s^{-1}) and a slightly modified version of the Brooks Herring model, we matched the entire curve of mobility versus density from low to high doping and carrier densities. This serves as calibration of the model to the pristine material. Fig. 5(a) shows the phonon limited mobility (black-dot line) and the total phonon plus Ionized Impurity Scattering (IIS) mobility (black-solid line). Full model details and theory are presented in Ref. [23].

The electrical conductivity of the composite multi-barrier structures is computed as a series resistance combination of the three different regions well (W), barrier (B) and transition region (I) shown in Fig. 3(b). As demonstrated in a previous work based on fully quantum mechanical simulations [46], any quantum tunneling effects degrade the power factor only for semi-transparent ultra-narrow barriers of just a few nanometers. The effect of tunneling can be neglected for the thicker barriers of the present work, thus only the over-the-barrier transport is considered. For the transition region we consider for simplicity only the mid-level potential between the well and the barrier. This provides very similar results as taking more refined variations. The overall electrical conductivity σ_{total} is given by:

$$L_{total}\sigma_{total}^{-1} = L_W\sigma_W^{-1} + L_I\sigma_I^{-1} + L_B\sigma_B^{-1} \qquad (1)$$

where the resistivity of each region is scaled by the length of the region. We assume that the carriers are thermionically emitted over the barriers, suffering only little energy relaxation (of ≈ 20 %) when they propagate into the well. This is justified since the energy relaxation MFP in Si is of the order of tens of nanometers, similar to the well lengths [47]. Thus, carriers above the barrier height V_B are the ones mostly contributing to transport, and the ones below V_B are assumed to be mostly frozen in the potential wells. After computing the conductivity of the device, it is illustrative to extract the mobility in the device for the three cases presented in the main text above

(colored lines in Fig. 5(a)). As expected, the mobility is very small for low densities, since most carriers are frozen in the wells and only a small minority is contributing to conductivity. Instead, it sharply increases, even approaching the phonon-limited mobility value (dashed line), when E_F reaches a threshold at which enough carriers make it over the barrier height, and those high energy carriers have velocities large enough for the strength of IIS to be reduced. This allows for a significant conductivity in the device, despite the presence of large potential barriers. Indeed, the mobility of the isolated hot carriers (mobile holes), with energy above V_B is very high, as shown in Fig. 5(b), much higher than the mobility of carriers in pristine bulk.

Seebeck coefficient model. We consider both the diffusive S_d and phonon drag S_{pd} contributions to the Seebeck coefficient. The latter can be as large as S_d depending on the carrier density. For the diffusive part, which depends on the potential variations, we computed the overall $S_{d, total}$ as weighted average of the local diffusive Seebeck coefficients in the well, intermediate and barrier regions as:

$$\left(\frac{L_W}{\kappa_W} + \frac{L_I}{\kappa_I} + \frac{L_B}{\kappa_B}\right)S_{d, total} = \frac{L_W S_{d, W}}{\kappa_W} + \frac{L_I S_{d, I}}{\kappa_I} + \frac{L_B S_{d, B}}{\kappa_B} \qquad (2)$$

Where κ_W, κ_I and κ_B are the thermal conductivities of the three regions. The components in each region are computed separately again using the Boltzmann transport equation. Heavy doping causes some reduction of the phonon thermal conductivity down to $\kappa_W = 100$ W m^{-1}K^{-1} [48] from its bulk value $\kappa_B = 148$ W m^{-1}K^{-1}, which we assume for the undoped barrier regions. Calculations show that the electronic thermal conductivity, κ_e, in the heavily doped region can be as high as 5–10 W m^{-1}K^{-1}, while in the lightly doped barrier region it is negligible. Thus, the total thermal conductivities sum up to $\kappa_B = 140$ W m^{-1}K^{-1} and $\kappa_W = 110$ m^{-1}K^{-1}. Due to this minor difference between thermal conductivities, the temperature drop is almost uniform along the length of the material, so $S_{d, total}$ is only marginally affected.

To estimate S_{pd}, we proceed as follows: (1) we find the total Seebeck coefficient of bulk silicon, S_{total}, versus carrier density p from measured data in the literature, and interpolate these data across densities, as shown in Fig. 5(c) (black dashed lines). (2) We compute S_d using fully ab initio electronic structure and transport considerations as described in Ref. [49]. At every carrier density we then subtract the computed S_d from the measured S_{total} values and obtain S_{pd}. The distinction between the two parts of the Seebeck coefficient is necessary, because S_d is affected by energy filtering from the potential barriers, whereas S_{pd} is affected by the variation in the local doping density. For the individual components of the total phonon drag $S_{pd} = S_{total} - S_d$ in each of the three regions, we note that other than the doping variation, the potential well/barrier formation does not directly influence the phonon flow, and hence the phonon drag part. The total phonon drag contribution to the Seebeck coefficient is then given by:

$$L_{total}S_{pd, total} = L_W S_{pd, W} + L_I S_{pd, I} + L_B S_{pd, B}. \qquad (3)$$

Above we assume that the phonon drag contributions can be separately computed in the three regions and merged in a weighted average series

combination. This is an approximation, since the acoustic phonons involved in the phonon drag contribution are long range with long MFPs. Note, however, that computing S_{pd} at the average carrier density of the composite channel, rather than from the three regions independently, provides very similar values. Thus, using Eq. (3) we estimate $S_{pd} \approx 220$ μV/K. Remarkably, the phonon drag contribution for the average dopant density in our structure ($\approx 3.5 \times 10^{19}$ cm^{-3}) is instead 150 μV/K. These values are of similar order. However, the slightly higher values in the multi-barrier structure could indicate that multi-barrier device might utilize phonon drag slightly better. Finally, the total Seebeck coefficient is obtained as the sum of the two components, namely $S_{total} = S_{d, total} + S_{pd, total}$.

CRediT authorship contribution statement

Antonella Masci: Writing – original draft, Investigation, Formal analysis, Data curation. **Elisabetta Dimaggio:** Writing – review & editing, Validation, Investigation, Formal analysis. **Neophytos Neophytou:** Writing – review & editing, Validation, Funding acquisition, Formal analysis, Conceptualization. **Dario Narducci:** Writing – review & editing, Validation, Methodology, Conceptualization. **Giovanni Pennelli:** Writing – review & editing, Validation, Supervision, Investigation, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Appendix A. Supplementary data

Supplementary material related to this article can be found online at https://doi.org/10.1016/j.nanoen.2024.110391.

Data availability

Data will be made available on request.

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