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A 4-Channel Ultra-Low Power Front-End Electronics in 65 nm CMOS for ATLAS MDT Detectors

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Abstract: A 4-channel front-end electronics ($4 \times$ FEE) system for the muon drift tube in the ATLAS detector in the High-Luminosity LHC is presented. The overall channel architecture is optimized to reduce the power and area of the design. Each channel comprises a charge-sensitive preamplifier (CSP), shaper, discriminator and differential low-voltage signaling drivers. The proposed channel operates with a 5–100 fC input charge and exhibits a linear sensitivity of 8 mV/fC for the entire input charge range. The peaking time delay of the analog channel is 14.6 ns. At the output, the time representation of the input signal is provided in terms of the CMOS level and in scalable low-voltage signal (SLVS). The FEE consumes a current of 10.6 mA per channel from a single 1.2 V supply voltage. The full $4 \times$ FEE design is realized in TSMC 65 nm CMOS technology and its die-area is $2 \text{ mm} \times 2 \text{ mm}$.



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Citation: Shah, S.A.A.; De Matteis, M.; Kroha, H.; Fras, M.; Kortner, O.; Richter, R.; Baschirotto, A.

A 4-Channel Ultra-Low Power Front-End Electronics in 65 nm CMOS for ATLAS MDT Detectors. *Electronics* **2022**, *11*, 1001. <https://doi.org/10.3390/electronics11071001>

Academic Editors: João Paulo Pereira do Carmo, Subhanshu Gupta and Kunhee Cho

Received: 15 February 2022

Accepted: 22 March 2022

Published: 24 March 2022

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Keywords: read-out channel; front-end electronics; ATLAS experiment; monitored drift tube

1. Introduction

The upgrade of the Large Hadron Collider (LHC) to discover novel physics particles creates new challenges for the readout electronics. After a decade of successful operation, the ATLAS experiment, including the muon spectrometer, has to be upgraded to cope with the high data and radiation rates in High Luminosity LHC operation [1,2]. The luminosity of the Large Hadron Collider (LHC) accelerator at CERN will be upgraded by a factor of about seven compared to its previous performance. Muon drift tube (MDT) detectors are the main precision tracking detectors of the muon spectrometer in the ATLAS experiment in the Large Hadron Collider (LHC) [1]. The sense wires of the drift tubes are connected to the channels of an ASD chip [2] to process the signals generated by the ionization electrons created by muons traversing the tubes filled with an argon:CO₂ (93:7) gas mixture.

To cope with the new challenges of a high data rate and high luminosity, a new state-of-the-art version of the ASD chip [3–5] has been designed in 130 nm CMOS technology. Its analog chain includes a charge-sensitive preamplifier (CSP) and a three-stage shaper. It is operated in dual mode, either with a signal charge measurement using a Wilkinson ADC (W-ADC) or in time-over-threshold (ToT) mode. With a detector capacitance of 60 pF, it features a sensitivity (voltage-to-charge ratio) of 14 mV/fC, 15 ns peaking time delay, and 15 dB signal-to-noise ratio (SNR) for minimum input charge. Each channel consumes a power of 33 mW from a 3.3 V supply.

In the process of renewing the MDT readout electronics, one of the main objectives is to make a significant low-power and area-efficient design using long-term sustainable technology, along with achieving all the functional parameters of MDT-ASD [3]. In this design the technology is scaled down from a 130 nm to a 65 nm TSMC CMOS process and the circuit is operated from a single 1.2 V supply voltage (down from 3.3 V). With the

key target of power and area efficiency optimization, the full analog channel architecture is changed, and each block of the analog channel is designed accordingly with the new architecture and, as a consequence, with new specifications. Each channel starts with a single-ended CSP, which converts the incoming charge signal to a voltage pulse. The signal in the analog channel is converted into a pair of differential signals in later stages to improve the power supply rejection ratio. The design incorporates a two-stage shaper to implement bipolar shaping of the input signal. This design has a single mode of operation, time-over-threshold. The W-ADC mode, used for signal charge measurement and time-slewing corrections in the reference model, has become unnecessary due to the larger gain observed at the unchanged input-referred noise level of the new-generation chips, so it has been eliminated. To avoid bulky capacitors, as used in the three-stage shaper of the previous design, the sizing of passive components has been optimized to minimize RC component sizes, resulting in a 4x area shrinking factor in the shaper stage w.r.t. to the previous design. SLVS drivers have been designed to provide an interface for the FEE system to TDC, which is the subsequent stage of the readout chain.

The power consumption of each channel is 12.8 mW, which is 61.2 percent lower than in the previous design. Each channel occupies an area of 0.235 mm², which is only 58.75 percent of the previous design. These significant savings are achieved while guaranteeing a performance level in terms of a 14.6 ns peaking time of the analog channel and a 15 dB minimum SNR, as in the previous design. The design displays a linear sensitivity of 1.1 mV/fC and 8 mV/fC, for an input charge range of 5–100 fC, at the output of the CSP and analog channel, respectively.

2. ATLAS Experiment

ATLAS is one of two general-purpose experiments at CERN which contributed in the discovery of the Higgs Boson particle in 2012, and it is further used to investigate other particles that could make up dark matter [6]. As a general-purpose experiment, it is designed to study hard proton–proton collision processes at center-of-mass energies of up to 14 TeV. As a result of these collisions, some charged and neutral particles are generated. Muons are the most penetrating charged particles emerging from proton–proton collisions. In order to determine the energy and direction of the secondary particles emerging from the p–p collisions, a sequence of specialized detectors are used for the detection. The majority of tracking detectors are monitored drift tubes (MDTs) [2], which consist of gas-filled aluminium tubes with a central anode wire. The muons pass through the gas-filled pressurized tubes and ionize the gas molecules. The free electrons drift towards the centre anode wire, due to the electric field. The time of arrival of these charges at the wire is used to measure the distance of the track from the wire. Detailed information about MDT ATLAS readout electronics is provided in [1,2,6].

3. Implementation of the MDT-FEE Circuit

The architecture of a single-channel FEE is shown in Figure 1. The complete design is composed of four similar channels. The design has been realized in TSMC 65 nm CMOS technology. The input signal of each channel is a current pulse coming from the sense wire of the detector. The input signal is converted into a voltage pulse by the charge-sensitive preamplifier (CSP). The CSP's output pulse is amplified and shaped by the two-stage bipolar shaper (SH1, SH2). The CSP and shaper together constitute the analog signal processing chain of the design, which is connected with the discriminator through coupling capacitors. Two programmable DACs are used to set the threshold value for the discriminator. The discriminator compares the bipolar signal with the threshold value to yield the output, time-over-threshold. SLVS drivers are designed to provide an interface for the individual FEE channels with the subsequent TDC chip. Test-point buffers are added at the output of CSP and the shaper for diagnostic purposes. A central bias block has been designed, which mirrors the current to each channel from a reference source of 50 µA.

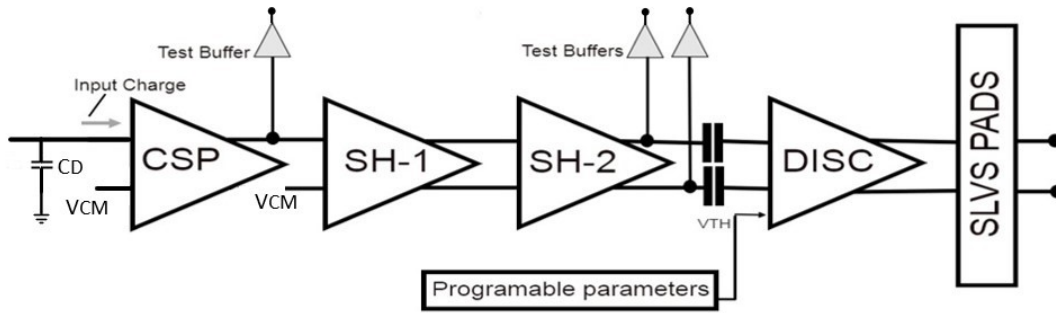


Figure 1. Generic block diagram of one channel of the FEE chip.

3.1. Charge-Sensitive Preamplifier

In the MDT-FEE design, the performance parameters of the CSP are of key importance. The design involves a two-stage, single-ended amplifier topology, as shown in Figure 2. The input signal, coming from the sense wire of the tube, is connected to the negative terminal of the CSP. A large parasitic capacitance ($C_D = 60$ pF) is connected between the CSP input node and ground, which is which is mainly due to the capacitance of the tube-wire system and the signal routing on the PCB. The positive input has been fixed by means of a resistor divider (R_{b1} and R_{b2}) to 700 mV, implemented on-chip for better matching. To suppress the substrate noise, a capacitor of 16 pF is attached to the positive terminal of the CSP on-chip. The feedback network of the CSP is a parallel combination of a resistor $R_F = 25$ k Ω and a capacitor $C_F = 920$ fF in parallel.

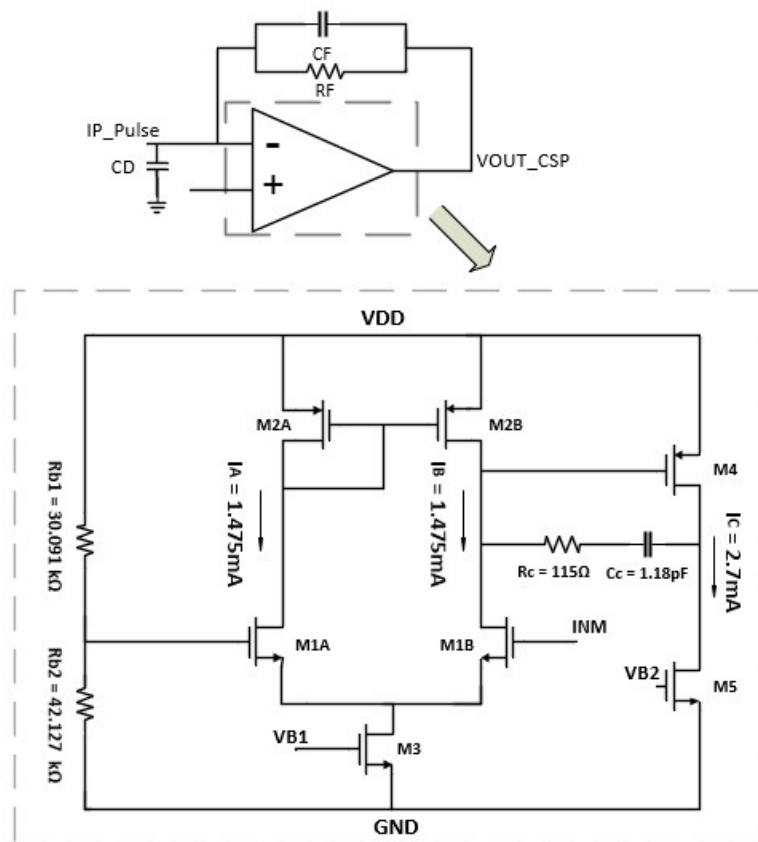


Figure 2. CSP and operational amplifier transistor-level scheme.

The CSP design is critical as it defines several key functional parameters of the design, such as signal rise-time, overall power consumption, and noise. Along with the high specification criteria, the functionality of this block is adversely affected by the large value of the detector capacitance. It has a highly deteriorating effect on the closed-loop-gain, bandwidth, sensitivity, and signal peaking time delay.

The most important performance parameters of the CSP in our design are the peaking time delay and signal-to-noise ratio. The peaking time delay is important for the precise determination of the arrival time of the signal, given the wide range of signal amplitudes as they occur in the experiment. CSP noise and the speed of response are optimized by using a suitable input device transconductance (gm_1). The differential input transistors (M1A–M1B), of size $W/L = 580 \text{ um}/330 \text{ nm}$, operate in moderate inversion (to mitigate the increase in power consumption) with a nominal current of 1.475 mA in order to have very large transconductance, $gm_1 = 25 \text{ mA/V}$. This is in accordance with the minimum thermal noise requirement. The input charge pulse for the FEE comes from a single source (the sense wire of the tube); thus, a single-ended topology has been chosen for the CSP, hence saving a current of 2.7 mA in the output stage of the amplifier, as shown in Figure 2. In this way, the use of common-mode feedback circuit is also eliminated. To minimize the peaking time delay, the OpAmp is designed with a very high unity-gain bandwidth of 2.4 GHz, with a phase margin of 60 degree, ensuring good stability. With these open-loop characteristics, the CSP exhibits a very fast peaking time of 4 ns without the detector capacitor and 11 ns with the large (60 pF) detector capacitor, as shown in Figure 3.

The load impedance of the CSP stage is the input impedance of shaper-1. It is a parallel combination of a resistor, R_1 , and a series connection of a resistor and a capacitor— R_2 and C_2 , respectively. The CSP transfer function depends on the feedback network, the transconductance of the input transistor (M1A–B), the load impedance Z_L and the detector capacitance C_D . The CSP transfer function can be approximated by Equation (1).

$$T(s) = \left(\frac{-R_F \left(1 - \frac{sC_F}{gm_{M1}}\right)}{\left(1 + sC_{FRF} \left(1 + \frac{C_D}{C_F} \frac{1}{gm_{M1}Z_L}\right)\right)} \right) \tag{1}$$

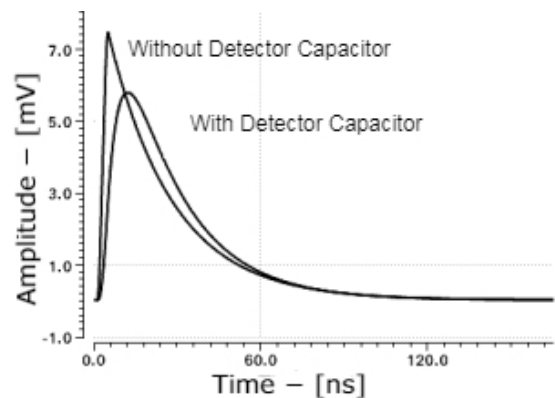


Figure 3. Transient response of CSP with and without a detector capacitor.

Similarly, the input impedance transfer function is given approximately by Equation (2). It is almost constant ($Z_{IN} = 44 \text{ } \Omega$) at low frequencies and below $73 \text{ } \Omega$ for all in-band frequencies, as shown in Figure 4.

$$Z_{IN} = \left(\frac{T(s)}{gm_1Z_L} \right) \tag{2}$$

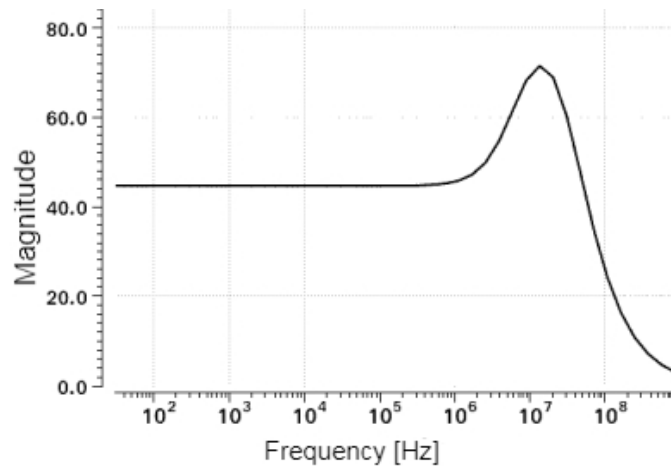


Figure 4. Input impedance of charge-sensitive preamplifier.

3.2. Shaper Section

The Preamplifier stage is followed by a two-stage shaper section to implement bipolar shaping of the pulse in order to mitigate signal pile-up at high signal rates. Each stage of the shaper is based on two-stage differential amplifiers, as shown in Figure 5. The two-stage differential topology is more robust to the load and allows for a higher output voltage swing. The transconductance value of input MOSs is 2.5 mA/V and sinks a current of 104 μ A in each input stage (I_a and I_b) and 418 μ A in each output stage, as shown in Figure 5. The output-stage MOSs have been designed with an overdrive voltage of 70 mV (i.e., moderate inversion) to maximize the output swing range, and to achieve a linear sensitivity for the full range of input charges up to 100 fC. To set the common-mode voltage a separate common-mode feedback (CMFB) network has been designed. The W/L values of the CMFB network are half of those of the main amplifier input stage in order to reduce the current consumption. The CMFB network is attached to the main amplifier through a sensing network, consisting of a pair of resistors with capacitors in parallel for better performance at higher frequencies. The values of currents are given in Figure 5.

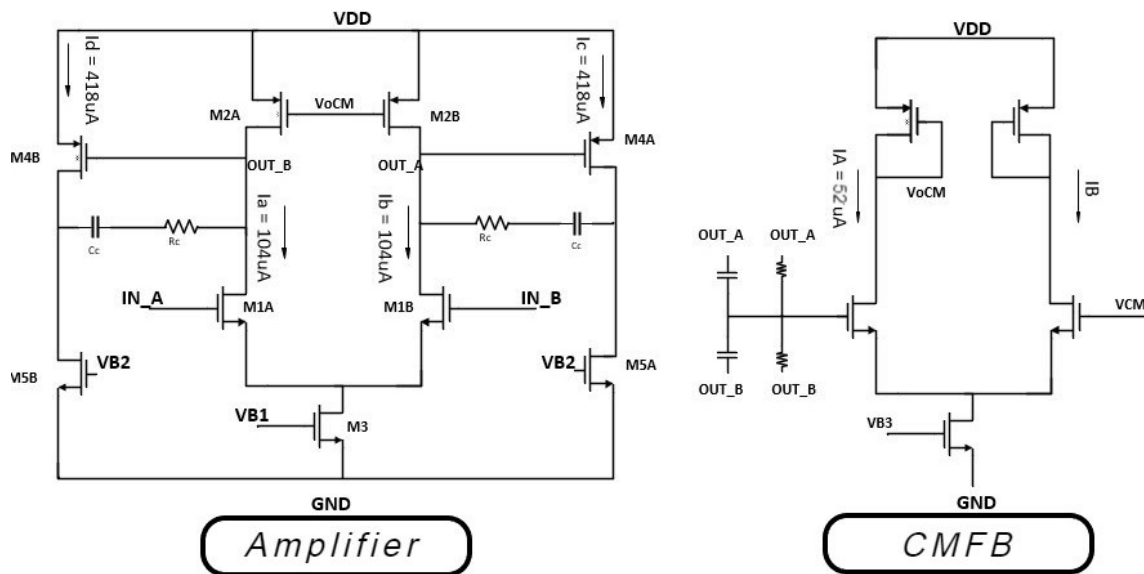


Figure 5. Shaper operational amplifier transistor-level scheme.

Each stage of the shaper (shaper 1–2) has an input impedance network and a resistive feedback loop, as shown in Figure 6. The poles and zeroes used to implement the bipolar shaping are the same as in ASD, at 130 nm [3], selected to cancel the very long time constant component of the positive ion MDT pulse [2]; however, the values Z-RC are greatly changed, shrunk by almost a factor of four, with the aim of an area-efficient design. The values of impedance network components are given in Table 1.

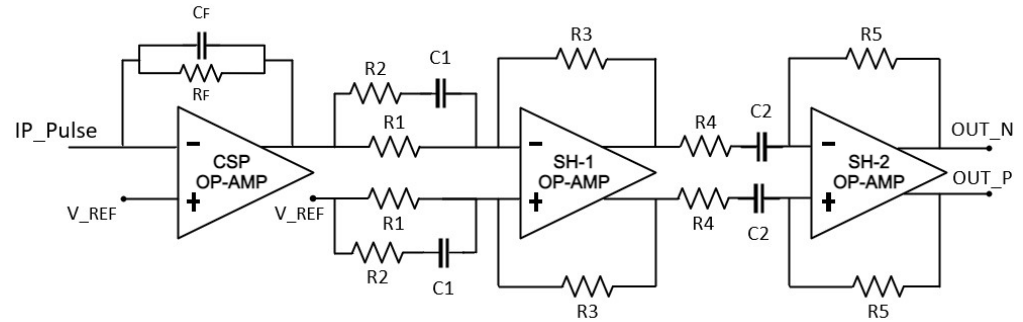


Figure 6. Analog signal-processing chain.

The transfer function of each shaper stage depends on the input impedance and feedback network. Equations (3) and (4) show the transfer function of shaper-1 and shaper-2, respectively.

$$T(s) = \frac{R_3}{R_1} \left(\frac{1 + sC_1(R_1 + R_2)}{1 + sC_1R_2} \right) \tag{3}$$

$$T(s) = \left(\frac{sC_2R_5}{1 + sC_2R_4} \right) \tag{4}$$

Table 1. Shaper Impedance network component values.

Stage	Component	Value
Shaper-1	R ₁	9.8 kΩ
Shaper-1	C ₁	10.2 pF
Shaper-1	R ₂	10.1 kΩ
Shaper-1	R ₃	9.8 kΩ
Shaper-2	R ₄	9.8 kΩ
Shaper-2	C ₂	11.5 pF
Shaper-2	R ₅	37.8 kΩ

The open-loop gain and unity-gain-bandwidth of the shaper amplifier are 50 dB and 500 MHz, respectively. With these open-loop characteristics, the closed loop-gain values of shaper 1–2 vary by less than 4 percent as compared to ideal amplifiers. The pass-band gain is given by the ratio between Z2 and Z1, whereas the bandwidth is fixed by the resistive and capacitive loads. The frequency response of each stage of the analog channel is plotted in Figure 7. The shaper features a pass-band width of 1.06–172.6 MHz and a pass-band gain of 17.6 dB.

At the output of the CSP and the shaper, test-point buffers have been designed, for diagnostic purposes, using a common-drain topology as shown in Figure 8. The buffer’s load resistance of 800 Ω is placed off-chip, on a PCB board.

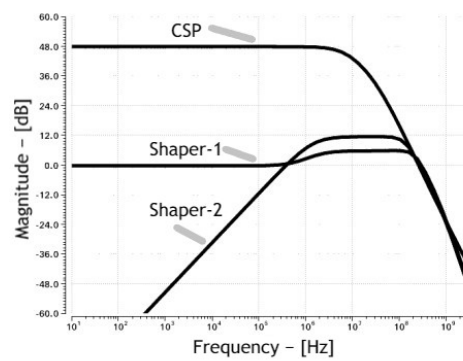


Figure 7. CSP and shaper stage (1–2) frequency response.

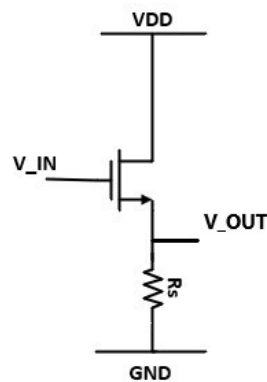


Figure 8. Test-point buffer.

3.3. Digital Circuit of FEE System

The output signal of the analog signal-processing chain is fed into the discriminator through coupling capacitors, where it is compared to a programmable threshold value, which ultimately yields the digital ToT output pulse.

The comparator has been designed using a two-stage single ended amplifier topology without compensation, as shown in Figure 9. It consists of a high gain amplification stage, followed by a series of inverters to produce the output, referred to as high or low, depending on the input signal and threshold value. The threshold value for the main comparator is set differentially. Two sets of 8-bit string-DACs and 3-to-8 bit decoders are used to set the threshold values, which are programmable up to 256 mV across the common mode voltage with an LSB of 2 mV. Each string-DAC is composed of a main-string and a sub-string to divide the reference voltage and give the output voltage with an LSB of 1 mV. Complementary CMOS switches were designed for selecting the required output voltage to set the threshold value.

A hysteresis block is added with the comparator to unbalance the current in the main differential amplifier (M1A-M1B) according to a programmable value. Its significance is to remove glitches in the output of the comparator, which arise due to noise. The hysteresis can be varied from 0–50 mV by means of the programmable digital word set externally at run-time.

A dead-time block is used to introduce a delay in the discriminator response up to 500 ns, programmable in steps of 30 ns, thus allowing a large set of dead-time options. To set all these programmable and channel parameters, a digital word carried by a 50 bit shift register is used. A new design approach, as compared to the reference design [3], of using parallel arrays of serial-in-parallel-out (SIPO) and parallel-in-serial-out (PISO) blocks is utilized in the design of the shift register. The digital word is shifted serially into the SIPO block from an external board. At the instance of loading the digital word from the SIPO block to the channel, it is loaded into the PISO block as well. At the output pad, the

contents of the PISO block can be visualized to verify the data loaded into the channel. The digital word is passed from an external board through a JTAG interface.

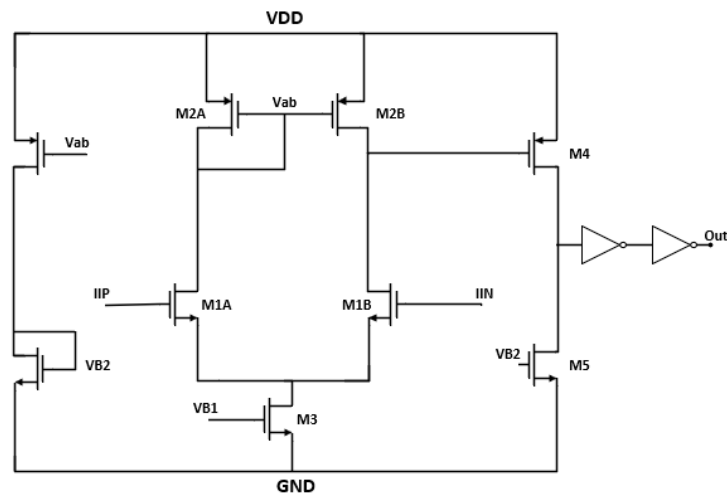


Figure 9. Comparator transistor-level scheme.

3.4. SLVS Output Drivers

Modern experiments, such as ATLAS, consist of large number of data-processing channels. Consequently, decreasing power consumption and improving the data transmission rate of readout electronics is important. For these reasons, along with providing the CMOS-level signal at the output, SLVS drivers are designed for connecting the FEE channels with the external components of the TDC. The SLVS standard is defined in [7] and describes a differential current-steering protocol. It has a voltage swing of 200 mV, across a common mode voltage of 200 mV. The load resistor on the receiver end is of the value of 100 Ω. At the output, the differential voltage is 400 mV and a current of 2 mA flows through the load resistor. The SLVS transmitter operates as a current source with switched polarity. The output current flows through the load resistance, external to the chip, building the differential output voltage swing of 400 mV. The proposed transmitter circuit, presented in Figure 10, uses the arrangement of four MOS switches in the H-bridge configuration [8,9], implemented with the M1–M2 (AB) NMOS transistors.

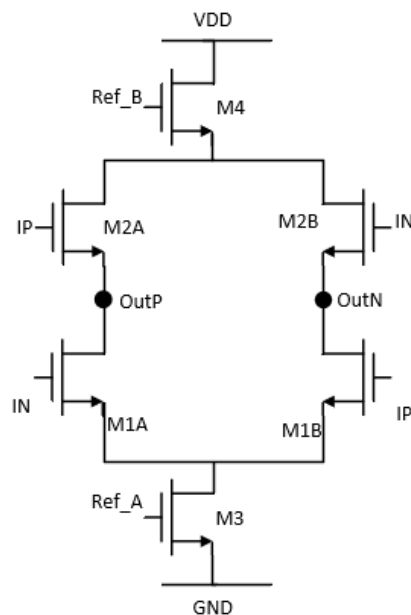


Figure 10. SLVS driver H-bridge transistor-level scheme.

4. Simulation Result

The FEE system has been designed in TSMC 65 nm CMOS technology. The four channels in the layout design are arranged and connected in order to guarantee the symmetry of paths with respect to the bias circuit, placed in the center region of the design. Each channel occupies an area of 0.235 mm². The total area of the design is 4 mm². Each channel consumes a current of 10.6 mA from a single 1.2 V supply voltage.

In post-layout simulations, the design was validated for different input charges (QIN) in the entire input range of 5–100 fC. The analog section output voltage ranged from 40 mV up to 800 mV for an input charge of 5–100 fC, as shown in Figure 11. Figure 12 shows that the analog chain exhibited a linear sensitivity (i.e. the peak-voltage of the curves vs. the input charge) of 8 mV/fC for the entire range of input charges. The design performance was also tested with respect to process, voltage, and temperature (PVT) variations to check for the robustness of the design. In PVT simulations, the design performance was tested with respect to different process corners (tt,ff,ss,fs,sf), a 10% variation in voltage supply, and a temperature range of 0–120 fC. In the worst case, the CSP exhibited a minimum sensitivity of 0.97 mV/fC and a maximum PTD of 14 ns.

When the test point buffers in channel 4 were switched on, the sensitivity of this channel was reduced to 6 mV/fC due to the loading effect of the buffers. However under normal operation conditions, when the buffer switches were off, all the channels exhibited a uniform sensitivity. The analog chain had a constant peaking time delay of 14.6 ns for the entire range of input charges. The baseline recovery time, complete time duration of overshoot and undershoot, of the bipolar signal was almost 400 ns for the full input range of 5–100 fC. At the output pads, the time representation of the input signal is provided as both the CMOS level with a voltage level of 0–1.2 V and the low-voltage differential signal with a voltage swing of 200 mV across a 200 mV common mode voltage, as shown in Figure 13. The complete layout design is shown in Figure 14. Table 2 summarizes the most important performance parameters of the presented FEE for the MDT-ATLAS-read-out, compared with our reference design [3].

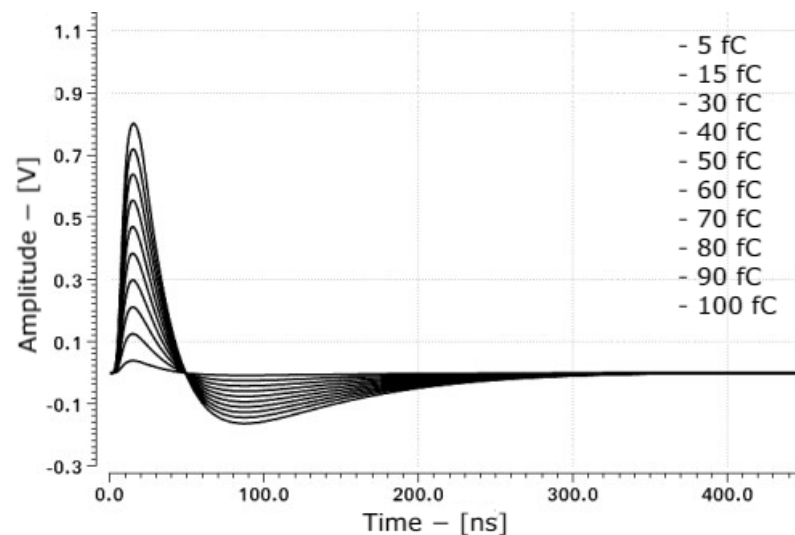


Figure 11. Analog channel output signal vs. input charge (5 fC–100 fC).

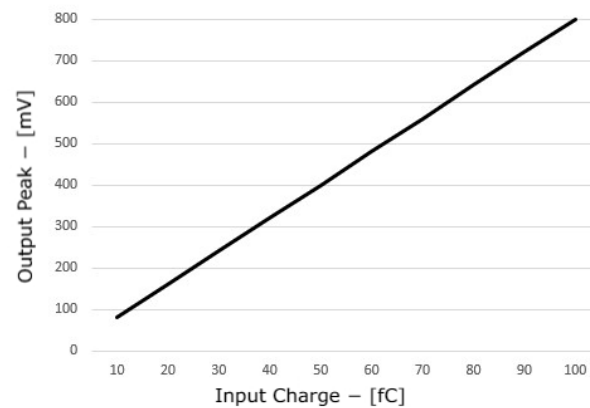


Figure 12. Sensitivity (V_{out}/Q_{in}) at the output of the analog section.

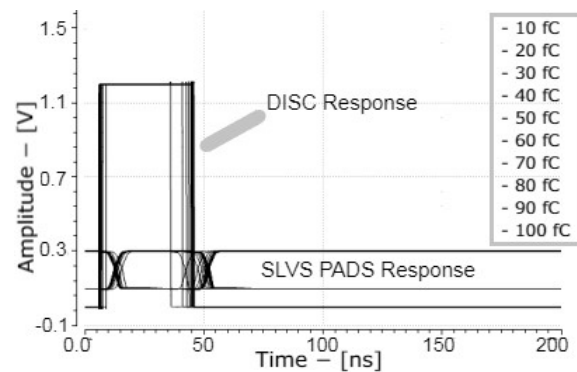


Figure 13. Comparator and SLVS drivers post-layout simulation results vs. input charges.

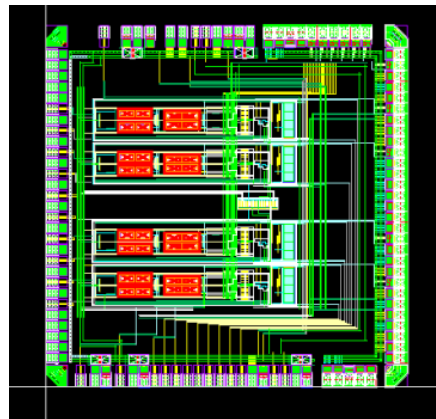


Figure 14. Four-channel FEE design layout.

5. Conclusions

A 4-channel FEE design for MDT ATLAS detectors at CERN LHC has been presented. The design has been realized in TSMC 65 nm CMOS technology, aiming for a power- and area-efficient design, matching the same performance parameters as that of the ATLAS MDT detectors [3]. As seen in Table 2, by scaling the technology to 65 nm CMOS and changing the design architecture of each block, the FEE channel is 61.3% more power efficient and utilizes 58.75% of the area as compared to the previous version. The key performance parameters—signal quality (SNR), peaking time and input signal dynamic range—are the same as for the previous design.

Table 2. State-of-the-art comparison.

Parameter	FEE 65 nm	ASD 130 nm
Technology	65 nm	130 nm
Channel Area	0.235 mm ²	0.4 mm ²
Supply Voltage	1.2 V	3.3 V
Channel Power	12.8 mW	33 mW
Detector Capacitance	60 pF	60 pF
Shaping Function	Bipolar	Bipolar
Input Charge	5–100 fC	5–100 fC
Signal Peaking Time	14.6 ns	15 ns
Sensitivity	8 mV/fC	14 mV/fC
SNR	15 dB	15 dB

Author Contributions: Conceptualization, A.B., M.D.M., H.K., M.F., O.K. and R.R.; methodology, A.B.; software, S.A.A.S.; formal analysis, S.A.A.S. and M.D.M.; writing—original draft preparation, S.A.A.S. and A.B.; writing—review and editing, M.D.M., H.K. and R.R.; supervision, A.B.; project administration, A.B. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

LHC	Large Hadron Collider
MDT	Monitored Drift Tube
FEE	Front-End Electronics
CSP	Charge-Sensitive-Preamplifier
PTD	Peaking Time Delay
SNR	Signal-to-Noise-Ratio
ASD	Amplification-Shaper-Discriminator
TDC	Time-to-Digital Converter
BLR	Baseline Recovery
LSB	Least Significant Bit
ToT	Time-over-Threshold
SIPO	Serial-In-Parallel-Out
PISO	Parallel-In-Serial-Out

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