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Supply-Embedded Communication in Differential Automotive Networks

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by

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To my Family

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Abstract

The advancements in modern vehicles are mainly due to electrical and electronic components that support a growing demand for lower emission levels, higher safety and comfort. These components communicate more and more via bus systems, which leads to increasingly complex cable harnesses in modern vehicles. Today, the wiring harness of an automobile is one of the most complex components. Therefore, techniques to reduce the amount of wiring are becoming increasingly important.

In the context of this work, a new method for the integration of communication and power supply of the network participants on a differential bus is examined. In contrast to methods such as Power over Ethernet (PoE), the discussed approaches use defined charges to emit pulses into the communication bus, which also serves as a power supply line. Two switched-capacitor approaches are proposed, the charge alternation (CA) and the charge pump (CP) method. While the proposed CA method, operating at $2Mbps$, consumes only 50% of the power of an equivalent resistive load modulation, the CP method further improves energy efficiency due to the inherent reuse of the charge. The two approaches are verified with a demonstrator and a transmitter test chip, which was manufactured in a 180nm BCD-on-SOI technology. The results of both realizations confirm the efficiency of the concept. Furthermore, a suitable receiver is discussed and implemented as part of a transceiver test chip fabricated in the same technology.

The work is structured as follows: After an introduction and the motivation for this research project in Chapter 1, the basic transmission concepts are described and the modeling of the differential bus based on a twisted pair line is analysed in Chapter 2. Chapter 3 examines both switched-capacitor transmission concepts in detail regarding pulse shape, coding and power consumption. To verify the proposed transmission methods in a real environment, a demonstrator with off-the-shelf components is discussed and evaluated in Chapter 4, which replaces the existing physical layer of a CAN-like state-of-the-art application for interior car illumination with the proposed techniques. The validation also shows that the standards in terms of electromagnetic emissions can be achieved with the proposed solutions. A test chip implementation for the transmitter that realizes both methods is described in detail in Chapter 5. This includes the architecture of the required switching elements, the design of the ESD protection that enables an HBM stress level of $> 8kV$ and all necessary components for a chip implementation, which are necessary for use in a real network environment. At the end of this chapter, the measurement results of the transmitter test chip are discussed. Chapter 6 proposes the receiver concept and the implementation of the transceiver test chip, which extends the implementation of the transmitter test chip. The promising results of the realized transceiver test chip are

discussed before conclusions are drawn in Chapter 7.

Abstract

I recenti progressi tecnologici in ambito automotive sono dovuti principalmente alla diffusione di nuovi componenti elettrici ed elettronici che favoriscono la riduzione dei livelli di emissione e garantiscono maggiore sicurezza e comfort. Il progressivo aumento di questi componenti, che sono generalmente connessi tramite un bus, sta rendendo il sistema di cablaggio automobilistico sempre più complesso fino a farlo divenire uno dei blocchi maggiormente critici da progettare. Pertanto, si sta cercando di sviluppare nuove tecniche per ridurre il numero d'interconnessioni.

In questo lavoro viene analizzato un nuovo metodo per integrare la comunicazione e l'alimentazione su un unico bus differenziale. Diversamente dai metodi Power over Ethernet (PoE), l'implementazione proposta si basa sull'iniezione di cariche ben definite sul bus di comunicazione, che allo stesso tempo alimenta i vari dispositivi, al fine di generare dei pulsi. Sono proposti due approcci basati su capacità di commutazione: il Charge Alternation (CA) e il Charge Pump (CP). Il metodo CA, a $2Mbps$, richiede il 50% della potenza di modulazione del carico resistivo, mentre il metodo CP grazie alla capacità di riutilizzare parzialmente la carica immagazzinata offre prestazioni ancora migliori. Entrambi i circuiti di trasmissione sono verificati da una scheda dimostrativa e da un test chip in tecnologia 180nm BCD-on-SOI da cui si sono ottenuti risultati eccellenti che confermano la validità della proposta. Inoltre, un circuito di ricezione è analizzato e implementato in un test chip che quindi realizza il ricetrasmettitore completo.

La tesi è organizzata come segue: L'introduzione e le motivazioni alla base dell'attività svolta sono mostrate nel Capitolo 1. Nel Capitolo 2 sono analizzati il concetto basico di trasmissione e la modellazione del bus differenziale. I due trasmettitori proposti sono esaminati nel Capitolo 3 mostrando nel dettaglio la caratteristica dei pulsi, lo schema di codifica e il consumo energetico. Nel Capitolo 4 viene illustrata una scheda dimostrativa realizzata con componenti discreti e i relativi test svolti su di essa dove un layer fisico di un'applicazione simil-CAN per l'illuminazione interna delle auto è rimpiazzato con successo. Inoltre, viene mostrato anche che i requisiti standard sulle emissioni elettromagnetiche sono soddisfatti. L'implementazione in silicio del trasmettitore, inclusivo di entrambi i circuiti sviluppati, è descritta dettagliatamente nel Capitolo 5. In particolare, vengono mostrati l'architettura degli switch ad alta tensione, la protezione ESD che fornisce un livello di HBM $> 8kV$ e gli ulteriori blocchi necessari al funzionamento del chip. Alla fine dello stesso capitolo vengono mostrate le prestazioni ottenute dal chip integrato. Nel Capitolo 6 viene proposto un circuito di ricezione e la composizione del test chip che implementa il ricetrasmettitore completo utilizzando una struttura di base simile a quella precedentemente utilizzata. I risultati dei test effettuati sul chip sono quindi esplicati e

infine sono tratte le conclusioni.

Kurzfassung

Die Innovationskraft von modernen Fahrzeugen ist hauptsächlich auf elektrische und elektronische Komponenten zurückzuführen, die eine steigende Nachfrage nach niedrigeren Emissionswerten, höherer Sicherheit und Komfort unterstützen. Diese Komponenten kommunizieren mehr und mehr über Bussysteme, was zu immer komplexeren Kabelbäumen in modernen Fahrzeugen führt. Heutzutage zählt der Kabelbaum eines Automobils zu einem der komplexesten Bauteile. Daher werden Techniken zur Reduzierung des Verdrahtungsaufwands immer wichtiger.

Im Rahmen dieser Arbeit wird eine neue Methode zur Integration von Kommunikation und Stromversorgung der Netzwerkteilnehmer auf einem differenziellen Bus untersucht. Im Gegensatz zu Verfahren wie Power over Ethernet (PoE) verwenden die diskutierten Ansätze definierte Ladungen, um Impulse in den Kommunikationsbus zu emittieren, welcher gleichzeitig als Stromversorgungsleitung dient. Es werden zwei Switched-Capacitor Techniken vorgeschlagen: die Charge Alternation (CA) und die Charge Pump (CP) Methode. Während die vorgeschlagene CA-Methode, welche bei $2Mbps$ arbeitet, nur 50% der Leistung einer äquivalenten ohmschen Lastmodulation verbraucht, verbessert die CP-Methode die Energieeffizienz aufgrund der inhärenten Nachnutzung der Ladung noch weiter. Die beiden Ansätze werden mit einem Demonstrator und einem Transmitter-Testchip verifiziert, welcher in einer 180nm BCD-on-SOI Technologie hergestellt wurde. Die Ergebnisse beider Realisierungen bestätigen die Leistungsfähigkeit des Konzepts. Weiterhin wird ein passender Receiver diskutiert und als Teil eines Transceiver-Testchips implementiert, welcher in derselben Technologie hergestellt wurde.

Die Arbeit ist wie folgt gegliedert: Nach einer Einführung und der Motivation für dieses Forschungsprojekt in Kapitel 1 werden die Übertragungskonzepte beschrieben sowie die Modellierung des differenziellen Busses auf Basis einer Twisted-Pair Leitung in Kapitel 2 analysiert. Kapitel 3 untersucht beide Switched-Capacitor Techniken im Detail hinsichtlich Pulsform, Codierung und Stromverbrauch. Um die vorgeschlagenen Übertragungsmethoden in einer realen Umgebung zu überprüfen, wird in Kapitel 4 ein Demonstrator mit handelsüblichen Komponenten diskutiert und bewertet, der die vorhandene physikalische Schicht eines CAN-ähnlichen Protokolls durch die vorgeschlagenen Techniken ersetzt. Die Validierung zeigt auch, dass die Standards im Hinblick auf elektromagnetische Verträglichkeit (EMV) mit den vorgeschlagenen Lösungen erreicht werden können. Eine Testchip-Implementierung für den Transmitter, die beide Methoden realisiert, wird in Kapitel 5 ausführlich beschrieben. Dies beinhaltet die Architektur der erforderlichen Schaltelemente, das Design des ESD-Schutzes, die einen HBM-Stresslevel von $> 8kV$ ermöglichen, und alle notwendigen Komponenten für eine Chipimplementierung, welche für den Einsatz in einer realen

Netzwerkumgebung notwendig sind. Am Ende dieses Kapitels werden die Messergebnisse des Transmitter-Testchips diskutiert. Kapitel 6 beschreibt das Empfängerkonzept und die Implementierung des Transceiver-Testchips, welcher die Implementierung des Transmitter-Testchips erweitert. Die vielversprechenden Ergebnisse des realisierten Transceiver-Testchips werden diskutiert, bevor in Kapitel 7 Schlussfolgerungen gezogen werden.

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Acronyms

ADC	Analog-to-digital converter
AM	Amplitude modulation
ASIL	Automotive safety integrity level
AWG	Arbitrary waveform generator
BCD	Bipolar-CMOS-DMOS
BOX	Buried oxide
CA	Charge alternation
CA-CHG 1-4	Charge alternation mode - charge S_1-S_4 state
CA-CHG 2-3	Charge alternation mode - charge S_2-S_3 state
CAN	Controller area network
CDL	Circuit design language
CMC	Common-mode choke
CMOS	Complementary metal-oxide semiconductor
CMRR	Common-mode rejection ratio
CP	Charge pump
CP-CHG	Charge pump mode - charge state
CP-DIS	Charge pump mode - discharge state
CW	Continuous wave
DMI	Differential-mode inductor
DPI	Direct power injection
DTI	Deep trench isolation
DUT	Device under test
EMC	Electro-magnetic compatibility
ESD	Electro-static discharge
ESR	Equivalent series resistance
FPGA	Field-programmable gate array
FSM	Finite-state machine

HBM	Human-body-model
Hi-Z	High-impedance or floating output
HV	High voltage
HVNMOS	High-voltage n-type metal-oxide semiconductor
HVPMOS	High-voltage p-type metal-oxide semiconductor
HW	Handle wafer
I/O	Input/Output
JP	Jumper
LDMOS	Lateral double-diffused metal-oxide semiconductor
LED	Light-emitting diode
LF	Length factor for twisted pair cables
LV	Low voltage
LVDS	Low-voltage differential signaling
MeLiBu®	Melexis Light Bus
MOS	Metal-oxide semiconductor
MV	Medium voltage
NBL	N-buried layer
NMOS	N-type metal-oxide semiconductor
PCB	Printed circuit board
PHY	Physical protocol layer
PLC	Power line communication
PMOS	P-type metal-oxide semiconductor
PoDL	Power over data lines
PoE	Power over ethernet
POR	Power-on reset
PoX	Power over ethernet or data lines
PRBS	Pseudo-random bit stream

PTFE	Polytetrafluoroethylene
QFN	Quad flat narrow package
RBW	Resolution bandwidth
RZ	Return-to-zero code
SEC	Supply-embedded communication
SOI	Silicon-on-insulator
SPST	Single-pole/single-throw
TLP	Transmission-line pulse
UART	Universal asynchronous receiver-transmitter
URZ	Unipolar return-to-zero code
USB	Universal serial bus
UTP	Unshielded twisted-pair

List of Symbols

BER	Bit error rate
c_0	Electro-magnetic propagation velocity in vacuum, 299,792,458 m/s
C'	Capacitance per unit length in the transmission line model
C_{dg}	Drain-gate capacitance
C_{ds}	Drain-source capacitance
C_{gs}	Gate-source capacitance
C_L	Load capacitance
C_P	Parallel, parasitic capacitance
C_S	Functional switched capacitance
D	Distance between the wire centres of a twisted pair cable
d	Diameter of a wire, without coating
DR	Data rate
ε_{eq}	Equivalent dielectric constant
v_{TP}	Propagation speed of a twisted pair cable
f	Frequency
GBW	Gain-bandwidth product
G'	Conductance per unit length in the transmission line model
g_m	Transconductance
g_o	Output conductance
I_d	Drain current
I_L	Load current
I_{max}	Maximum current
I_{TLP}	Transmission-line pulse current
I_{trg}	Trigger current
k	Coupling factor
L_C	Choke, coupling inductance

$L^{'}$	Inductance per unit length in the transmission line model
ϑ	Temperature
m	Modulation index
$M^{'}$	Mutual inductance per unit length in the transmission line model
$M_{N_{FS}}$	Floating switch NMOS transistor
$M_{P_{HS}}$	High-side switch PMOS transistor
$M_{N_{LS}}$	Low-side switch NMOS transistor
μ_0	Vacuum magnetic permeability, $4\pi \times 10^{-7} H/m$
$\mu_{r_{cu}}$	Relative magnetic permeability of copper, 0.999994
$n_{tw}^{'}$	Number of twists per unit length of the twisted pair cable
ω	Angular frequency
$\overline{P}_{AM}$	Average power of an amplitude modulated signal
P_{CW}	Power of a continuous wave signal
Q_{C_S}	Charge of the functional switched capacitance
$R^{'}$	Resistance per unit length in the transmission line model
$R_{ds_{on}}$	On-resistance of drain-source channel
R_{on}	On-resistance
R_{sw}	Resistance of a switch
R_T	Termination resistor
s	Variable in complex frequency domain
S_1	Switch between BH and C1 in CA mode, and BH and CL in CP mode
S_2	Switch between C1 and BL in CA mode, and CH and BL in CP mode
S_3	Switch between BH and C2 in CA mode, and CL and CH in CP mode
S_4	Switch between C2 and BL in CA mode

σ_{cu}	Conductivity of copper, $56.3 \times 10^6 S/m$ at $\vartheta = 20°C$
σ_d	Conductivity of a dielectric material
t	Time
V_5	$5V$supply voltage
V_B	DC voltage of the bus
V_{bdo}	Break-down voltage
V_{BG}	Bandgap voltage
V_{clamp}	Clamping voltage
V_{CORE}	Core supply voltage
V_{ds}	Drain-source voltage
V_{f_D}	Diode forward voltage
V_{gs}	Gate-source voltage
V_{HBM}	Voltage level according human-body-model (HBM)
V_{hold}	Holding voltage
V_{op}	Operational voltage level
V_{trg}	Trigger voltage
Z_C	Characteristic impedance of a cable
Z_{FS}	Free-space impedance, 377Ω

List of Interfaces and Parameters

AIO	Analog input/output (I/O) pin
BH	Connection pin to the bus (positive)
BL	Connection pin to the bus (negative)
C1	Connection pin to capacitor in CA mode (S_1, S_2)
C2	Connection pin to capacitor in CA mode (S_3, S_4)
CH	Connection pin to BH-connected capacitor in CP mode
CK	Clock input pin
CL	Connection pin to BL-connected capacitor in CP mode
CNT1	Hysteresis setting for receiver channel 1
CNT2	Hysteresis setting for receiver channel 2
CTRL	Control signal for supply block
DISV5	Disable input control pin for $5V$-regulator, open = disabled, grounded = enabled
DIVD	Capacitive divider ratio, upper nibble *BL*-related, lower *BH*-related
DIVSW	Control of capacitive divider outputs
DR_DIVIDER	Data rate setting in FPGA
EN_DOUT	Enable of the digital output pins *RXO1*, *RXO2*
EN_RX	Enable of the receiver
EN_TEST	Enable of test mode, input for external FPGA controller
EN_OD	Enable of the open-drain mode of the digital output pins
EOM	End of measurement indication of bit error test
GND	Ground connection pin
GNDIO	Ground pin for the I/O interfaces
IPD5U	Internal pull-down current of $5\mu A$
MAX_ERR	Maximum permitted errors during BER test
RNI	Reset of the digital control, low active

RXCK	Receiver clock input
RXCK_DIV	Division factor between RXCK and the master clock of the FPGA
RXO1	Receiver data output, channel 1
RXO2	Receiver data output, channel 2
SCHEME	Modulation setting in FPGA
SN	Switch control signal of the demonstrator for S_2, S_3 in CAmode and S_3 in CP mode
SP	Switch control signal of the demonstrator for S_1, S_4 in CA mode and S_1, S_2 in CP mode
QN	Output of the lower comparator in the receiver part of the demonstrator
QP	Output of the upper comparator in the receiver part of the demonstrator
RxD	Receive data signal, part of the UART interface
SSEL	Solution selection control input pin, '0' = CA approach, '1' = CP approach
SSTATE<1:0>	State selection input control pins
START	Start signal for digital and bandgap, upon reaching the POR threshold
TxD	Transmit data signal, part of the UART interface
VAUX	Auxiliary supply provided by external devices
VREFH	Upper threshold voltage in the receiver of the demonstrator
VREFL	Lower threshold voltage in the receiver of the demonstrator
SWC	Switch control output latch/register
TCK	Test input pin, clock for test register
TDA	Test input pin, data for test register
TMOUT	Test mode output latch/register
TMREG	Test mode input shift register

TMSHIFT	Test mode shift state indication
TMUX	Internal selection signal for AIO
TRIM	Internal trimming setting for bandgap and $5V$-regulator
V5	5V supply pin, for decoupling the regulated supply or external sourcing
VBG	Internal bandgap reference voltage ($1.2V$)
VBIAS	Internal bias voltage
VCORE	Internal core supply ($3.8V$)
VIO	Supply pin for the I/O interfaces
VS	Supply connection pin
W_BIT_CNT	Bit width of symbol counter of the BER test
W_EOM_CNT	Bit width of counter for EOM pulse width
W_ERR_CNT	Bit width of error counter in BER test

Glossary

Arduino

is an open-source electronics platform based on easy-to-use hardware and software. It's intended for anyone making interactive projects. (Source: arduino.cc)

baseline wander

is an extraneous, low-frequency signal component known from ECG processing [1], which is introduced in the context of this work by the finite inductance in the feeding network under presence of time-varying DC content of the transmitted data signal

latch-up

is happening in a n-p-n-p parasitic structure which acts as a combination of an n-p-n and p-n-p transistors. As soon as one is turned on, it will trigger the other as well, so that both devices mutually hold each other in saturation until power-off.

pad-limited layout

is a chip layout that is area-constrained by the number of required pads. Usually, the core circuit requires a smaller area, by contrast to a core-limited chip layout, where the core circuit defines the net area of the chip.

punch-through

is happening in n-p-n or p-n-p structures having two depletion regions. In case of applied reverse bias, an extension of one depletion region occurs and intersects with the other. As a result, a conduction path establishes which yield to a breakdown.

PXI

PCI eXtensions for Instrumentation (PXI) is one of several modular electronic instrumentation platforms in current use. PXI is based on industry- standard computer buses and permits flexibility in building equipment. One can select the modules from a number of vendors and integrate them into a single PXI system. (Source: Wikipedia)

Raspberry Pi

is a series of small single-board computers (SBCs). Raspberry Pi SBCs feature a Broadcom system on a chip (SoC) with an integrated ARM-compatible central processing unit (CPU) and on-chip graphics processing unit (GPU). (Source: Wikipedia)

Schmitt-Trigger

is a comparator circuit with hysteresis, implemented by applying positive feedback to the non-inverting input of a comparator or differential amplifier. It is named after its inventor, Otto Schmitt. (Source: Wikipedia)

StrongARM latch

is an electronic latch circuit topology first proposed by Toshiba engineers Tsuguo Kobayashi et al. [2] and got significant attention after being used in StrongARM microprocessors. It is widely used as a sense amplifier, a comparator, or just a robust latch with high sensitivity. (Source: Wikipedia)

T-switch

is a series of two complementary MOS switches. The centre tap between the switches is grounded by an NMOS switch in case the T-switch is in open state to avoid cross-coupling between its terminals.

CHAPTER 1

Introduction

> I have not failed. I've just found 10,000 ways that won't work.
>
> Thomas A. Edison

In the last few decades, the importance of electronic components in automotive environments has grown dramatically. The need for controlling and connecting them, let the automotive harness become one of the most complex building blocks in today's vehicles. Presently, a multitude of Electrical Control Units (ECUs) are distributed over the whole vehicle that would require automotive power line communication (PLC) systems to perform in direct contact with the battery harness, which is highly disturbed by electrical actuators due to switching transients. Commercially available and proposed solutions based on carrier modulation, show that PLC in automotive networks can comply with disturbed environments [3–5]. However, a break-through not took place until now. This might be linked to the enormous increase in electrical and electronic components attached to the power harness of a car. In parallel to this, the demand for reliability and safety is increasing, since the number of elements contributing to a dedicated function increases as well. Since 2011, the ISO 26262 standard is specifying automotive safety aspects and classifies the automotive safety integrity level (ASIL) [6]. PLC might be seen as ambitious to realize, connecting distributed functions in automotive environments under tight safety considerations.

Since recent years, other techniques became popular: power over ethernet (PoE) [7] and power over data lines (PoDL) [8]. The philosophy is different to PLC, since the power supply for the connected nodes is embedded in the data connection lines. This can be formulated as supply-embedded communication (SEC), which will be investigated on a differential bus system in this work.

The research project was done together with Federico D'Aniello. His thesis [9] focusses on the circuit design of the transmitter and receiver of the proposed implementations. This thesis is aimed to investigate the concept, the system architecture, as well as design of the

digital control, supply, and protection scheme.

1.1 Motivation

According to [10], automotive bus architectures are becoming increasingly separated in functional domains, where automotive sub-systems are divided from a direct connection to the battery by Domain Control Units (DCUs). Such domains are typically power train & chassis, Advanced Driver Assistance Systems (ADAS) & safety, infotainment, comfort, and connectivity. Domain-specific sensors and actuators are typically connected by low data-rate single-ended network approaches such as the Local Interconnect Network (LIN)[11] or high-speed differential networks following the controller area network (CAN) standard or CAN-like implementations [12]. Especially for differential networks, this provides an opportunity to embed the power supply for the nodes into the communication lines.

The main objective in this work is a low-cost solution for a CAN-like protocol that operates at data rates of $2Mbps$. It requires a low latency of less than one bit time to allow an implementation in high-speed event-driven networks ($\geq 1Mbps$), such as CAN[13]. Said solutions are not addressable by carrier-based systems, since the signal extraction from the frequency band of interest to baseband, often take several bit times. This is because of the introduced group delays in the reception chain, caused by signal down-conversion, filtering and detection. Furthermore, a carrier-based approach requires a precise time base for the synthesis of the carrier. The latter is typically not available in low-cost implementations.

Hence, a real-time implementation at the speed of $2Mbps$ can only be implemented with a baseband approach, where the data signal is directly modulated.

1.2 The differential network approach

The main motivation for implementing differential bus systems is the inherent capability to discriminate the wanted information under presence of large common-mode signals. It gives an advantage in highly disturbed environments, such as in a car, where large load transients can couple into the communication lines. With a differential bus that is highly symmetrical, these disturbances turn in to common-mode disturbances and therefore not in a differential signal, which can harm the detection. However, asymmetries in the wiring, lead to a differential disturbance which is related to the amount of asymmetry. In case the signal level range is identical between the signal lines like in low-voltage differential signaling (LVDS), also no threshold for the detection is needed, because of the level crossing. However, in CAN, PoE or PoDL this is not applicable directly since the DC-level differs between the lines.

Another advantage of the differential bus is the low electro-magnetic compatibility (EMC) emission compared to single-ended bus topologies. It leads to a low radiation capability

because the current flowing through both communication lines is equal in magnitude, but opposite in phase, while the area that the two wires are encircling to build a loop antenna, is ideally zero. Usually, such differential buses are implemented by twisted pair cables, since the twist balances inhomogeneous environments between the lines. For cost reasons, mostly unshielded twisted-pair (UTP) cables are used.

Any common-mode signal applied to a differential network will cause an excitation on one side of the transmission line, so that radiation can occur. In this case, the transmission line operates in an “antenna” mode, which is highly unwanted. To predict a potential radiation, differential networks are often qualified, by so called, conducted emissions measurements, where the sum of both lines is observed and compared to a standard reference. In case of CAN, this is the IEC 62228-3 [14].

CHAPTER 2

Fundamentals

2.1 Transmission approaches

The aim is that the network nodes are supplied with power from the differential bus. Therefore, a DC-coupling network is required that provides a DC-path between the local supply reservoir and the power source. Instead of two loosely coupled inductors, a differential-mode inductor (DMI) can be of advantage since it also provides a low-ohmic path for common-mode AC-signals [15]. This is because the magnetic flux, caused by common mode currents, is eliminated due to opposite turns, so that common-mode signals experiencing a low-ohmic path. As a result, the common-mode signal is attenuated by the impedance of the reservoir capacitor or the attached power supply. A DC-coupling network is required in both, the power supply which injects the necessary supply for the nodes, and in the nodes itself. At the ends of the network, a termination is required that is equal to the characteristic impedance Z_C of the transmission line. At the same time, it is necessary that the DC-coupling network does not load the transmission line at the frequency band of the data transmission f_{DTA}, so that the feeding inductances becomes

$$L_F \gg \frac{Z_C}{4\pi f_{DTA}}\,. \tag{2.1}$$

A typical example for power over ethernet or data lines (PoX) is shown in Fig. 2.1 [16]. Here, the local supply of the node is extracted by a DMI and stored in a reservoir capacitor C_{DEC}. The local ground of the node has parasitic capacitances to the local environment. The transmitter, associated with the physical layer (PHY), is capacitively connected to the bus by C_C. Depending on the application, there is a common-mode choke (CMC) inserted between the node connections and the bus lines, or in series to C_C (not shown). The latter case can be beneficial, since the DC-current is not flowing over the CMC. This lowers the demand on its equivalent series resistance (ESR), that would cause otherwise an unwanted voltage drop in the first case because of the power consumption of the node [15]. Different to a DMI, the aim of a CMC is to increase the impedance for common-mode signals because the magnetic flux is rised for common mode signals, which effectively

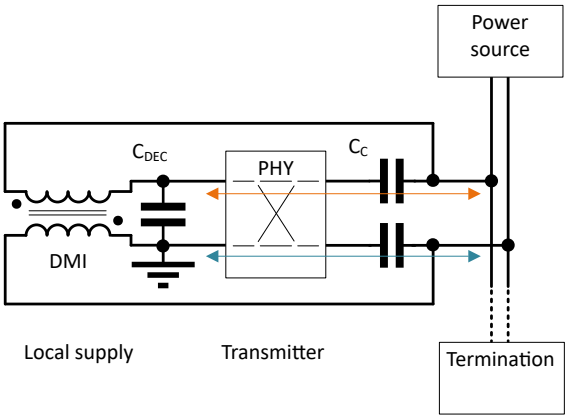


Figure 2.1: Signal paths in PoX transmitters

increases the inductance. For differential signals, the CMC is low-ohmic. Because of driver asymmetry, a CMC is often needed to achieve the required EMC specifications, especially in CAN-bus applications certified according to IEC 62228-3 [14].

Turning back to Fig. 2.1, it can be seen from the illustration, that each of the bus connections have a separate conduction path to the local supply domain through the transmitter block. This is because, if one side is driven high, the other side need to be driven low, and vice versa. This implies that the conduction to high- and low levels are performed by different elements of the transmitter. Since these levels are provided by the local supply of the node, all parasitic capacitances between the local supply and the local environment, are temporarily connected by the driver impedance to the bus during a transmission. In case of an asymmetric transmitter, i.e. the dynamic characteristics are not complementary matching in terms of turn-on time and transition behaviour, the sum of both is temporarily not constant. That results in an unwanted common-mode signal, which requires mostly further suppression by a CMC.

A different approach could be a load modulation, where a direct path to the local supply domain is avoided. Only the control instance for varying the load impedance are controlled by the local supply domain, as indicated in Fig. 2.2.

There is only one conduction path needed so that the parasitic capacitances between the local supply and the local environment have only a minor impact. Since the power required for the communication is taken directly from the network, there is comparably a lower amount of power required from the local supply reservoir, which can reduce the demand on decoupling and filtering of the local supply. Only the power for driving the load modulation is necessary, which can be beneficial for e.g. sensor nodes that requires a clean power supply. In this work, a capacitive load modulation approach is proposed and will further be discussed in Chapter 3.

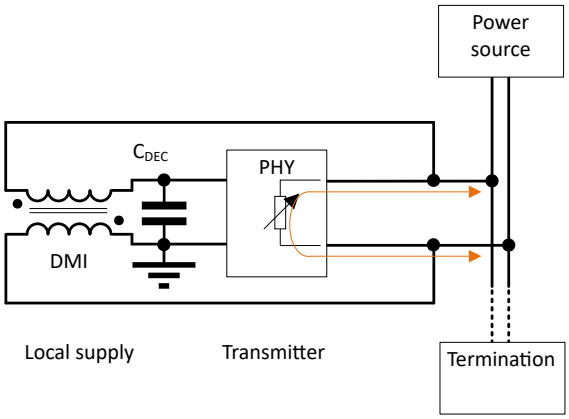


Figure 2.2: Signal path in a load modulating transmitter

2.2 Bus model

In differential networks such as CAN and PoX, twisted pair cables are used. They are mostly implemented as unshielded version. For the investigations in this work, it is essential to build a model, which can be used for further analysis and simulations. The following section is describing the theoretical calculation method based on physical properties of UTPs. A verification based on measurement will verify the theoretical assumptions.

2.2.1 Transmission line model

From the telegrapher's equations, it is known that a transmission line can be modeled by an equivalent RLGC circuit per unit length. Fig. 2.3 shows the physical representation in the upper part and the equivalent single-ended and differential circuit in the middle and the lower part, respectively. The complete model, over a wire length l, can be seen as a series of subsequent RLGC circuits. With an increasing number of elements per wire length, the model will become closer to the real behaviour.

The characteristic impedance Z_C of a lossy transmission line can be expressed as

$$Z_C = \sqrt{\frac{R'(\omega) + j\omega L'(\omega)}{G'(\omega) + j\omega C'(\omega)}}\,. \tag{2.2}$$

There is a dependency on ω due to e.g. the skin and proximity effects in the conductor. These 2$^{\text{nd}}$ order effects are not considered here because they become relevant at much higher frequencies than considered in this work. From Lefferson [17] it is known that the characteristic impedance of two parallel wires can be expressed as

$$Z_C = \frac{Z_{FS}}{\pi\sqrt{\varepsilon_{eq}}}\, cosh^{-1}\left(\frac{D}{d}\right), \tag{2.3}$$

where Z_{FS} represents the impedance of free space which is 377Ω, ε_{eq} the equivalent dielectric constant, D and d are the spacing between the wire centres and the diameter of the wire without coating, respectively.

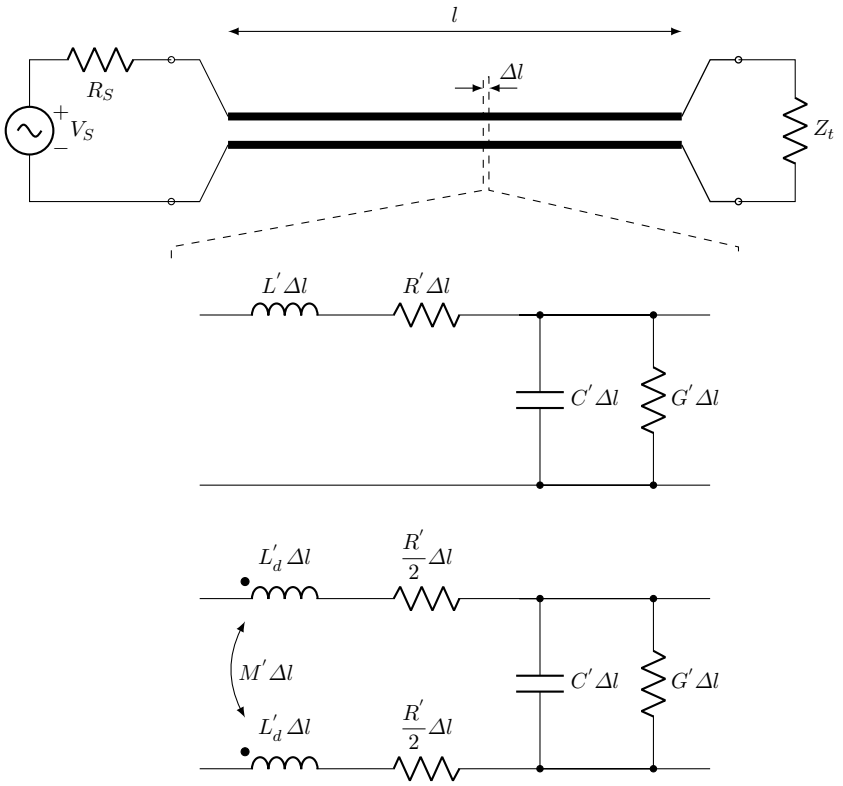


Figure 2.3: Transmission line model

The equivalent dielectric constant can be determined from the electro-magnetic propagation speed v_{TP} of the twisted pair cable, that includes twisting and the coating properties, in comparison to the electro-magnetic propagation velocity in vacuum c_0.

$$\sqrt{\varepsilon_{eq}} = \frac{c_0}{v_{TP}} \tag{2.4}$$

However, the effective length of a wire is increased by the twisting. A length factor (LF) can be used to correct this influence for further calculation of the RLGC elements with the number of twists per unit length n'_{tw}:

$$LF = \sqrt{1 + (n'_{tw}\,\pi\,D)^2}\,. \tag{2.5}$$

With this, the equivalent elements $R^{'}$, $L^{'}$, $G^{'}$ and $C^{'}$ can be calculated for the single-ended model [18]:

$$R^{'} = \frac{8\,LF}{\pi\,d^2\,\sigma_{cu}} \tag{2.6}$$

$$L^{'} = \frac{\mu_0\,\mu_{r_{cu}}\,LF}{\pi}\;cosh^{-1}\left(\frac{D}{d}\right) \tag{2.7}$$

$$C^{'} = \frac{\pi\,\varepsilon_{eq}\,LF}{\mu_0\,c_0^2\,cosh^{-1}\left(\frac{D}{d}\right)} \tag{2.8}$$

$$G^{'} = \frac{\pi\,\sigma_d\,LF}{cosh^{-1}\left(\frac{D}{d}\right)} \tag{2.9}$$

Since the conductivity of the dielectric is very low, $G^{'}$ becomes very low, e.g. σ_d of polytetrafluoroethylene (PTFE) is $\approx 10^{-21} S/m$. In the frequency range below $1GHz$, the conductive portion $G^{'}$ is therefore be assumed as negligible and is not considered further for the model. The coupled inductor in the differential model shown in the lower part of Fig. 2.3, can further be determined by knowing the coupling factor k between the two wires.

$$L^{'} = 2L_d^{'} - 2M_d^{'} = 2L_d^{'}\,(1-k) \tag{2.10}$$

$$L_d^{'} = \frac{L^{'}}{2(1-k)} \tag{2.11}$$

2.2.2 Extraction

A twisted pair cable (*VW 000 979 987*) with a length of $10m$ was analysed. The cable was reeled on plastic pipe with a diameter of $160mm$ and a length of $0.6m$. To avoid coupling between the windings, the turns were separated by $\approx 25mm$. With an LCR meter the coupling factor, the DC-resistance and the propagation delay could be measured, which is listed together with the geometrical parameters in Table 2.1.

Table 2.1: Measured parameter of the UTP cable *VW 000 979 987*

Parameter	Symbol	Value	Unit
Effective wire diameter	d	0.6614	mm
Wire spacing	D	1.25	mm
No. of twists	$n_{tw}^{'}$	50	m^{-1}
Loop DC-resistance	$R^{'}$	0.106	Ω/m
Propagation delay	$t_{d_{TP}}$	5.2	ns/m
Coupling factor	k	0.62	-

The effective diameter of the wire is calculated from the effective cross-section of the wire, which contains 7 strands, each with a diameter of $0.25mm$. Using Eqs. 2.3 to 2.11 yield to the cable parameters, listed in Table 2.2. For further investigations and simulations, a scalable balanced model has been created based on the extracted parameters as depicted in Fig. 2.7. The model is using Verilog-A and has up to 32 RLC segments over the length parameter.

Table 2.2: Calculated parameter of the UTP cable *VW 000 979 987*

Symbol	Value	Unit
LF	1.0191	-
v_{TP}	195.98×10^{6}	m/s
ε_{eq}	2.3389	-
Z_C	98.2	Ω
$R^{'}$	0.1059	Ω/m
$C^{'}$	53.03	pF/m
$L^{'}$	509.9	nH/m
$L_d^{'}$	670.9	nH/m
$M^{'}$	416.0	nH/m

Furthermore, the 10m UTP cable setup has been measured with a network analyser, as shown in Fig. 2.4. A translation from S-parameter to RLGC transmission line parameters was done with the function *s2lrgc* of the RF-toolbox of MATLAB. The extracted cable characteristics and well as the measured RLGC elements, are depicted in Fig. 2.5 and 2.6. It should be noted that the resonance frequency of this setup was observed around $8MHz$. Therefore, the parameters at lower frequencies than $8MHz$ indicates $Z_C \approx 100\Omega$, $C^{'} \approx 54pF/m$ and $L^{'} \approx 496nH/m$. The DC value of $R^{'} \approx 70m\Omega/m$ is observable. Overall, the measured parameters fit well to the calculated ones so that the model can be used for simulations. Fig. 2.7 show the balanced model of the UTP cable.

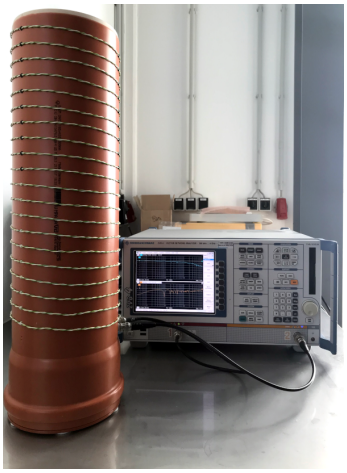


Figure 2.4: Setup for measurement of the $10m$ UTP cable

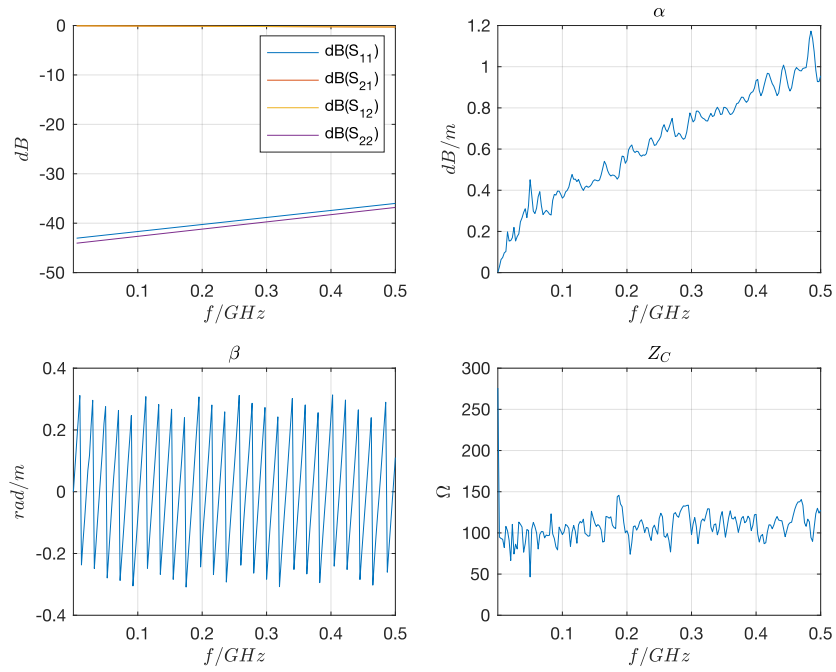


Figure 2.5: Extracted cable characteristics from S-parameter measurement

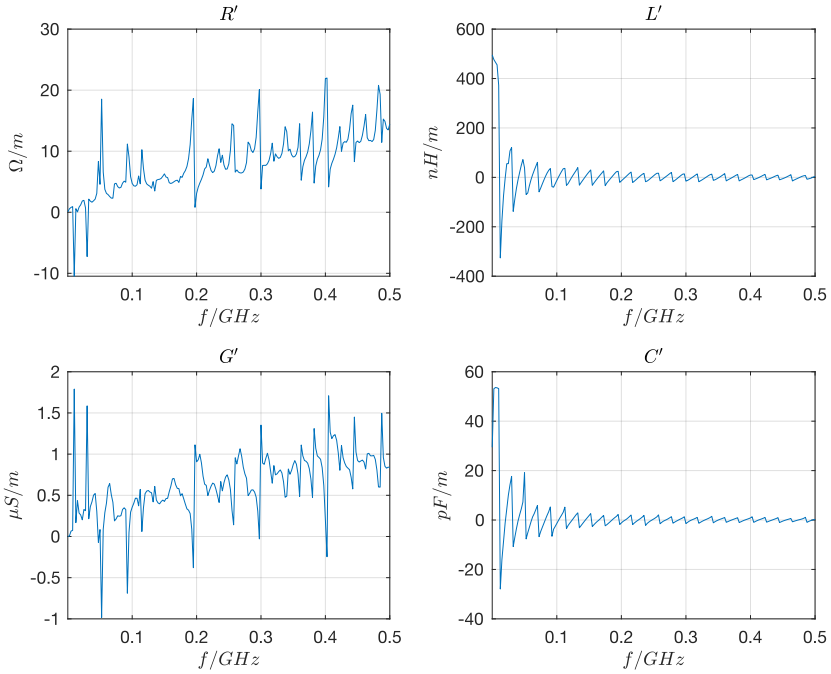


Figure 2.6: Extracted RLGC characteristics from S-parameter measurement

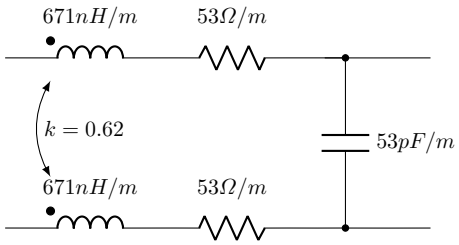


Figure 2.7: RLC-model of the twisted pair cable *VW 000 979 987*

CHAPTER 3

Baseband switched-capacitor modulation concept

As discussed in Section 2.1, a load modulation principle is developed in this work, which is based on the switched-capacitor principle. A coupling feed between the power source and the network is required to separate the supply from the communication channel [19]. The local supply of the nodes is taken from the bus, so that a coupling feed is also required here to satisfy Eq. 2.1, and to ensure that the network impedance in the communication channel frequency range is dominated by the characteristic impedance Z_C of the transmission line. There are two main principles investigated and compared with a classical resistive load modulation at the end of this chapter.

3.1 Principle

A capacitor C_S containing an initial charge Q_{C_S} is connected to the terminated transmission line by a switch with the finite resistance R_{sw}. At the connection point, there is also a parallel capacitor C_S associated with the physical implementation aspects, as indicated in Fig. 3.1.

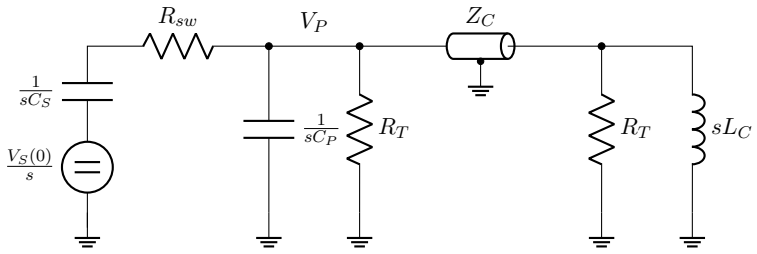


Figure 3.1: Equivalent s-domain model of the charge transfer

Under matched conditions (R_T=Z_C), and assuming a sufficiently high coupling inductance ($X_{L_C} >> |Z_C|$), the s-domain equation can be expressed as

$$\frac{V_P(s)}{V_S(s)} = \frac{C_S\,R_T}{s^2 C_S C_P R_T R_{sw} + s\left[C_S\left(2R_{sw}+R_T\right)+C_P R_T\right]+2}\,. \tag{3.1}$$

Because of the linear circuit, V_S can be set unity to obtain V_P in relation to the constant V_S. The time-domain solution can be calculated by the inverse Laplace transform, yielding to

$$V_P(t) \;=\; \mathcal{L}^{-1}\{V_P(s)\} \;=\; V_{peak}\left(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}\right), \tag{3.2}$$

whereas τ_r and τ_f represent rising and falling time constants, respectively. The peak voltage yield to

$$V_{peak} = \frac{Q_{C_S} R_T}{\kappa} \approx \frac{Q_{C_S} R_T}{C_P R_T + C_S\left(2R_{sw} + R_T\right)}, \tag{3.3}$$

with

$$\kappa = \sqrt{\left(C_P R_T + C_S\left(2R_{sw} + R_T\right)\right)^2 - 8\, C_S C_P R_{sw} R_T}\,. \tag{3.4}$$

Using a non-zero switch on resistance R_{sw} and parallel capacitor C_P, rising and falling time constants $\tau_{r,f}$ yield to

$$\tau_{r,f} = \frac{2C_S C_P R_{sw} R_T}{C_P R_T + C_S\left(2R_{sw} + R_T\right) \pm \kappa}\,. \tag{3.5}$$

A significantly lower parallel capacitor than the charging capacitor, yield to the approximation for the falling time constant

$$\tau_f \approx C_S\left(R_{sw} + \frac{R_T}{2}\right), \forall C_P \ll C_S\,. \tag{3.6}$$

A representative pulse waveform in time log-scale, for $V_{C_S}(0) = 1V$, C_S= $1nF$, C_P= $10pF$, R_{sw}= 10Ω and R_T= 100Ω is shown in Fig. 3.2 in comparison to a transient circuit simulation using the built-in transmission line model of the *QucsStudio* simulator [20], where an AWG22 UTP cable ($l = 5m, Z_C = 100\Omega$) and an inductive feed L_C is added. It shows a good conformity. However, the main difference located in the subside phase is introduced by the finite coupling inductance. This usually lead to a data dependent base-line wander, which has a low frequency component that can easily be removed by high-pass filtering at the receiver.

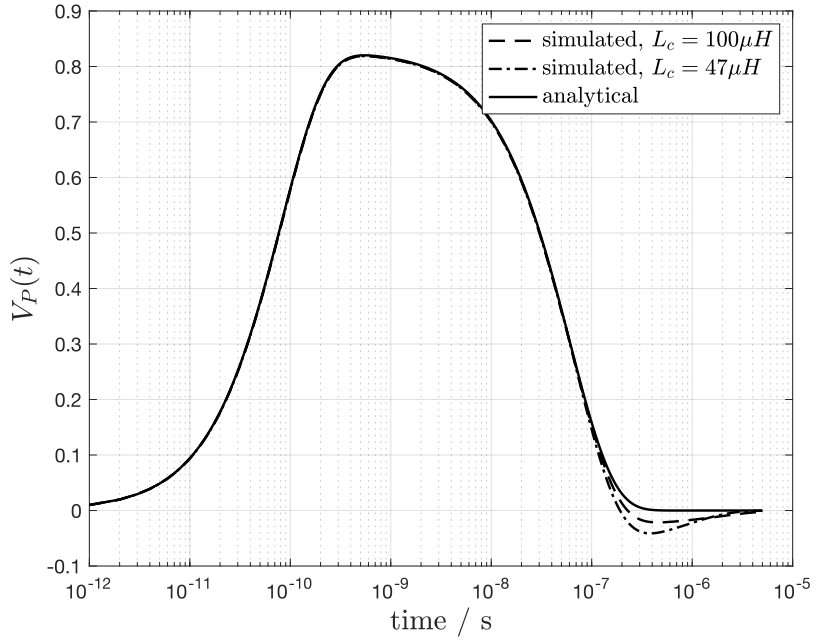


Figure 3.2: Pulse waveform in log time scale

3.2 Charge alternation approach

In the charge alternation (CA) implementation, the capacitor C_S is temporarily connected to the transmission line, which contains a non-zero DC component V_B to supply the nodes in the network. As soon as the charge Q_{C_S} reaches the level of $C_S \times V_B$, the connection is open to unload the network so that other subscribers can subsequently participate in the communication. Meanwhile, the charge of C_S is preserved for a next pulse transmission, which is initiated by connecting C_S to the transmission line but now with opposite polarity. In this way, except for the very first connection, the charge Q_{C_S} alternates, i.e.

$$Q_{C_{s_{n+1}}} = -Q_{C_{s_n}} \, . \tag{3.7}$$

In Fig. 3.3 the approach is depicted. The DC power supply is differentially coupled to the terminals of the transmission line BH and BL, by two DC-feed inductors L_C, which are bypassed by $R_T/2$ to produce a match to the line impedance. The transmission line is symmetrically terminated using an AC-coupling capacitor C_C in series to two $R_T/2$ connected to the ends of the transmission line.

During a transmission, the incoming data sequence is encoded in terms of pulses to be sent. After each pulse, the next charge state is alternated. This is done by simultaneously switching S_1 and S_4, as well as S_2 and S_3. It is essential that the on-state of the two

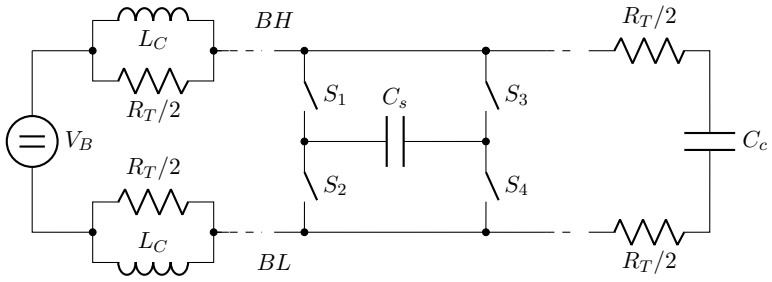


Figure 3.3: CA principle applied to a differential network

switch groups are non-overlapping, to avoid short currents paths. Therefore, an open state is introduced between two charging states, as summarized in Table 3.1. Consequently, the charging time constant should allow that the steady-state of the charge Q_{C_S} is reached sufficiently before the next charging state starts, to ensure sufficient time for an 'open' state.

Table 3.1: States of the CA approach

State	S_1, S_4	S_2, S_3	Description
Open	Open	Open	C_s not connected to the bus, charges are preserved
CHG 1-4	Close	Open	charge accumulated during CHG 2-3 phase is recharged to V_B level
CHG 2-3	Open	Close	charge accumulated during CHG 1-4 phase is recharged to $-V_B$ level

A direct data encoding to pulses leads to an ambiguity on the receiver side since falling or rising edges of the data signal cannot be distinguished as shown in Fig. 3.4. Hence, for an uncoded data stream applied to the TX, the protocol frame structure needs to be considered so that a message header like in [11] can be used to assign the correct data polarity. But the simplest encoding to resolve the ambiguity is to encode the data as unipolar return-to-zero (URZ) stream [21] as shown in Fig. 3.5. Here the polarity of the data is unambiguous.

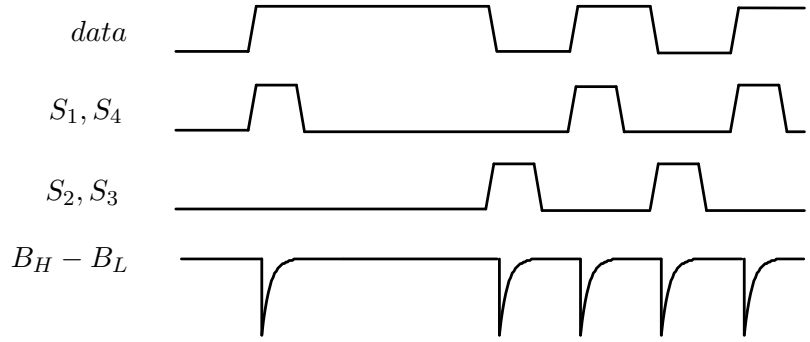


Figure 3.4: Transmission waveform of the CA approach, edge encoding

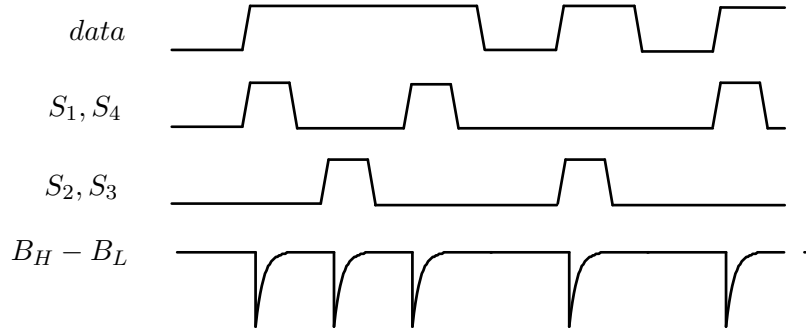


Figure 3.5: Transmission waveform of the CA approach, URZ encoding

3.3 Charge pump approach

Another switched-capacitor principle, which is applicable, is the charge pump (CP) approach. Here two equal capacitors $C_{S_{1/2}}$ are simultaneously connected to the bus, as indicated in Fig. 3.6, C_{S_1} by the switch S_1 to BH and C_{S_2} by S_2 to BL until a charge of $2C_S \times V_B$ is reached.

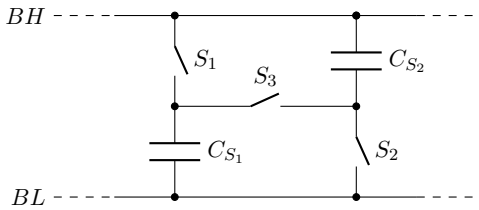


Figure 3.6: Network node using the CP principle

Afterwards, and similar to the principle described in Section 3.2, the capacitors are disconnected while the charges are preserved. In a next phase, the capacitors are discharged over the bus by connecting both capacitors in series by the switch S_3 until the overall charge reduces to $\frac{1}{2}C_S \times V_B$, which is the initial condition for the subsequent charging.

As a result of the CP sequence listed in Table 3.2 and shown in Fig. 3.7, positive and negative pulses are applied to the transmission line, which can be used to unambiguously extract the original data stream. Since the coding indicates the transition in the digital information, it is called Dicode [21].

Table 3.2: States of the CP approach

State	S_1, S_2	S_3	Description
Open	Open	Open	C_{S_1}, C_{S_2} not connected to the bus, charges are preserved;
CHG	Close	Open	C_{S_1} and C_{S_2} are connected in parallel to the bus an charged to V_B level
DIS	Open	Close	C_{S_1} and C_{S_2} discharged in series to $V_B/2$

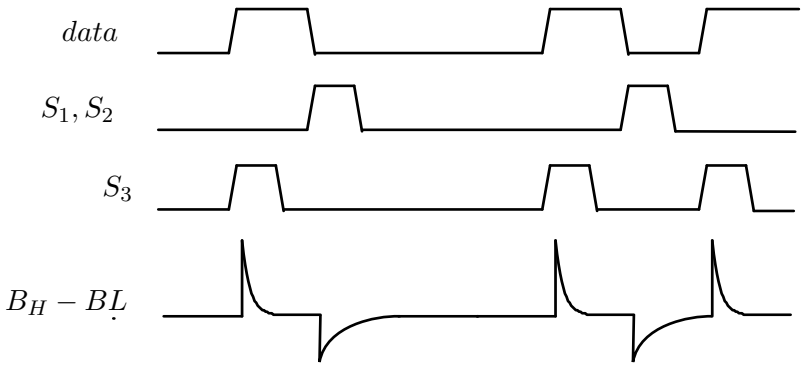


Figure 3.7: Transmission waveform of the CP approach, Dicode

Due to the change between parallel and series connection of $C_{S_{1,2}}$ the charge balance over one cycle yields to

$$Q_{C_{S_{CHG}}} = 2Q_{C_{S_{DIS}}}\,, \tag{3.8}$$

because of the charge transitions

$$\rightarrow \quad Q_{C_{S_{CHG\_end}}} = 2C_S V_B \quad \rightarrow \quad Q_{C_{S_{DIS\_start}}} = C_S V_B \tag{3.9}$$

and,

$$\rightarrow \quad Q_{C_{S_{DIS\_end}}} = \frac{1}{2} C_S V_B \quad \rightarrow \quad Q_{C_{S_{CHG\_start}}} = C_S V_B\,. \tag{3.10}$$

While in the CA principle, the peak voltage of the pulses is constant, it differs between

the charge and discharge in the CP approach by

$$\left|\frac{V_{peak_{CHG}}}{V_{peak_{DIS}}}\right| \approx \frac{2C_P R_T + C_S(2R_{sw} + R_T)}{C_P R_T + 2C_S(2R_{sw} + R_T)} \gtrsim \frac{1}{2}\,, \tag{3.11}$$

because of the initial level of C_S of $V_B/2$ and $2V_B$ in charge and discharge mode, respectively. Likewise, the time constants differ and assuming C_S dominates the capacitances, the relation of the falling time constants is $\tau_{f_{CHG}} \approx 4\tau_{f_{DIS}}$.

3.4 Energy balance

To compare the approaches energy-wise, a first view on a simple resistive load modulation gives a benchmark. According Fig. 3.8, both network terminations are merged into two $R_T/4$ in series to the load modulator.

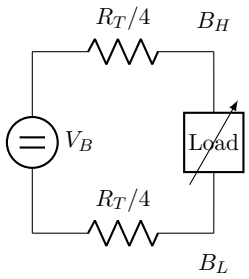


Figure 3.8: Equivalent circuit for load modulation

Assuming that the load modulator varies the load between an 'open' and R_M, the differential AC-amplitude and the average power yield to

$$v_{amp} = V_B \left(1 - \frac{R_M}{R_M + \frac{R_T}{2}}\right) \tag{3.12}$$

and,

$$\overline{P}_{RES} = \overline{m}_{code}\; dc_{msg} \frac{V_B^2}{R_M + \frac{R_T}{2}}\,, \tag{3.13}$$

where $\overline{m}_{code}$ represents the mean value of the data signal, and dc_{msg} the duty-cyle of the messages. Usually, a uniform distribution between '0' and '1' can be assumed ($\overline{m}_{code} = 0.5$), which is used for comparisons here. For the duty-cycle, it assumes a constant message stream, so that $dc_{msg} = 1$. For example, with $V_B = 12V$, $R_T = 100\Omega$, $R_M = 100\Omega$, the

differential AC-amplitude is $4V$ and an average power of $480mW$ is consumed. This is independent of the data rate DR.

In case of the CA approach, the average current consumption due to the charge alternation taking Eq. 3.7 into account, yield to

$$\overline{I}_{CA} = Q_{CA}\,\overline{m}_{code}\,dc_{msg}\,DR \;=\; 2C_S V_B\,\overline{m}_{code}\,dc_{msg}\,DR\,. \tag{3.14}$$

The average power consumption is then

$$\overline{P}_{CA} = \overline{I}_{CA}\left(\frac{R_T\,\overline{I}_{CA}}{2} + V_B\right). \tag{3.15}$$

In the CP approach the charge is partially reused, so that with using Eq. 3.9 and 3.10

$$Q_{C_{CP}} = Q_{C_{S_{CHG\_end}}} - Q_{C_{S_{CHG\_start}}} + Q_{C_{S_{DIS\_end}}} - Q_{C_{S_{DIS\_start}}} = \frac{1}{2}C_S V_B\,. \tag{3.16}$$

Due to the fact, that a bit is encoded with its start and end, further reduces compared to Eq. 3.14 by a factor of two. As a result, the average current consumption yields to

$$\overline{I}_{CP} = \frac{1}{2}Q_{CP}\,\overline{m}_{code}\,dc_{msg}\,DR \;=\; \frac{1}{4}C_S V_B\,\overline{m}_{code}\,dc_{msg}\,DR\,, \tag{3.17}$$

which is eight times less than in CA mode. Similar to Eq. 3.15, the power consumption is then

$$\overline{P}_{CP} = \overline{I}_{CP}\left(\frac{R_T\,\overline{I}_{CP}}{2} + V_B\right). \tag{3.18}$$

Comparing it to the initial example of the resistive load modulation, shows a considerable energy saving potential, as listed in Table 3.3. It is taking, in addition to the previous example, $C_S = 820pF$ and $DR = 2Mbps$ into account. The achievable amplitudes are similar.

Table 3.3: Comparison of consumptions

Item	resistive	CA-mode	CP-mode	Unit
Current consumption	80	19.7	2.46	mA
	100	24.6	3.1	%
Power consumption	480.0	255.5	29.8	mW
	100	53.2	6.2	%
Energy per bit	240.0	127.5	14.9	nJ

Although the CP approach needs two capacitors, it outperforms in terms of energy

budget. I will be described in Section 5.1, that the CP approach has also benefits for the protection scheme.

3.5 Proposed implementation and specifications

From the previous analysis it can be concluded that the concept should be investigated as a demonstrator using off-the-shelf components, and in parallel an integration to a semiconductor process. The target data rate should be 2Mbps, but also the capability to address higher data rates could be beneficial. To reach the steady-state for charging the capacitor(s), with a reasonable time for an open state in between the charging states, it is useful to consider $\tau_f \approx 0.1$ to $0.15\,DR^{-1}$. According to Eq. 3.5 and 3.6, the R_{sw} should be ≈ 10 to 30Ω to keep the termination resistance dominant. In this way, the device dependencies of the switches are less contributing. On the other hand, a low R_{on} of the switches will also lead to a higher area of the switch transistor, and thus to higher parasitics that could increase the power consumption unnecessarily. Therefore, a good balance needs to be found.

CHAPTER 4

Demonstrator

In order to confirm the investigations of the operating principle for the CA and CP transmission schemes, a breadboard demonstrator was built using off-the-shelf components. The top-level schematic of the demonstrator is shown in Fig. 4.1. It consists of five sub-blocks:

- a local supply, that provides the necessary supply levels for the other sub-blocks, while taking the raw supply from either a universal serial bus (USB) port or from dedicated lab equipment,
- a transmitter which contains the switching elements for realizing both transmission schemes,
- a receiver that provides a reception path and a level comparator for 2-level discriminating the received signal,
- an analog-to-digital converter (ADC) section, which converts the analog received and conditioned signal to the digital domain,
- and a 3^{rd} party FPGA board for the digital signal processing.

The demonstrator can be configured as a master network node that injects the supply on the bus using the connector *J3*. It can also be configured as a slave node, that extracts the local supply from the bus. A UART connector, *J6*, connects the demonstrator to external master and slave devices which are providing the protocol layer. With *J4* and *J5*, the supply-embedded data lines from preceding and subsequent nodes are connected. An image of the populated demonstrator printed circuit board (PCB) in shown in Fig. 4.2. Receiver and ADC sections are located below the field-programmable gate array (FPGA) daughter board.

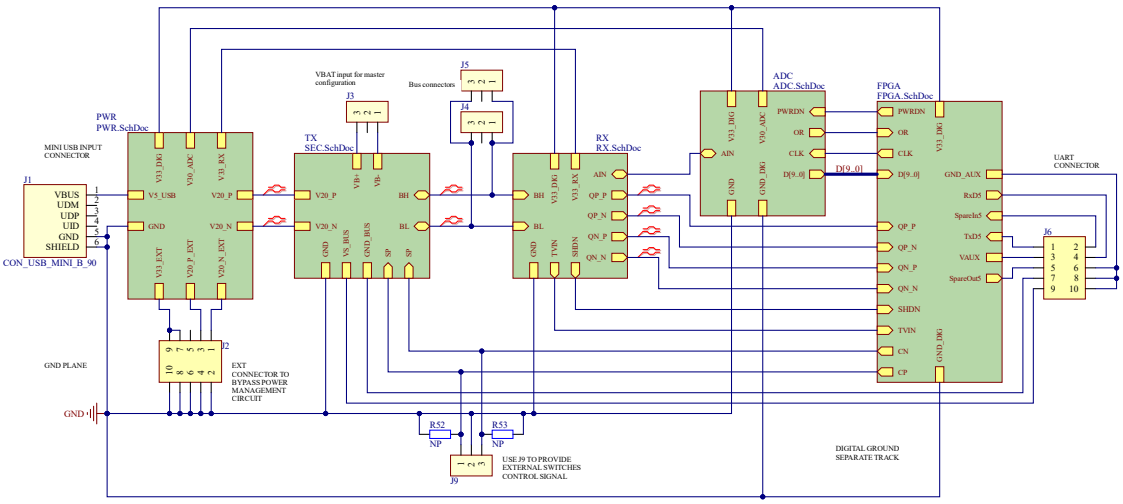


Figure 4.1: Top-level schematic of the demonstrator

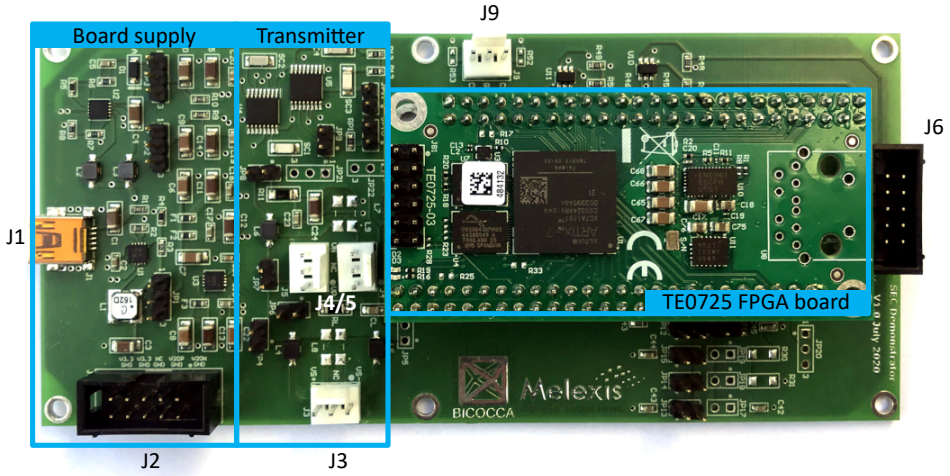


Figure 4.2: Demonstrator PCB

4.1 Supply

The external USB connector provides a raw $5V$ supply, from which the first local $3.3V$ supply is generated by the synchronous step-down DC/DC converter ADP2119 from Analog Devices [22]. As shown in Fig. 4.3, this $3.3V$ supply is further be used for the digital, the receiver, and the ADC sub-blocks. Each branch is decoupled by a ferrite pearl-based filter to suppress the noise induced by the DC/DC converter. The supply for the ADC is further regulated to $3.0V$ by the linear regulator ADM7170 [23], to be compliant to the ADC specifications. Since the transmitter switches need to be supplied beyond the level of the bus DC voltage V_B, a dual DC/DC converter LT3463 [24] is providing $\pm 20V$. After

filtering, it is delivered to the transmitter sub-block. Optionally, the main $3.3V$ supply and the dual $\pm 20V$ supply can be provided from external sources.

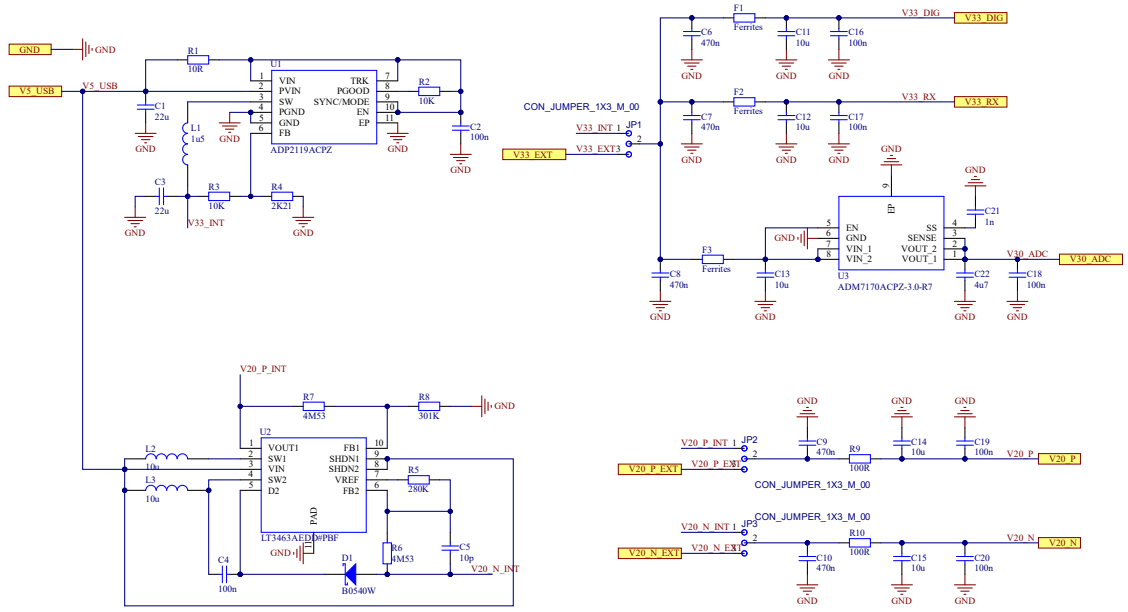


Figure 4.3: Supply schematic of the demonstrator

4.2 Transmitter

The transmitter sub-block realizes the CA and CP modes by jumper (JP) configurations. Each scheme is implemented by a separate single-pole/single-throw (SPST) quad switch ADG5413 [25] using the dual supply of $\pm 20V$ provided by the supply sub-block. There are two switch control signals coming from the $3.3V$ domain of the FPGA, SP and SN, to control the switch states. Herein, SP controls S_1, S_4 in CA mode and S_1, S_2 in CP mode, while SN controls S_2, S_3 in CA mode and S_3 in CP mode. According to [25], the R_{on} of the switches is $\approx 10\Omega$. By setting JP21/22 to 1-2, the CA mode is selected and by a 2-3 setting the demonstrator is operating in CP mode. Since digital inputs of the ADG5413 allows a minimum high-level of $2V$, the high-active control signals SP and SN are directly be driven by the $3.3V$ voltage domain of the FPGA sub-block. It is ensured by the digital circuit, realized in the FPGA, that these control signals are non-overlapping. This avoids short currents between BH and BL, which would be caused by a simultaneous turn-on of S_1-S_2, S_3-S_4 during CA mode or S_1-S_2-S_3 during CP mode. That is also important during the start-up of the demonstrator. In case the control signals are in a high-impedance (Hi-Z) state, a pull-down resistor is added to each control input as shown in Fig. 4.1, to safely turn off all switches.

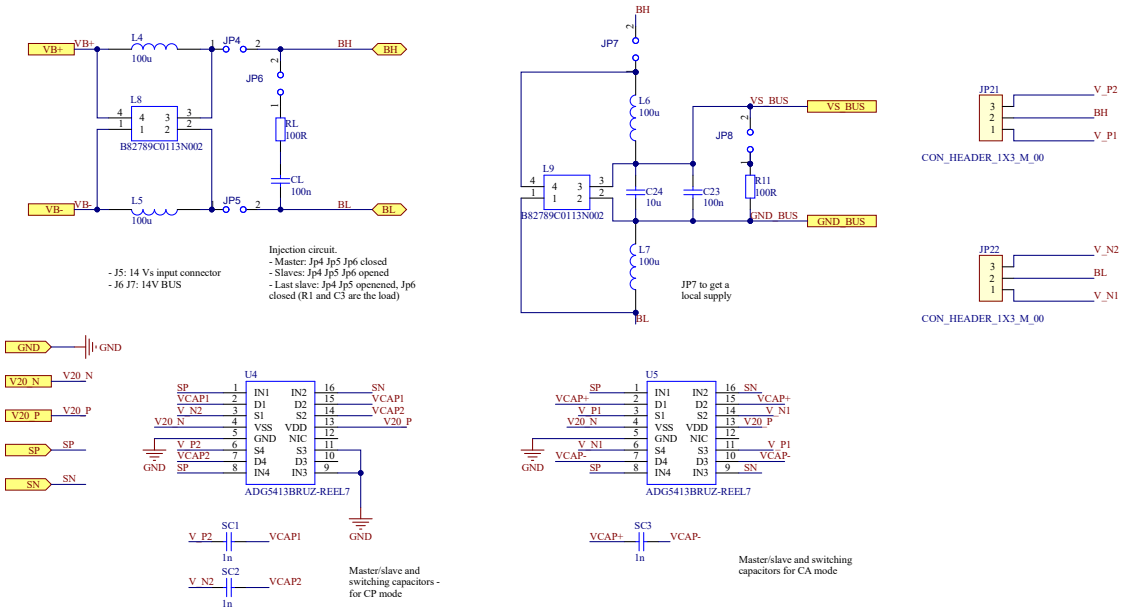


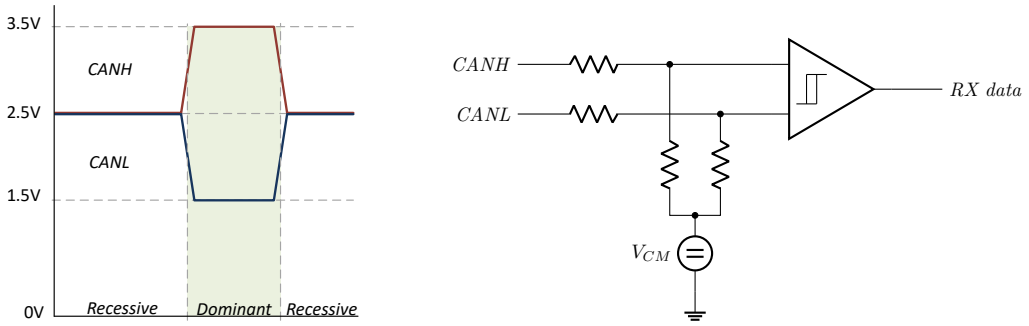
Figure 4.4: Transmitter schematic of the demonstrator

4.3 Receiver

In order to decode the data reliably, a reception chain needs to extract the differential data signal from the bus lines. In a CAN bus implementation, the bus lines *CANH* and *CANL* have a typical common level of $2.5V$ in the *recessive* state. In the CAN PHY, this is a non-active modulation state, where network subscribers can start a *dominant* modulation state by actively driving *CANH* and *CANL* to $3.5V$ and $1.5V$, respectively. An example waveform is depicted in Fig. 4.5(a). Typically, the reception of a differential CAN signal is implemented by a symmetric resistive divider, where the centre tap is connected to the common level of $2.5V$, and hence all network subscribers realize the level of $2.5V$ in the *recessive* modulation state. The differential resistance between *CANH* and *CANL*, specified by the standard [13] should be between $12k\Omega$ and $100k\Omega$. Fig. 4.5(b) illustrates the principle of the CAN receiver. An attenuation before a comparator discriminates the data signal set by divider-ratio between outer and inner resistors.

In case of the proposed switched-capacitor modulation scheme, the CAN receiver can support the CA mode only, but preferably with two separate comparators, related to *BH* and *BL*, respectively. This is because the differential modulation signal might always have an offset $V_{B_H} - V_{B_L} > 0$.

In order to address both modulation schemes with a signal reception chain, a capacitive coupling is proposed. Since the target data rate is $> 1Mbps$, the coupling capacitors might be area-wise not an issue for an integrated solution. Fig. 4.6 depicts the receiver sub-block



(a) CAN signal waveform **(b)** Basic CAN receiver

Figure 4.5: CAN bus signal reception

of the demonstrator. It is implemented by an AC-coupled differential amplifier topology using a 4GHz bandwidth operational amplifier LTC6268-10 [26]. Since the differential input signal is in the range of several volts, a gain of $-20dB$ is implemented, so that the output signal for the discrimination is $|V_O| < 1V$. Due to the AC-coupling at the input and output of the differential amplifier, two high-pass corner frequencies are present:

$$f_{HP_1} \approx \frac{1}{2\pi\, R_1\, C_1} = 1.42kHz \tag{4.1}$$

and,

$$f_{HP_2} \approx \frac{1}{2\pi\, \frac{R_{23}R_{24}}{R_{23}+R_{24}}\, C_4} = 37kHz\,. \tag{4.2}$$

According to [26], a pole formed by the parasitic input capacitance C_{IN} and the feedback resistor R_{FB}, which limits the achievable bandwidth to

$$f_{BW} \approx \sqrt{\frac{GWB}{2\pi\, R_{FB}\, C_{IN}}}\,, \tag{4.3}$$

where GBW denotes the gain-bandwidth product of the operational amplifier. To limit the contribution of the AC-coupling capacitors to C_{IN}, the parallel resistors R_6 and R_7 are added to the amplified inputs. The positive input of the amplifier R_5 provides a bias path to the positive supply. In the pass-band region, the output voltage of the differential amplifier can be expresses by

$$V_O = V_{B_H}\,\frac{R_2}{R_3}\,\frac{R_P}{R_N} - V_{B_L}\,\frac{R_2}{R_1} + V_{33}\,\frac{R_2}{R_5}\,\frac{R_P}{R_N}\,. \tag{4.4}$$

Whereas R_P, R_N are representing the parallel combination of the resistors on the input

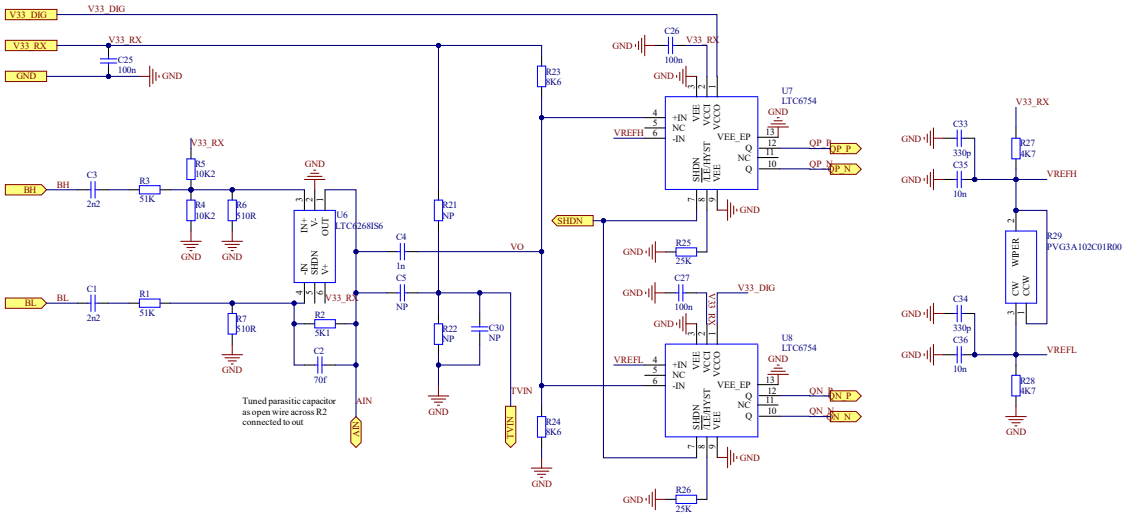


Figure 4.6: Receiver schematic of the demonstrator

terminals of the operational amplifier, i.e.

$$R_P = \left(\frac{1}{R3} + \frac{1}{R4} + \frac{1}{R5} + \frac{1}{R6} \right)^{-1} \tag{4.5}$$

and,

$$R_N = \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R7} \right)^{-1} . \tag{4.6}$$

To avoid a common mode gain, both dynamic factors in Eq. 4.4 need to be matched so that

$$\frac{R_2}{R_3} \frac{R_P}{R_N} = \frac{R_2}{R_1} . \tag{4.7}$$

For the same input impedance on both terminals, R_1 should be equal to R_3. A value of $51k\Omega$ was selected to provide a reasonably high impedance to the network terminals BH and BL. For a gain of $-20dB$ the feedback resistor R_2 must be $5.1k\Omega$ and therefore also the parallel combination $R_4||R_5$, in case $R_6 = R_7$, in order to satisfy Eq. 4.7. In this case, also the DC-term in Eq. 4.4 yields to half of the supply voltage $V33$, thus to the common mode level at the amplifier output. The differential gain of the circuit at this point then simplifies to

$$A_D = \frac{V_{B_H} - V_{B_L}}{V_O} = \frac{R_2}{R_1} . \tag{4.8}$$

As suggested in [26], a feedback capacitor C_{FB} should be applied across the feedback resistor to introduce damping to stabilize the loop gain

$$C_{FB} \geq \sqrt{\frac{C_{IN}}{\pi\, R_{FB}\, GBW}}\,. \tag{4.9}$$

By simulations, the feedback capacitor $C_2 = 65fF$ and $R_6 = R_7 = 510\Omega$ was determined to be optimal for a stable transient operation and for an amplifier bandwidth $f_{BW} \approx 590MHz$. The small feedback capacitor is implemented as a parasitic capacitance formed by a wire across R_2, soldered at the output node of the operational amplifier. This needs to be tuned during setup of the demonstrator board. Fig. 4.7 shows the AC simulation of the differential gain A_D using resistors with a tolerance of 1%.

To estimate the sensitivity to common-mode signals on the bus, the common-mode gain of the amplifier is crucial. Using Eq. 4.4 the common-mode gain can be expressed by assuming that the AC-signals v_{B_H} and v_{B_L} are identical, so that

$$A_{CM} = \frac{v_{B_{H/L}}}{v_O} = \frac{R_2}{R_3}\frac{R_P}{R_N} - \frac{R_2}{R_1}\,, \tag{4.10}$$

which ideally yields zero. However, due to the limited matching of the different resistors, it becomes non-zero. Knowing that the resistor ratio R_2/R_1 adjusts the differential gain A_D, Eq. 4.10 can be re-written to

$$A_{CM} = A_D\left(\frac{R+\Delta R}{R-\Delta R} - \frac{R-\Delta R}{R+\Delta R}\right) = A_D\frac{4\frac{\Delta R}{R}}{1-\left(\frac{\Delta R}{R}\right)^2}\,, \tag{4.11}$$

assuming that all resistors have the same tolerance specification. The common-mode rejection ratio (CMRR) of the circuit, i.e. the suppression of common-mode signals compared to the gain of differential signals, yield to

$$CMRR = \frac{A_D}{A_{CM}} = \frac{1-\left(\frac{\Delta R}{R}\right)^2}{4\frac{\Delta R}{R}}\,. \tag{4.12}$$

With a tolerance $\Delta R/R$ of 1%, the common-mode gain yields to $-48dB$ as the AC simulation shows in Fig. 4.8, that is using all tolerance combinations. Consequently, the CMRR results to $28dB$. Eq. 4.11 assumes an ideal common-mode behaviour of the operational amplifier. The LTC6268-10 offers a high CMRR of typically $80dB$ at frequencies below $100kHz$. However, it degrades with increasing frequency and drops below $30dB$ above $\approx 60MHz$ [26]. As a result, the A_{CM} is dominated by the operational amplifier for frequencies above $\approx 60MHz$, as indicated by Fig. 4.8.

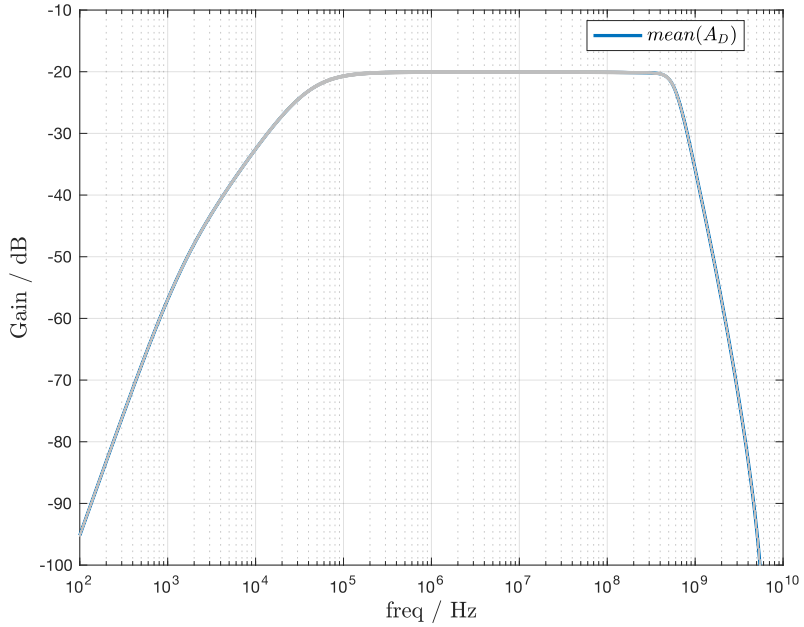


Figure 4.7: Gain A_D of the differential amplifier with 1% resistor matching

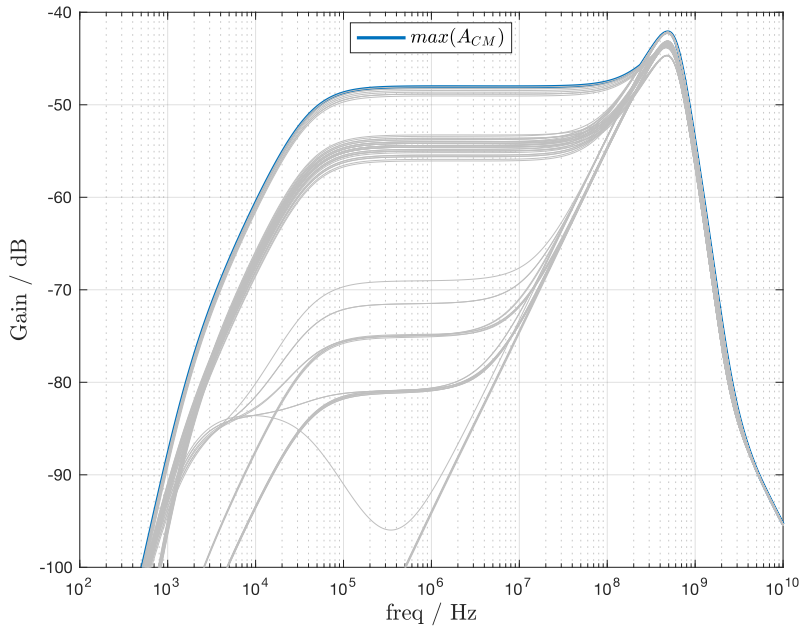


Figure 4.8: Gain A_{CM} of the differential amplifier with 1% resistor matching

The AC-coupled output signal of the amplifier is compared with two thresholds $VREFH$ and $VREFL$ which are derived from an adjustable R-divider formed by $R_{27} - R_{29}$. The thresholds are set to $\pm 120mV$, around the common-mode of $V_{33}/2$. For a fast communication to the digital, each comparator is implemented by a LTC6754 [27], that contains an LVDS output. This is also compliant to the used FPGA and allows low latency. A built-in hysteresis of $40mV$ is used, so that the on-thresholds are finally $\approx \pm 140mV$ and the off-thresholds $\approx \pm 100mV$, around $V_{33}/2$.

4.4 Analog-to-digital converter

As an option, the conditioned received signal can also be converted to digital with a 10bit resolution using the pipe-line ADC AD9214 [28]. It operates from the low-noise $3V$ supply generated by the supply sub-block. The digital outputs are internally level-shifted to the $3.3V$ digital domain. With the $100MHz$ clock provided by the FPGA, a $100Mbps$ conversion is possible due to the pipe-line architecture which requires 5 clock cycles, so that a propagation delay between analog input and digital output is $50ns$. For the antialiasing function, the receiver signal path would need to be reconfigured w.r.t. bandwidth, i.e. by adapting the external elements of the operational amplifier. However, in this demonstrator, the ADC sub-block is considered as an alternative to the proposed receiver implementation using the window comparison described in Section 4.3. It is not being used further in this work.

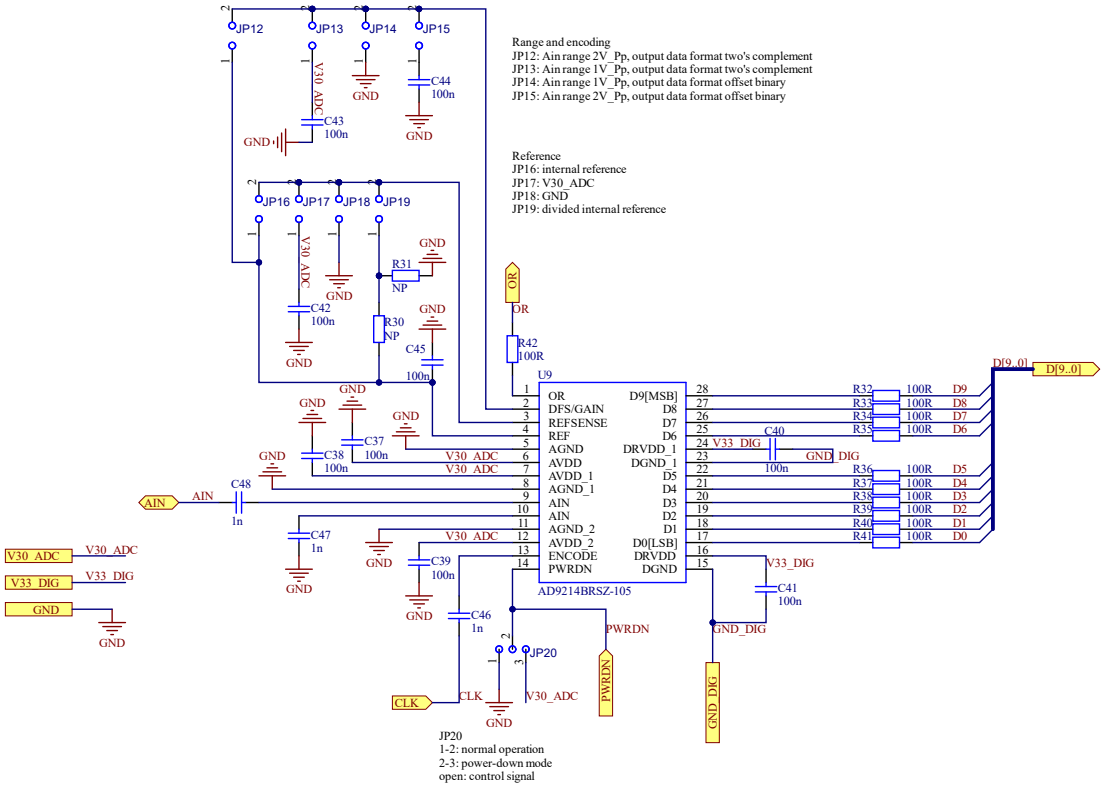


Figure 4.9: ADC schematic of the demonstrator

4.5 Digital Control

For the digital control, the daughter board TE0725 from Trenz [29] that hosts a Xilinx Artix-7 XC7A100T [30], is used. The board provides all digital interfaces to the sub-blocks of the demonstrator. For connecting external master and slave devices, the signals for the universal asynchronous receiver-transmitter (UART) interface, TxD and RxD, are translated from/to the auxiliary supply $VAUX$, which is provided by the external devices and can range from $3V$ to $5.5V$. This level-shift is implemented by buffers with open-drain outputs [31], as shown in Fig. 4.10.

4.5.1 Loop-back

For testing the approaches, a loop-back circuit is implemented in the digital, which is handled as a configuration file that can be uploaded to the FPGA. The block level schematic of the loop-back implementation is depicted in Fig. 4.11. It gets the comparator outputs from the receiver, QP and QN, and synchronize them to the master clock of the FPGA, which has a frequency of $100MHz$. Subsequently, a decoder extracts the data signal, using the information on the data coding scheme and the data rate. The data rate is set up

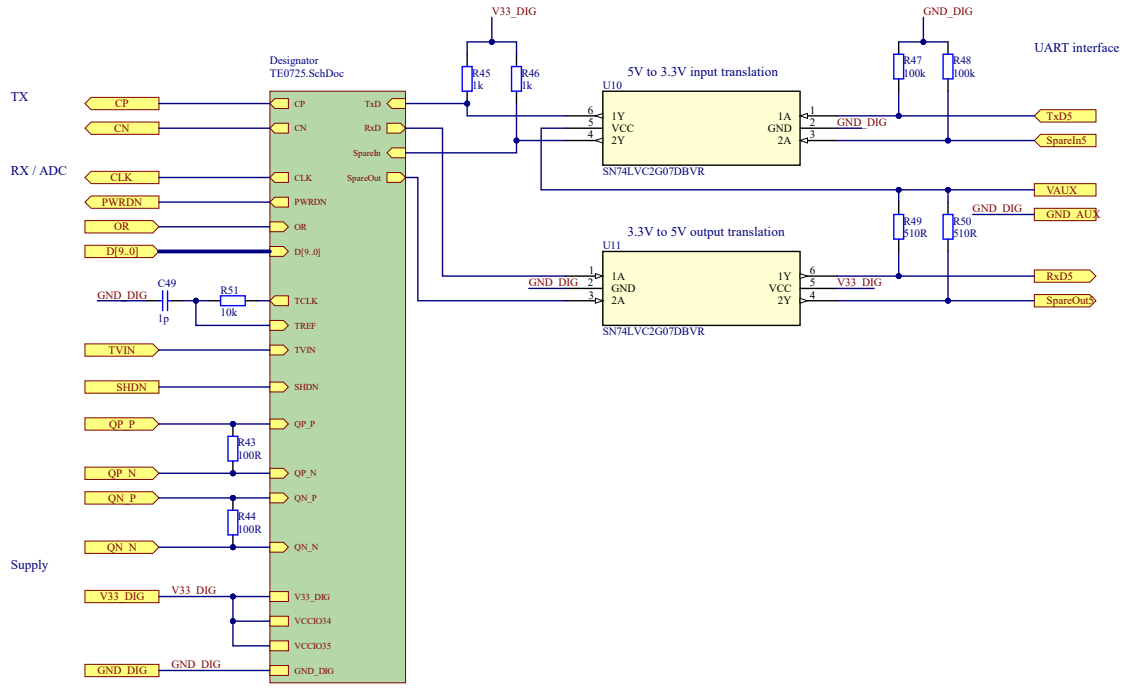


Figure 4.10: FPGA schematic of the demonstrator

as a division of the master clock, e.g. a *DR_DIVIDER* of 50 results in a data rate of $2Mbps$. With *SCHEME*, the coding can be selected according to Table 4.1. The decoded signal is verified by the monitor block, which compares the received and transmitted data stream. In case the error counter overflows, an error flag is set, which is visualized by a light-emitting diode (LED) located on the FPGA board. As a data source, a 9-bit pseudo-random bit stream (PRBS) generator is implemented (PN9). The received data stream and the recovered clock is available at the *Spare_out* and the *RxD* connectors of the UART interface. For more details, the Verilog code of the loop-back implementation can be found in Section A.1.1.

Table 4.1: Coding scheme selection

SCHEME	Description
0	Simple coding for CA mode
1	Direct coding for CP mode
2	Unipolar return-to-zero code (RZ), for CA mode

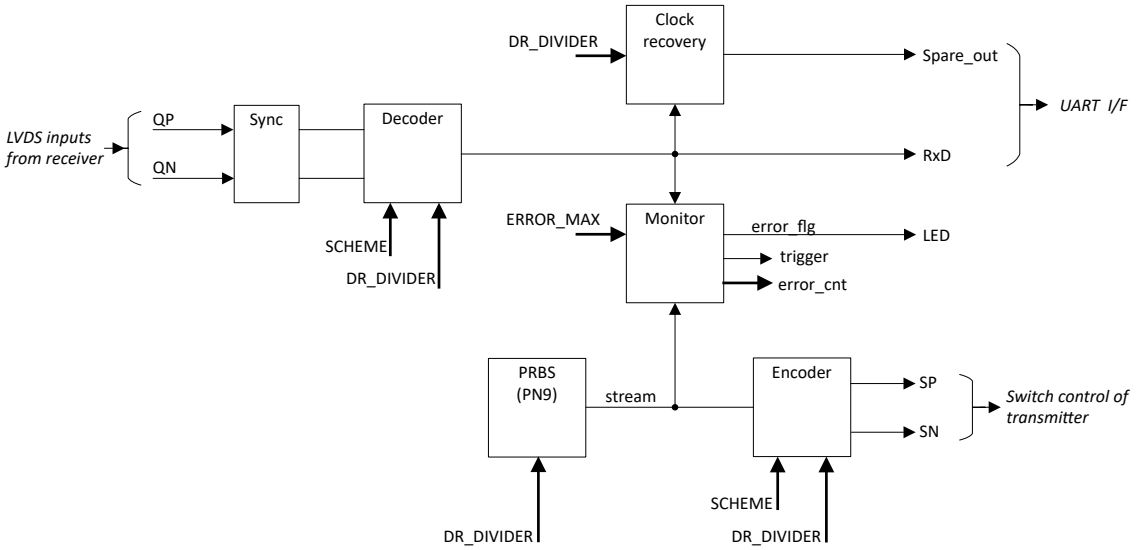


Figure 4.11: Block diagram of the loop-back implementation

4.5.2 Bridge to external devices

In the frame of this work, an already available CAN-like bus implementation [12], named Melexis Light Bus (MeLiBu®), is used as protocol layer. MeLiBu® is incorporating a physical layer similar as used in CAN bus systems. It does not use an arbitration mechanism, where multiple master devices can access the bus simultaneously to prioritize the message [11]. The bridge implementation is shown in 4.12. It receives the data for transmission from the *TxD* input of the UART interface. At first, it will be synchronized to the FPGA clock (*txd_synced*). The data from the bus are conditioned to the *rxd_local* signal in the same way as described in the loop-back implementation (4.5.1). The release of *rxd_local* to output it as *RxD*, as well as start of encoding of *txd_synced*, depends on the direction of the data stream. Otherwise, a loop-back is built because the transmitted data would instantaneously appear in *RxD*. The synchronization is used to identify the intended direction of the data stream because it introduces several clock delays, depending on the number of synchronization taps. In the demonstrator, three taps are used, yielding to a synchronization delay of $30ns$. As a result, it is possible to detect the direction of the data stream by observing if either (*rxd_local*) or (*txd_synced*) changes first. This function is implemented by the director block. For more details, the Verilog code of the loop-back implementation can be found in Section A.1.2.

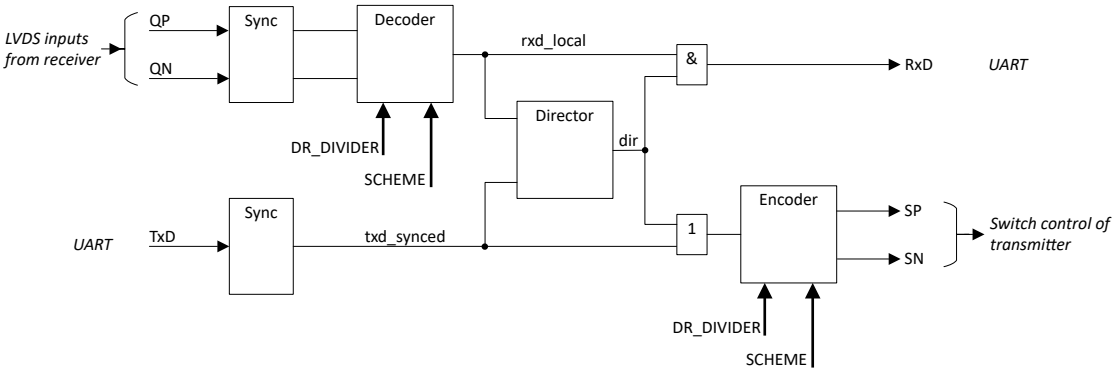


Figure 4.12: Bridge implementation

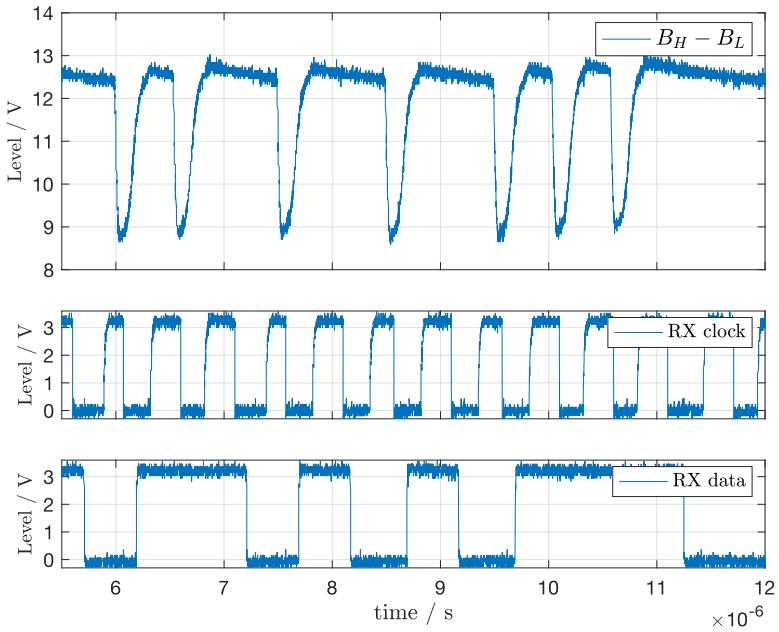
4.6 Results

4.6.1 Loop-back test

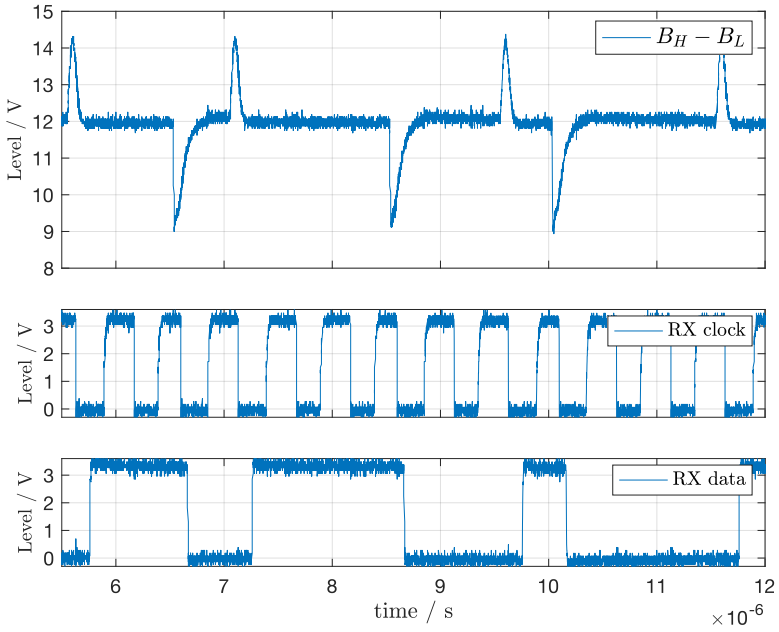
The demonstrator board could successfully be initialized and brought together with the FPGA board. The comparator thresholds *VREFH* and *VREFL* were adjusted for an error-free reception by employing the loop-back implementation from Section 4.5.1. Fig. 4.13 shows the relevant waveforms in case of the $2Mbps$ PRBS data stream. The upper traces depict the differential bus signals that confirms the correct operation of the intended modulation. Decoded data and clock is shown in the lower traces.

4.6.2 Application test

To validate the approaches on application level, an existing LED-strip demonstrator containing 6 RGB-LED driver ICs [32] were used. Each IC can drive four RGB-LEDs and is connected via the MeLiBu® to a controller-based master device, that is further connected to a PC. With the front-end program on the PC, the colour and brightness control for each individual LED is provided. In the experiment, the existing CAN-PHY is replaced by the CA and CP approaches. For this purpose, two demonstrators were configured in the bridge mode with their UART interfaces connected to the LED-strip on one side and to the master device on the other side. A small UART-to-CAN interface board was needed to connect the hardware without modifications. Fig. 4.14 shows the schematic of the experimental setup, and Fig. 4.15 shows an image of the setup in operation. Both communication approaches, CA and CP, could successfully be validated with a communication speed with the existing devices that uses $1Mbps$. Due to the DC loop resistance, resulting out of the wire resistance, and the ESR of the coupling inductors, a voltage drop of max. $2V$ at the slave node could be observed, depending on the state of activity of the various LEDs, which does not affect the communication. Only an increased load activity, that leads to a drop of $> 6V$, starts to introduce bit errors. The cable length were varied between $0.5m$ and $6m$.



(a) $2Mbps$ communication using the CA approach, URZ encoding



(b) $2Mbps$ communication using the CP approach, Dicode

Figure 4.13: Measured waveforms at the demonstrator in loop-back configuration

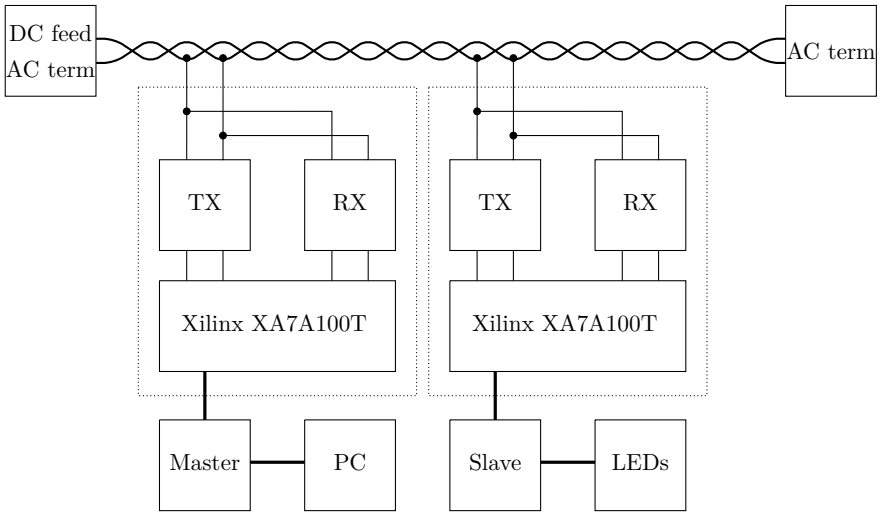


Figure 4.14: Experimental setup schematic

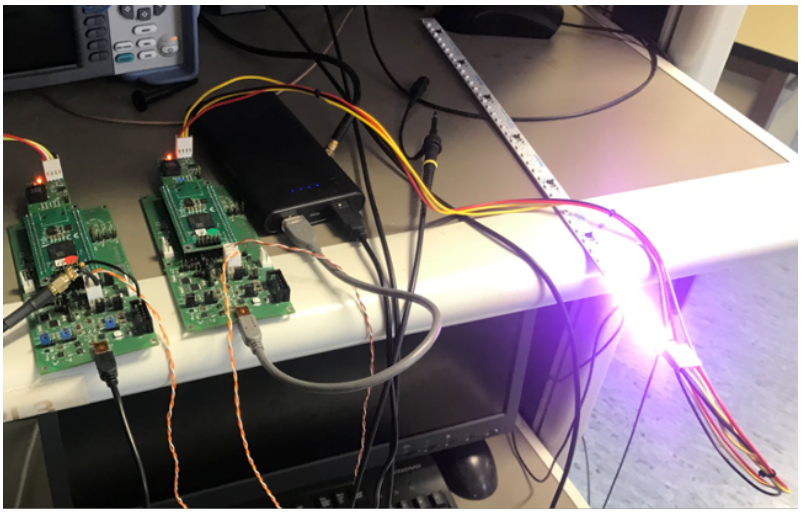


Figure 4.15: Experimental setup

4.6.3 Conducted emission measurements

In order to check the implementation on EMC, the conducted emissions have been verified by using a 150Ω-coupling network as shown in Fig. 4.16 according to IEC 61967-4 [33]. Conducted emissions are commonly used for characterizing differential networks because it observes the common mode level, which is the sum of both differential lines. Any time-varying asymmetry in the signaling, lead to an AC-signal of the common mode which lead to a potential radiation, since a differential transmission line is acting as an antenna in this case. Therefore, conducted emission measurements can show-up potential EMC

problems early in the product design stage.

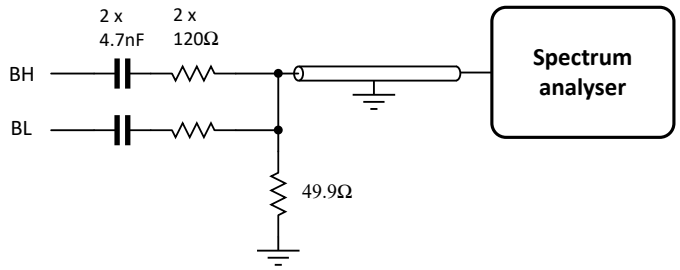


Figure 4.16: 150Ω-coupling network according to IEC 61967-4

Although for the CA and CP approaches no dedicated standard is available, it is appropriate to test the conducted emissions regarding the CAN network limits defined in IEC 62228-3 [14]. The test was performed on the demonstrator setup, described in the previous section, by adding the coupling network connected to the output of the demonstrator on the master side. The measurement results are shown in Fig. 4.17. The spectral response of the setup shows an increased noise level in case no communication is performed. This is likely linked to the cable harness, which is required during the measurement, but not used in a standard setup. The 'jump' in the levels at $30MHz$ is linked to the change in the resolution bandwidth (RBW) at this frequency that is requested by the standard. The spectral views on the CA and CP approaches are very similar. As a result, class I of IEC 62228-3 can be reached with the experimental setup below $100MHz$, higher frequencies are likely affected by the demonstrator wiring and the physical size of the setup itself. Moreover, the discrete solution might introduce imbalances caused by device tolerances. It is expected that a fully integrated solution would reach lower emission levels since long signal paths for control as well as imbalances causing radiation can be limited.

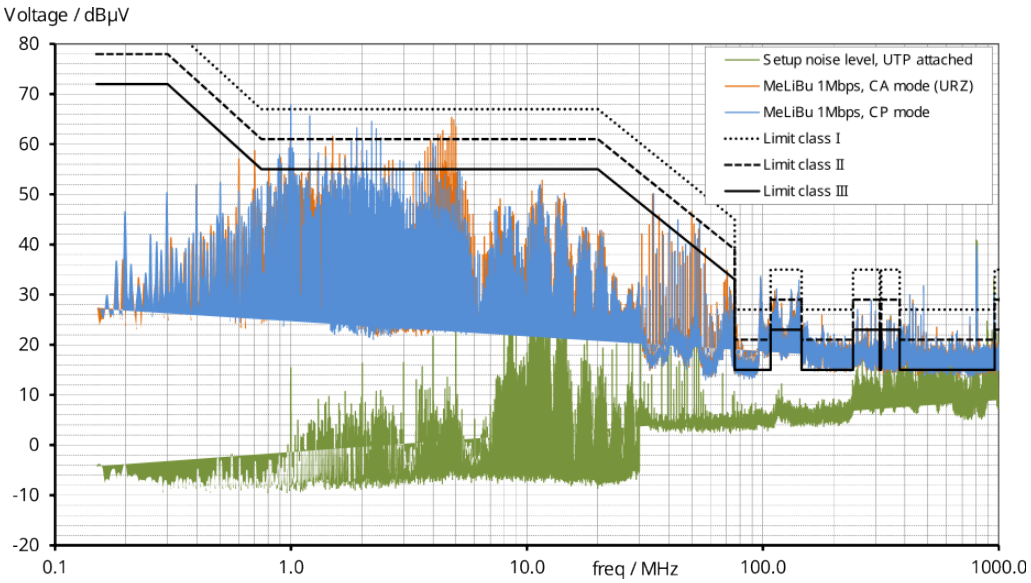


Figure 4.17: Conducted emission level of the demonstrator

CHAPTER 5

Transmitter Test Chip

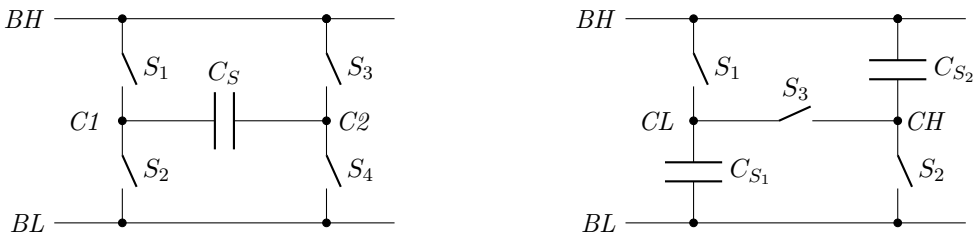
In this chapter, an integrated solution for the transmitter part of the proposed CA and CP approaches is evaluated. First, the operating range for the switches are discussed, which is important for selecting a suitable silicon technology as well as for the proper choice of primitive devices available therein. Further, the block design implementation of the switches as well as the design of the necessary service blocks and protection circuits are described. The composition of the test chip and its experimental results finalizes this chapter.

5.1 Operating range of the transmitter

Since the voltage level at bus and capacitor pins can reach values higher than V_B as well as lower than $0V$, a dedicated switch design and an appropriate protection circuit is needed to allow such voltage swings. First, the possible minimum and maximum levels are investigated. To secure a reliable operation, it is assumed that the load introduced by the bus and network subscribers is not attached, which under normal operation of the transmitter can be intentional or due to a connection failure (e.g. a broken wire). This gives the prediction for the highest swing in normal operation, to specify the conditions for the design of the switches and the electro-static discharge (ESD) protection scheme.

Referring to Section 3, both transmissions schemes showing the relevant nodes can be redrawn as depicted in Fig. 5.1. Because the size of the functional capacitors C_S is expected in the range of several hundred pico farads, they will be implemented as external components of the transmitter test chip. Therefore, nodes *C1*, *C2*, *CH* and *CL* are becoming pins in addition to *BH* and *BL*, to connect the switches of the test chip to the external functional capacitors.

Considering the charge of the capacitor C_S to be zero, none of the possible switching states lead to an excursion beyond the level of V_B or below $0V$ on pins *BH*, *BL*, *C1*, *C2*, *CH* and *CL*, respectively. But with a charged capacitor, it will. In the CA mode, the charge to be considered is Q_{C_s} is $\pm V_B\, C_S$, while there are two switches in series required to establish the conduction for charging. In an ideal case, both switches are turning on



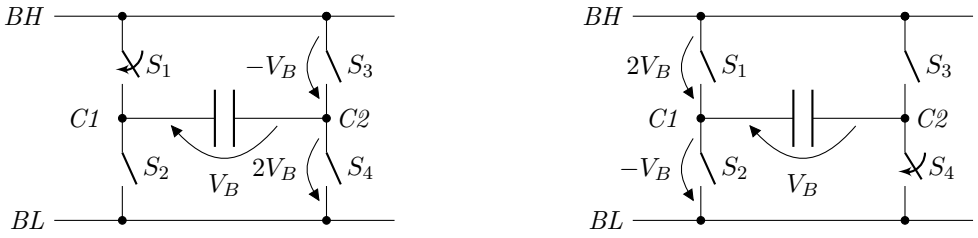
(a) CA approach **(b)** CP approach

Figure 5.1: Node assignment of the switched-capacitor modulation approaches

simultaneously, but in reality this is not achievable, since

- the switches have different implementations (high-side vs. low-side switch), which result in different timings, and
- the driver circuit might be of the same implementation, but mismatch among them would also lead to different timings.

This results in an asymmetric conduction, where the switch which is conducting first will change the voltage level by $2V_B$ across the other switch with the delayed turn-on, because of the charge alternation. The case, where the high-side switch turns on first, is illustrated in Fig. 5.2(a). Here S_1 is closing while S_4 is still off. Since the capacitor was in charge alternation mode - charge S_2-S_3 state - (CA-CHG 2-3) before, rises the voltage level at pin *C2* from V_B to $2V_B$ w.r.t. pin *BL* and from $0V$ to V_B w.r.t. pin *BH*.



(a) High-side switch conducts first **(b)** Low-side switch conducts first

Figure 5.2: Asymmetric conduction during transition from open to charge alternation mode - charge S_1-S_4 state - (CA-CHG 1-4)

The complementary case, where the low-side switch turns on before the high-side switch, is illustrated in Fig. 5.2(b). Now the voltage level at pin *C1* changes from $0V$ to $-V_B$ w.r.t. pin *BL* and from $-V_B$ to $-2V_B$ w.r.t. pin *BH*. Although there is conceptually no voltage level excursion of pins *C1* and *C2* above *BH* and below *BL*, in a real implementation it is needed to allow them without clamping so that no portion of the charge is dissipated because of a limited headroom. However, the static node capacitance at the *C1*, *C2* nodes, mainly

consisting of C_{dg}, C_{ds} of the switching transistors and other parasitic capacitances, lead to a charge redistribution and therefore to a loss of available charges for the transmission proportional to the ratio between the said capacitances and the functional capacitor C_S.

In the CP approach (referring to Fig. 5.1(b)), there is only one switch required in charge and discharge conduction paths, since in charge pump mode - charge state - (CP-CHG), the two functional capacitors C_{S_1}, C_{S_2} are charged separately with dedicated switches S_1, S_2. In charge pump mode - discharge state - (CP-DIS), S_3 connects the capacitors in series. Consequently, voltage glitches caused by asymmetric conduction as described like in CA mode, will not appear in the CP approach, so that the maximum voltage level for pins *CL* and *CH* w.r.t. pins *BH* and *BL*, is $-V_B$ and V_B, respectively.

For the bus pins *BH*, *BL* itself, a voltage excursion vs. the local supply pins *VS*, *GND* should be considered. Whereas in CA mode, the bus pins are not exceeding V_B nor fall below $0V$, in CP mode the maximum voltage level for pins *BH* and *BL* w.r.t. pins *VS* and *GND*, is $-V_B$ and V_B, respectively. A summary of the maximum and minimum voltage level at the high voltage (HV) pins are shown in Table 5.1. To ensure a reliable operation, the ratings marked in bold need to be accepted by the circuits, both the switching and the protection circuits.

Table 5.1: Maximum and minimum levels at HV pins during state transitions with obtained specifications marked in bold

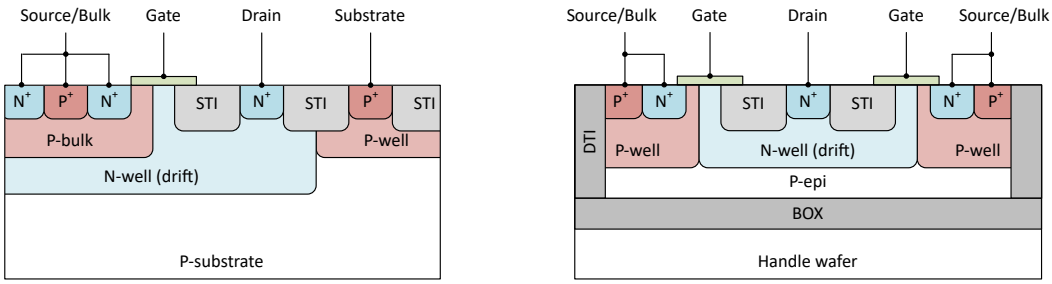
Pin	*BH*				*BL*				*C1/2* in CA; *CH/L* in CP			
Ref.	*GND*		*VS*		*GND*		*VS*		*BL*		*BH*	
State	min	max	min	max	min	max	min	max	min	max	min	max
CA-CHG	**0**	V_B	$\mathbf{-V_B}$	0	0	$\mathbf{V_B}$	$-V_B$	**0**	$\mathbf{-V_B}$	$\mathbf{2V_B}$	$\mathbf{-2V_B}$	$\mathbf{V_B}$
CP-CHG	**0**	V_B	$\mathbf{-V_B}$	0	0	$\mathbf{V_B}$	$-V_B$	**0**	0	V_B	$-V_B$	0
CP-DIS	V_B	$\mathbf{2V_B}$	0	$\mathbf{V_B}$	$\mathbf{-V_B}$	0	$\mathbf{-2V_B}$	$-V_B$	0	V_B	$-V_B$	0

5.2 Wafer process

In the previous section it was shown, that the bus terminals *BH* and *BL* are exceeding the range of the local supply, especially in CP-DIS mode. On the other hand, it is essential for the switch transistors to connect their sources to either *BH* and *BL*. For a low-side switch, a high-voltage n-type metal-oxide semiconductor (HVNMOS) transistor with the source connected to *BL* is considered, while for a high-side switch a high-voltage p-type metal-oxide semiconductor (HVPMOS) transistor with its source connected to *BH* is appropriate. In a complementary metal-oxide semiconductor (CMOS) wafer process with a p-type substrate, the HVNMOS transistor is typically implemented as a lateral double-diffused metal-oxide semiconductor (LDMOS) transistor as depicted in Fig. 5.3(a). The n-well provides the

drift region between the p-bulk and the drain n^+ implant, which is aimed for providing high V_{ds} breakdown voltages. Its lateral and vertical dimension (drift length and thickness) as well as the doping concentration are the main parameters which influences the HV parameters of the transistor. In circuit implementations using a p-type wafer material, the substrate is usually connected to the ground node, which should be kept undisturbed to avoid coupling into sensitive circuit parts. The p-n-p structure formed by the p-bulk, the n-well drift implant and the p-substrate, provides an isolation between source/bulk and the p-substrate. However, it is sensitive to punch-through, in case it is reverse biased by few volts [34]. This prevents the usage of standard CMOS implementation in CP-DIS, since *BL* can fall well below *GND* because a lower potential at *BL* would cause a breakdown.

To avoid this, modern Bipolar-CMOS-DMOS (BCD) processes have an N-buried layer (NBL) implemented between the p-substrate and the LDMOS, which highly reduces the punch-through effect. Furthermore, silicon-on-insulator (SOI) wafer technologies offer an even higher degree of freedom by placing a buried oxide (BOX) layer between the circuit elements (primitive devices) and a so-called handle wafer (HW), as shown in Fig. 5.3(b). With few hundreds of nm thickness, the BOX layer introduces an isolation which allows several tens of volts difference between the HV circuit elements and the HW without altering the device performances. For a lateral isolation, usually a deep trench isolation (DTI) is available so that a fully isolated tub for primitive devices can be designed.



(a) Asymmetric n-type LDMOS in bulk CMOS

(b) n-type LDMOS in SOI

Figure 5.3: Typical implementations of an HV NMOS in bulk CMOS and SOI technology [34]

In the present project, a 180nm BCD-on-SOI technology [35] is used. It provides various flavours of fully isolated HV transistors with a low $R_{ds_{on}}$ and drain-source breakdown voltage levels between $10V$ and $200V$. The choice is also supported by the fact that a reasonable number of libraries for interfaces, digital gates and ESD protection elements are provided by the foundry. Furthermore, IP macro blocks are available from predecessor projects, which allows building the chip infrastructure for the supply macro block with

only minor adaptations. Table 5.2 lists the main properties of the selected wafer process options.

Table 5.2: Selected properties of the wafer process

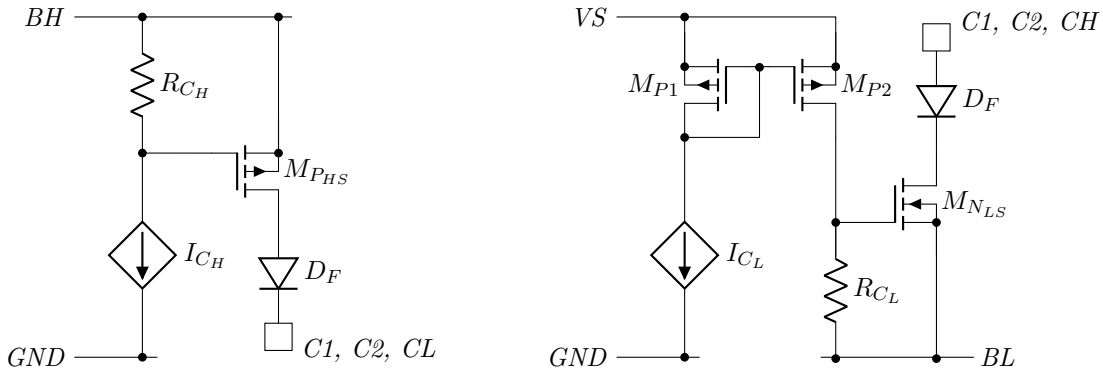
Process name	XT018
Metalization option	Al, 5 thin, 1 thick (top)
Isolation	BOX, DTI
LV transistors	1.8V, 5V
HV transisors	40V
Capacitors	fringe, p-type varactor
Resistors	diffusion, well, poly and high-R poly

5.3 Switches

The most relevant parts of the transmitter are the switches for the CA and CP implementations. As analysed in Section 5.1, the voltage swing can be as high as $2V_B$. Consequently, with a maximum operational voltage level of $V_B = 14V$, the low-$R_{ds_{on}}$ 40V class transistors *nhvta* and *phvta* were chosen. This gives enough headroom for the operation as well as a reliable ESD protection window. The architecture for the high-side switch (S_1 and S_3 in CA, and S_1 in CP approach) is shown in Fig. 5.4(a). Here, the V_{gs} of the HVPMOS switch transistor $M_{P_{HS}}$ is controlled by the voltage drop across R_{C_H} using a *GND*-referenced controlled current source I_{C_H}. To turn-on $M_{P_{HS}}$, V_{gs} should be $-5V = -R_{C_H} I_{C_H}$ in order to achieve the minimum layout area needed for the required $R_{ds_{on}}$, as discussed in Section 3.5. In the silicon implementation which is reported in [9] also the influences of C_{gs} and other parasitic capacitances w.r.t. turn-on and turn-off times as well as gate protection of the switch transistor are tackled. From Section 5.1 it follows that in CA mode the pins *C1* and *C2* can be V_B higher than the source of $M_{P_{HS}}$. To avoid a parasitic current flow over the drain-bulk diode in this case, a reverse protection HV-diode D_F is used. In the CP implementation D_F is not necessary, but due to simplification reason, all high-side and low-side switches are realized with the same block.

The low-side switch implementation is complementary as shown in Fig. 5.4(b). For controlling the operation of $M_{N_{LS}}$, V_{gs} is generated by the voltage drop over R_{C_L} with a *VS*-related pull-up current. It is provided by M_{P2}, which mirrors the *GND*-referenced controlled current I_{C_L}. This provides the advantage that the current control can be provided from a low-voltage domain circuit that is referenced to *GND*. Not shown, but implemented as reported in [9], are the HV-cascoding elements for the current mirrors and sources, which can be implemented in this case with medium voltage (MV) or low voltage

(LV) transistors ($1.8V$ or $5V$). This offers the advantage that they can be implemented with a much lower size and higher accuracy compared to HV-transistors. The HV-cascodes are protecting the low-voltage current source transistors from non-permitted operating voltages and keeping the change of V_{ds} vs. I_d of the current sources is very low and thus yielding to a high output conductance $g_o \approx \delta I_d / \delta V_{ds}$. Also in the low-side switch, a reverse protection HV-diode D_F is used to avoid the drain-bulk diode of $M_{N_{FS}}$ becoming forward biased in case the level of BL goes below GND.



(a) High-side **(b)** Low-side

Figure 5.4: Principle of high- and low-side switch implementations

A more complex case is the floating switch S_3 used in the CP approach for discharging the capacitors in series. Referring to Fig. 5.1(b), it can be seen that from a previous charging state (CP-CHG) the capacitor pins have pre-determined levels which are $0V$ for CH and V_B for CL. As a result, the discharge current is unidirectional so that a single HV transistor can implement the function of the switch without forward biasing of its drain-bulk diode. Consequently, the floating switch is realized by the HVNMOS transistor $M_{N_{FS}}$ connected with its source to CH as shown in Fig. 5.5. However, there are unintended discharges during an ESD event possible, which would bias the drain-bulk diode of $M_{N_{FS}}$ in forward direction. For this case, it is assumed that its area is sufficient to carry the current stress by the drain-bulk diode, that enables a self-protection for $M_{N_{FS}}$ when biased reversely. An ESD stress simulation will carry out if this is the case, or if an additional diode in the conduction path is needed.

In order to control V_{gs}, the source level is tracked and decoupled from the control circuit by a unity gain buffer, which allows applying V_{gs} as a voltage drop across a resistor R_{C_F}, without drawing a current from the source node CH. To turn $M_{N_{FS}}$ on, M_{P2} provides a VS-related pull-up current which is larger than the permanent GND-related pull-down

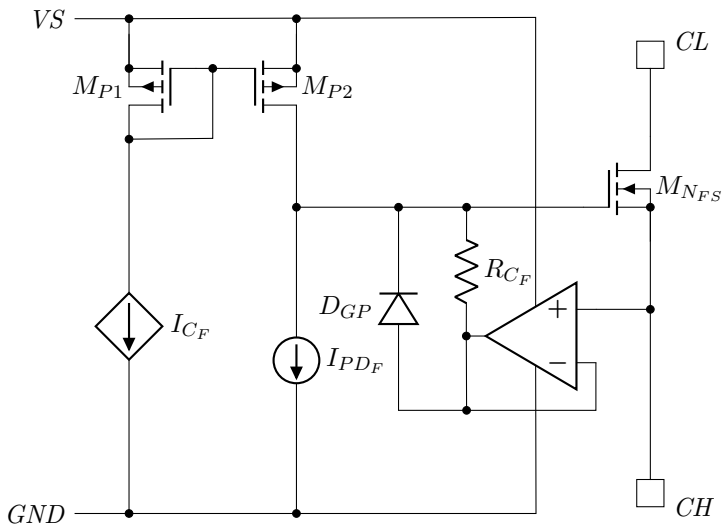


Figure 5.5: Implementation principle of the floating switch

current I_{PD_F}, used for pulling down the gate in off-state, so that the difference current flows into R_{C_F} to provide a V_{gs} of $\approx 5V$. To turn the floating switch off, the controlled current I_{C_F} is set to zero so that I_{PD_F} remains, which reverses the polarity and as a result, the protection diode D_{GP} becomes forward biased, yielding to a V_{gs} of $\approx -0.7V$ which turns $M_{N_{FS}}$ off.

5.4 Chip architecture

To implement both, CA and CP approaches in a transmitter test chip, an infrastructure is required, that provides the necessary supply, control, and protection. It should also be possible to connect the chip to various devices which can steer the activity of the transmitter part, configure which approach is intended to be used, and set the trimming and test registers. Besides the standard laboratory equipment such as a PXI test system and an arbitrary waveform generator (AWG), also an FPGA or open-source single-board microcontrollers like an Arduino or a Raspberry Pi board, should be considered. Such a flexibility requires a dedicated supply domain for the interfaces to the external equipment that cover a larger supply range than the internal supply domain. This is also because the internal control of the switches needs to be at a dedicated level, to ensure the target $R_{ds_{on}}$ can independently be met, and therefore need to be decoupled from the level of the interfaces. Consequently, the supply for the I/Os is provided by the external equipment using the dedicated pins *VIO* and *GNDIO*.

The driver circuit for the switches is supplied with $5V$ to ensure enough headroom, also in perspective of the receiver part, which will be implemented in the transceiver test chip.

An internal supply macro-block, based on available IP blocks, provides this voltage supply, regulated from the external supply *VS*. It is available on pin *V5* for external decoupling by a capacitor. A lower level internal voltage *VCORE* is supplying all circuitry that is not part of the transmitter.

The top-level architecture can be seen in Fig. 5.6, where the supply domains are color coded. The main macro-blocks are supply, digital control, transmitter and the I/O interface with its ESD-protection circuitry (not shown).

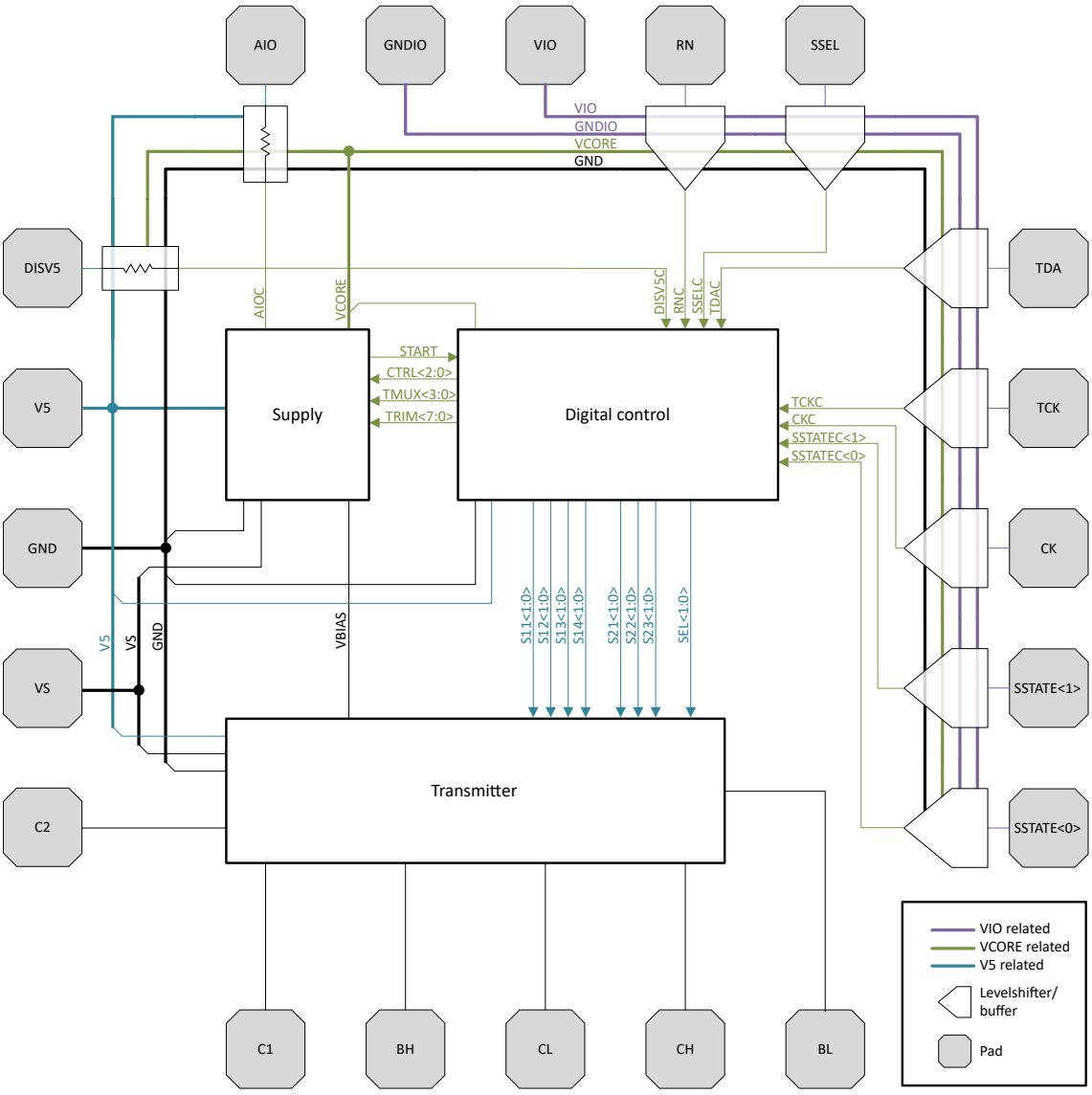


Figure 5.6: Top-level block diagram of transmitter test chip

5.5 Supply

The supply macro block aims to generate the necessary supply voltages for the chip from the externally applied VS. The level of VS can be between 5.5V and 18V. As explained in Section 5.4, a supply of $5V$ is required for the transmitter part. To have a safe margin to the maximum permitted V_{gs} and V_{ds} for the MV transistors of $5.5V$, an accuracy of $V5$ of $\pm 5\%$ is appropriate. A level span of applied external supply levels and internal supply domains are shown in Fig. 5.7. Although the external supply VS is typically $14V$,

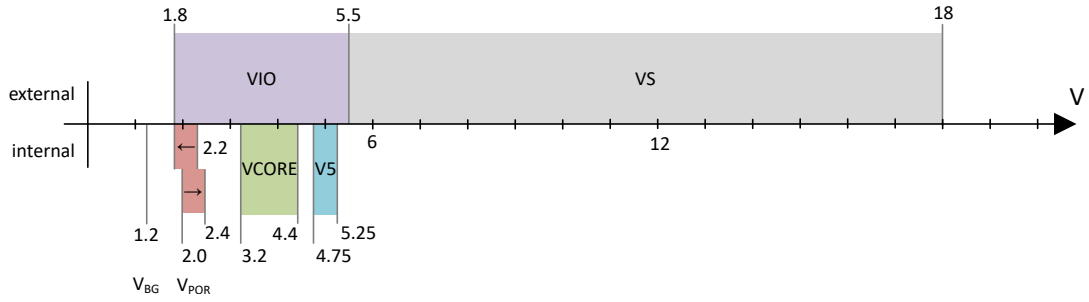


Figure 5.7: Level span of internal and external supply domains

it can range between $5.5V$ and $18V$. To generate a reliable $V5$, a coarse regulation step to $VCORE$ is implemented. This serves as the internal non-interruptible supply for the bandgap reference, the $V5$-regulator and the digital control of the test chip. Fig. 5.8 shows the block diagram of the supply block. $VCORE$ is typically $3.8V$ and is monitored by a power-on reset (POR) block during start-up and ramp down of VS according to the threshold ranges denoted in Fig. 5.7. A hysteresis between the positive and negative threshold is $\approx 150mV$ to ensure a glitch-free transition of the $START$ signal, which releases the reset state of the digital control circuit and enables the bandgap reference if requested by the digital control. This enable signal for the bandgap is delayed by a turn-on delay of $\Delta_t \approx 40\mu s$ to start up the linear $5V$-regulator when VBG is close to or has reached its steady-state of $\approx 1.2V$. This results in a smooth turn-on of $V5$ as shown in Fig. 5.9, which represents the simulated waveforms of the supply block implementation. During ramp-down of the external supply, bandgap and $5V$-regulator turn off upon reaching the negative threshold of the POR. To provide the bias for the transmitter part, a pull-up current of $5\mu A$ is provided by a p-type metal-oxide semiconductor (PMOS) current source inside the coarse regulator. This is connected to an n-type metal-oxide semiconductor (NMOS) current mirror inside the transmitter part, which defines the level of $VBIAS$ by its V_{gs}. The bias current is a copy of an internal current derived from a voltage applied to a poly-silicon resistor, that is generated from a 1^{st} order bandgap core. As a result,

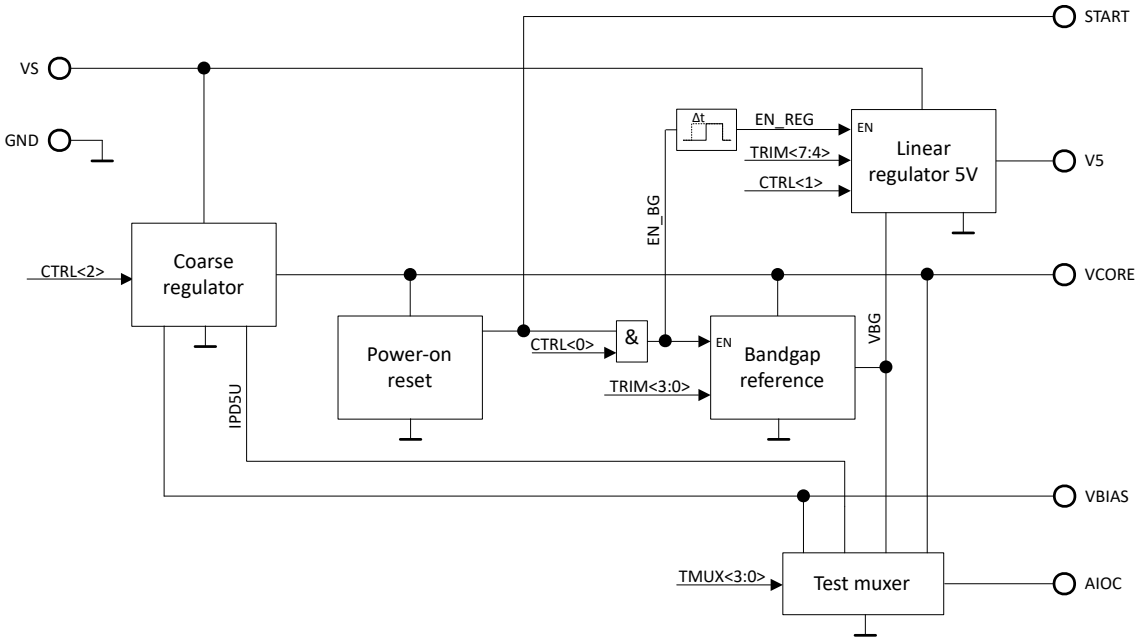


Figure 5.8: Implementation of the supply

the current is inverse proportional to this poly-silicon resistor, so that the bias current can be used in the transmitter to apply a well controlled V_{gs} for the switch transistors by using the same type of resistor there. With this approach, the spread of the process w.r.t. the sheet resistance of this type of resistor can be eliminated, so that only matching constraints are remaining.

Furthermore, the supply block has three control signals for manipulating its operation. A $5\mu A$ pull-down current, *IPD5U* to output via *AIO*, can be enabled as well as a $25\mu A$ current sink which avoids overshoots of the $5V$-regulator in the case of light loads during start-up. As a fall-back option, the $5V$-regulator can be disabled by leaving pin *DISV5* open, which translates the level of this pin to the level of *VCORE* by a pull-up resistor in the pad circuit of the pin. In this case, an external $5V$ supply applied to *V5* can drive the circuit. Table 5.3 lists the control options for the supply block.

Table 5.3: Control signals of the supply block

Control input	Description	Default/connection
CTRL<2>	enables *IPD5U*	0
CTRL<1>	enables the current sink inside the $5V$- regulator	1
CTRL<0>	enables the $5V$- regulator	$\overline{DISV5}$

For tuning and trimming of the supply, the correct settings of *TRIM* needs to be found.

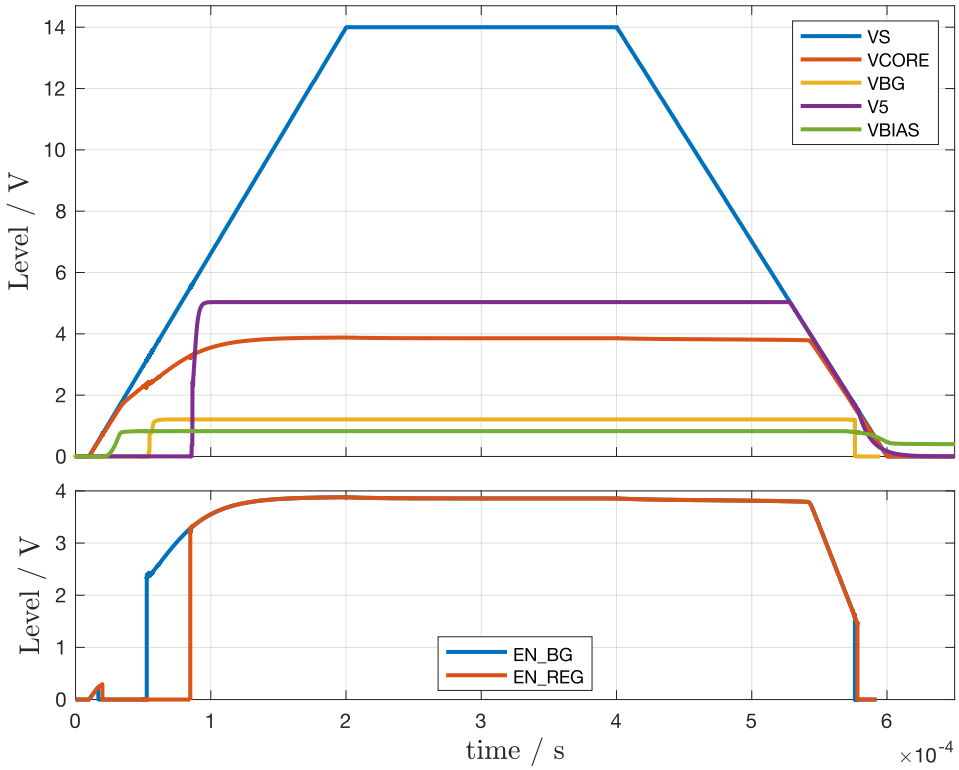


Figure 5.9: Waveform of supply regulation during ramp-up/down

As a consequence, a copy of the internal bias current *IPD5U* and nodes *VBIAS*, *VBG* and *VCORE* of the supply block, are available to the external equipment by an analog I/O pin (*AIO*), which is connected to the supply block through *AIOC*. This is achieved by a muxer, consisting of T-switches that are controlled by the 1-active signal *TMUX*, as listed in Table 5.4. The digital control allows setting of only one channel out of four (see Section 5.6) to avoid cross-currents. The performance parameter of the supply block, that are provided in a temperature range from $-40°C$ to $125°C$, are listed in Table 5.5. The process spread includes a 6σ variation capability.

Table 5.4: Test signal mux to *AIOC*

Muxer input	Signal to *AIOC*
TMUX<3>	*VBIAS*
TMUX<2>	*VCORE*
TMUX<1>	*VBG*
TMUX<0>	*IPD5U*

Table 5.5: Performance parameters of the supply block, for a temperature range of $\vartheta = -40°C$ to $125°C$, and a process spread of 6σ

Parameter	Symbol	Condition	min	typ	max	Unit
External supply level	V_B		5.5	14	18	V
Core voltage level	V_{CORE}	$I_L = 10\mu A$, $C_L = 200pF$	3.7	4.0	4.5	V
		$I_L = 200\mu A$, $C_L = 200pF$	3.5	3.8	4.3	V
Bias current	I_{PU5U}		3.0	5.5	9.4	µA
Bandgap reference	V_{BG}	trimmed	1.201	1.204	1.209	V
$5V$-regulation level	V_5	trimmed, $I_L < 70mA$, $C_L = 220nF$	4.96	5.02	5.03	V
Reset threshold	$V_{POR_\uparrow}$		2.0	2.2	2.4	V
	$V_{POR_\downarrow}$		1.8	2.0	2.2	V
Reset hysteresis	$V_{POR_{HY}}$		90	150	250	mV
Reset pulse width	t_{POR}		70			ns

5.6 Digital control

The operation of the test chip is controlled by a digital circuit. It translates the few external control signals into an appropriate internal control for the blocks. Static signals for setting the trimming of the $V5$-regulator and the bandgap ($TRIM$), the supply control ($CTRL$) and the test muxer ($TMUX$), are indirectly accessible by a test register. This can be configured in a *shift*-mode using the test clock pin TCK and the test data pin TDA. One exception for a static control signal is $DISV5$: here the knowledge, if the internal $5V$-regulator is requested or if an external regulator is applied to the chip, is mandatory to avoid a start-up condition, where the internal regulator is competing with an external regulator. As described in Section 5.5, the pin $DISV5$ contains an internal pull-up resistor to $VCORE$ so that the user only needs to either short this pin to ground for enabling the internal $5V$-regulator. Alternatively, it should be left open to disable the internal regulator. In the later case, the $V5$-supply is then provided from an external power supply. All other external control signals are referenced to the VIO-domain and are level-shifted to the $VCORE$-domain. The translated external control signal then contains a *'C'*-letter internally, at the end of the signal name.

The control of the switches of the transmitter is realized by a translation from the switch state inputs *SSTATE<1:0>*. It is addressing an open state of the switches, two different active switch states that are required for CA and CP approaches, and a test mode where the configuration of the test registers is accomplished. With the positive clock edge of CK, the requested switch state is applied, i.e., in the *apply* state, as shown in Fig. 5.10. The highest value of *SSTATE<1:0>* is reserved for the *shift* mode. The internal low-active reset RNI is an AND combination of the external low-active reset and $START$ signal from

the supply block. It initializes the small finite-state machine (FSM).

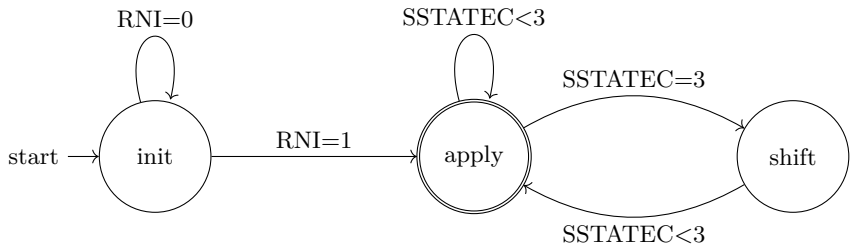


Figure 5.10: State diagram of the digital control

With the selection pin *SSEL*, that chooses the transmitter approach to be used, the control of the relevant switch is completed as shown by Table 5.6. Although during *shift* mode it would be possible to use *CK* as clock input for shifting the trimming data into the shift register *TMREG*, the option for a separate test clock *TCK* is implemented. This is to drive the switch control and the test access from different instances, either inside an FPGA or physically by separate equipments. Moreover, this prevents toggling of the configuration signal to the analog part during the shift operation, without the need for more hardware effort. However, pins *CK* and *TCK* can be combined off-chip if appropriate.

Table 5.6: State control

SSEL	*SSTATE<1:0>*	Mode	Switches to turn on
0	00	*open*	
	01	CA-CHG 1-4	CA part: S_1, S_4
	10	CA-CHG 2-3	CA part: S_2, S_3
	11	*shift*	
1	00	*open*	
	01	CP-CHG	CP part: S_1, S_2
	10	CP-DIS	CP part: S_3
	11	*shift*	

As shown in the digital implementation in Fig. 5.11, the control outputs to the switches are level-shifted to the *V5*-domain in which the transmitter part is located. This is because it benefits from the higher gate-overdrive capability and the more precise supply in terms of load and line regulation when compared to *VCORE*.

The state output signals for the analog part are latched in the switch control register *SWC* and the test output register *TMOUT*. The *shift* state is indicated by *TMSHIFT* and allows passing the serial data from *TDA* into *TMREG*. To comply with the timing constraints of the digital library provided by the wafer foundry, the implementation was

synthesized from the Verilog source listed in Section A.2.1. The test registers are 16-bit wide to allow two additional spare control signals if needed during the design process, and support a byte-wise programming in the external equipment. Consequently, whenever a change in the test register *TMOUT* is required, the complete 16-bit configuration need to be shifted-in with LSB-first. The next positive clock edge on *CK* is applying the setting to the analog part by transferring the configuration from *TMREG* to *TMOUT*.

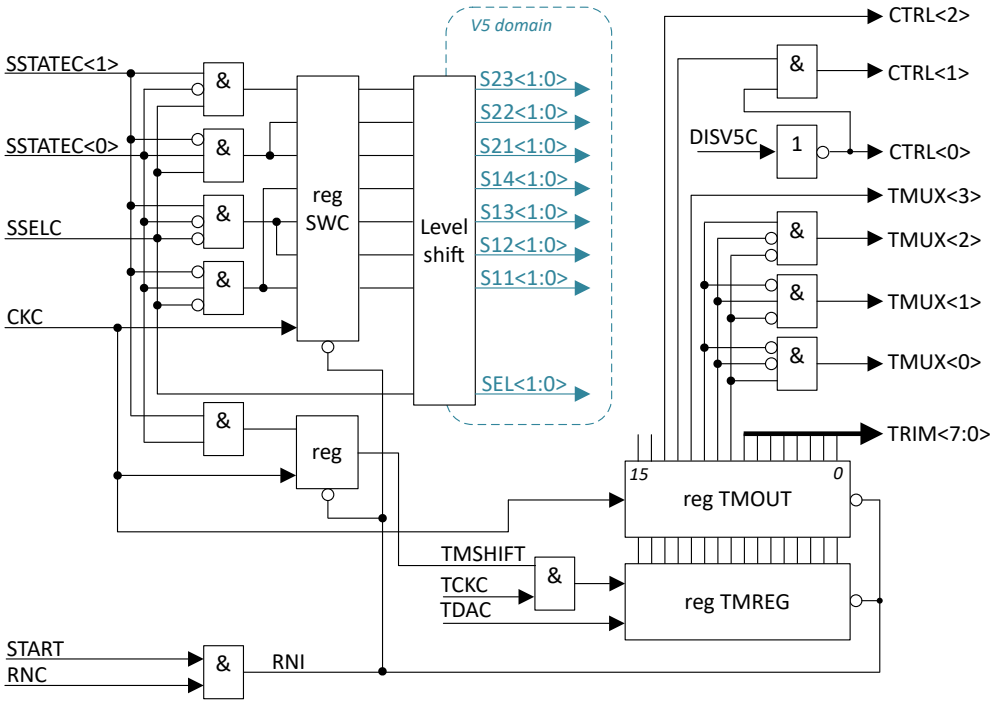


Figure 5.11: Block schematic of the digital control for the transmitter test chip

5.7 ESD protection

To protect the test chip from ESD due to handling, a dedicated protection scheme is necessary. Since the voltage level at bus and capacitor pins can reach values higher than V_B as well as lower than $0V$ as analysed in Section 5.1, a dedicated protection circuit is needed to allow such voltage swings. The maximum permitted V_{ds} of the HV transistors *nhvta* and *phvta* is $40V$ and $-40V$, respectively. On the other hand, the voltage levels can reach $\pm V_B$ around the related HV pin, according to the theoretical assumptions taken in Section 5.1. This would require an operation range of $\pm 36V$, at the maximum V_B of $18V$. However, in the real implementation two aspects need to be considered:

- The implementations of high- and low-side switches, as proposed in Section 5.3, require

a current, drawn from the bus nodes BL and BH for generating a sufficient V_{gs} to turn-on the switches. By contrast to the ideal switch assumed in the operating range exploration (5.1), high- and low-side will not turn on without a proper connection of the bus pins. A missing bus connection is therefore not the worst-case condition for the consideration of the extreme voltage levels during switch operation.

- With the real circuit implementation, the turn-on tolerance between high- and low-side switch in CP mode can be estimated by simulations.

A simulation of the circuit implementation reported in [9] is shown in Table 5.7. It assumes the maximum supply voltage V_B of $18V$ over a process spread of 6σ in a temperature range from $-40°C$ to $125°C$. The connected C_S is $1nF$, and the parasitic node capacitance is assumed with $20pF$. Accordingly, the operating range of the implementation can be

Table 5.7: Simulation of maximum and minimum levels at HV pins during state transitions for a temperature range of $\vartheta = -40°C$ to $125°C$, and a process spread of 6σ

Pin	*BH*				*BL*				*C1/2* in CA; *CH/L* in CP			
Ref.	*GND*		*VS*		*GND*		*VS*		*BL*		*BH*	
State	min	max	min	max	min	max	min	max	min	max	min	max
CA-CHG	10.1	18.0	-7.9	0	0	7.8	-18.0	-10.2	-13.4	26.7	-29.3	10.7
CP-CHG	14.7	18.0	-3.3	0	0	3.3	-18.0	-14.7	0.8	17.2	-17.2	-0.8
CP-DIS	18.0	20.8	0	2.8	-2.8	0	-20.8	-18.0	0.8	17.2	-17.2	-0.8

assumed to $\approx \pm 30V$. That gives a $10V$ margin at upper and lower limits for the 40V class transistors *nhvta* and *phvta* that are used. In Fig. 5.12 the operating range of those transistors are depicted. The application window, marked in green, illustrates the operating range of the implementation, elaborated previously. The maximum V_{ds} is $V_{ds_{nmax}}$ and $V_{ds_{p_{min}}}$ for *nhvta* and *phvta*, respectively. Herein, the transistors are operating within normal ratings. Beyond that level, the minimum ESD window starts until $\pm 50V$, where HV transistors can trigger a parasitic bipolar, which shows typically a snap-back behavior with inhomogeneous triggering. The parasitic bipolar transistor for a HVNMOS and HVPMOS are illustrated in Fig. 5.13. Triggering those parasitic transistors lead to a permanent damage of the HV transistors. Any excursion beyond $\pm 40V$ should therefore be avoided and intercepted by a proper ESD protection structure.

To achieve a reliable application window and suppress voltage excursions due to ESD events beyond $\pm 40V$, a HV clamping stack based on trench isolated MV (5V) PMOS transistors have been selected. With the number of stacked transistors, the protection level is controlled. Due to the high clamping voltage V_{clamp}, these structures are latch-up robust and are capable to absorb and dissipate a high power during an ESD event. A

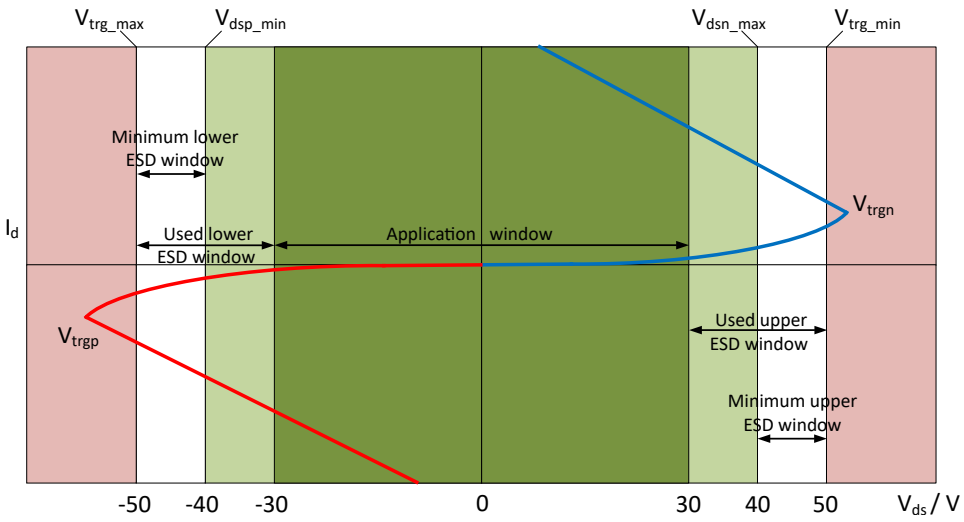
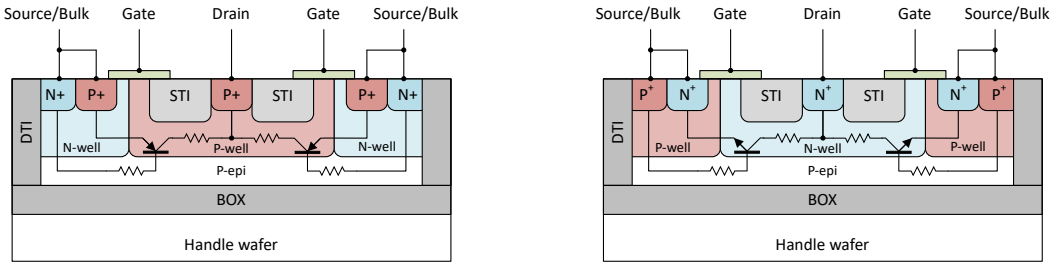


Figure 5.12: Operating range of the HV transistors



(a) HVPMOS with parasitic p-n-p transistor **(b)** HVNMOS with parasitic n-p-n transistor

Figure 5.13: Parasitic bipolar transistors in HV devices

typical characteristic is shown in Fig. 5.14. When a positive voltage is applied, it will draw very low current until the breakdown voltage V_{bdo} is reached. Usually, at the breakdown level, a current of $1\mu A$ is drawn. With a further increase, the HV-ESD clamping stack will trigger the snap-back behavior at V_{trg} if the necessary trigger current I_{trg} is provided. After triggering, the clamp device becomes low-ohmic. With further increased ESD current, the voltage across the clamp is lowering down to the holding level V_{hold} first, before it start to increase again with even higher ESD current until V_{clamp} is reached. This is the maximum voltage level before the HV-ESD clamp damages.

The electrical properties of the selected HV-ESD clamp are shown in Table 5.8. It provides a compliant operation window to the transmitter chip. Negative levels applied to the clamp are shorted by the drain-bulk diodes associated with the PMOS stack, but it is recommended to apply an additional HV protection diode in parallel to provide an additional discharge path. To share such a HV-ESD clamping stack between multiple HV pins, the test chip uses a centralized clamp approach, that connects pads with the ESD

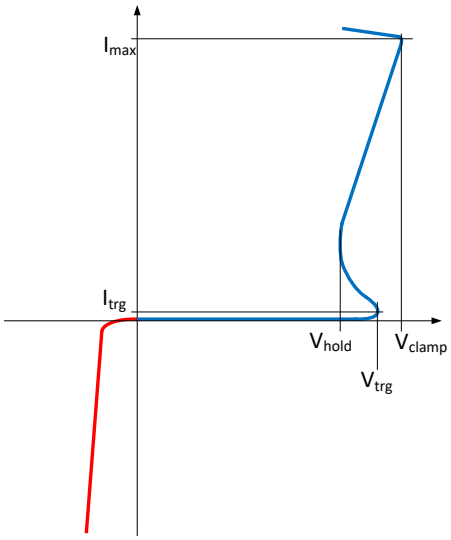


Figure 5.14: behavior of the PMOS ESD protection stack

Table 5.8: Performance data of the selected HV-ESD clamp

Parameter	Symbol	Value	Unit
Max. operational level	V_{opmax}	28	V
Min. operational level	V_{opmin}	-0.3	V
Break-down voltage	V_{bdo}	32	V
Trigger voltage	V_{trg}	35	V
Trigger current	I_{trg}	70	mA
Holding voltage	V_{hold}	30	V
Clamping voltage	V_{clamp}	39	V
Max. current	I_{max}	7	A

protection device by diodes. This principle is illustrated in Fig. 5.15. Each pad has its connection to both sides of the ESD clamp. Hence, the available operation range for the voltage difference between pads/pins is

$$|V_{pad_A} - V_{pad_B}| \leq V_{op_{max}} + 2V_{f_D}. \tag{5.1}$$

Here, V_{f_D} expresses the forward voltage of the diodes. In case the level of pad A vs. pad B exceeds the maximum operational voltage of the clamp plus two diode forward voltages $2V_{f_D}$, that are usually $\approx 0.8V$, the protection path opens from pad A $\rightarrow$ diode $D_{2A} \rightarrow$ clamp stack $\rightarrow$ diode D_{1B}. Similarly, from pad B $\rightarrow$ diode $D_{2B} \rightarrow$ clamp stack $\rightarrow$ diode D_{1A} if the level of pad B vs. pad A exceeds this level. A protection diode in parallel to the clamp is added to the clamp stack to support the clamp in reverse mode, as mentioned

previously. Both internal ESD rails can be used for multiple pads.

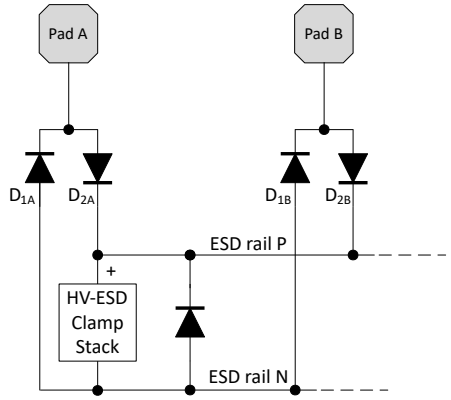


Figure 5.15: Common HV clamp stack approach

The HV-ESD of the transmitter test chip is illustrated in Fig. 5.16, here four HV-protection sections are considered:

- *VS* and *GND*:
  Here a normal HV protection scheme is needed, where HV-clamp 1 and a protection diode in parallel connects both pins. The clamping level is the same as for the other sections, according to the data in Table 5.8.
- *CL* and *CH*:
  Both pins are connected to external capacitors used in CP mode and vary between $0V$ and V_B during operation, which is confirmed by Table 5.7. Consequently, *VS* and *GND* can be considered as protection rails for *CL* and *CH*. Therefore, diodes are used to connect both pins to *VS* and *GND*. In normal operation, it can be considered that $V_{CL} \geq V_{CH}$, so that the floating switch transistor $M_{N_{FS}}$ can protect itself by its drain-bulk diode in case $V_{CL} < V_{CH}$ caused by an ESD event, as illustrated in Fig. 5.16.
- *C1* and *C2*:
  Both connections to the external capacitor in CA mode, *C1* and *C2*, can have a voltage difference of $\pm V_B$. Hence, the scheme of Fig. 5.15 is implemented by HV-ESD clamp 4 and a parallel protection diode, yielding to two internal HV-ESD rails, *ESD rail P* and *ESD rail N*. To establish a discharge path to *VS* and *GND*, *ESD rail P* is clamped by HV-ESD clamp 2 to *GND*, and *ESD rail N* is clamped by HV-ESD clamp 3 to *VS*. This limits the excursion of the internal HV-ESD rails w.r.t. external supply nodes.
- *BH* and *BL*:

The bus connection pins *BH* and *BL* are connected by diodes to *GND* and *VS*, respectively, since the following assumptions can be made:

$$V_{BH} \geq V_{GND} \qquad \text{and} \qquad V_{BL} \leq V_{VS}. \tag{5.2}$$

The level of *BH* is always below the level of *ESD rail P* so that a diode is connected between them. Similarly, the level of pin *BL* cannot be higher than the level of *ESD rail N*, also here a diode is connected between *ESD rail N* and *BL*.

The discharge paths for *C1* and *C2* w.r.t. pins *BH* and *BL* are indicated by colored lines in Fig. 5.16. All discharge paths for the HV pins are listed in Table 5.9.

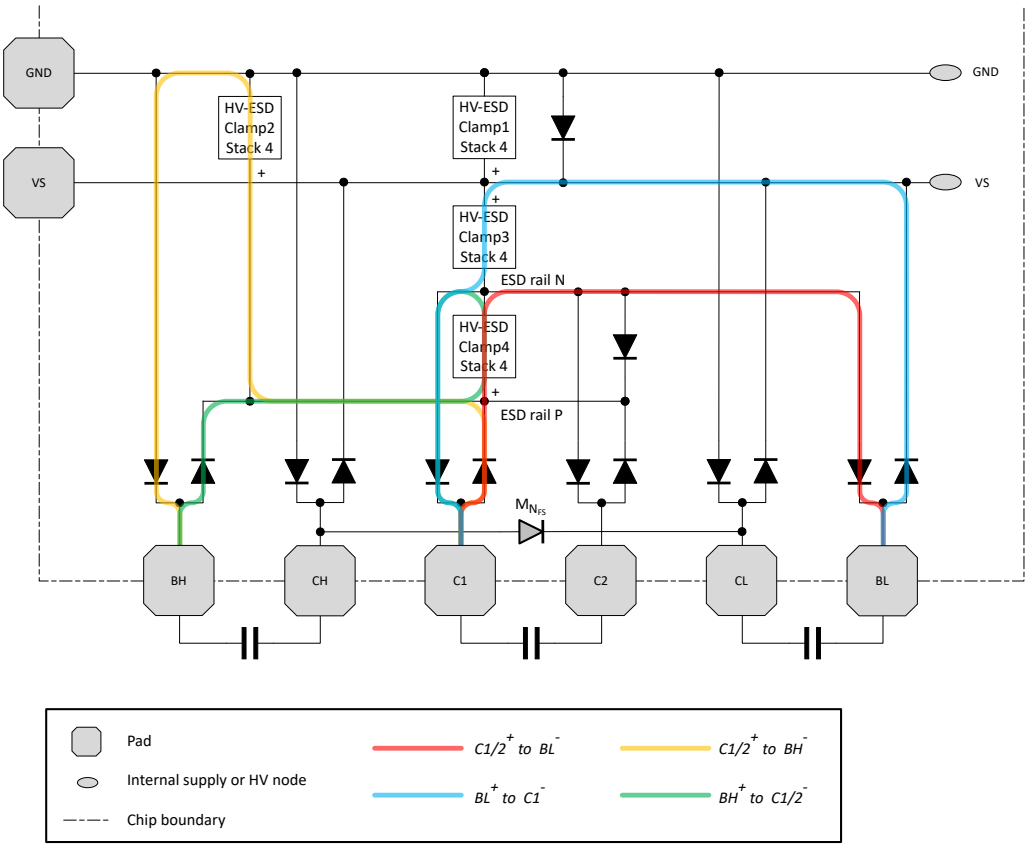


Figure 5.16: ESD protection: detailed view on HV part with discharge paths for C1 and C2

The complete ESD protection scheme for the test chip is shown in 5.17. It also contains elements for the transceiver test chip described in Section 6.4. In the MV part of the circuit, the maximum operating voltage level for the metal-oxide semiconductor (MOS) transistors in terms of V_{gs} and V_{ds} is $5.5V$ ($7V$ as the absolute maximum rating). Similar

Table 5.9: Discharge paths of proposed HV-ESD scheme; *D* indicates a diode and the integer number represents the number of the HV-clamp referred to Fig. 5.16

	BH^+	VS^+	CH^+	$C1^+$	$C2^+$	CL^+	GND^+	BL^+
BH^-		1←D	D←1←D	D←2←D	D←2←D	D←1←D	D	D←1←D
VS^-	D←2←D		D	D←2←D	D←2←D	D	D	D
CH^-	D←2←D	1←D		D←2←D	D←2←D	D←1←D	D	D←1←D
$C1^-$	D←4←D	3←D	D←3←D		D←4←D	D←3←D	D←3←D	D←3←D
$C2^-$	D←4←D	3←D	D←3←D	D←4←D		D←3←D	D←3←D	D←3←D
CL^-	D←2←D	1←D	D($M_{N_{FS}}$)	D←2←D	D←2←D		D	D←1←D
GND^-	D←2	1	D←1	D←2	D←2	D←1		D←1
BL^-	D←4←D	3←D	D←3←D	D←4←D	D←4←D	D←3←D	D←3←D	

to the HV section, a PMOS-clamp is used, whose electrical parameters are shown in Table 5.10. The MV protection part of the test chip considers three sections:

Table 5.10: Performance data of the selected MV-ESD clamp

Parameter	Symbol	Value	Unit
Max. operational level	V_{opmax}	7.0	V
Min. operational level	V_{opmin}	-0.3	V
Break-down voltage	V_{bdo}	8.0	V
Trigger voltage	V_{trg}	8.8	V
Trigger current	I_{trg}	30	mA
Holding voltage	V_{hold}	7.6	V
Clamping voltage	V_{clamp}	10.5	V
Max. current	I_{max}	4	A

- *VIO* and *GNDIO*:
  Both pins are protected by MV-clamp 1 for ESD stress applied between *VIO* and *GNDIO*. The connected input pads, related to *VIO*, have two series connected protection diodes to *VIO* and *GNDIO* that provides a discharge path from the input pad to either *VIO* or *GNDIO*, depending on the polarity of the ESD stress event. Those inputs have a second diode protection branch after a current-limiting resistor, which protects the Schmitt-Trigger-based digital input stages. To decouple the ground of the I/Os and normal ground, *GNDIO* and *GND* are connected by antiparallel diodes. In this way, a common ground can be established off-chip, so that no di/dt-related voltage drop across the ground lines can interfere to the other.
- *V5*:
  The $5V$ supply pin is used for external decoupling in case the internal $5V$ regulator is

active, or as a supply input in case the $5V$ supply is provided by an external source. For both cases, the MV-clamp 2, connected to *GND*, realizes the protection for *V5* and provides a discharge path to other pins.

- *VCORE*:
  The internal core supply is not connected directly to any pin, therefore MV-clamp 3 sufficiently protects *VCORE* from stress, eventually entered via the pull-up resistor on *DISV5*.

An ESD simulation based on the *XESDC* tool [36] was performed to verify the concept and design of the protection scheme. It uses a circuit design language (CDL) or SPICE netlist as input and performs a transmission-line pulse (TLP) current simulation based on the technology specific ESD model library. It solves the TLP characteristic for the given pin combination(s) and indicates the voltage and current stress levels in the identified discharge paths. The stress levels are representing the current and voltages as a portion of their maximum ratings. A simulation of the complete test chip has been performed to evaluate the impact on the core circuit during the ESD stress event. This would illuminate an improper or weak protection, e.g., in case an ESD protection device would be selected so that its ESD window is well above the breakdown levels of the core circuit elements. It also shows discharge paths which are hard to identify in circuits with a high level of complexity.

A first simulation with a TLP-current $I_{TLP}= 3A$ applied between every pin combination, showed that all relevant ESD stress is absorbed by the protection scheme, which confirms the functionality of the designed approach. A summary of the clamping level at $I_{TLP}= 3A$ for every pin combination is shown in Fig. 5.20. The HV pins located in the upper-left confirms the discharge paths via the diode/clamp combinations listed in Table 5.9. Furthermore, Fig. 5.18 and 5.19 depict the voltage and current stress levels of the related ESD-protection devices. It shows that still a margin of a few percents is available. The level of ESD robustness for component level HBM, according to JEDEC/ESDA JS-001 [37], can be assumed from the TLP characteristics [38] with,

$$V_{HBM} \approx \frac{3}{2} I_{TLP} \left[\frac{kV}{A}\right]. \tag{5.3}$$

As a result, any pin-to-pin combination of the test chip should at least withstand $V_{HBM}= 4.5kV$.

The bus pins *BL* and *BH* are connected to elements outside the module and should therefore withstand higher stress levels. Therefore, the protection elements of the HV-section are sized to accomplish this. Accordingly, an ESD-stress simulation predicts a

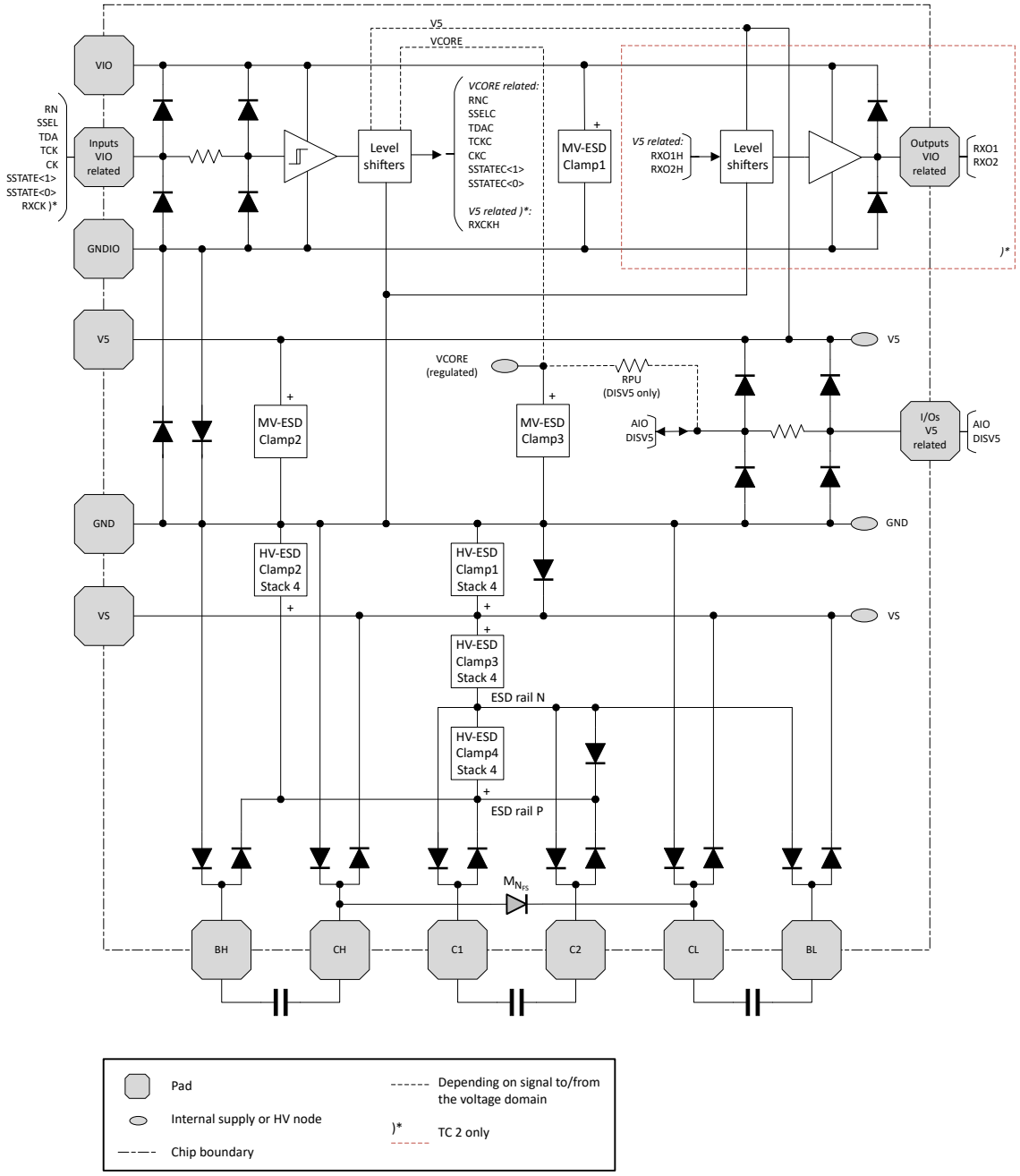
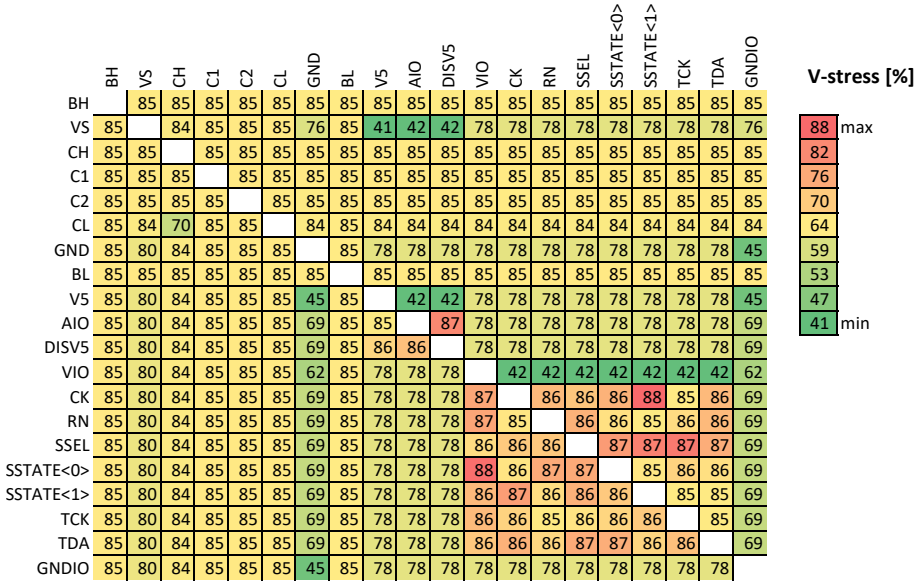
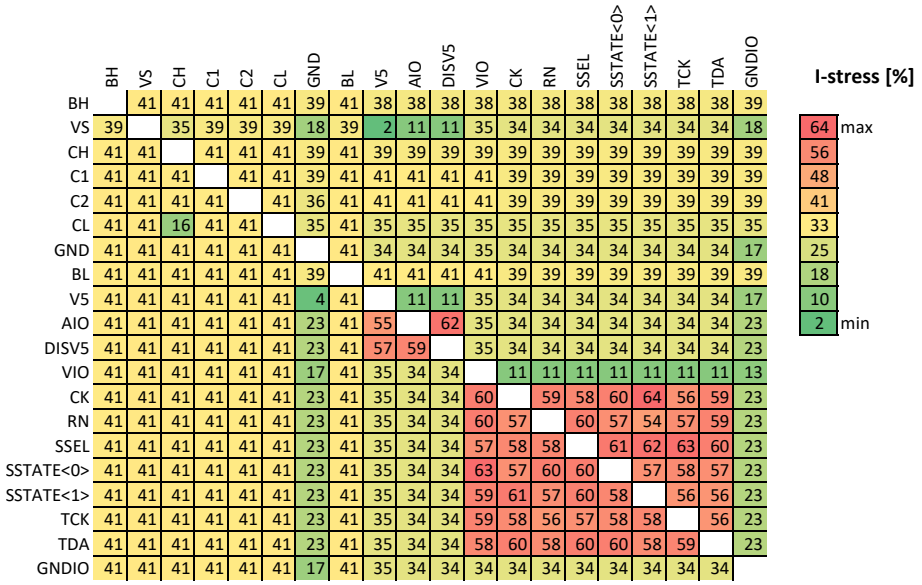


Figure 5.17: Complete ESD protection concept



	BH	VS	CH	C1	C2	CL	GND	BL	V5	AIO	DISV5	VIO	CK	RN	SSEL	SSTATE<0>	SSTATE<1>	TCK	TDA	GNDIO
BH		85	85	85	85	85	85	85	85	85	85	85	85	85	85	85	85	85	85	85
VS	85		84	85	85	85	76	85	41	42	42	78	78	78	78	78	78	78	78	76
CH	85	85		85	85	85	85	85	85	85	85	85	85	85	85	85	85	85	85	85
C1	85	85	85		85	85	85	85	85	85	85	85	85	85	85	85	85	85	85	85
C2	85	85	85	85		85	85	85	85	85	85	85	85	85	85	85	85	85	85	85
CL	85	84	70	85	85		84	85	84	84	84	84	84	84	84	84	84	84	84	84
GND	85	80	84	85	85	85		85	78	78	78	78	78	78	78	78	78	78	78	45
BL	85	85	85	85	85	85	85		85	85	85	85	85	85	85	85	85	85	85	85
V5	85	80	84	85	85	85	45	85		42	42	78	78	78	78	78	78	78	78	45
AIO	85	80	84	85	85	85	69	85	85		87	78	78	78	78	78	78	78	78	69
DISV5	85	80	84	85	85	85	69	85	86	86		78	78	78	78	78	78	78	78	69
VIO	85	80	84	85	85	85	62	85	78	78	78		42	42	42	42	42	42	42	62
CK	85	80	84	85	85	85	69	85	78	78	78	87		86	86	86	88	85	86	69
RN	85	80	84	85	85	85	69	85	78	78	78	87	85		86	86	86	85	86	69
SSEL	85	80	84	85	85	85	69	85	78	78	78	86	86	86		87	87	87	87	69
SSTATE<0>	85	80	84	85	85	85	69	85	78	78	78	88	86	87	87		85	86	86	69
SSTATE<1>	85	80	84	85	85	85	69	85	78	78	78	86	87	86	86	86		85	85	69
TCK	85	80	84	85	85	85	69	85	78	78	78	86	86	85	86	86	86		85	69
TDA	85	80	84	85	85	85	69	85	78	78	78	86	86	86	87	87	86	86		69
GNDIO	85	80	84	85	85	85	45	85	78	78	78	78	78	78	78	78	78	78	78	

Figure 5.18: ESD stress simulation results: $I_{TLP}= 3A$, voltage stress level pin to pin



	BH	VS	CH	C1	C2	CL	GND	BL	V5	AIO	DISV5	VIO	CK	RN	SSEL	SSTATE<0>	SSTATE<1>	TCK	TDA	GNDIO
BH		41	41	41	41	41	39	41	38	38	38	38	38	38	38	38	38	38	38	39
VS	39		35	39	39	39	18	39	2	11	11	35	34	34	34	34	34	34	34	18
CH	41	41		41	41	41	39	41	39	39	39	39	39	39	39	39	39	39	39	39
C1	41	41	41		41	41	39	41	41	41	41	41	39	39	39	39	39	39	39	39
C2	41	41	41	41		41	36	41	41	41	41	41	39	39	39	39	39	39	39	39
CL	41	41	16	41	41		35	41	35	35	35	35	35	35	35	35	35	35	35	35
GND	41	41	41	41	41	41		41	34	34	34	35	34	34	34	34	34	34	34	17
BL	41	41	41	41	41	41	39		41	41	41	41	39	39	39	39	39	39	39	39
V5	41	41	41	41	41	41	4	41		11	11	35	34	34	34	34	34	34	34	17
AIO	41	41	41	41	41	41	23	41	55		62	35	34	34	34	34	34	34	34	23
DISV5	41	41	41	41	41	41	23	41	57	59		35	34	34	34	34	34	34	34	23
VIO	41	41	41	41	41	41	17	41	35	34	34		11	11	11	11	11	11	11	13
CK	41	41	41	41	41	41	23	41	35	34	34	60		59	58	60	64	56	59	23
RN	41	41	41	41	41	41	23	41	35	34	34	60	57		60	57	54	57	59	23
SSEL	41	41	41	41	41	41	23	41	35	34	34	57	58	58		61	62	63	60	23
SSTATE<0>	41	41	41	41	41	41	23	41	35	34	34	63	57	60	60		57	58	57	23
SSTATE<1>	41	41	41	41	41	41	23	41	35	34	34	59	61	57	60	58		56	56	23
TCK	41	41	41	41	41	41	23	41	35	34	34	59	58	56	57	58	58		56	23
TDA	41	41	41	41	41	41	23	41	35	34	34	58	60	58	60	60	58	59		23
GNDIO	41	41	41	41	41	41	17	41	35	34	34	34	34	34	34	34	34	34	34	

Figure 5.19: ESD stress simulation results: $I_{TLP}= 3A$, current stress level pin to pin

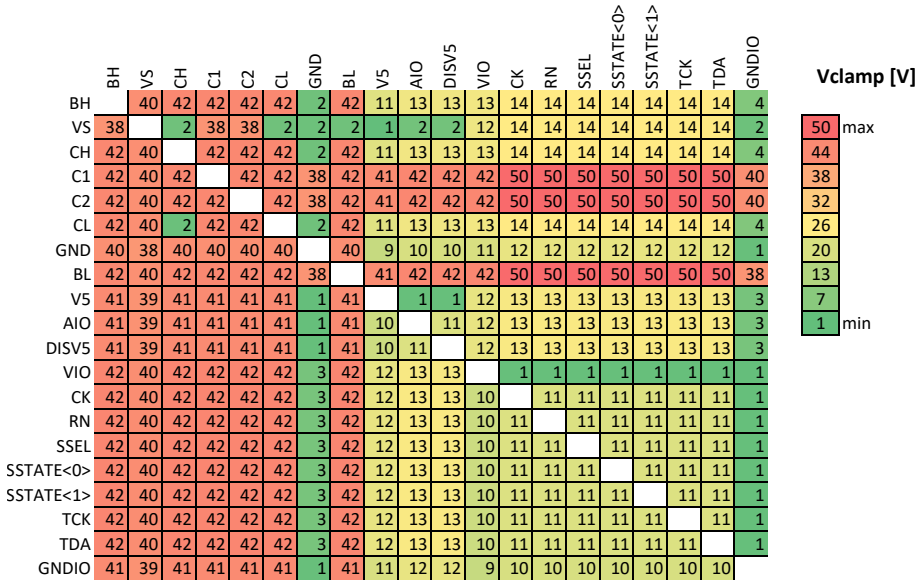
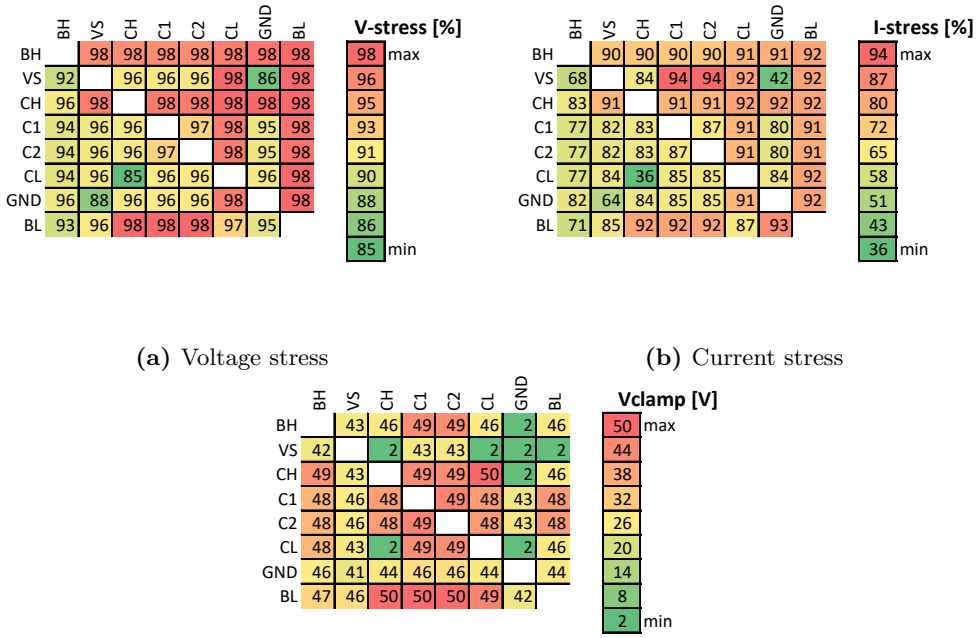


Figure 5.20: ESD stress simulation results: I_{TLP}= 3A, clamping level pin to pin

maximum acceptable level of I_{TLP}= 7A, as show in Fig. 5.21. Here, the maximum clamping level is 50V, which is also the minimum trigger level V_{trg} of the *nhvta* and *phvta* transistors used for the switches. The floating switch transistor $M_{N_{FS}}$ seems the most critical one, since it does not contain a reverse polarity diode, which is implemented in the high- and low-side switches to allow negative voltages w.r.t. the source of the switches. The reverse case for the floating switch (discharge path $CH \rightarrow CL$) is not critical, since simulated voltage and current stress levels for the drain-bulk diode of $M_{N_{FS}}$ are below the average with 85% and 36%, respectively. Overall, the current and voltage stress for the ESD-protection devices reach up to 94% and 98%, respectively, which indicates that the maximum of the acceptable TLP current for the test chip is at 7A. With Eq. 5.3, an HBM level of at least 10kV can be expected.

Typical simulated TLP stress curves are depicted in Fig. 5.22. In Fig. 5.22(a) the discharge from $VS \rightarrow GND$ directly shows the behavior of the HV-ESD clamp 1, while Fig. 5.22(b) depicts the reverse case. Here, with increasing TLP current, the parallel protection diode begins to limit at a voltage level of $\approx 1V$. From $\approx 2V$ onwards, the stacked drain-bulk diodes of the clamping stack of HV-ESD clamp 1 provides an additional current path, which decreases the path resistance further. The bus pins *BH* and *BL* stressed against each other, indicates a symmetrical operating window of $\pm 30V$ and a clamping of $\pm 50V$ at I_{TLP}= 7A, which is in accordance to the initial requirement drawn in Fig. 5.12. Another example is shown with by the discharge path from $BL \rightarrow GND$ and vice versa in Fig. 5.22(e) and 5.22(f), respectively. For $BL \rightarrow GND$, the curve is similar to

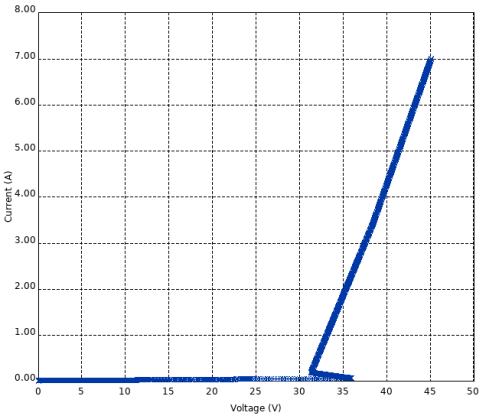


(a) Voltage stress **(b)** Current stress

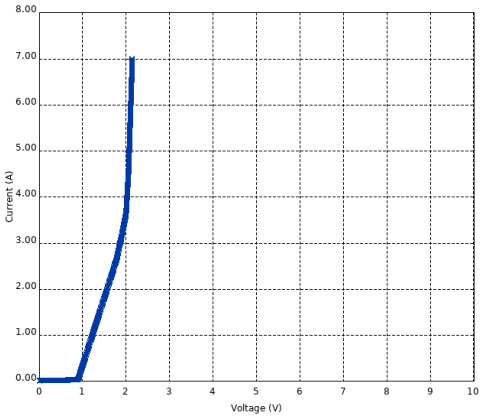
(c) Clamping voltage

Figure 5.21: ESD stress simulation results of HV section with I_{TLP}= 7A

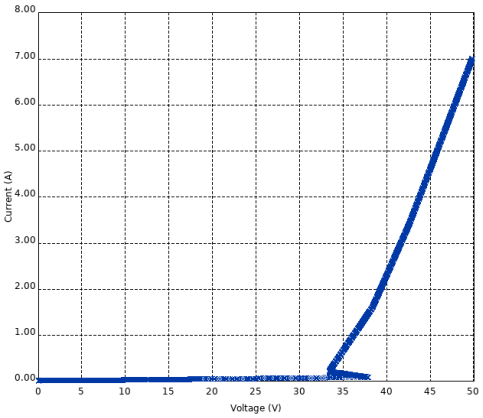
$VS \rightarrow GND$, just that it is right-shifted by one V_{f_D} because of the series-connected diode to HV-ESD clamp 1. In the reverse direction, shown in Fig. 5.22(f), the voltage is first growing after triggering HV-ESD clamp 3, but setback by $\approx 3V$ at $I_{TLP} \approx 1.4A$ because a concurrent discharge path opens. This is formed by the stacked drain-bulk diodes of HV-ESD clamp 2, the HV-ESD clamp 4 and a diode in series to pin BL. It triggers at higher voltages than the primary path because there is a higher voltage drop than one V_{f_D} across the stacked drain-bulk diodes HV-ESD clamp 2. Such a secondary path supports the energy dissipation during an ESD event in addition. It also exists from GND to $C1$ and $C2$.



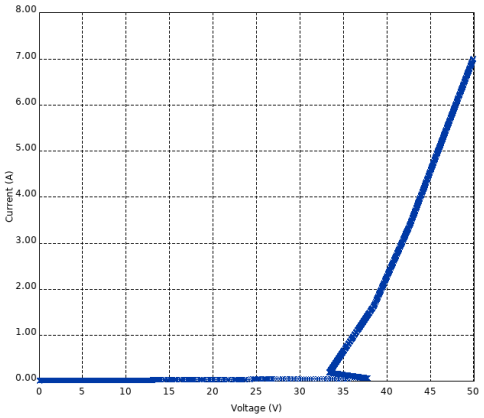
(a) $VS \rightarrow GND$



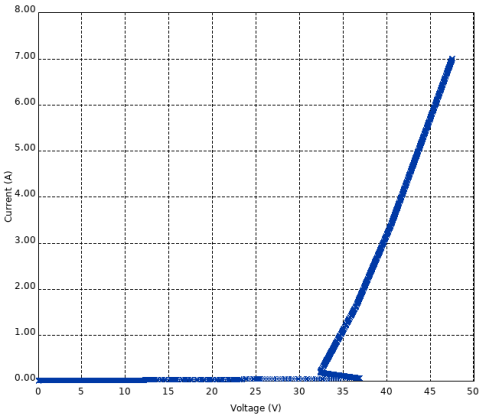
(b) $GND \rightarrow VS$



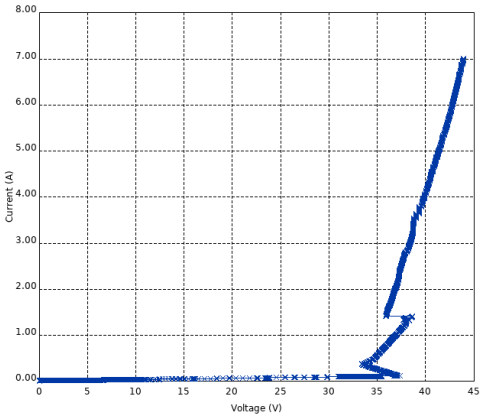
(c) $BH \rightarrow BL$



(d) $BL \rightarrow BH$



(e) $BL \rightarrow GND$



(f) $GND \rightarrow BL$

Figure 5.22: Representative TLP curves for different pin combinations

5.8 Physical arrangement

The transmitter test chip has been implemented in X-FAB's XT018 SOI technology (referring to Table 5.2). The outer supply ring is implemented in four traces, whereas two traces are stacked vertically. The upper traces are implemented in the upper thick metal layer, the lower ones by combining metals M4 and M5. The ring connects all ESD related elements and pad circuits, that are located below the ring structure in lower metal layers (M1 to M3). The pad-limited layout is depicted in the chip micrograph in Fig. 5.23. On the upper and rightmost periphery, the MV digital I/Os are located. Here *GND* is the outer upper, *VCORE* the inner upper, *GNDIO* the outer lower and *VIO* the inner lower trace of the ring. Leftmost and lower periphery host the HV I/Os. The ring in this area consists of *GND* which is the outer upper, *VS* the inner upper, *ESD rail N* the outer lower and *ESD rail P* the inner lower trace. Due to the planar wafer process, non-used areas are filled with dummy pattern, so that only elements of the upper thick metal layer are visible, like the top wiring. The HV-ESD clamps are located close to the HV I/Os on the left. Besides the macro-blocks of supply digital control and the transmitter, decoupling capacitors are implemented for *V5* and *VCORE* between the main blocks. Between the digital I/Os, a distributed *VCORE*-decoupling is added. The decoupling capacitors are implemented as unit elements formed by a stack of a P-type MV accumulation mode MOS varactor and a fringe capacitor, that uses metal layers M1 to M5. This unit capacitor provides a capacitance of $410fF$ for a terminal voltage $\geq 2V$. The amount of decoupling added to *V5* and *VCORE* is $\approx 350pF$ and $\approx 210pF$, respectively. To reduce the parasitic coupling of the digital control signals to the substrate and among each other, the wiring is done in metal M4 and M5. This is also supported by employing a higher distance between the metal traces than the minimum design rules allows. The circuit blocks are arranged as an L-shape to allow an easy plug-in of the receiver part in the upper-right corner for the subsequent transceiver test chip. The overall chip size is $1.97mm^2$.

The transmitter test chip has been assembled in a $4 \times 4mm^2$ quad flat narrow (QFN) package with 24 pins, where only 20 pins (5 per side) are used. This gives also the flexibility for a subsequent transceiver test chip, which requires more pins. Fig 5.24 shows the application diagram following the pin order of the package. Only few external components are needed. Besides the functional capacitors for CA and CP mode, there are external decoupling capacitors for the supply voltages $C_{DEC_{VS}}$ and $C_{DEC_{V5}}$. The *VS*-supply can be provided locally (dashed option) or by a DMI from the bus.

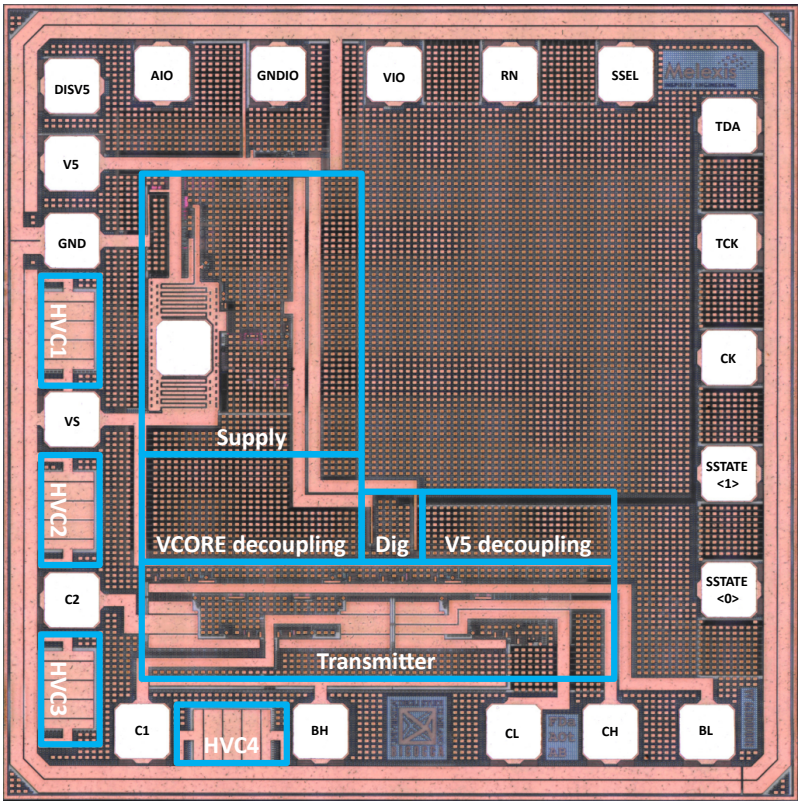


Figure 5.23: Chip micrograph of the transmitter test chip

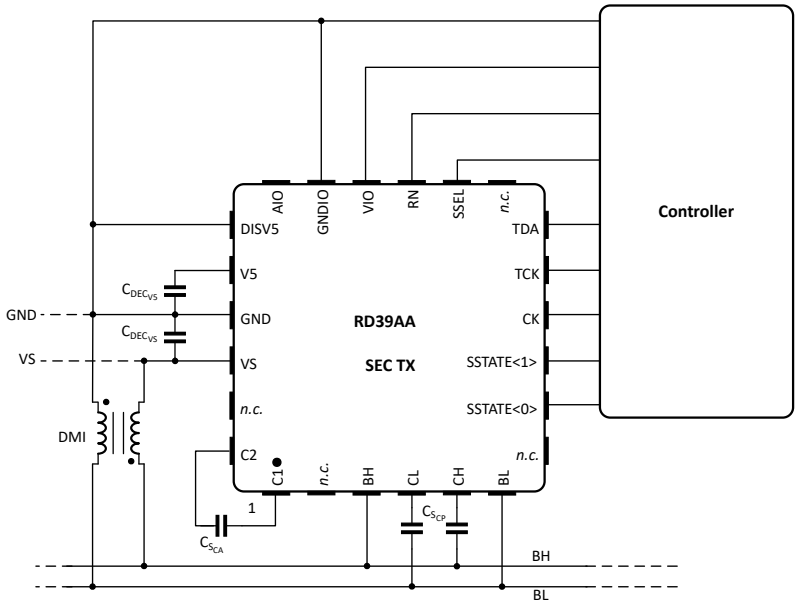


Figure 5.24: Transmitter test chip application diagram

5.9 Results

5.9.1 Top-level simulation

A top-level simulation verifies that all components are working together in the intended way. Therefore, a mixed-signal simulation has been done on the back-annotated netlist. The digital part was excluded from the extracted netlist to save computational efforts. The digital part was verified upfront, to ensure that the synthesized design matches the behavioral model implemented in Verilog. The simulation test bench is depicted in Fig. 5.25 and incorporates two TLP cables of $1m$ between the supply feed and the transmitter, as well as between the transmitter and the network termination. The cable model has 16 RLGC segments of the model which was developed previously. The termination was set to $R_T = 100\Omega$ and the inductor to $L_T = 100\mu H$.

A Verilog stimulus takes care of the setting of the test chip and controls the state of activity and selects the modulation approach to be used. As illustrated in Fig. 5.26, the transmission starts with three data packets of 16bit each, at $\approx 240\mu s$. Pins *BH* and *BL* are showing the intended CA modulation scheme. *C1* and *C2* show the charge alternation waveform. Because the C_S capacitors of the CP part are also present in the simulation setup, pins *CH* and *CL* are showing the same level excursion as *BH* and *BL*, although not actively driven.

At $\approx 300\mu s$, the next two data packets are sent in the CP format, since the control signal *SSEL* went high before. At this time step, the expected waveform from the CP approach can be seen. Charge and discharge of the capacitors lead to the typical waveform at pins *BH* and *BL*. Since pins *C1* and *C2* are Hi-Z during this period of time, there are small transients observable that are caused by small parasitic capacitances.

5.9.2 Chip measurements

The evaluation of the transmitter test chip was done for the static parameters first. As reported in [9], a Python-based test setup was built, which is running on a Raspberry Pi3, that is connected to the *VIO*-related control inputs of the test chip. With this setup, all relevant configurations were successfully confirmed. All measurements were done at room temperature for 7 devices. The performance of the supply block agrees with the simulated results according to Table 5.5. High- and low-side switches show an average R_{on} of 25Ω and 16Ω, respectively. The floating switch has an R_{on} of 10Ω. All switches show an off-state leakage current below $10nA$.

For the dynamic behavior, the board of the test chip was connected to the FPGA of the demonstrator. The receiver part of the demonstrator was employed to decode the messages from the bus. The encoder, which was previously used to control the switches of the transmitter part of the demonstrator, was modified in the sense that the switch control

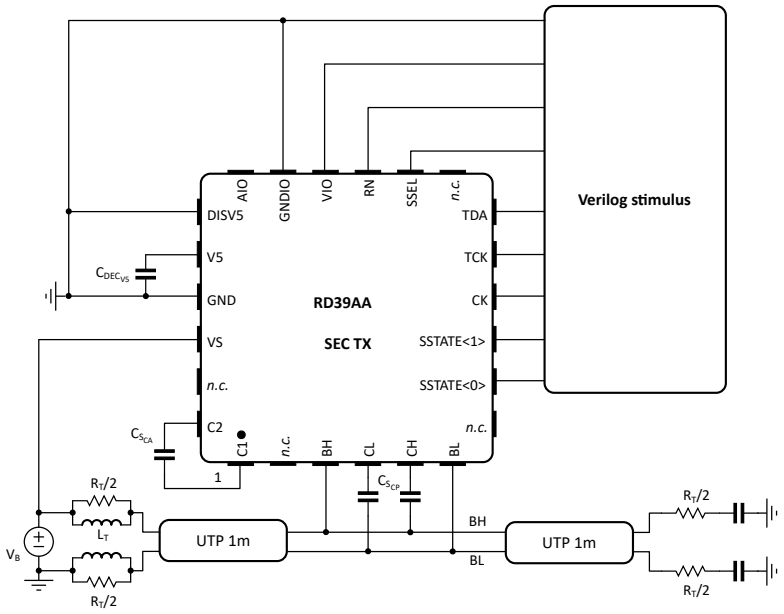


Figure 5.25: Top-level simulation schematic

signals *SP* and *SN* were re-directed as *SSTATE<1:0>* for the test chip. In addition, the clock *CK* for the test chip is generated in the modified encoder circuit, as listed in A.2.2.

As reported in [9], the bus *BH* and *BL* of the demonstrator and board of the test chip were connected by a UTP cable of different lengths. The FPGA was setup with the loop-back configuration that enables the transmitter test chip to send a PRBS stream. Simultaneously, the receiver of the demonstrator was decoding the information. In Fig. 5.27 the differential signal on the bus and the recovered clock and demodulated data is shown for both communication approaches at the receiver, that was connected by a $6m$ UTP cable to the transmitter.

Furthermore, communication tests with data rates up to 10Mbps, using smaller $C_S = 330pF, 180pF$ have been carried out. Due to the smaller portion of C_S on the overall capacitance, the amplitudes become smaller due to a smaller ratio of C_S/C_P. Overall, the dynamic behavior of the transmitter could successfully be validated with these tests.

5.9.3 ESD performance validation

After the evaluation of the test chip showed a good yield, an ESD test has been performed. The test was done on the *MK.1TE ESD and Static Latch-up Test System* from *Thermo Fisher Scientific*. Three groups of pin combinations were checked:

- all pins vs. pin *GND*,
- all pins vs. pin *VS*, and

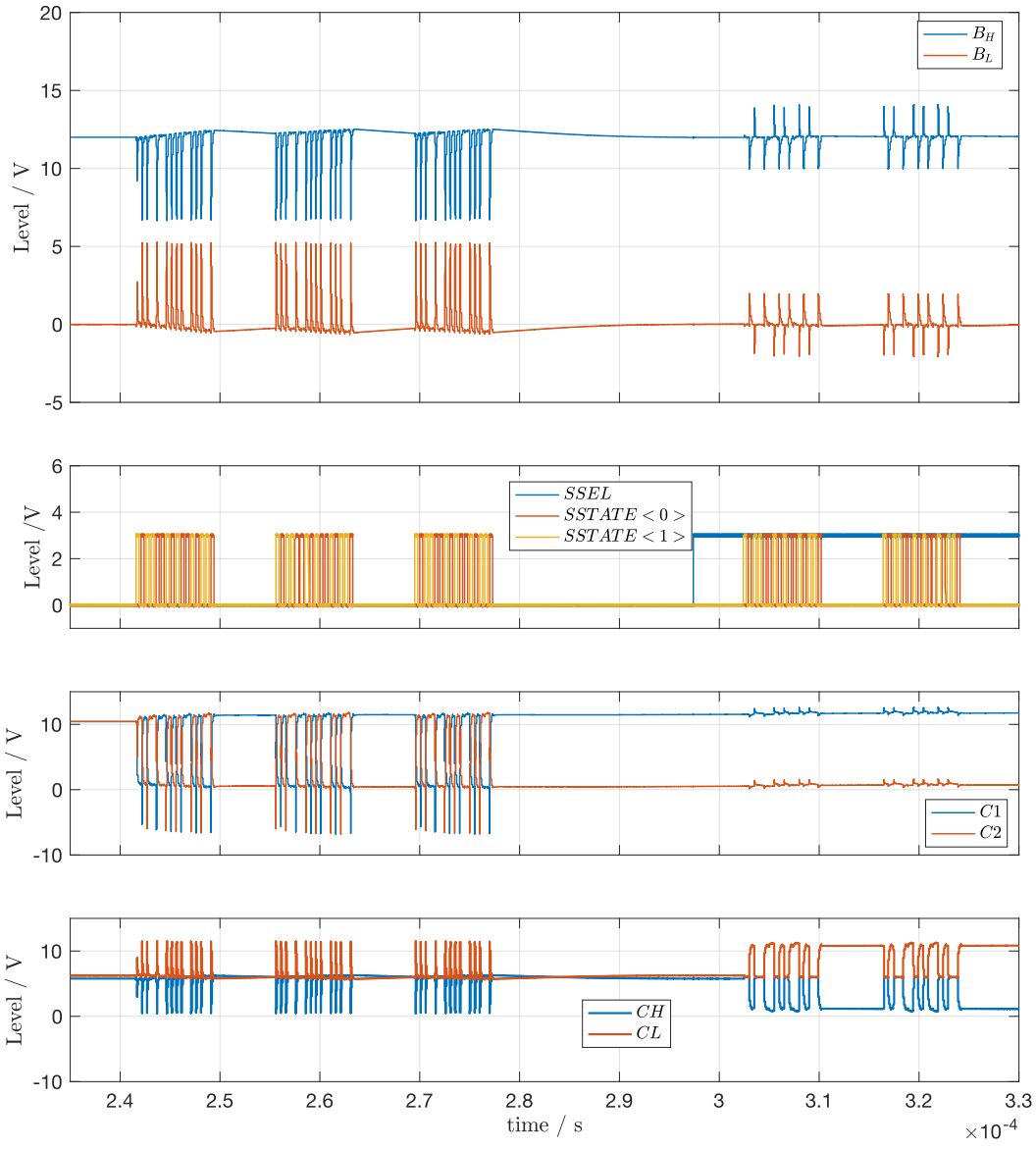
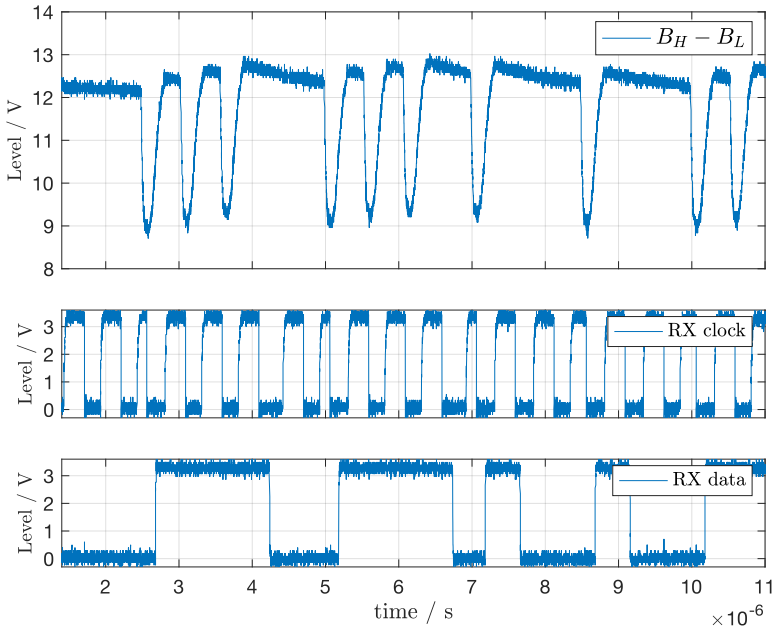
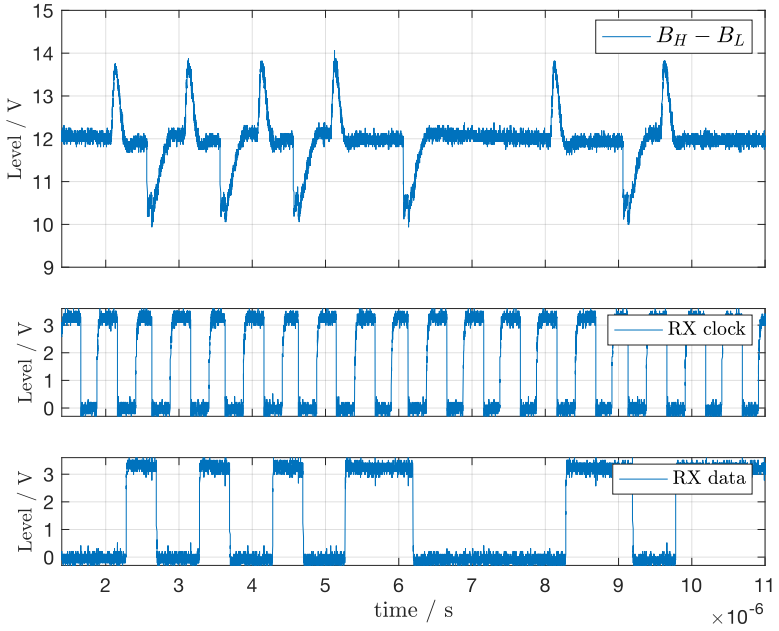


Figure 5.26: Top-level simulation result: CA and CP transmission waveforms



(a) $2Mbps$ communication using the CA approach, URZ encoding



(b) $2Mbps$ communication using the CP approach, Dicode

Figure 5.27: Measured waveforms at the receiver that was connected by a $6m$ UTP cable to the transmitter

- all pins vs. all.

Each of the combinations were verified with three test chips per step of the ESD-stress level. It started with HBM levels of $500V$ and $1kV$. The level was further incremented by $1kV$, up to $8kV$, which is the maximum level provided by the test system. As a result, 81 devices were checked. The following test procedure was applied:

1. the V-I curve of the concerned pin is measured vs. *GND* and *GNDIO*,
2. positive and negative HBM stress levels are sequentially applied, and
3. the measurement of 1) is repeated and compared to it.

Up to the level of $8kV$, no damage could be observed. Only minimal degradations are visible, as it can be seen, e.g., from Fig. 5.28(a), which shows the V-I characteristic of the *VS* pin. The small deviation of $10\mu A$, at $\approx 2.3V$, is located around the start-up of the supply block. It might hypothetically be linked to the fact that the internal decoupling of *VAUX* or *V5* was charged during the stress event, and hence the remaining charge changes the start-up dynamic during the curve tracing. Another example given in Fig. 5.28(b). Here, the curve tracing shows the characteristics of pin *C1*, which can be considered as an 'open' between $-30V$ and $30V$ w.r.t. *GND*. It should be noted here, that the continuity check of the test system is visible, since the active V-I curve indicates a negative resistance of $-100k\Omega$.

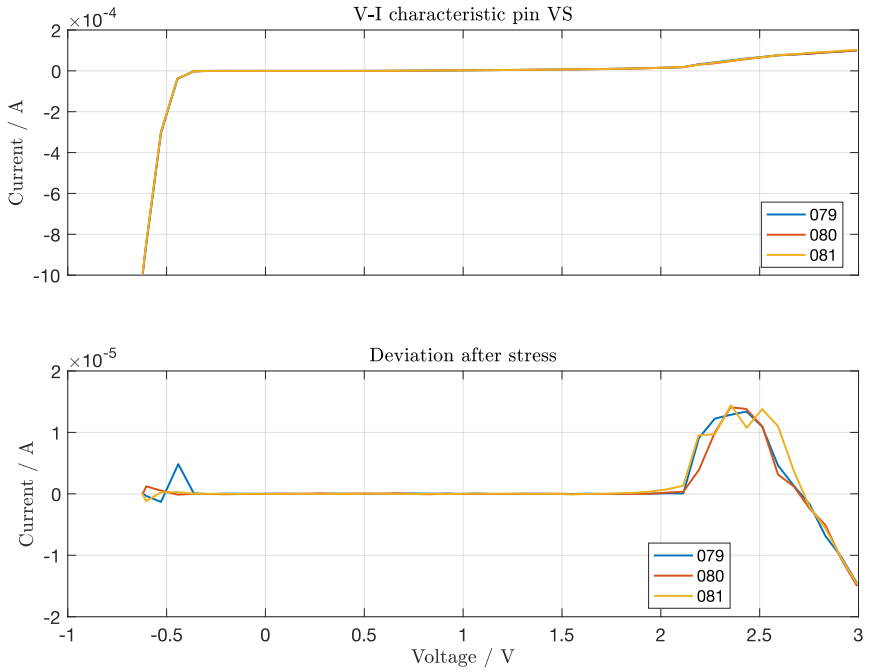
The peak deviations, measured in μA, for all pins of the three devices 79, 80 and 81, that have seen the $8kV$ pin-to-pin stress, are listed in Table 5.11. All values are within a small boundary of deviations, and were considered as 'pass' by the test system. No hard fail or damage could be observed.

As a result, it can be concluded, that the ESD-concept is working fine and even outperforms the critical simulations done in Section 5.7, that predicts a maximum ESD stress level of at least $4.5kV$ for the MV pins. The predicted ESD robustness of the HV-section, of at least $10kV$ could not be tested, due to the maximum achievable stress level of $8kV$ that can be applied with the available ESD test system.

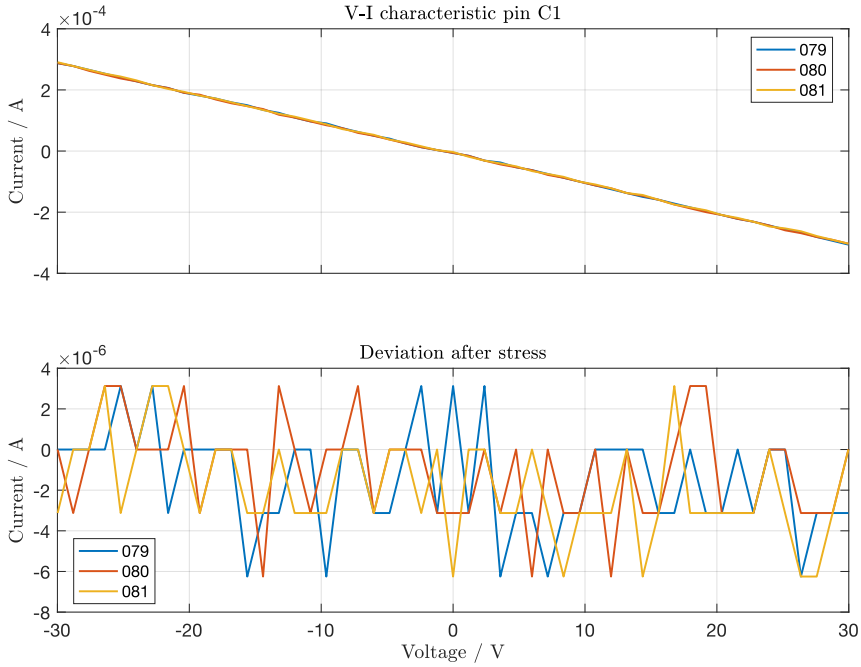
5.9.4 Conducted emission measurements

Similar as in Section 4.6.3 the transmitter test chip was characterized on EMC w.r.t. conducted emissions according to IEC 61967-4 [33]. The supply for the network is emulated by a $100\mu H$ DMI (*WE-DD 744870101*). As termination of the network, two series resistors of $R_T/4$ in parallel to the windings of the DMI are used. As depicted in Fig. 5.29, a bus DC-supply of $V_B = 12V$ is used to perform the measurements.

In a first case, the noise level of the setup is determined. The spectral view, shown in Fig. 5.30, indicates a low noise level in case the setup of the test chip is turned off (supply



(a) *VS→GND*



(b) *C1→GND*

Figure 5.28: Representative V-I curve tracings before and after a HBM stress of $8kV$

Table 5.11: Maximum deviation after 8kV HBM stress, measured during V-I curve tracing in μA

Device no.	*79*		*80*		*81*	
Pin	min	max	min	max	min	max
C1	-6.25	3.13	-6.25	3.13	-6.25	3.13
BH	-0.02	0.06	-0.03	0.15	-0.02	0.02
CL	-0.10	0.30	-0.31	0.02	-0.26	0.68
CH	-0.05	0.50	-0.22	0.11	-0.11	0.41
BL	-3.15	0.01	-3.06	0.02	-2.91	0.02
SSTATE<0>	-0.81	5.57	-1.05	6.64	-0.91	5.74
SSTATE<1>	-2.34	1.32	-2.90	1.34	-3.24	2.00
CK	-2.05	0.96	-3.39	0.89	-2.99	0.53
TCK	-0.58	4.74	-0.75	4.80	-0.71	4.50
TDA	-0.02	3.65	-0.02	3.66	-0.04	3.73
SSEL	-0.18	3.01	-0.10	2.93	-0.09	2.71
RN	-0.84	6.46	-0.01	5.04	-1.74	6.13
VIO	-2.22	0.01	-2.05	0.02	-2.83	0.01
AIO	-0.13	0.34	-0.02	0.76	-1.77	0.27
DISCV5	-0.06	0.23	-0.09	0.17	-0.03	0.15
V5	-0.55	0.08	-0.31	0.02	-0.82	0.06
VS	-14.56	13.41	-15.00	14.09	-14.63	14.41
C2	-6.25	6.25	-6.25	3.13	-6.25	3.13

and digital control from the FPGA). However, as soon as the FPGA is operational, a significant noise level is introduced. There are two cases shown, where:

1. the bus supply is off, so that only the control signals *SSTATE<1:0>* and *CK* are toggling with the data to be transmitted, and
2. the FPGA is in configuration mode, where the control signals are quiet.

In both cases, a noise floor is introduced, mainly due to the operation of the FPGA itself. That is likely caused by the setup, since still a lot of wiring between the test board and the FPGA board is required. For this reason, it is not possible to predict the emission level to a high level of confidence. A complete integration of the system, meaning that the control is completely provided internally by the chip, is more favorable in this aspect, since it would reduce the coupling between the control circuitry and the bus.

The conducted emission tests have been performed with the PRBS implementation in the FPGA as described in Section 4.5.1. An emission spectrum for a data rate of $2Mbps$ is shown in Fig. 5.31. It shows the result for a C_S of $820pF$ for the CA mode using normal edge encoding as well as URZ encoding. Both encoding schemes result in the same spectral

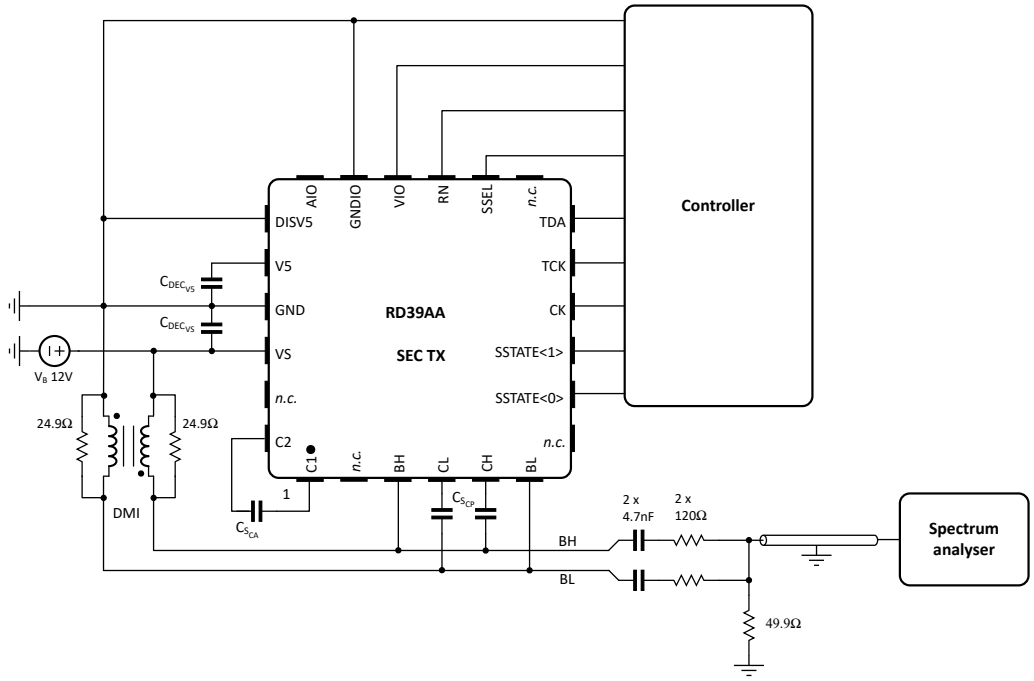


Figure 5.29: Conducted emission measurement schematic using the 150Ω-coupling network according to IEC 61967-4

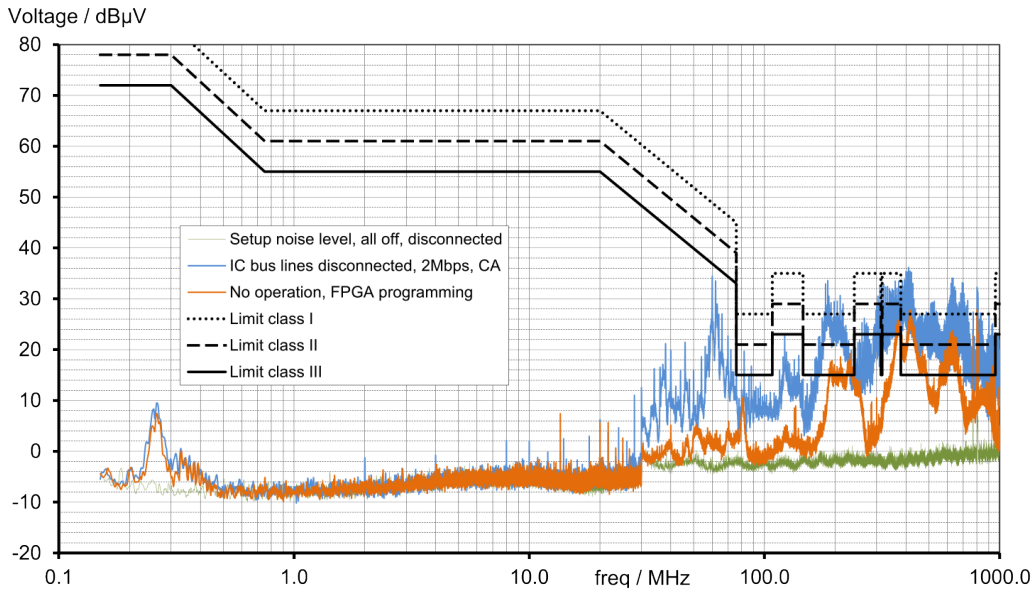


Figure 5.30: Conducted emission noise level

representation. This has been confirmed as well for data rates of $1Mbps$ and $5Mbps$. Consequently, only the spectrum for the edge encoding is further used. The emission in CA mode shows a compliance to the limit of class I defined in IEC 62228-3 [14] up to $76MHz$. At higher frequencies, the defined spectral mask is violated. However, this might be attributed to the non-ideal setup because the used evaluation board was not primarily designed for EMC measurements. As indicated by the noise measurement, a significant contribution comes from the operation of the FPGA and its delivered control signals for modulating the test chip. In CP mode, the spectrum is lower, so that class I can be reached until $146MHz$. The advantage of the CP approach, of a lower power transfer compared to the CA mode, results in a lower emission level. Above $\approx 75MHz$, the contribution of the setup is dominating. Both modes have been additionally measured with $C_S = 180pF$ and $330pF$, as shown in Fig. 5.32 and 5.33. At frequencies below $1MHz$, high C_S have a higher emission level due to the higher power consumption of the communication. At higher frequencies, the differences are negligible. As a result, it can be concluded that the symmetry, offered by the integrated solution, when compared with the discrete setup of the demonstrator (Fig. 4.17), yield to a significant improvement of the conducted emissions below $\approx 30MHz$.

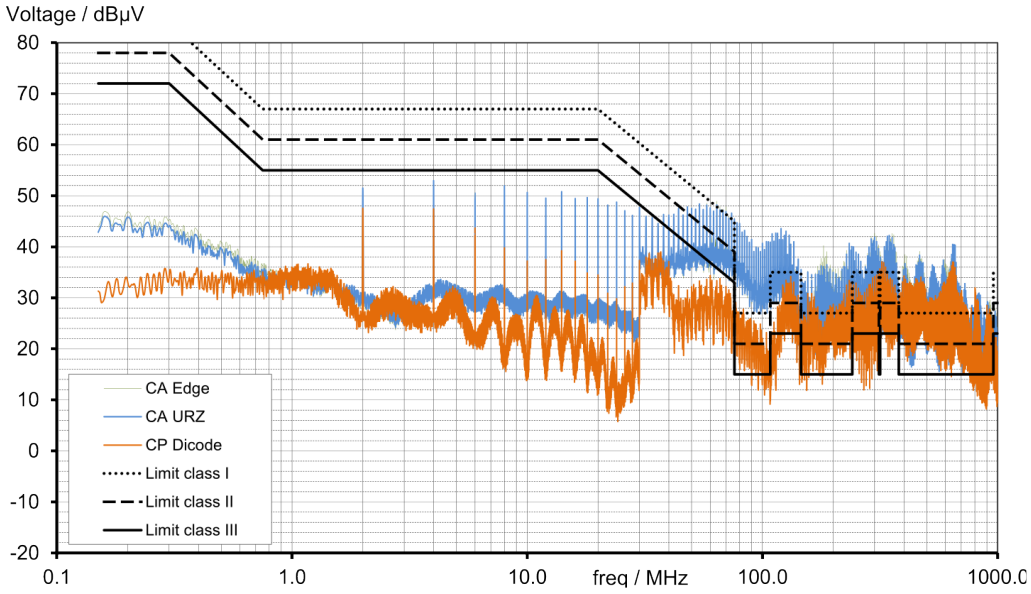


Figure 5.31: Conducted emission levels in CA and CP mode at $2Mbps$ and $C_S = 820pF$

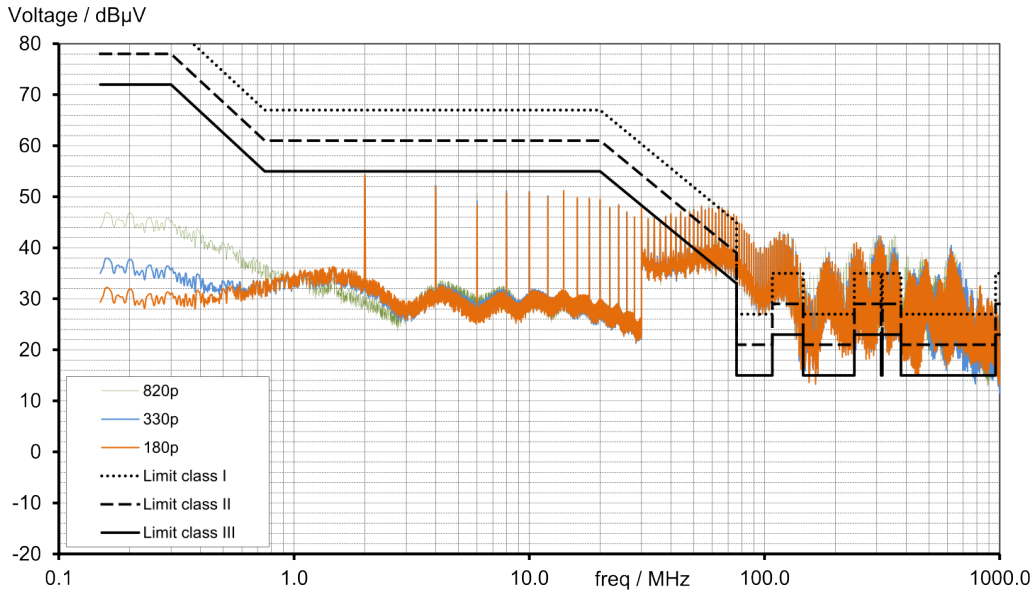


Figure 5.32: Conducted emission levels in CA mode at $2Mbps$ and different C_S

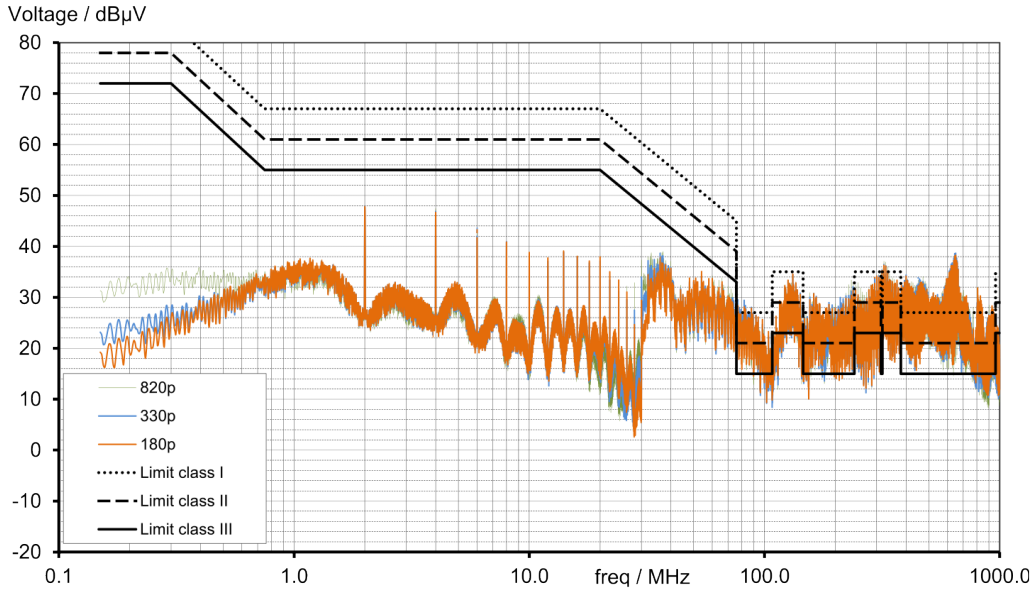


Figure 5.33: Conducted emission levels in CP mode at $2Mbps$ and different C_S

CHAPTER 6

Transceiver Test Chip

In this chapter, an integrated solution for a full transceiver, compliant to the proposed CA and CP approaches, is described. A block level receiver implementation is suggested, followed by the necessary extensions regarding the transmitter test chip. The composition of the test chip and its experimental results finalizes this chapter.

6.1 Receiver

The receiver is extracting the data signal from the bus lines. Because of the differential nature of the baseband signaling, it is beneficial to implement the receiver chain completely in a differential fashion as well. This is especially important for a reliable reception under large common mode signals on the bus, such as baseline wander and coupled common mode interferers. Different from the receiver chain implemented in the demonstrator, as described in Section 4.3, the integrated solution is benefitting much more in terms of matching than a discrete solution. Because the elements on the same chip are fabricated with identical processing steps. Hence, all circuit blocks in the reception chain are kept fully differential. A system-level schematic of the receiver is depicted in Fig. 6.1. By contrast to the discrete solution, the gain is realized by a capacitive divider in open loop, whose gain can be adjusted between of $-30dB$ and $-20dB$. This offers the advantage that the differential signal between BH and BL is scaled, as well as the DC component is removed, so that an MV buffer can maintain the differential signal (gain of $\approx 0dB$) before a signal discrimination is performed. As comparators, differential latches are suitable because of the inherent conversion and synchronization to digital domain. A well-known implementation is the StrongARM latch topology [39]. It is a sampled dynamic latch where the branch which conducts first disconnects the other. However, the hysteresis might be linked to symmetry and mismatches in the circuit. But an intended offset in terms of capacitive load can be added to one branch more than to the other, to introduce a hysteresis. Since the used wafer technology also offers tuneable / programmable capacitors in form of accumulation mode varactors, as mentioned in Table 5.2, a programmable hysteresis is implemented as reported in [9] to adjust the hysteresis according to the application. However, the

CMRR of a StrongARM latch is not very high. Therefore, a buffer with sufficient CMRR is needed between the capacitive dividers at the input and the latches. As reported in the implementation [9], a CMRR of $\approx 40dB$ is achieved by a resistively degenerated differential pair, whose output common mode level is adjusted to the input common mode of the latches.

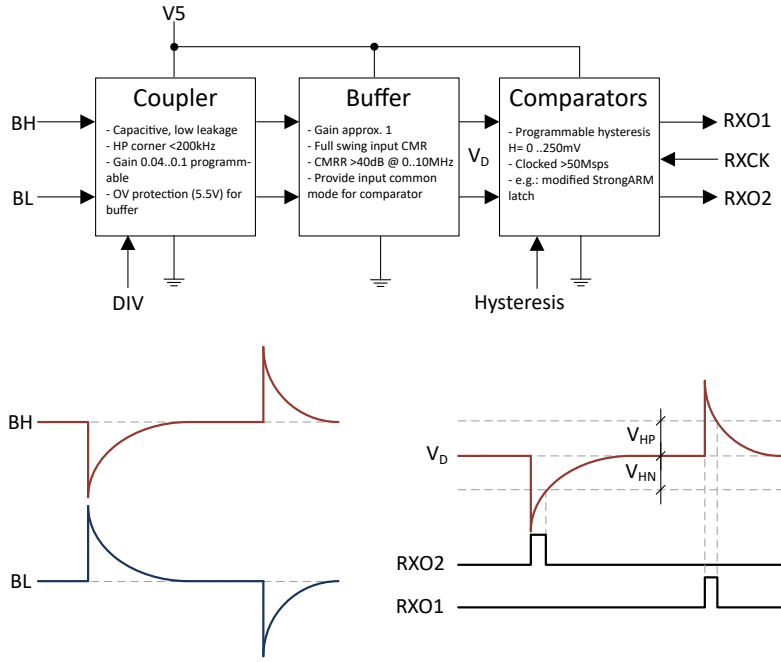


Figure 6.1: Receiver system level diagram

The clock for the comparators is provided by an external source connected to pin *RXCK*. By this way, the FPGA is controlling the latches by its system clock. To allow a sufficient oversampling, the latches and the related I/O circuit are designed to reliably reach $50MSps$. The output of the latches are stored in subsequent flip-flops, to toggle the output only when the received signal crosses the threshold. Internally, the receiver is supplied from *V5*. This allows enough headroom for the StrongARM latch operation. Consequently, the digital interfaces to/from the receiver block are in the *V5* domain.

6.2 Chip architecture

Based on the results obtained with the transmitter test chip, almost all components can be re-used without changes. This is valid for the supply and the transmitter blocks as it can be seen from Fig. 6.2, compared to the transmitter chip architecture, previously shown in Fig. 5.6. In this test chip implementation, three additional pins are required: the receiver output channels, *RXO1* and *RXO2*, as well as the sampling clock input *RXCK* for the

receiver. Those pins are located in the upper-right corner so that they are:

- close to the receiver part according to the floor planning and,
- the available pinout / chip layout of the transmitter test chip can highly be re-used.

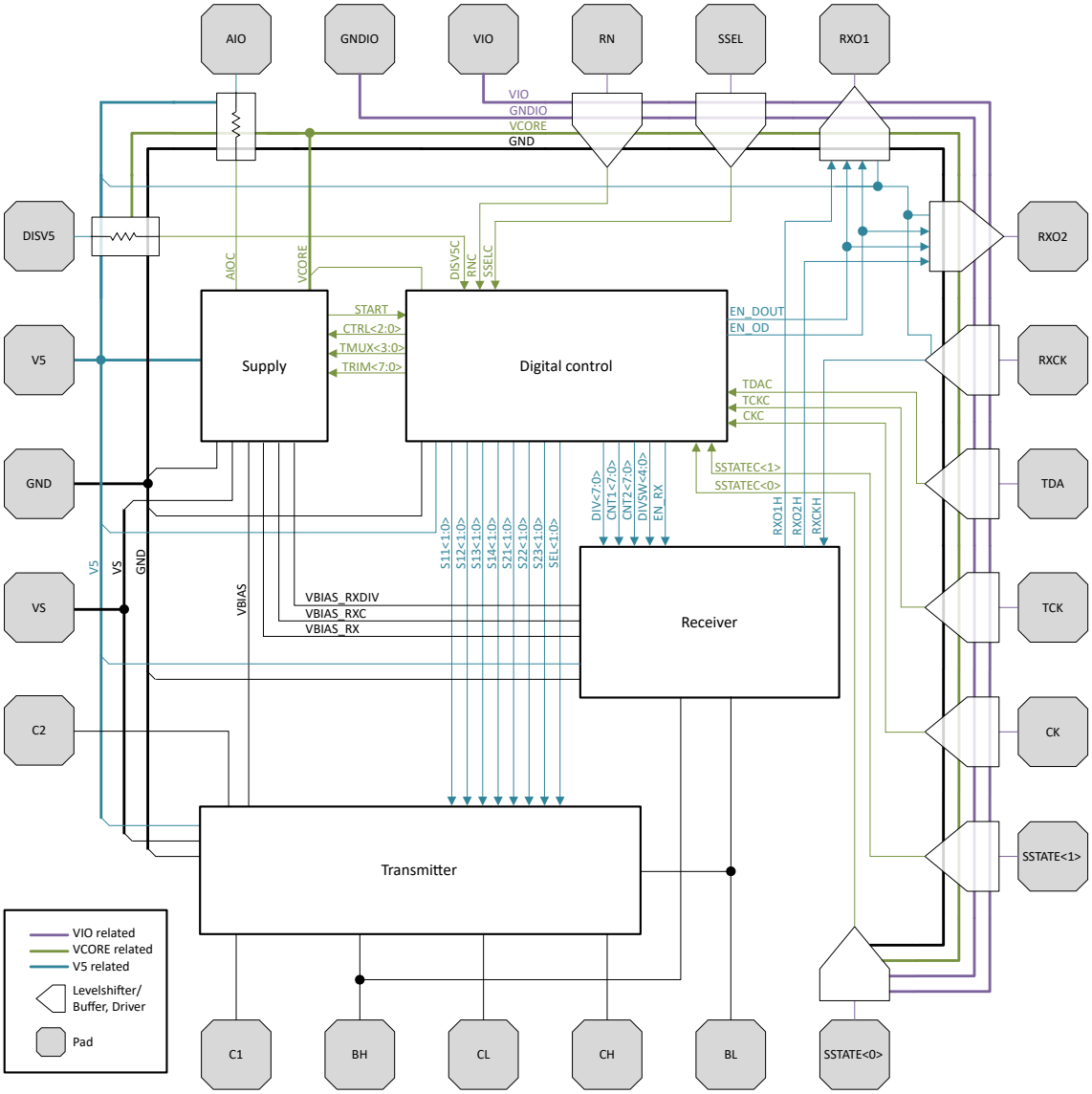


Figure 6.2: Top-level block diagram of transceiver test chip

6.3 Digital control

The digital control uses the same states as in the transmitter test chip, since the receiver operation is independent of the state of activity of the switches. Therefore, the control and

configuration of the receiver is completely done by sending the configuration data to the shift register *TMREG*. Compared to the transmitter test chip, additional control signals are required by the receiver part, as listed in Table 6.1. As shown in the implementation schematic of the digital in Fig. 6.3, the outputs to the receiver are level-shifted to the *V5*-domain. Some spare control signals are added, intended to support potential add-ons requested during the design of the test chip. However, those spare signals are not being used, but will remain for potential re-spins of the test chip. The Verilog code used for the synthesis, place, and route of the digital part is listed in A.3.1.

Table 6.1: Additional control signals in the transceiver test chip

Signal	Description
DIVD<7:0>	Capacitive divider ratio, upper nibble *BL*-related, lower *BH*-related
DIVSW<4:0>	Control of capacitive divider outputs
CNT1<7:0>	Hysteresis setting for receiver channel 1
CNT2<7:0>	Hysteresis setting for receiver channel 2
EN_RX	Enable of the receiver
EN_DOUT	Enable of the digital output pins *RXO1*, *RXO2*
EN_OD	Enable of the open-drain mode of the digital output pins
SPARE<7:0>	Spare output for future use

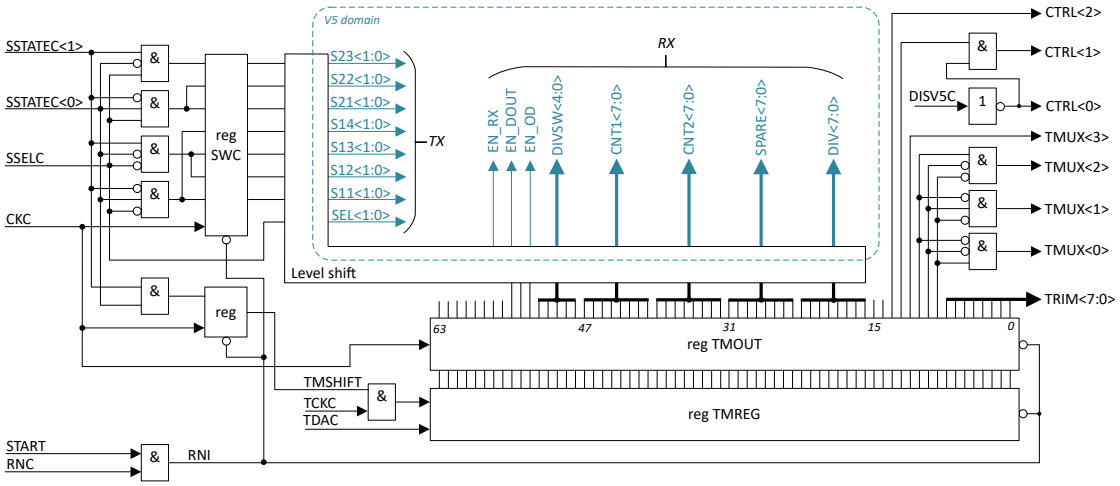


Figure 6.3: Block schematic of the digital control for the transceiver test chip

6.4 ESD protection

Since the evaluation of the transmitter test chip showed very promising results, the same concept is implemented also in the transceiver test chip. There are two digital output pins and one digital input required in addition. These pins are externally referenced to the *VIO*-domain and are internally shifted to the *V5*-domain. As an indication, the internal signal name contains a 'H'-letter at the end of the signal name, similar to the 'C'-letter when an external signal is translated to the *VCORE*-domain, as mentioned in Section 5.6. The required extension of the ESD-concept is already shown in Fig. 5.17, indicated by the dashed red rectangle and the ')*' indication.

An ESD simulation based on the *XESDC* tool [36] was also performed for this test chip, to verify the concept and design of the protection scheme. The simulation of the complete netlist of the chip, with a TLP-current I_{TLP}= 3A applied between every pin combination, showed that here also all relevant ESD stress is absorbed by the protection scheme, which confirms the functionality of the designed approach. A summary of the voltage and current stress as well as the clamping level at I_{TLP}= 3A for every pin combination is shown in Fig. 6.4-6.6. Since the HV part of the test chip is netlist-wise identical, the simulation result from Section 5.7 can also be applied here. Consequently, the same HBM-ESD compliance level as in the transmitter test chip can be expected.

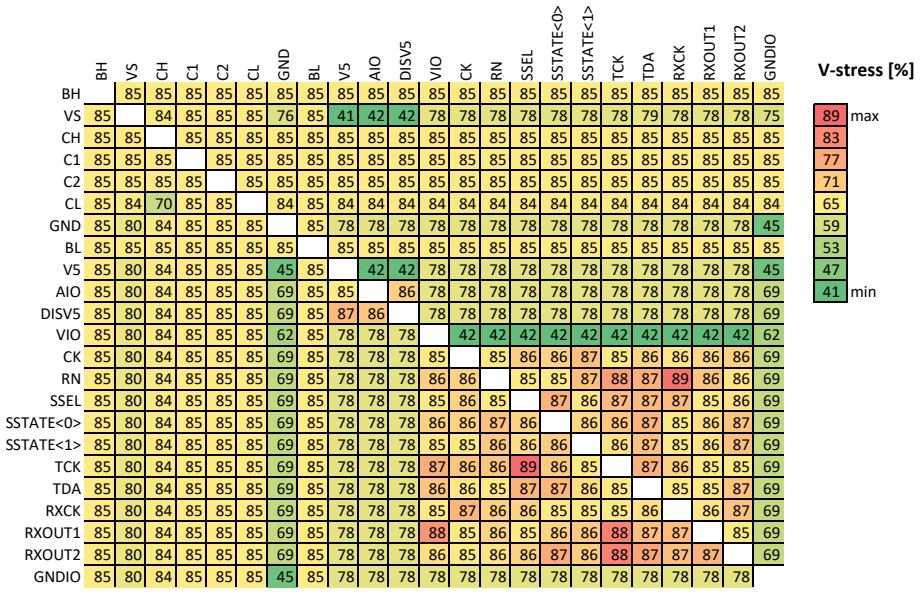


Figure 6.4: ESD stress simulation results: I_{TLP}= 3A, voltage stress level pin to pin

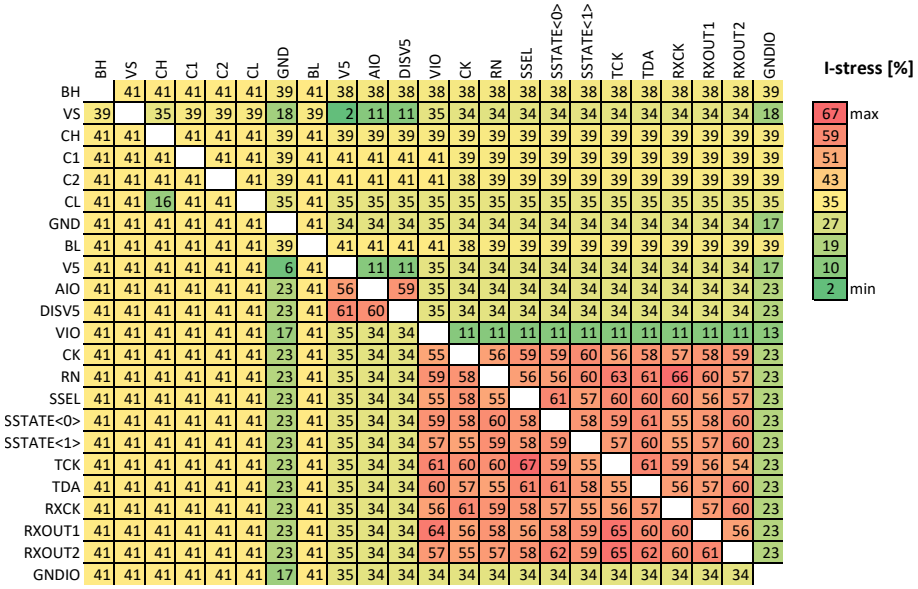


Figure 6.5: ESD stress simulation results: I_{TLP}= 3A, current stress level pin to pin

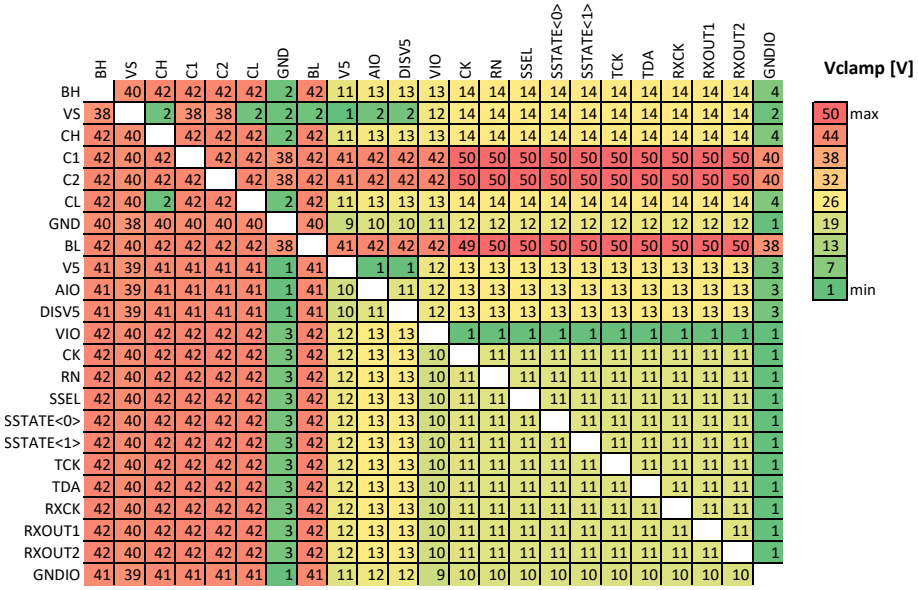


Figure 6.6: ESD stress simulation results: I_{TLP}= 3A, clamping level pin to pin

6.5 Physical arrangement

The transceiver test chip uses the same infrastructure as the transmitter test chip that already reserved some area in the upper right of the layout. Besides the layout effort for the receiver part, the necessary re-arrangements are limited to the pad ring, the larger digital part and the decoupling capacitor placement. The chip micrograph is depicted in Fig. 6.7. The overall chip size is $1.97mm^2$, that is the same as the chip size of the transmitter test chip.

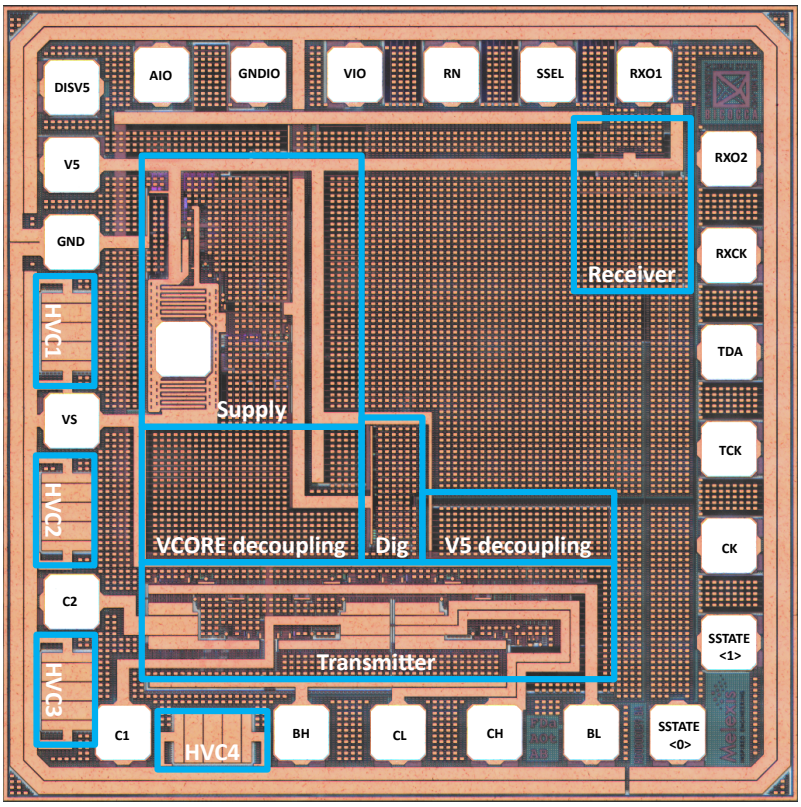


Figure 6.7: Chip micrograph of the transceiver test chip

The transceiver test chip is assembled in a $4 \times 4mm^2$ QFN package with 24 pins, where only 23 pins are used. Fig 6.8 shows the application diagram following the pin order of the package. Only few external components are needed. Besides the functional capacitors for CA and CP mode, there are external decoupling capacitors for the supply voltages $C_{DEC_{VS}}$ and $C_{DEC_{V5}}$. The *VS*-supply can be provided locally (dashed option) or by a DMI from the bus.

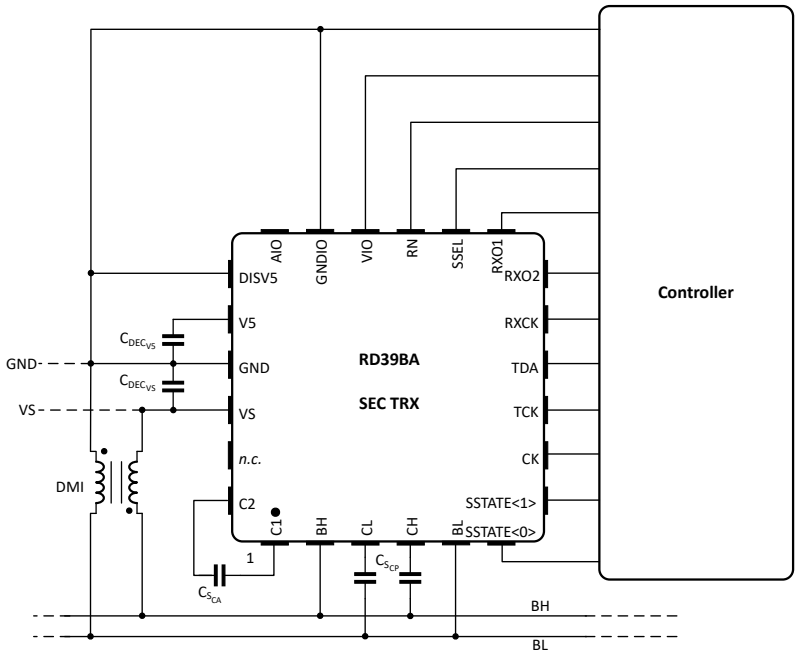


Figure 6.8: Transceiver test chip application diagram

6.6 Results

6.6.1 Top-level simulation

The transceiver test chip has been verified with the back-annotated layout. A top-level simulation, using two transceiver test chips, is shown in Fig. 6.9. The transceiver, which is acting as a transmitter, is located at the supply feed of the bus. The transceiver, that acts as a receiver, is connected by a UTP cable of $1m$. The cable model derived in Section 2.2 was also applied in his simulation with a segmentation of 16. The switched capacitors were set to $C_{S_{CA}} = 820pF$ and $C_{S_{CP}} = 680pF$, for CA and CP mode, respectively. The upper trace shows the bus signals at the receiver side. The receiver is set to an input division of 7 and the hysteresis for receiver channels 1 and 2 were set to $150mV$. The input clock on pin *RXCK*, which samples the latches, was running at $20MHz$. A first CA transmission is starting at $170\mu s$. Receiver channel 2 is decoding the pulses and output them on pin *RXO2*. Receiver channel 1 is silent in this case, since no positive pulses are available in this mode. It can also be seen that the baseline wander is not leading to any false detection, since it is filtered by the internal AC-coupling in the receiver chain. At $188\mu s$, the CP mode is entered with the rising edge of *SSEL* at the transmitter, so the next transmission starts at $\approx 194\mu s$. Now, both receiver channels detecting the intended pulses, as it can be seen by the alternating behavior between pins *RXO1* and *RXO2*.

This complex mixed-signal simulation, that includes two of the test chips simultaneously,

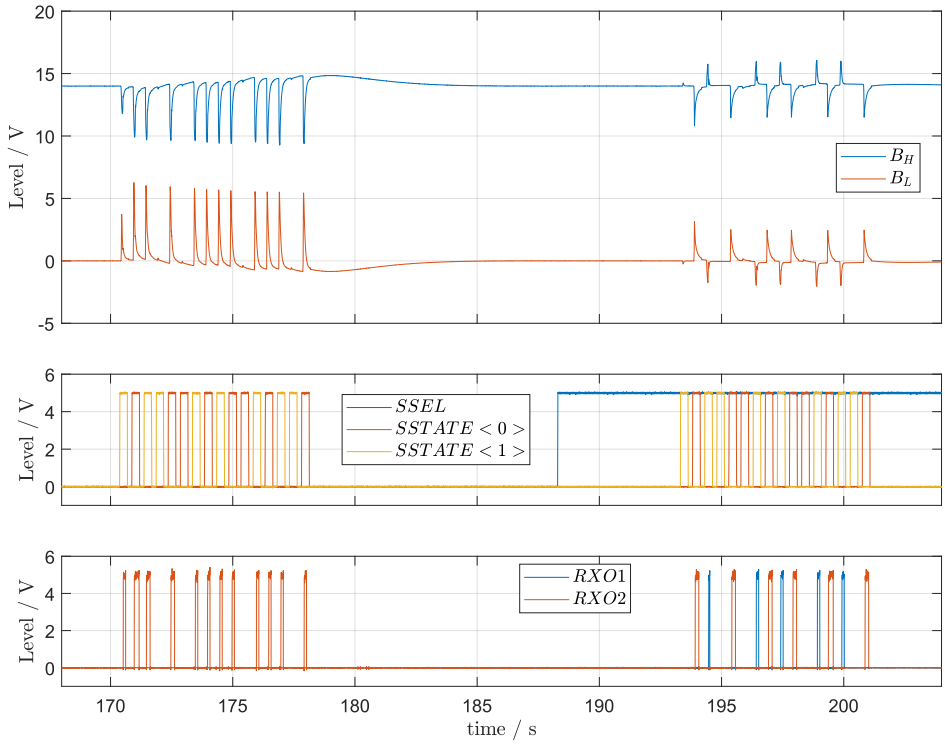


Figure 6.9: Layout-extracted top-level simulation of two transceiver test chips, participating in the network, separated by a $2m$ UTP cable

confirms that the transceiver implementation should work as expected. More details on the receiver part implementation and simulation results are reported in [9].

6.6.2 External digital control

To evaluate the transceiver test chip on the different settings which are accessed by *TMREG*, the external control is shared between the FPGA, which is located on the demonstrator board, and a Raspberry Pi3 board. The latter controls all quasi-static settings, such as the choice of the transmission approach (via *SSEL*) and the test register setting. *SSEL* is also applied to the FPGA so that encoder and decoder can be reconfigured without reprogramming the FPGA for a dedicated modulation *SCHEME*. The Python scripts used on the Raspberry Pi3 are described in [9].

The dynamic control for the transmitter and receiver part of the transceiver test chip is implemented in the FPGA. The sample clock *RXCK* for the StrongARM latches of the receiver is provided by the FPGA's master clock of $100MHz$ divided by *RXCK_DIV*. In the characterization measurements, the *RXCK_DIV* is set to 2. Fig. 6.10 shows the block diagram of the digital circuit implemented in the FPGA. Mainly, encoder and monitor circuit differs from the implementation described in Section 4.5.1.

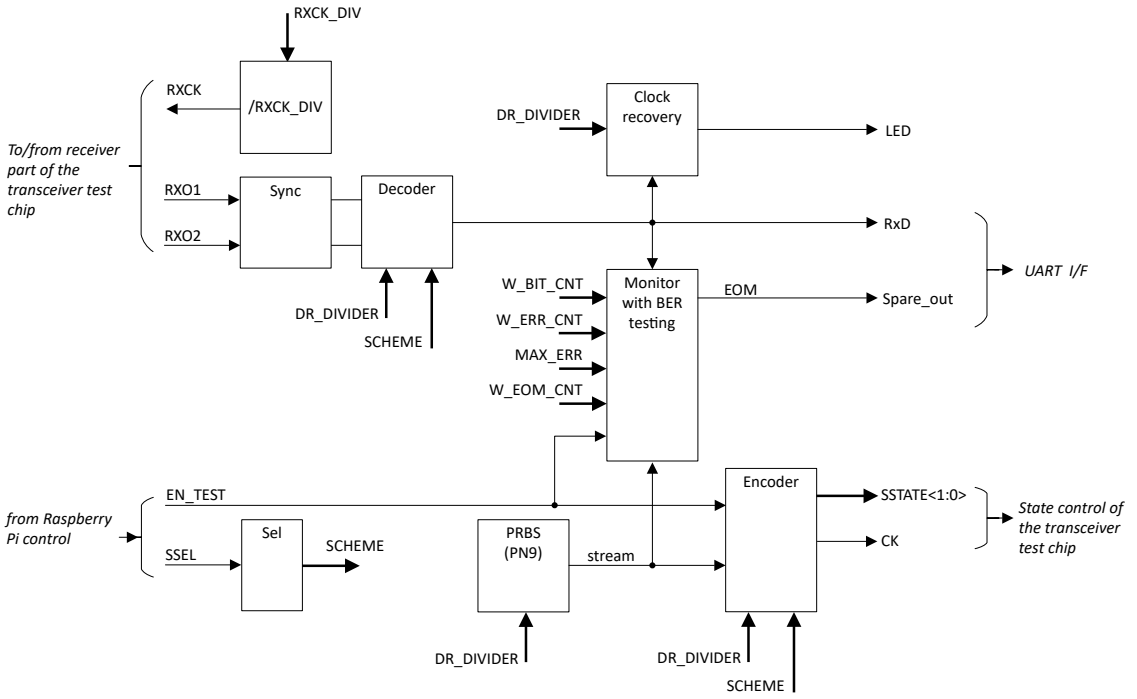


Figure 6.10: Block diagram of the loop-back implementation

Now, the encoder needs to enter in shift state (refer to Table 5.6) upon the L/H transition of *EN_TEST*. This enable signal is provided by the Raspberry Pi3 in case a new configuration is requested to be loaded to *TMREG*.

The monitor circuit contains bit and error counters, which are aimed to evaluate the bit error rate BER. This is important for more complex evaluations where the communication quality is used in an automated test environment, such as a direct power injection (DPI) test as described in Section 6.6.4 afterward. During the BER test, $2^{W\_BIT\_CNT}$-1 sent and received symbols are compared. If a detected symbol is unequal to the transmitted symbol, a W_ERR_CNT-bit wide error counter is incremented. At the end of a BER measurement cycle, the error count is compared with the maximum permitted errors, MAX_ERR. In case the error count is exceeding this limit, the BER test is declared as fail.

Each measurement cycle that passes the BER criterion, is reported as a 1-pulse with a duration of $[2^{W\_EOM\_CNT}\text{-}1] \times 10ns$ at the end-of-measurement signal EOM, which is available on the *SpareOut* of the demonstrator board. In case of a failing test, the pulse duration is halved.

For more details, the Verilog code of the external control implemented in the FPGA, can be found in Section A.3.2.

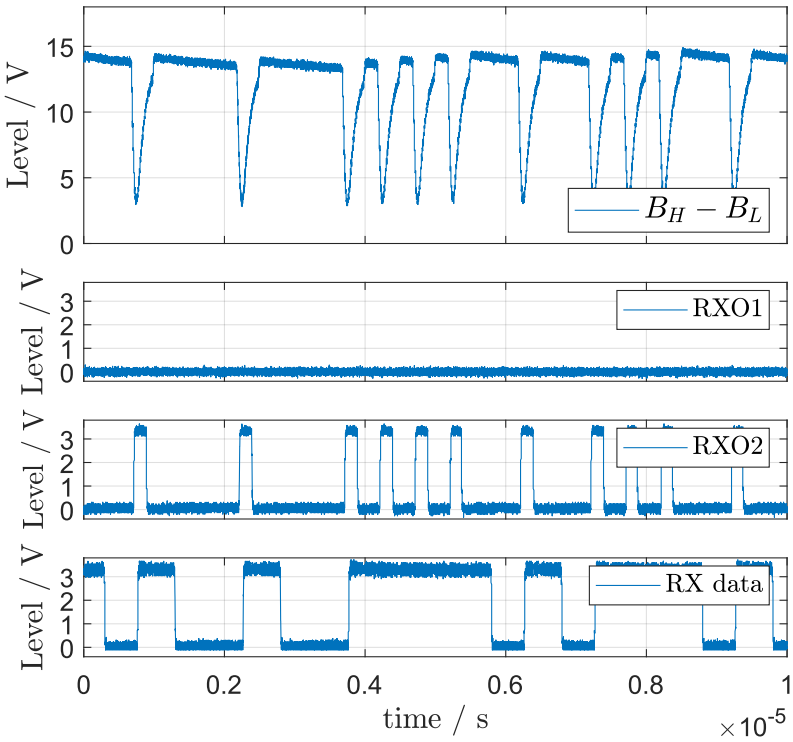
6.6.3 Chip measurements

The transceiver test chip was measured on a characterization board, indicated by the gray area in Fig. 6.12. With a C_S of $820pF$ and a typical setting according to Table 6.2, the waveforms shown in Fig. 6.11(a) at $DR = 2Mbps$ could be observed. In CA mode, only the second RX channel is used because only *RXO2* carries the received signal. The lower trace shows the decoded data from *RXO2*. Fig. 6.11(b) shows the receiver outputs during CP mode, using similar settings according to Table 6.2. Furthermore, the data could be decoded successfully from both outputs, *RXO1* and *RXO2*. The receiver operates as expected. More measurement details can be found in [9].

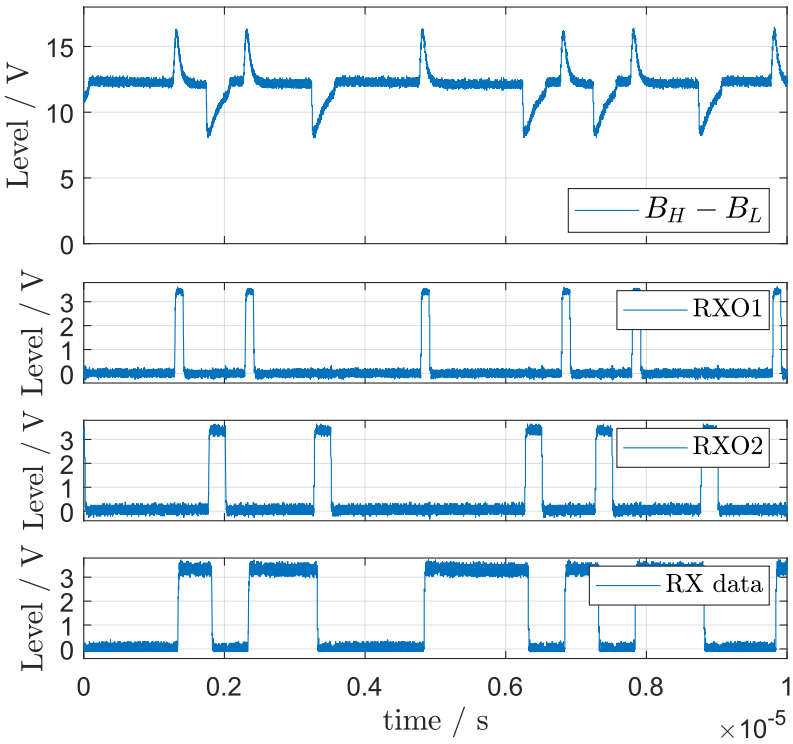
Table 6.2: Receiver settings for measurement in CA mode

Signal	Setting	Value[1]	Description
DIVD	0xff	14.9	Capacitive input divider ratio
CNT1	0x0f	220mV[2]	Hysteresis RX channel 1
CNT2	0x70	-85mV	Hysteresis RX channel 2

1 The values are obtained by simulation, as reported in [9].
2 In CA mode, this channel is not used further. Nonetheless, the highest setting for the hysteresis is to keep the channel silent.



(a) Receiver output signals during reception in CA mode



(b) Receiver output signals during reception in CA mode

Figure 6.11: Measured waveforms at the receiver for a PRBS stream at $2Mbps$

Table 6.3: Receiver settings for measurement in CP mode

Signal	Setting	Value[1]	Description
DIVD	0x00	5.2	Capacitive input divider ratio
CNT1	0x07	85mV	Hysteresis RX channel 1
CNT2	0x70	-85mV	Hysteresis RX channel 2

6.6.4 DPI measurements

The test chip was characterized under exposure of large disturbing common-mode interferers. Since there is no agreed standardization available for the presented communication approaches, the closest specification for electromagnetic immunity using the DPI method is the IEC 62228-3 [40] and the IEC 62132-4 [41] in particular. In the highest class (III), a circuit without a CMC shall operate without any functional deficit under a maximum DPI-stess of $36dBm \mathrel{\widehat{=}} 4W$ (depending on the frequency of the interferer). For lower classes, II and I, the specification mask is relaxed by $3dB$ and $6dB$, respectively. The interferer is either a continuous wave (CW) or an amplitude modulation (AM) signal with a modulation frequency $f_m = 1kHz$ and a modulation index $m = 0.8$. The peak power of the AM signal shall be equal to the power of the CW signal.

In the characterization of the transceiver test chip, the BER is used as pass/fail criterion. This is not part of the mentioned standard, since signal shape used in the proposed approaches is different from the CAN PHY. Fig. 6.12 illustrates the DPI test setup. In contrast to the conducted emission test (refer to Fig. 5.29), the coupling network does not use a 50Ω termination at the injection point. The interferer test signal is provided by an RF generator and subsequent amplification stages to a directional coupler, that divides the signal power between its upper left and lower left ports. The dividing ratio depends on the impedance match at the injection point. A power sensor and meter is applied to the lower left port of the coupler. With the measured power, there and the known incident power at the upper right of the coupler, the actual injected power delivered to the device under test (DUT) is calculated. This is implemented in a PC-based measurement controller to regulate the gain in the RF amplification chain to ensure a well-defined power injection.

The IEC 62228-3 requests a dwell time for the interferer exposure to $1s$ per measurement step. In this evaluation, the dwell time was increased to $2s$ to get sufficient time for the BER test. The *EOM* output of the demonstrator board give a defined pulse at the end of each measurement. Its width is elaborated by a scope envelope mask around the pulse so that any violation is recognized, like the pulse width reduction that happens if a BER test fails. As a result, the pass/fail trigger signal from the scope is used by the PC-based measurement controller to decide on the amount of power injection. Usually, the power

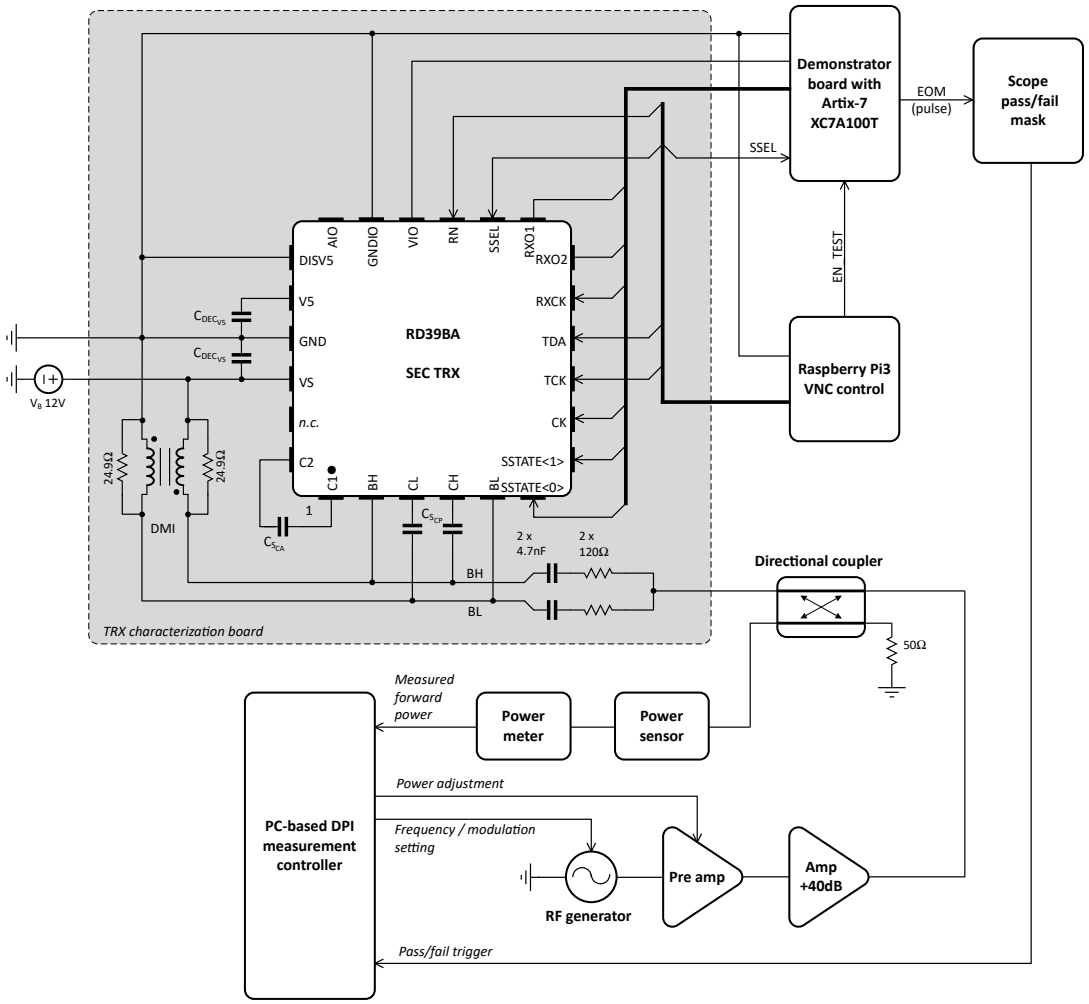


Figure 6.12: DPI test setup

injection starts on a moderate level, e.g., $26dBm$, at the lowest frequency. If after the dwell time the BER criterion is fulfilled, the power injection is increased by $1dB$ until the maximum power is reached, unless the BER test fails. In case the measurement fails, the injected power is reduced in $1dB$ steps until the BER criterion is fulfilled again. The achieved injection power is recorded and the measurement restarts at the next frequency point with the achieved power level at the current measurement frequency.

The transceiver test chip was verified for a $BER = 1e^{-3}$. Bit and error counters were sized to 20 and 17 bits, respectively. Therefore, MAX_ERR was set to 1049. In Fig. 6.13, the DPI result for the CA approach is shown for CW and AM mode interferers. The receiver is configured according to Table 6.4. At frequencies below $\approx 2MHz$, the circuit is robust against common-mode interferers and withstand at least an injection

power of $36dBm$. In addition to the CMRR of the receiver front-end, this is on one hand because of the AC-coupled input stage so that the interferer signals below the high-pass cut-off frequency of $f_c = 49kHz$ [9] are attenuated. On the other hand, the used DMI (*WE-DD 744870101*) suppresses common-mode signals below its self-resonance frequency at $\approx 4MHz$.

Table 6.4: Receiver settings for DPI measurement in CA mode

Signal	Setting	Value	Description
DIVD	0xff	14.9	Capacitive input divider ratio
CNT1	0x0f	220mV	Hysteresis RX channel 1
CNT2	0x60	-70mV	Hysteresis RX channel 2

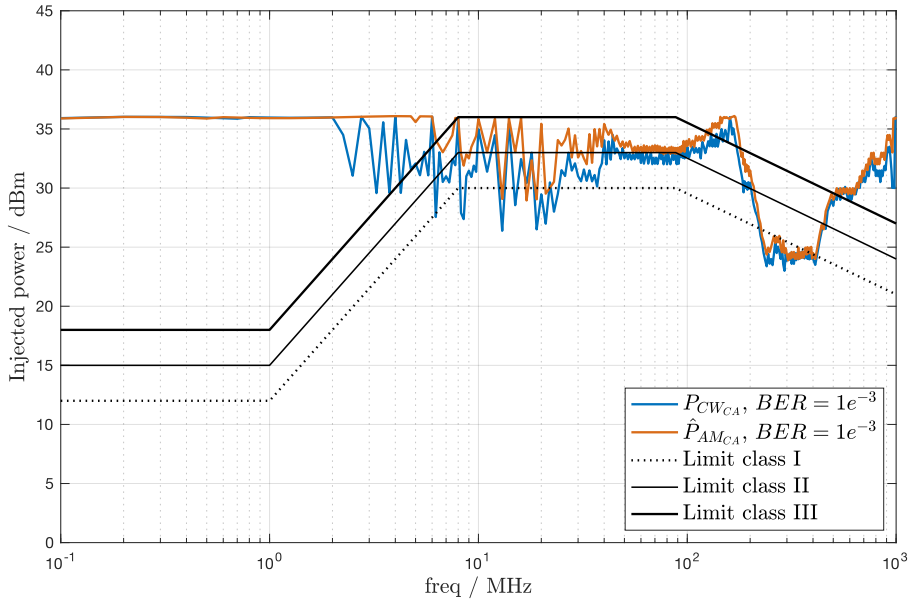


Figure 6.13: DPI measurement result in CA mode, with $BER = 1e^{-3}$ for CW and AM with $f_m = 1kHz$, $m = 0.8$

At frequencies above, these two items disappear, so that the CMRR capabilities of the receiver become dominant. As can be seen, up to a frequency of $\approx 180MHz$, the circuit withstands an injection power of $\approx 27dBm \mathrel{\widehat{=}} 0.5W$ for a CW mode interferer and $\approx 30dBm \mathrel{\widehat{=}} 0.5W$ for an AM mode interferer. As a result, the circuit would almost fulfil the limit class I of IEC 62228-3. The circuit shows a better robustness in the AM interferer test. This seems to indicate that modulation itself does not have an influence but the

injected average carrier power. For a peak power $\hat{P}_{AM}$ equal to P_{CW}, the average power $\overline{P}_{AM}$ is $3.9dB$[1] less than P_{CW}. As a result, less power is injected on average. That is likely the reason for slightly higher $\hat{P}_{AM}$ levels shown in Fig. 6.13.

The results of the DPI test for the CP approach is depicted in Fig. 6.14. The receiver is configured according to Table 6.5. Although the energy required for the communication is eight times less, the robustness to common-mode disturbances seems slightly better. As a result, the circuit would almost fulfil the limit class I of IEC 62228-3 as well.

Table 6.5: Receiver settings for DPI measurement in CP mode

Signal	Setting	Value	Description
DIVD	0x33	7.1	Capacitive input divider ratio
CNT1	0x07	85mV	Hysteresis RX channel 1
CNT2	0x70	-85mV	Hysteresis RX channel 2

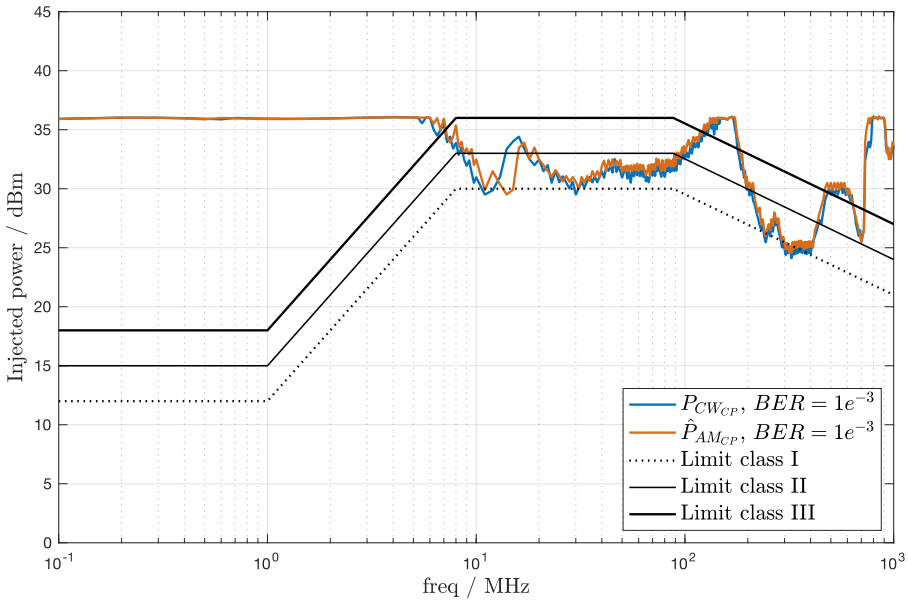


Figure 6.14: DPI measurement result in CP mode, with $BER = 1e^{-3}$ for CW and AM with $f_m = 1kHz$, $m = 0.8$

1 In an AM, $\hat{P}_{AM}$ is $(1+m)^2$ higher than the power of an equivalent CW signal. Therefore, the carrier power needs to be reduced by this amount (for $m = 0.8$ that gives $-5.1dB$). On the other hand, the average power $\overline{P}_{AM}$ is $1 + \frac{m^2}{2}$ higher than the carrier power because of the two AM sidebands (for $m = 0.8$ that gives $1.2dB$).

The difference in acceptable peak power between CW and AM mode interferers that was observed in the CA approach, especially below $50MHz$, could not be observed here. Below this frequency, the DPI response also seems less volatile than in the CA approach, which might be supported by the bipolar pulses that allow an unambiguous data extraction. In the CA approach, any detected extra pulse caused by a disturbance would lead to a code error. That is less severe in the CP operation because a detected extra pulse, in the same polarity as a previous pulse that was part of a symbol, is ignored. Of course, it would cause a code error if the detected extra pulse has the opposite polarity.

To check how steep the transition to a bit error is, the DPI measurement was repeated for $BER = 1e^{-2}$ and $1e^{-5}$. Accordingly, MAX_ERR was adapted to 10486 and 105, respectively. The results for the AM interferer are shown in Fig. 6.15 and Fig. 6.16. As can be seen, the transitions around $10 - 20MHz$ are less steep than at lower and higher frequencies. It can be assumed that in this region, extra pulses lead to bit errors, so that the effect of the injected interferer power on the BER is clearly visible. At lower frequencies, the AC-coupling and the CMRR properties of the receiver front-end, block the interferer signal sufficiently, so that $36dBm$ can be achieved also with a $BER = 1e^{-5}$.

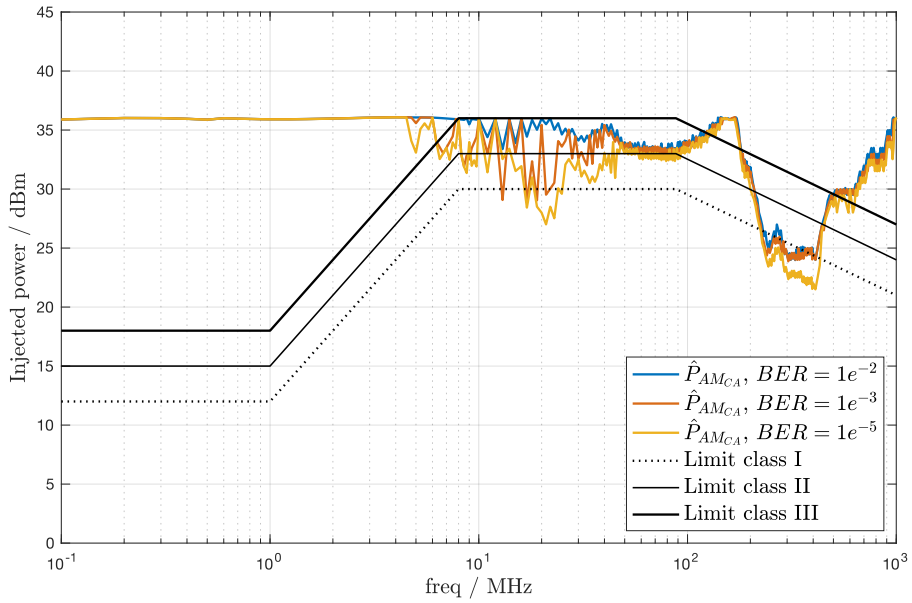


Figure 6.15: DPI measurement result in CA mode, with different BER for AM with $f_m = 1kHz$, $m = 0.8$

At frequencies above $50MHz$, the steepness of the transition to a communication error seems quite high, since the BER curves are very close. This might be caused by

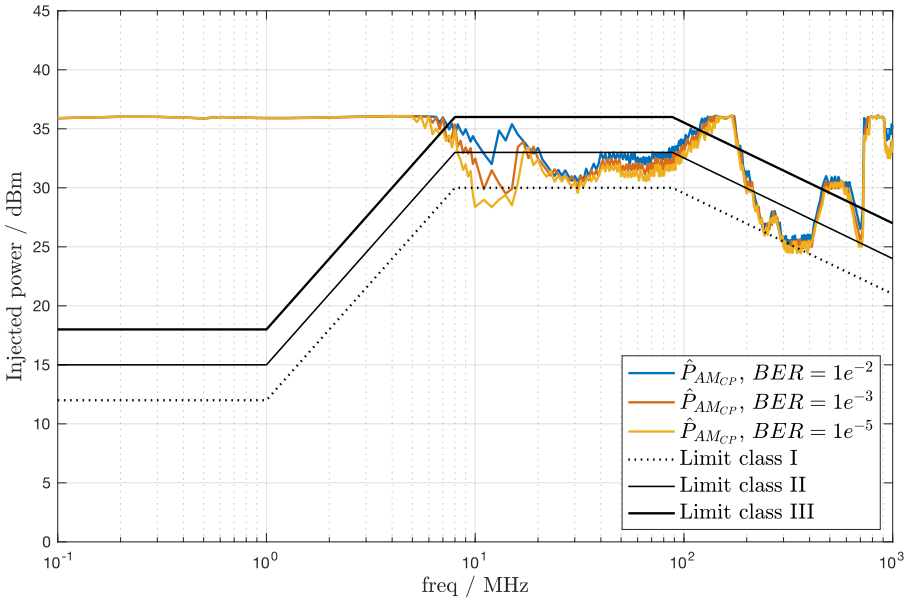


Figure 6.16: DPI measurement result in CP mode, with different BER for AM with $f_m = 1kHz$, $m = 0.8$

nonlinearities leading to shift of operation points in the receiver circuit. As a result of such a shift, the error rate will suddenly rise as soon as sufficient interferer power is available. For the DPI test, the characterization board was used. For more accurate results, a dedicated board would be required. The DPI tests as such showed that the proposed modulation approaches are robust against common-mode interferers.

CHAPTER 7

Conclusions

In this work, a new method for supply-embedded communication was explored. Starting from a theoretical assessment, two modulation approaches, CA and CP, have been proposed and successfully demonstrated by replacing the PHY layer of an existing CAN-like protocol with it, in a state-of-the-art application for interior car illumination. To achieve this, a demonstrator using off-the-shelf components was built, followed by real silicon implementations.

In a first test chip, which was dedicated to the transmitter part, a comprehensive protection scheme was necessary, because of the direct connection to the bus that can have signal excursions beyond the limits of the local supply. A reliable switching concept could be presented, which was realized in a 180nm BCD-on-SOI technology reported in [9]. A transmitter test chip was designed, able to work in a real environment together with existing ICs, since it includes a dedicated protection scheme, digital control and supply regulation. Thanks to the flexible I/O concept, several external control sources could be connected, including the previously developed demonstrator containing an FPGA board. The experimental results are confirming the theoretical assumptions from Chapter 3. The excellent results from the HBM-ESD test show that the proposed protection scheme allows withstanding stress levels $> 8kV$.

A second test chip, including all components to build a complete transceiver front-end, has been designed and fabricated in the same wafer technology. This transceiver test chip contains a receiver chain using modified StrongARM latches for discriminating the conditioned received signal. Experimental results show a good agreement with the simulations and together with the signal processing implemented in an external FPGA, a complete transceiver for the proposed supply-embedded signaling methods could be demonstrated. Measurements on the immunity against unwanted interferers using the DPI method, show a robustness level of $\geq 27dBm$ below $180MHz$ for modulated and CW signals in case of the CA approach. The CP approach reaches a $\approx 3dB$ better performance.

The two transmissions concepts differ slightly in hardware effort, required protection and emission properties. Table 7.1 lists a comparison. The CA approach requires only

one external capacitor, but four switches, where the CP approach requires three. The level excursions on the capacitor nodes *C1* and *C2* used in CA mode, can reach higher values because of a possible asymmetric conduction, as described in Section 5.1. This requires reverse protection diodes in series to the drains of high- and low-side switches. In the CP approach, this is not necessary, since an asymmetric conduction does not have an impact. In terms of power consumption, the CP approach requires eight times less compared to CA, thanks to the reuse of the charges between charge and discharge mode. As a consequence, also the EMC emissions seem to be lower, due to the lower current transfer over the network nodes. The fact that in CP approach, two distinguishable pulsed are emitted, eliminates the demand on pre-coding of the data signal that needs to be transmitted. Since these pulses are subsequently positive and negative, almost no baseline wander is observable. In addition, it helps to improve the immunity against disturbances, in comparison to the CA approach.

Table 7.1: Comparison of the transmission schemes

Item	CA-approach	CP-approach
External capacitors	1	2
High-side switches	2	1
Low-side switches	2	1
Floating switch	-	1
Level range of capacitor pins	$-V_B$ to $2V_B$	0 to V_B
Encoding	Pre-coding necessary	Direct coding possible
Power consumption	$\sim C_S V_B^2 DR$	$\sim C_S V_B^2 DR/8$
EMC emission[1]	Limit class I $\leq 76MHz$	Limit class I $\leq 146MHz$
EMC immunity[2]	$\geq 27dBm$ below $180MHz$	$\geq 30dBm$ below $180MHz$

If two external capacitors are allowed by the application, the CP approach would technically bring the best performance.

In a future work, the proposed transmission schemes could be applied to different applications in the car, to hopefully contribute to a lowering of the amount of wiring, complexity and cost of the networks.

1 Conducted emissions, according IEC 61967-4 [33]
2 Direct power injection, according IEC 62132-4 [41]

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A Appendix

A.1 Verilog listings of demonstrator

A.1.1 Loop-back implementation

Top level

```
1  module top #(
2  parameter DR_DIVIDER = 100,  // division of master clock for DR => 50 for 2Mbps
3  parameter MOD_SCHEME = 3'b001   // 000 - CA phase unknown, simple toggle
4                                  // 001 - CP qp, qn transitions, phase known
5                                  // 010 - CA unipolar RZ
6                                  // 011 -
7  )
8  (
9  input clk,
10 input reset,
11 input qp,
12 input qp_n,
13 input qn,
14 input qn_n,
15 output sp,
16 output sn,
17 output shdn_rx_comp,
18 output rxd,
19 output spare_out,
20 output led
21 );
22 reg [2:0] scheme;
23 reg [7:0] error_max;        // max error cnt setting
24 wire stream;
25 wire qp_rxd;
26 wire qn_rxd;
27 wire trigger;
28 wire [7:0] error_cnt;
29 wire error_flg;
30 wire rxc;
31 assign spare_out = rxc;
```

```
32 assign led = error_flg;
33 always @ (posedge clk or posedge reset)
34 begin
35     if (reset==1)
36         begin
37             scheme <= MOD_SCHEME;
38             error_max <= 8'b00001100;
39         end
40 end
41 prbs #(DR_DIVIDER) prbs_i(
42     .clk(clk),
43     .reset(reset),
44     .stream(stream)                 // prbs output
45 );
46 encoder_tc #(DR_DIVIDER) encoder_i(
47     .clk(clk),
48     .reset(reset),
49     .scheme(scheme),                // which encoding
50     .raw_data_in(stream),           // encoder in
51     .sn(sn),                        // encoder output cn on bord
52     .sp(sp),                        // encoder output cp on bord
53 );
54 syncin_rx_comp syncin_rx_comp_i(
55     .clk(clk),
56     .reset(reset),
57     .qp(qp),                        // LVDS inputs
58     .qp_n(qp_n),
59     .qn(qn),
60     .qn_n(qn_n),
61     .shdn_rx_comp(shdn_rx_comp),    // activate comparators
62     .qp_rxd(qp_rxd),                // sync-ed outputs
63     .qn_rxd(qn_rxd)
64 );
65 decoder #(DR_DIVIDER) decoder_i(
66     .clk(clk),
67     .reset(reset),
68     .scheme(scheme),                // which decoding
69     .qp_rxd(qp_rxd),                // sync-ed inputs
70     .qn_rxd(qn_rxd),
71     .rxd(rxd)                       // received output
72 );
```

```
clock_recovery #(DR_DIVIDER) clock_recovery_i (
    .clk(clk),
    .reset(reset),
    .rxd(rxd),
    .rxc(rxc)                       // recovered clock
);
monitor monitor_i(
    .clk(clk),
    .reset(reset),
    .txd(stream),
    .rxd(rxd),
    .error_max(error_max),          // max allowable bit errors
    .trigger(trigger),              // trigger out, pulse when comparing
    .error_cnt(error_cnt),          // no. of counted errors
    .error_flg(error_flg)           // flag when max error cnt is exceeeded
);
endmodule
```

PRBS

```
module prbs #(
parameter DR_DIVIDER = 50                       // default for 2Mbps
)
(
input wire clk,
input wire reset,
output wire stream
);
localparam DR_CNT_WIDTH = $clog2(DR_DIVIDER);   // clock divider for DR
reg [DR_CNT_WIDTH-1:0] counter;
wire stream_pn9;
reg gate;
always @ (posedge clk or posedge reset)
begin
    if (reset==1)
        begin
            counter <= 0;
            gate <= 1'b0;       // reset clock gating
        end
    else
        begin
            counter <= counter + 1'b1;
```

```
                if (counter >= DR_DIVIDER-1)
                    begin
                        //open the gate for get a clk step for pn9
                        gate <= 1;
                        counter <= 0;
                    end
                else
                    gate <=0;
        end
end
assign stream = stream_pn9; // connect to output of module
pn9 pn9_i(
    .clk(clk),
    .reset(reset),
    .gate(gate),         // clock gate
    .stream(stream_pn9)  // PN9 output
);
endmodule
```

PN9

```
module pn9
(
input wire clk,
input wire reset,
input wire gate,
output wire stream
);
reg [8:0] q;
reg enable;
wire gclk;
always @(negedge clk)
    enable <= gate;
always @(posedge gclk or posedge reset)
    begin
        if (reset == 1)
            q <= 9'b111111111;
        else
            q <= { q[7:0], q[8] ^ q[4] }; // Concatenation
    end
assign gclk = enable & clk;
assign stream = q[8];
```

```
22 endmodule
```

Encoder

```
1  module encoder#(
2  parameter DR_DIVIDER = 50     // default for 2Mbps
3  )
4  (
5  input wire clk,
6  input wire reset,
7  input wire [2:0]scheme,
8  input wire raw_data_in,
9  output wire sp,
10 output wire sn
11 );
12 reg [7:0] pulse_cnt; // count the number of clocks before release a switch
13 reg [7:0] gap_cnt;  // count the number of clocks before new switch turn on
14 reg [1:0] sstate;   // 00-open, 01-CH14/CHG, 10,-CH23/DIS, 11-not used/open
15 reg [1:0] lastchargestate;    // " "
16 reg lastbit;                  // the last polarity of the sent bit
17 localparam integer ONCYCLES = $ceil(DR_DIVIDER*0.64); // switches on-time
18 localparam integer OFFCYCLES = DR_DIVIDER -ONCYCLES - 1; // off-time
19 localparam integer SYMCYCLES = $ceil(DR_DIVIDER*1.00);     // max. symbol time
20 localparam integer SYMCYCLES_WIDTH = $clog2(SYMCYCLES);    // no. of symbols
21 reg [SYMCYCLES_WIDTH-1:0] sym_cnt;
22 always @ (posedge clk or posedge reset)
23 begin
24     if (reset==1)
25         begin
26             pulse_cnt <= 8'b0;
27             gap_cnt <= 8'b0;
28             sstate <= 2'b0;
29             lastbit <= 1'b0;
30             lastchargestate <= 2'b10;
31             sym_cnt <= SYMCYCLES;
32         end
33     else
34         begin
35             // change at flip of incoming data if all other stuff has finished
36             if (pulse_cnt==0 & gap_cnt==0 & (lastbit^raw_data_in))
37                 begin
38                     pulse_cnt <= ONCYCLES; // precharge
```

```
39                      gap_cnt <= OFFCYCLES; // precharge
40                      lastbit <= raw_data_in;  // memorize to detect transition
41                      if (raw_data_in == 1)
42                          begin
43                              lastchargestate[0] <= ~lastchargestate[0];  // revert
44                              lastchargestate[1] <= ~lastchargestate[1];  // revert
45                          end
46                  end
47              if (pulse_cnt !=0)
48                  begin
49                      pulse_cnt <= pulse_cnt - 1'b1;
50                      case(scheme)
51                          // CA only ones are coded (uni RZ)
52                          3'b010: if (raw_data_in == 1)
53                                      begin
54                                          sstate[0] <= lastchargestate[1];
55                                          sstate[1] <= lastchargestate[0];
56                                      end
57                                  else
58                                      begin
59                                          gap_cnt <= 0;
60                                          pulse_cnt <= 0;
61                                      end
62                          // CA, CP default
63                          default: sstate <= 2'b01 + lastbit;
64                      endcase
65                  end
66              else
67                  sstate <= 0;                    // disconnect switches
68              if (pulse_cnt ==0 & gap_cnt != 0) // decrement gap cnt if pulse cnt
    ended
69                  gap_cnt <= gap_cnt - 1'b1;
70              if (sym_cnt != 0)
71                  sym_cnt <= sym_cnt - 1'b1;
72              case(scheme)
73                  //sol 1 only ones are coded (uni RZ)
74                  3'b010: if (sym_cnt == 0 & raw_data_in ==1)
75                              begin
76                                  pulse_cnt <= ONCYCLES; // precharge
77                                  gap_cnt <= OFFCYCLES; // precharge
78                                  sym_cnt <= SYMCYCLES-1;
```

```
79                                  lastchargestate[0] <= ~lastchargestate[0];
80                                  lastchargestate[1] <= ~lastchargestate[1];
81                              end
82                  //CA, CP default
83                  default: ;
84              endcase
85          end
86  end
87  assign sp = ~sstate[1] & sstate[0];     //01-CH14/CHG
88  assign sn = sstate[1] & ~sstate[0];     //10-CH23/DIS
89  endmodule
```

Synchronizer for received data

```
1   module syncin_rx_comp
2   (
3   input wire clk,
4   input wire reset,
5   input wire qp,
6   input wire qp_n,
7   input wire qn,
8   input wire qn_n,
9   output reg shdn_rx_comp,
10  output wire qp_rxd,
11  output wire qn_rxd
12  );
13  wire qp_se;         // single-ended converted LVDS inputs
14  wire qn_se;
15  reg [2:0] qp_sync;  // input sync shift reg
16  reg [2:0] qn_sync;
17  IBUFDS ibuf_qp (
18     .I   (qp),
19     .IB  (qp_n),
20     .O   (qp_se)
21  );
22  IBUFDS ibuf_qn (
23     .I   (qn),
24     .IB  (qn_n),
25     .O   (qn_se)
26  );
27  assign qp_rxd = & qp_sync;              // & of all
28  assign qn_rxd = & qn_sync;
```

```
always @ (posedge clk or posedge reset)
begin
    if (reset==1)
        begin
            shdn_rx_comp <= 1'b1;
            qp_sync <= 3'b0;
            qn_sync <= 3'b0;
        end
    else
        begin
            qp_sync <= qp_sync >> 1;    // right shift
            qn_sync <= qn_sync >> 1;
            qp_sync[2] <= qp_se;        // LSB first
            qn_sync[2] <= qn_se;
        end
end
endmodule
```

Decoder

```
module decoder#(
parameter DR_DIVIDER = 50       // default for 2Mbps
)
(
input wire clk,
input wire reset,
input wire [2:0] scheme,        // which decoding
input wire qp_rxd,              // sync-ed inputs
input wire qn_rxd,
output reg rxd                  // received output
);
localparam integer SYMCYCLES = $ceil(DR_DIVIDER*1.05); // symbol with 5% margin
localparam integer SYMCYCLES_WIDTH = $clog2(SYMCYCLES);    // no of symbols
reg [SYMCYCLES_WIDTH-1:0] sym_cnt;
reg qn_past;                    // qn value in previous clock phase
always @ (posedge clk or posedge reset)
begin
    if (reset==1)
        begin
            rxd <= 1'b0;
            qn_past <= 1'b0;
            sym_cnt <= SYMCYCLES;
```

```
23          end
24      else
25          begin
26              case(scheme)
27                  // simple decoding CA, i.e. every neg transition flips
28                  3'b000: begin
29                              if (!rxd & qn_rxd & !qn_past)
30                                  rxd <= 1'b1;
31
32                              if (rxd & qn_rxd & !qn_past)
33                                  rxd <= 1'b0;
34                          end
35                  // simple decoding CP, i.e. every pos edge -> qp, negedge -> qn
36                  3'b001: begin
37                              if (!rxd & qp_rxd & !qn_rxd)
38                                  rxd <= 1'b1;
39
40                              if (rxd & !qp_rxd & qn_rxd)
41                                  rxd <= 1'b0;
42                          end
43                  // CA, only ones are coded (uni RZ), if no qn transitions
44                  // occuring -> reset to zero after 1.1 Tsym
45                  3'b010: begin
46                              if (qn_rxd & !qn_past)
47                                  sym_cnt <= SYMCYCLES;
48                              else if (sym_cnt > 0)
49                                  begin
50                                      sym_cnt <= sym_cnt - 1'b1;
51                                      rxd <= 1;
52                                  end
53                              else
54                                  rxd <= 0;
55                          end
56                  default:begin
57                              if (!rxd & qn_rxd & !qn_past)
58                                  rxd <= 1'b1;
59
60                              if (rxd & qn_rxd & !qn_past)
61                                  rxd <= 1'b0;
62                          end
63                  endcase
```

```
64              qn_past <= qn_rxd;
65          end
66  end
67  endmodule
```

Clock recovery

```
1   module clock_recovery#(
2   parameter DR_DIVIDER = 50                       // default for 2Mbps
3   )
4   (
5   input wire clk,
6   input wire reset,
7   input wire rxd,
8   output reg rxc
9   );
10  // timeout for posedge of rcx if no bit transition happened:
11  localparam integer TIMEOUT = $ceil(DR_DIVIDER*1.05);
12  // time for positive clock edge (rxc) for taking the data:
13  localparam integer PTIME = $ceil(DR_DIVIDER/2);
14  localparam integer DR_CNT_WIDTH = $clog2(DR_DIVIDER);   // clock divider
15  reg [DR_CNT_WIDTH-1:0] counter;
16  reg [1:0] trigger_sh;    // incoming rxd in 2b-shift reg for edge detection
17  wire trigger;
18  assign trigger = ^trigger_sh; // xoring the bits for edge detection
19  always @ (posedge clk or posedge reset)
20  begin
21      if (reset==1)
22          begin
23              rxc <= 1'b0;
24              counter <= 0;
25              trigger_sh <= 2'b0;
26          end
27      else
28          begin
29              trigger_sh <= trigger_sh >> 1;      // right shift
30              trigger_sh[1] <= rxd;               // LSB 1st
31              if(trigger)
32                  begin
33                      counter <= 0;
34                      rxc <= 1'b0;
35                  end
```

```
36              else
37                  begin
38                      counter <= counter + 1'b1;
39                      if(counter == PTIME-0)
40                          rxc <= 1'b1;
41                      if(counter == TIMEOUT-1)
42                          begin
43                              rxc <= 1'b0;
44                              // pre-charge divider to meet the next bit slot:
45                              counter <= TIMEOUT - DR_DIVIDER;
46                          end
47                  end
48          end
49  end
50  endmodule
```

Monitor

```
1   module monitor
2   (
3   input wire clk,
4   input wire reset,
5   input wire txd,
6   input wire rxd,
7   input wire [7:0] error_max,     // max allowable bit errors
8   output wire trigger,            // trigger out, pulse when comparing
9   output reg [7:0] error_cnt,     // no. of counted errors
10  output reg error_flg            // flag when max error cnt is exceeded
11  );
12  reg [1:0] trigger_sh;
13  assign trigger = ^trigger_sh;  // xoring the bits for edge detection
14  always @ (posedge clk or posedge reset)
15  begin
16      if (reset==1)
17          begin
18              error_cnt <= 8'b0;
19              trigger_sh <= 2'b0;
20              error_flg <= 1'b0;
21          end
22      else
23          begin
24              trigger_sh <= trigger_sh >> 1;       // right shift
```

```
25              trigger_sh[1] <= rxd;                // LSB 1st
26              if (trigger)
27                  error_cnt = error_cnt + txd^rxd; // inc errror cnt if not eq.
28              if(error_cnt > error_max-1)
29                  error_flg <= 1'b1;       // turn on LED for error indication
30          end
31  end
32  endmodule
```

A.1.2 Bridge implementation

Only modules that are different than in Section A.1.1 are listed in this section.

Top level

```
33  module top_sec_bridge #(
34  parameter DR_DIVIDER = 50,       // division of master clock => 50 for 2Mbps
35  parameter BITS_TO_SEND = 16,
36  parameter BIT_GAP = 1,
37  parameter PREAMBLE = 8'b01100010,
38  parameter PREAMBLELEN = 8,
39  parameter MOD_SCHEME = 3'b001   // 000 - CA phase unknown, simple toggle
40                                  // 001 - CP qp, qn transitions, phase known
41                                  // 010 - CA unipolar RZ
42                                  // 011 -
43  )
44  (
45  input clk,
46  input reset,
47  input qp,
48  input qp_n,
49  input qn,
50  input qn_n,
51  input txd,
52  input spare_in,
53  output sp,
54  output sn,
55  output shdn_rx_comp,
56  output rxd,
57  output spare_out,
58  output led
59  );
60
```

```
61  reg [2:0] scheme;
62  reg [7:0] error_max;          // max error cnt setting
63  reg [2:0] txd_reg;
64  wire qp_rxd;
65  wire qn_rxd;
66  wire trigger;
67  wire [7:0] error_cnt;
68  wire error_flg;
69  wire ack;
70  wire dir;
71  wire txd_synced;
72
73  reg rxd_temp;
74  wire rxd_local;
75  assign rxd = rxd_local | !dir;  //only when SEC->CAN
76  assign spare_out = dir;
77  assign led = error_flg;
78  assign txd_synced = |txd_reg;
79  always @ (posedge clk or posedge reset)
80  begin
81      if (reset==1)
82          begin
83              scheme <= 3'b001;
84              error_max <=8'b00011100;
85              rxd_temp <= 1'b1;
86          end
87      else
88          begin
89              txd_reg <= txd_reg >> 1;    // right shift, syncin of txd
90              txd_reg[1] <= txd;          // LSB first
91          end
92  end
93  encoder #(DR_DIVIDER) encoder_i(
94      .clk(clk),
95      .reset(reset),
96      .raw_data_in(txd_synced | dir), // encoder in
97      .sn(sn),                        // encoder output sn
98      .sp(sp)                         // encoder output sp
99  );
100 director #(DR_DIVIDER) director_i(
101     .clk(clk),
```

```
102     .reset(reset),
103     .data_in(txd_synced),           // input of from CAN
104     .data_out(rxd_local),           // data received on SEC for sending to CAN
105     .dir(dir)                       // data flow: 1 => SEC->CAN, 0 => CAN->SEC
106 );
107 syncin_rx_comp syncin_rx_comp_i(
108     .clk(clk),
109     .reset(reset),
110     .qp(qp),                        // LVDS inputs
111     .qp_n(qp_n),
112     .qn(qn),
113     .qn_n(qn_n),
114     .shdn_rx_comp(shdn_rx_comp),    // activate comparators
115     .qp_rxd(qp_rxd),                // sync-ed outputs
116     .qn_rxd(qn_rxd)
117 );
118 decoder #(DR_DIVIDER) decoder_i(
119     .clk(clk),
120     .reset(reset),
121     .scheme(scheme),                // which decoding
122     .qp_rxd(qp_rxd),                // sync-ed inputs
123     .qn_rxd(qn_rxd),
124     .rxd(rxd_local)                 // received output
125 );
126 endmodule
```

Director

```
1  module director#(
2  parameter DR_DIVIDER = 50                    // default for 2Mbps
3  )
4  (
5  input wire clk,
6  input wire reset,
7  input wire data_in,             // input of from the CAN
8  input wire data_out,            // data received, to be sent on the CAN
9  output reg dir                  // data flow: 1:SEC=>CAN, 0:CAN=>SEC
10 );
11 wire data_xor;
12 assign data_xor = data_in^data_out;
13 reg edge_detected;
14 reg data_in_mem;
```

```
15 always @ (posedge clk or posedge reset)
16 begin
17     if (reset==1)
18         begin
19             dir <= 0;
20             edge_detected <= 0;
21             data_in_mem <= 1;
22         end
23     else
24         begin
25             if(data_xor==1 && edge_detected == 0)
26                 begin
27                     edge_detected <= 1;
28                     if(data_in == data_in_mem)
29                         dir <= 1;
30                     else
31                         dir <= 0;
32                 end
33             else
34                 begin
35                     if(data_xor==0)
36                         begin
37                             edge_detected <= 0;
38                             data_in_mem <= data_in;
39                         end
40                 end
41         end
42 end
43 endmodule
```

A.2 Verilog listings - transmitter test chip

A.2.1 Digital control of the transmitter test chip

```
1 module DIG_CTRL(SSTATEC, SSELC, SSELC_O, CKC, RNC, SWC, START, DISV5C, TCKC, TDAC
  , EN_PULL, CTRL, TRIM, TMUX, SPARE);
2      input [1:0] SSTATEC;
3      input SSELC, CKC, RNC, START, DISV5C, TCKC, TDAC;
4      output SSELC_O;     // buffered SSELC for level shifter
5      output [6:0] SWC;   // control of the switches
6      output [7:0] TRIM;  // trimming for bandgap and regulator
7      output [3:0] TMUX;  // test muxer
8      output [1:0] SPARE; // some regs for spare signals if needed
```

```
9       output [2:0] CTRL;  // state control of supply block
10      reg [6:0] SWC;      // associate switch control as regs
11      reg TMSHIFT;        // indication of shift operation
12      reg [15:0] TMREG;   // input shift register
13      reg [15:0] TMOUT;   // configuration register (target after shift-in)
14
15      // reset inputs
16      wire RN;
17      assign RN = RNC & START;
18
19      // enable V5, ext. pull up to VCORE
20      // if grounded externally => V5 enabled
21      assign CTRL[0] = ~DISV5C;
22
23      // pass-through of SSELC (buffer it):
24      assign SSELC_O = SSELC;
25
26      // truth table switch state
27      wire [6:0] D;
28      assign D[0] = ~SSTATEC[1] & SSTATEC[0] & ~SSELC;  //S1, HSS, CA
29      assign D[1] = SSTATEC[1] & ~SSTATEC[0] & ~SSELC;  //S2, LSS, CA
30      assign D[2] = SSTATEC[1] & ~SSTATEC[0] & ~SSELC;  //S3, HSS, CA
31      assign D[3] = ~SSTATEC[1] & SSTATEC[0] & ~SSELC;  //S4, LSS, CA
32      assign D[4] = ~SSTATEC[1] & SSTATEC[0] & SSELC;   //S1, HSS, CP
33      assign D[5] = ~SSTATEC[1] & SSTATEC[0] & SSELC;   //S2, LSS, CP
34      assign D[6] = SSTATEC[1] & ~SSTATEC[0] & SSELC;   //S3, FS, CP
35
36      // test/trimming mode
37      wire D_TMSHIFT;
38
39      // assign STATE = '11' for shift operation
40      assign D_TMSHIFT = SSTATEC[1] & SSTATEC[0];
41
42      // Bandgap trimming
43      assign TRIM[3:0] = TMOUT[3:0];     // default = 0000
44
45      // V5 trimming
46      assign TRIM[7:4] = TMOUT[7:4];     // default = 0111
47
48      // better to avoid programmable shorts, mutual exclusion
49      assign TMUX[3] = TMOUT[11];
```

```
50      assign TMUX[2] = TMOUT[10] & ~TMOUT[9] & ~TMOUT[8];
51      assign TMUX[1] = TMOUT[9] & ~TMOUT[8] & ~TMOUT[10];
52      assign TMUX[0] = TMOUT[8] & ~TMOUT[10] & ~TMOUT[9];
53
54      // sink current inside regulator for V5 (pull operation)
55      // shall be off for external V5 regulator
56      assign CTRL[1] = TMOUT[12] & CTRL[0]; // default = 1 (on)
57
58      // 5uA current sink at AIO (requires TMUX<3> = 1)
59      assign CTRL[2] = TMOUT[13]; // default = 0 (off)
60
61      // assign MSB's of TOUT as spare outputs:
62      assign SPARE[1:0] = TMOUT[15:14];
63
64      // sequential statements
65      always @(posedge CKC or negedge RN)
66           begin
67                if (RN == 1'b0) begin
68                     SWC <= 0;
69                     TMSHIFT <= 0;
70                     end
71                else begin
72                     SWC <= D;
73                     TMSHIFT <= D_TMSHIFT;
74                     end
75           end
76
77      // shift register for test/trimming
78      always @(posedge TCKC or negedge RN)
79           begin
80                if (!RN)
81                begin
82                     TMREG <= 16'b0001000001110000;  // default shift reg
83                end else if( TMSHIFT == 1'b1)
84                begin
85                     TMREG <= TMREG >> 1;      // right shift
86                     TMREG[15] <= TDAC;  // LSB first
87                end
88           end
89
90      // take over the new settings with negedge of TMSHIFT
```

```
91      always @(posedge CKC or negedge RN)
92      begin
93           if (!RN)
94                TMOUT <= 16'b0001000001110000;  // default config reg
95           else if (TMSHIFT && !D_TMSHIFT)
96                TMOUT <= TMREG; // apply
97      end
98
99  endmodule
```

A.2.2 FPGA implementation for the transmitter test chip

The demonstrator board and the FPGA implementation is reused for the transmitter test chip data processing. Only modules that are different than in Section A.1.1 are listed in Section A.2.2.

Encoder

```
1  module encoder#(
2  parameter DR_DIVIDER = 50     // default for 2Mbps
3  )
4  (
5  input wire clk,
6  input wire reset,
7  input wire [2:0]scheme,
8  input wire raw_data_in,
9  output wire sp,
10 output wire sstate0,
11 output wire sstate1,
12 output reg ck,
13 output wire ssel
14 );
15 reg [7:0] pulse_cnt; // count the number of clocks before release a switch
16 reg [7:0] gap_cnt;  // count the number of clocks before new switch turn on
17 reg [1:0] sstate;   // 00-open, 01-CH14/CHG, 10,-CH23/DIS, 11-not used/open
18 reg [1:0] prevstate;     // memory for previous state
19 reg [1:0] lastchargestate;    // " "
20 reg lastbit;                  // the last polarity of the sent bit
21 localparam integer ONCYCLES = $ceil(DR_DIVIDER*0.64); // switches on-time
22 localparam integer OFFCYCLES = DR_DIVIDER -ONCYCLES - 1; // off-time
23 localparam integer SYMCYCLES = $ceil(DR_DIVIDER*1.00);     // max. symbol time
24 localparam integer SYMCYCLES_WIDTH = $clog2(SYMCYCLES);    // no. of symbols
25 reg [SYMCYCLES_WIDTH-1:0] sym_cnt;
```

```
26 always @ (posedge clk or posedge reset)
27 begin
28     if (reset==1)
29         begin
30             pulse_cnt <= 8'b0;
31             gap_cnt <= 8'b0;
32             sstate <= 2'b0;
33             prevstate <= 2'b0;
34             lastbit <= 1'b0;
35             lastchargestate <= 2'b10;
36             sym_cnt <= SYMCYCLES;
37         end
38     else
39         begin
40             // change at flip of incoming data if all other stuff has finished
41             if (pulse_cnt==0 & gap_cnt==0 & (lastbit^raw_data_in))
42                 begin
43                     pulse_cnt <= ONCYCLES; // precharge
44                     gap_cnt <= OFFCYCLES; // precharge
45                     lastbit <= raw_data_in;  // memorize to detect transition
46                     if (raw_data_in == 1)
47                         begin
48                             lastchargestate[0] <= ~lastchargestate[0];  // revert
49                             lastchargestate[1] <= ~lastchargestate[1];  // revert
50                         end
51                 end
52             if (pulse_cnt !=0)
53                 begin
54                     pulse_cnt <= pulse_cnt - 1'b1;
55                     case(scheme)
56                         // CA only ones are coded (uni RZ)
57                         3'b010: if (raw_data_in == 1)
58                                     begin
59                                         sstate[0] <= lastchargestate[1];
60                                         sstate[1] <= lastchargestate[0];
61                                     end
62                                 else
63                                     begin
64                                         gap_cnt <= 0;
65                                         pulse_cnt <= 0;
66                                     end
```

```
67                          // CA, CP default
68                          default: sstate <= 2'b01 + lastbit;
69                      endcase
70                  end
71              else
72                  sstate <= 0;                    // disconnect switches
73              if (pulse_cnt ==0 & gap_cnt != 0) // decrement gap cnt if pulse cnt
ended
74                  gap_cnt <= gap_cnt - 1'b1;
75              if (prevstate != sstate)            // initiate a ck pulse for the TC
76                  begin
77                      ck <= 1'b1;
78                      prevstate <= sstate;
79                  end
80              else
81                  ck <= 1'b0;
82              if (sym_cnt != 0)
83                  sym_cnt <= sym_cnt - 1'b1;
84              case(scheme)
85                  //sol 1 only ones are coded (uni RZ)
86                  3'b010: if (sym_cnt == 0 & raw_data_in ==1)
87                              begin
88                                  pulse_cnt <= ONCYCLES; // precharge
89                                  gap_cnt <= OFFCYCLES; // precharge
90                                  sym_cnt <= SYMCYCLES-1;
91                                  lastchargestate[0] <= ~lastchargestate[0];
92                                  lastchargestate[1] <= ~lastchargestate[1];
93                              end
94                  //CA, CP default
95                  default: ;
96              endcase
97          end
98  end
99  assign sstate0 = sstate[0];
100 assign sstate1 = sstate[1];
101 endmodule
```

A.3 Verilog listings - transceiver test chip

A.3.1 Digital control of the transceiver test chip

```
1  module DIG_CTRL(SSTATEC, SSELC, SSELC_0, CKC, RNC, SWC, START, DISV5C, TCKC, TDAC
   , EN_PULL, CTRL, TRIM, TMUX, SPAREC, DIVDC, DIVSWC, CNT1C, CNT2C, EN_RXC,
```

```
EN_DOUTC, EN_ODC);
    input [1:0] SSTATEC;
    input SSELC, CKC, RNC, START, DISV5C, TCKC, TDAC;
    output SSELC_O;     // buffered SSELC for level shifter
    output [6:0] SWC;   // control of the switches
    output [7:0] TRIM;  // trimming for bandgap and regulator
    output [3:0] TMUX;  // test muxer
    output [7:0] SPAREC;// some regs for spare signals if needed
    output [2:0] CTRL;  // state control of supply block
    output [7:0] DIVDC; // Capacitive divider ratio
    output [4:0] DIVSWC;// Control of capacitive divider outputs
    output [7:0] CNT1C; // Hysteresis setting for receiver channel 1
    output [7:0] CNT2C; // Hysteresis setting for receiver channel 2
    output EN_RXC;      // enable RX
    output EN_DOUTC;    // enable dig outputs
    output EN_ODC;      // enable dig outputs as open-drain
    reg [6:0] SWC;      // associate switch control as regs
    reg TMSHIFT;        // indication of shift operation
    reg [63:0] TMREG;   // input shift register
    reg [63:0] TMOUT;   // configuration register (target after shift-in)

    // reset inputs
    wire RN;
    assign RN = RNC & START;

    // enable V5, ext. pull up to VCORE
    // if grounded externally => V5 enabled
    assign CTRL[0] = ~DISV5C;

    // pass-through of SSELC (buffer it):
    assign SSELC_O = SSELC;

    // truth table switch state
    wire [6:0] D;
    assign D[0] = ~SSTATEC[1] & SSTATEC[0] & ~SSELC;  //S1, HSS, CA
    assign D[1] = SSTATEC[1] & ~SSTATEC[0] & ~SSELC;  //S2, LSS, CA
    assign D[2] = SSTATEC[1] & ~SSTATEC[0] & ~SSELC;  //S3, HSS, CA
    assign D[3] = ~SSTATEC[1] & SSTATEC[0] & ~SSELC;  //S4, LSS, CA
    assign D[4] = ~SSTATEC[1] & SSTATEC[0] & SSELC;   //S1, HSS, CP
    assign D[5] = ~SSTATEC[1] & SSTATEC[0] & SSELC;   //S2, LSS, CP
    assign D[6] = SSTATEC[1] & ~SSTATEC[0] & SSELC;   //S3, FS, CP
```

```
42
43      // test/trimming mode
44      wire D_TMSHIFT;
45
46      // assign STATE = '11' for shift operation
47      assign D_TMSHIFT = SSTATEC[1] & SSTATEC[0];
48
49      // Bandgap trimming
50      assign TRIM[3:0] = TMOUT[3:0];     // default = 0000
51
52      // V5 trimming
53      assign TRIM[7:4] = TMOUT[7:4];     // default = 0111
54
55      // better to avoid programmable shorts, mutual exclusion
56      assign TMUX[3] = TMOUT[11];
57      assign TMUX[2] = TMOUT[10] & ~TMOUT[9] & ~TMOUT[8];
58      assign TMUX[1] = TMOUT[9] & ~TMOUT[8] & ~TMOUT[10];
59      assign TMUX[0] = TMOUT[8] & ~TMOUT[10] & ~TMOUT[9];
60
61      // sink current inside regulator for V5 (pull operation)
62      // shall be off for external V5 regulator
63      assign CTRL[1] = TMOUT[12] & CTRL[0]; // default = 1 (on)
64
65      // 5uA current sink at AIO (requires TMUX<3> = 1)
66      assign CTRL[2] = TMOUT[13]; // default = 0 (off)
67
68      // assign  spare outputs:
69      assign SPAREC[7:0] = TMOUT[31:24]; // default 0x00
70
71      // assign  DIVDC
72      assign DIVDC[7:0] = TMOUT[23:16]; // default 0x00
73
74      // assign CNT1C, CNT2C to word2
75      assign CNT2C[7:0] = TMOUT[39:32]; // default?
76      assign CNT1C[7:0] = TMOUT[47:40]; // default?
77
78      // assign DIVSWC, EN_RXC, further SPARE to word3
79      assign DIVSWC[4:0] = TMOUT[52:48];      // default = 00110
80      assign EN_ODC = TMOUT[53];          // default = 0
81      assign EN_DOUTC = TMOUT[54];        // default = 0
82      assign EN_RXC = TMOUT[55];          // default = 0
```

```
83
84      // sequential statements
85      always @(posedge CKC or negedge RN)
86           begin
87                if (RN == 1'b0) begin
88                     SWC <= 0;
89                     TMSHIFT <= 0;
90                     end
91                else begin
92                     SWC <= D;
93                     TMSHIFT <= D_TMSHIFT;
94                     end
95           end
96
97      // shift register for test/trimming
98      always @(posedge TCKC or negedge RN)
99           begin
100               if (!RN)
101               begin
102                    TMREG [15:0]<= 16'b0001000001110000;  // default  word 0
103                    TMREG[31:16] <= 16'b0000000000000000; // default  word 1
104                    TMREG[47:32] <= 16'b0000000000000000; // default  word 2
105                    TMREG[63:48] <= 16'b0000000000000110; // default  word 3
106               end else if( TMSHIFT == 1'b1)
107               begin
108                    TMREG <= TMREG >> 1;     // right shift
109                    TMREG[63] <= TDAC;  // LSB first
110               end
111          end
112
113     // take over the new settings with negedge of TMSHIFT
114     always @(posedge CKC or negedge RN)
115     begin
116          if (!RN)
117               TMOUT [15:0]<= 16'b0001000001110000;  // default  word 0
118               TMOUT[31:16] <= 16'b0000000000000000; // default  word 1
119               TMOUT[47:32] <= 16'b0000000000000000; // default  word 2
120               TMOUT[63:48] <= 16'b0000000000000110; // default  word 3
121          else if (TMSHIFT && !D_TMSHIFT)
122               TMOUT <= TMREG; // apply
123     end
```

```
124
125 endmodule
```

A.3.2 FPGA implementation for the transceiver test chip

The demonstrator board and the FPGA implementation is reused for the transceiver test chip external data processing. Only modules that are different than in Section A.1.1 are listed in Section A.3.2.

Top level

```
1  module top #(
2  parameter DR_DIVIDER = 50,       // division of master clock => 50 for 2Mbps
3  parameter MOD_SCHEME = 3'b001,   // 000 - CA mode
4                                   // 001 - CP mode
5                                   // 010 - CA mode unipolar RZ
6                                   // this is now controlled by Raspi (SSEL)
7
8  parameter RXCK_DIV = 2,          // output freq. for TC2 = 100MHz/RXCK_DIV
9
10 parameter W_BIT_CNT = 20,        // bit width of bit cnt
11                                  // => test time:
12                                  // DR_DIVIDER*(2^WIDTH_BIT_CNT-1)/100MHz
13 parameter W_ERR_CNT = 17,        // bit width of error cnt
14 parameter MAX_ERR = 10,          // BER (1e-2, 1e-3, 1e-4, 1e-5, 1e-6)
15                                  // at 20/17: 10486, 1049, 105, 10, 1
16 parameter W_EOM_CNT = 17         // 2^17-1 / 100MHz = 1.311ms
17                                  // half (short pulse as error indicator)
18 )
19 (
20 input clk,
21 input reset,
22 output sp,
23 output sn,
24 output shdn_rx_comp,
25 output rxd,
26 output spare_out,
27 output led,
28 output sstate0,
29 output sstate1,
30 output cktc,
31 output rxck,    // input for receiver clock at test chip
32 input rxo1,     // becomes 1 for pos pulses (CP mode only)
```

```
33 input rxo2,      // becomes 1 for neg pulses
34 input en_test,   // input EN_TEST (from Raspberry)
35 input ssel       // new ssel (input from Raspberry)
36 );
37
38 reg [2:0] scheme;
39 reg [3:0] div_cnt;   // clock divider (max 4bit)
40 reg rxck;
41 wire stream;
42 wire rxo2_rxd;
43 wire rxo1_rxd;
44 wire eom;            // end of measurement
45 wire rxc;
46
47 assign spare_out = eom; // output to test set
48 assign led = rxc;
49 assign shdn_rx_comp = 1'b0;
50
51 always @ (posedge clk or posedge reset)
52 begin
53     if (reset==1)
54         begin
55             scheme <= MOD_SCHEME;
56             div_cnt <= 4'b0;
57             rxck <= 1'b0;
58         end
59     else
60         begin
61             if (div_cnt != (RXCK_DIV-2))
62                 div_cnt <= div_cnt + 1'b1;
63             else
64                 begin
65                     div_cnt <= 4'b0;
66                     rxck <= ~rxck; // RXCK output
67                 end
68         end
69     case(ssel)  // map external ssel(Raspi)to scheme:
70         1'b0: scheme <= 3'b010; //CA mode (unipolar RZ)
71         1'b1: scheme <= 3'b001; //CP mode (transitions, phase known)
72         default: scheme <= 3'b000;
73     endcase
```

```
74  end
75
76  prbs #(DR_DIVIDER) prbs_i(
77      .clk(clk),
78      .reset(reset),
79      .stream(stream)                 // prbs output
80  );
81
82  encoder_trx #(DR_DIVIDER) encoder_i(
83      .clk(clk),
84      .reset(reset),
85      .scheme(scheme),                // which encoding
86      .raw_data_in(stream),           // encoder in
87      .en_test(en_test),              // stop the transmission => shift mode
88      .sn(sn),                        // encoder output sn on bord
89      .sp(sp),                        // encoder output sp on bord
90      .sstate0(sstate0),              // state0 output to TC
91      .sstate1(sstate1),              // state1 output to TC
92      .cktc(cktc)                     // ck output to TC
93
94  );
95
96  syncin_rx_trx syncin_rx_trx_i(
97      .clk(clk),
98      .reset(reset),
99      .rxo1(rxo1),
100     .rxo2(rxo2),
101     .rxo1_rxd(rxo1_rxd),            // sync-ed outputs
102     .rxo2_rxd(rxo2_rxd)
103 );
104
105 decoder #(DR_DIVIDER) decoder_i(
106     .clk(clk),
107     .reset(reset),
108     .scheme(scheme),                // which decoding
109     .qp_rxd(rxo1_rxd),              // sync-ed inputs
110     .qn_rxd(rxo2_rxd),
111     .rxd(rxd)                       // received output
112 );
113
114 clock_recovery #(DR_DIVIDER) clock_recovery_i (
```

```
115     .clk(clk),
116     .reset(reset),
117     .rxd(rxd),
118     .rxc(rxc)                       // recovered clock
119 );
120 
121 monitor_ber #(W_BIT_CNT, W_ERR_CNT, MAX_ERR, W_EOM_CNT) monitor_ber_i (
122     .clk(clk),
123     .rxc(rxc),
124     .reset(reset | en_test),
125     .txd(stream),
126     .rxd(rxd),
127     .eom(eom)           // end of measurement
128 );
129 endmodule
```

Encoder

```
1  module encoder_trx#(
2  parameter DR_DIVIDER = 50   // default for 2Mbps
3  )
4  (
5  input wire clk,
6  input wire reset,
7  input wire [2:0]scheme,
8  input wire raw_data_in,
9  input wire en_test,
10 output wire sp,
11 output wire sn,
12 output wire sstate0,
13 output wire sstate1,
14 output reg cktc
15 );
16 reg [7:0] pulse_cnt;    // count the clocks before release a switch
17 reg [7:0] gap_cnt;      // count the clocks before accept new switch turn on
18 reg [1:0] sstate;       // 00-open, 01-CH14/CHG/CP, 10,-CH23/DIS/CN, 11-shift
19 reg [1:0] prevstate;    // previous state
20 reg [1:0] lastchargestate;    // indicates the last charging state
21 reg lastbit;            // the last polarity of the sent bit
22 
23 localparam integer ONCYCLES = $ceil(DR_DIVIDER*0.64);     // active on time
24 localparam integer OFFCYCLES = DR_DIVIDER -ONCYCLES - 1;
```

```
25
26 localparam integer SYMCYCLES = $ceil(DR_DIVIDER*1.00);     // max. symbol time
27 localparam integer SYMCYCLES_WIDTH = $clog2(SYMCYCLES);    // nob of symbol div
28 reg [SYMCYCLES_WIDTH-1:0] sym_cnt;
29
30 always @ (posedge clk or posedge reset)
31 begin
32     if (reset==1)
33         begin
34             pulse_cnt <= 8'b0;
35             gap_cnt <= 8'b0;
36             sstate <= 2'b0;
37             prevstate <= 2'b0;
38             lastbit <= 1'b0;
39             lastchargestate <= 2'b10;
40             sym_cnt <= SYMCYCLES;
41         end
42     else
43         begin
44             if (en_test == 0)
45                 begin
46                     // change at flip of incoming data when finished
47                     if (pulse_cnt==0 & gap_cnt==0 & (lastbit^raw_data_in))
48                         begin
49                             pulse_cnt <= ONCYCLES; // precharge pulse cnt
50                             gap_cnt <= OFFCYCLES;  // precharge gap cnt
51                             lastbit <= raw_data_in;  // memorize for detection
52                             if (raw_data_in == 1)
53                                 begin
54                                       // just revert the charge:
55                                     lastchargestate[0] <= ~lastchargestate[0];
56                                     lastchargestate[1] <= ~lastchargestate[1];
57                                 end
58                         end
59                     if (pulse_cnt !=0)
60                         begin
61                             pulse_cnt <= pulse_cnt - 1'b1;
62                             case(scheme)
63                                 // CA only ones are coded (uni RZ)
64                                 3'b010: if (raw_data_in == 1)
65                                             begin
```

```
66                                          // just revert the charge:
67                                           sstate[0] <= lastchargestate[1];
68                                           sstate[1] <= lastchargestate[0];
69                                      end
70                                  else
71                                      begin
72                                          gap_cnt <= 0;
73                                          pulse_cnt <= 0;
74                                      end
75                              default: sstate <= 2'b01 + lastbit;
76                          endcase
77                      end
78                  else
79                      sstate <= 0;                    // disconnect switches
80                  if (pulse_cnt ==0 & gap_cnt != 0)   //decrement gap cnt
81                      gap_cnt <= gap_cnt - 1'b1;
82                  if (sym_cnt != 0)
83                      sym_cnt <= sym_cnt - 1'b1;
84                  case(scheme)
85                      // CA only ones are coded (uni RZ)
86                      3'b010: if (sym_cnt == 0 & raw_data_in ==1)
87                                  begin
88                                      pulse_cnt <= ONCYCLES; // precharge pulse
89                                      gap_cnt <= OFFCYCLES;/ // precharge gap
90                                      sym_cnt <= SYMCYCLES-1;
91                                      lastchargestate[0] <=~lastchargestate[0];
92                                      lastchargestate[1] <=~lastchargestate[1];
93                                  end
94                      default: ;
95                  endcase
96              end
97          else
98              sstate <= 2'b11;
99          if (prevstate != sstate)            // initiate a ck pulse for the TC
100             begin
101                 cktc <= 1'b1;
102                 prevstate <= sstate;
103             end
104         else
105             cktc <= 1'b0;
106     end
```

```
107 end
108 assign sp = 1'b0;   // disable discrete TX on demo board
109 assign sn = 1'b0;   // dto.
110 assign sstate0 = sstate[0];
111 assign sstate1 = sstate[1];
112 endmodule
```

Synchronizer for received data

```
1  module syncin_rx_trx
2  (
3  input wire clk,
4  input wire reset,
5  input wire rxo1,
6  input wire rxo2,
7  output wire rxo1_rxd,
8  output wire rxo2_rxd
9  );
10
11 reg [2:0] rxo1_sync;  // input sync shift reg
12 reg [2:0] rxo2_sync;
13
14 assign rxo1_rxd = & rxo1_sync;              // & of all
15 assign rxo2_rxd = & rxo2_sync;
16
17 always @ (posedge clk or posedge reset)
18 begin
19     if (reset==1)
20         begin
21             rxo1_sync <= 3'b0;
22             rxo2_sync <= 3'b0;
23         end
24     else
25         begin
26             rxo1_sync <= rxo1_sync >> 1;    // right shift
27             rxo2_sync <= rxo2_sync >> 1;
28             rxo1_sync[2] <= rxo1;             // LSB first
29             rxo2_sync[2] <= rxo2;
30         end
31 end
32 endmodule
```

Monitor

```
module monitor_ber#(
parameter W_BIT_CNT = 20,       // bit width of bit cnt
                                // => test time:
                                // DR_DIVIDER*(2^W_BIT_CNT-1)/100MHz
parameter W_ERR_CNT = 17,       // bit width of error cnt
parameter MAX_ERR = 1049,       // BER (1e-2, 1e-3, 1e-4, 1e-5, 1e-6)
                                // at 20/17: 10486, 1049, 105, 10, 1
parameter W_EOM_CNT = 17        // 2^17-1 / 100MHz = 1.311ms
                                // half (short pulse as error indicator)
                                // at 20/17: 10486, 1049, 105, 10, 1
)
(
input wire clk,
input wire rxc,
input wire reset,
input wire txd,
input wire rxd,
output reg eom                  // end of measurement
);
reg[W_BIT_CNT-1:0] bit_cnt;     // bit counter
reg[W_ERR_CNT-1:0] error_cnt;   // error counter
reg[W_EOM_CNT-1:0] pulse_cnt;   // pulse counter for output pulse
reg[1:0] trigger_sh;
wire trigger;

assign trigger = !trigger_sh[1] & trigger_sh[0];   //falling edge of rxc

always @ (posedge clk or posedge reset)
begin
    if (reset == 1'b1)
        begin
            pulse_cnt <= 0;
            eom <= 1'b0;
            error_cnt <= 0;
            bit_cnt <= 0;
            trigger_sh <= 0;
        end
    else
        begin
            trigger_sh <= trigger_sh >> 1;      // right shift
```

```
41              trigger_sh[1] <= rxc;                   // LSB 1st
42              if (trigger & bit_cnt < 2**W_BIT_CNT-1 & pulse_cnt == 0)
43                  begin
44                      bit_cnt = bit_cnt + 1'b1;       // inc bit cnt
45                      if (txd^rxd && error_cnt < 2**W_ERR_CNT-1)
46                          error_cnt = error_cnt + 1'b1;   // inc error cnt if !=
47                  end
48              if (pulse_cnt < 2**W_EOM_CNT & bit_cnt == 2**W_BIT_CNT-1)
49                  begin
50                      if (pulse_cnt < 2**W_EOM_CNT)
51                          pulse_cnt = pulse_cnt + 1'b1;   // inc  if not ended
52                      if (pulse_cnt < 2**(W_EOM_CNT-1))
53                          eom <= 1'b1;   // min pulse width if BER is nok
54                      else
55                      begin
56                          if (error_cnt >= MAX_ERR || pulse_cnt == 2**W_EOM_CNT-1)
57                             eom <= 1'b0;
58
59                          if (pulse_cnt == 2**W_EOM_CNT-1)
60                              begin     // long pulse for reaching BER
61                                  pulse_cnt <= 0;
62                                  error_cnt <= 0;
63                                  eom <= 1'b0;
64                                  bit_cnt <= 0;
65                                  trigger_sh <= 0;
66                              end
67                      end
68                  end
69          end
70  end
71  endmodule
```

Publications

Paper

[1] F. D'Aniello, A. Ott, and A. Baschirotto. 'Supply Line Embedded Communication in Automotive Sensor / Actuator Networks'. In: *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*. Daegu, Korea (South): IEEE, 2021, pp. 7–11.

[2] F. D'Aniello, A. Ott, and A. Baschirotto. '2-Mbps Power-Line Communication Transmitter Based on Switched Capacitors for Automotive Networks'. In: *Electronics* 11.22 (2022), p. 3651.

[3] F. D'Aniello, A. Ott, and A. Baschirotto. 'StrongArm-Latch-Based Receiver for Supply Line Embedded Communication'. In: *2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. Villasimius, SU, Italy: IEEE, 2022, pp. 321–324.

[4] A. Ott, F. D'Aniello, and A. Baschirotto. 'A Switched Capacitor Approach for Power Line Communication in Differential Networks'. In: *2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*. 1. Villasimius, SU, Italy: IEEE, 2022, pp. 317–320.

Patents

[1] A. Ott, F. D'Aniello, A. Baschirotto, and T. Freitag. 'Transmitter For Power Line Communication'. EP3982513B1. 2022.

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[3] A. Ott, F. D'Aniello, A. Baschirotto, and T. Freitag. 'Transmitter For Power Line Communication'. US 11,522,677 B2. 2023.