Universita' degli Studi di Milano-Bicocca

PhD in Physics and Astronomy (Cycle 35) - Applied Physics and Electronics

High Frequency Buck Converter for Automotive Current Source Applications

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In memory of my parents

Since, during this PhD,
I have always appreciated the dedication to profession and commitment
shown by all the health staff of the nephrology departments of the
"San Daniele del Friuli Civil Hospital"
and the "Santa Maria della Misericordia Hospital" in Udine,
I would like to dedicate them this PhD.

I also want remember
those who donated us a normal life before they leave us,
...
because Humanity is a Big Team connected
in the past, present and future.

Acknowledgements

I would like to thanks Infineon and University of Milano Bicocca who gave me the opportunity to do this PhD. In particular Ing. Paolo Del Croce and Professor Andrea Baschirotto for their advice and collaboration.

Thanks to Günter and Mike for layouts.

Thanks to Paola, whose cheerfulness supported me during this period.

Thanks to my young PhD colleagues, especially Francesco and Marcello, for their help and the breath of fresh air they brought.

And a big thanks to all those who in various ways have shared this work.

Abstract

The advent in the 1980s of discrete high-voltage DMOS with more manageable threshold voltage values and consequent ease of drive, speed of response, and simplicity of construction compared to bipolar devices, led to an increased demand for power supplies for the increasingly popular electronic circuits. This has generated a growing interest in DC-DC power supplies over linear ones.

The big advantage of DC-DC power supplies, apart from their relative simplicity, is their efficiency, allowing them to easily achieve values above the 90%. These efficiencies represented a significant improvement over the linear ones dependent in the first approximation on the ratio between output and supply voltage.

Furthermore, it quickly became apparent that increasing the switching frequency would linearly reduce the size of DC-DC components, smaller Printed Circuit Boards (PCBs). and consequently reduced costs. The frequency increase for Power DC-DCs ($\geq 1A$) has grown steadily, but slowly, and only in recent years frequency have reached values in the order of MHz.

In the automotive field, electrical and electronic devices are powered by the battery, whose typical voltage with the engine running is around 14 V, but experiences transient voltages that can vary between 4.5V (e.g. during cold starting) to over 30V (during load-dumping).

In addition, new functions such as start & stop, increase the frequency of such transients with heavier electronic device operating requirements. This requires off-battery power ICs to function under more critical operating conditions in order to reliably supply the entire vehicle.

In the automotive industry, we see a continuous growth in the use of electronic equipment for both safety and entertainment, for instance lane change warning, sleep sensors, proximity sensors, touch screen displays, cameras and so on. In the lighting field there has been a rapid and progressive transition from incandescent lamps to xenon to LEDs for both exterior and interior lighting as they perform better in terms of energy efficiency than conventional ones. However, due to their electrical characteristics these systems must be supplied with current controlled equipment.

DC-DC converters offer a simple and efficient way to supply the recent electronics loads. In addition, DC-DC power supplies make it possible to effectively meet many safety requirements in modern automobiles. In fact, it is absolutely necessary that hazard lights, headlights and brake lights maintain their functionality under all conditions, especially during cold starting, when the battery voltage reaches very low values. Consequently, DC-DC converters, Buck, Boost and Buck-Boost, for automotive applications are of great interest due to their ability to quickly adapt to different supply voltages as well as their high efficiency. Finally, interest in monolithic solutions has been growing in recent years, and the integrated circuit companies with their BCD (Bipolar, CMOS, Dmos) technologies are very active in this field.

Furthermore, increasing the switching fequency means cheaper, smaller and more manageable DC-DC converters, which are welcome features not only in the automotive sector. This is why both academia and industry, increasingly interconnected, are proposing new technological and circuit solutions.

In this work, my goal is to develop a buck converter with a switching frequency in the order of a few MHz and an output current of a few A using the automotive-qualified BCD technologies available in our group and implementing circuit solutions to reduce discrete components with the aim of reducing costs and volumes.

Our BCD technologies are suitable for a high degree of integration as they enable the integration on a single chip of DMOS power transistors, current sense, bootstrap diodes, control logic and diagnostics.

Since the automotive field requires not only efficiency but also reliability and safety, mature and proven technologies are preferred. Moreover, since development costs are already amortised, they are less expensive, so that the increasingly pressing demand for low cost is also met.

To tackle this work, a literature search was carried out regarding both the latest innovations and the offers available on the market.

Three buck converters have been developed using new innovative solutions with frequencies of 1MHz, 4MHz and 10MHz. The 4MHz Buck Converter is currently the most interesting one for our market, while the 10MHz buck has an investigative role.

In addition the work carried out led to four patent applications.

Contents

Chapter 1

Constant Current Buck Converter for Automotive Current Source Application

1.1 Introduction

The global demand for energy savings is pushing for solutions other than traditional ones, and obviously the automotive sector is also playing its part. In cars, the source of electricity is the battery, which provides a voltage around 14V when the engine is running, while electronic equipment present in increasing quantities require supply voltages ranging from 3V to 6V, just think of the ever-increasing number of entertainment devices like parking cameras, proximity sensors and so on. This requires an increasing number of voltage adapters.

Conventional linear power supplies have a low efficiency, in first approximation proportional to the ratio V_{out}/V_{in} (20% - 40%), they are therefore increasingly being replaced by DC-DC converters that easily reach efficiencies of 90% and more. An emblematic case are both outdoor and indoor lights that are switched from battery-powered incandescent lamps to LED lamps. These are supplied with a constant current, so that the voltage across them varies greatly with temperature. At their ends they typically show voltages between 1.5 and 3.5 V. For LED, the DC-DC supplier is the ideal solution. While typically low-power indoor lights are usually group-powered, the much more powerful outdoor lights each require a dedicated DC-DC power supply.

Our Body Power division, despite its long tradition in ballasts for incandescent lamps and its enviable product portfolio, is looking with great interest at DC-DC converters [1] [2] [3] [4] [5] [6] [7] [8]. It has therefore initiated a collaboration plan with the University of Milan Bicocca, which, simplifying, we can divide into three parts (Figure 1.1) . The first step is to study the suitability of the proprietary BCD technology for the production of DC-DC converters and to design a 1MHz constant current Buck power supply. The second phase is to test the behaviour of Buck's high-frequency constant-current power supplies. Finally, with the third part, we want to build a prototype with constant voltage output and characteristics closer to market requirements. With the present work we deal with the second part, the target is to design three Buck converters with 3A constant output current operating at 1MHz, 4MHz and 10Hz. The main focus is on Buck at 4 MHz.

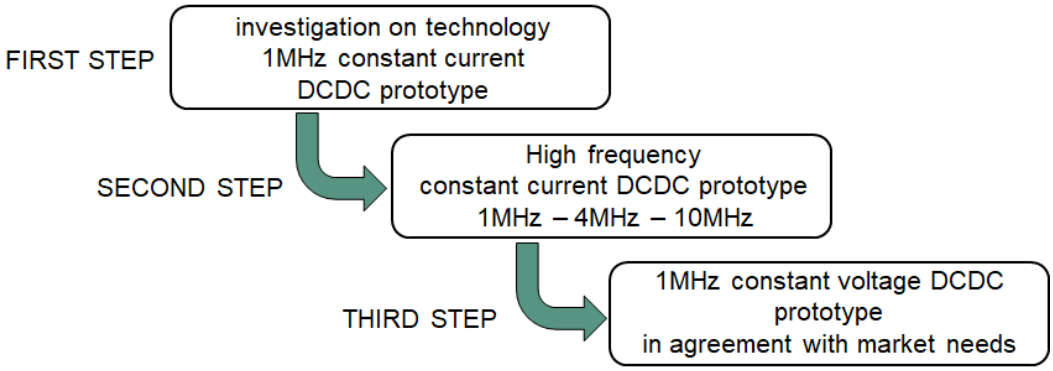


Figure 1.1: Development Plan in collaboration with the University of Milano Bicocca

1.2 DC-DC Converters, Basic Topologies Overview

With the increasing use of DC-DC converters, many topologies have been derived, but all can be developed from the three basic topologies Buck, Boost, Buck-Boost (Figure 1.2) [9].

- Buck: $V_{out}/V_{in} = D$. The output voltage is always lower than the input voltage. Ideal for the automotive sector because many loads must be supplied at lower voltages.

- Boost: $V_{out}/V_{in} = 1/(1-D)$. The output voltage is always higher than the input voltage. There are some automotive applications in which it is used.

- Buckboost $V_{out}/V_{in} = -D/(1-D)$. The output voltage can be either higher or lower than the input voltage, but has inverted polarity. This is why it is often used in many sectors with an inverting transformer. It is not used in automotive.

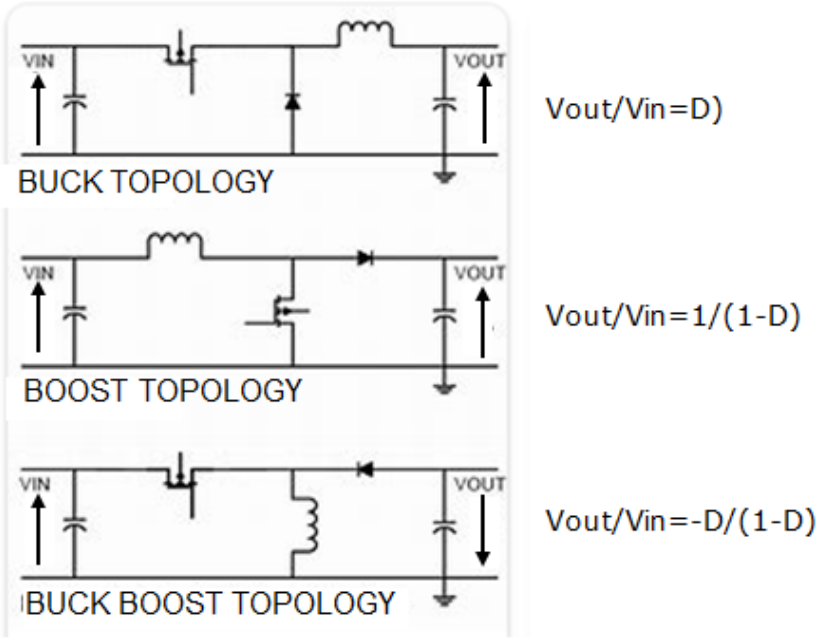


Figure 1.2: DC-DC Base Topologies

In automotive the Buck converter is suitable for driving electronic loads as the

requested supply voltage is $3 \sim 6$ V.

1.3 First Investigation

With this work, using the automotive qualified technologies available to our group, the aim is to make the Buck converter more economical and manageable. This can be achieved by increasing the integration level and by increasing the switching frequency to reduce the size of the discrete components in order to obtain smaller PCBs.

We can choose between two available BCD technologies that are similar in components, both of which allow the integration of a very efficient power DMOS, current sensing and bootstrap diode, but one allows through additional process steps the integration of large capacitors, even several nF, this feature allows on-chip bootstrap capacitor (I denote this technology by BCD-cap, the other simply by BCD).

BCD-cap was the first choice, and I also wanted to check whether it made sense to integrate an inductance of a few tens of nH into the silicon. Several articles in the literature deal with this topic [10] [11]. I thought of an elliptical structure Figure 1.3 and with the help of the process group, some simulations were carried out. Since the real inductance is associated with parasitic components, series resistance, conductance and capacitance in parallel, it is important to assess the effect of frequency on deterioration of the desired inductance.

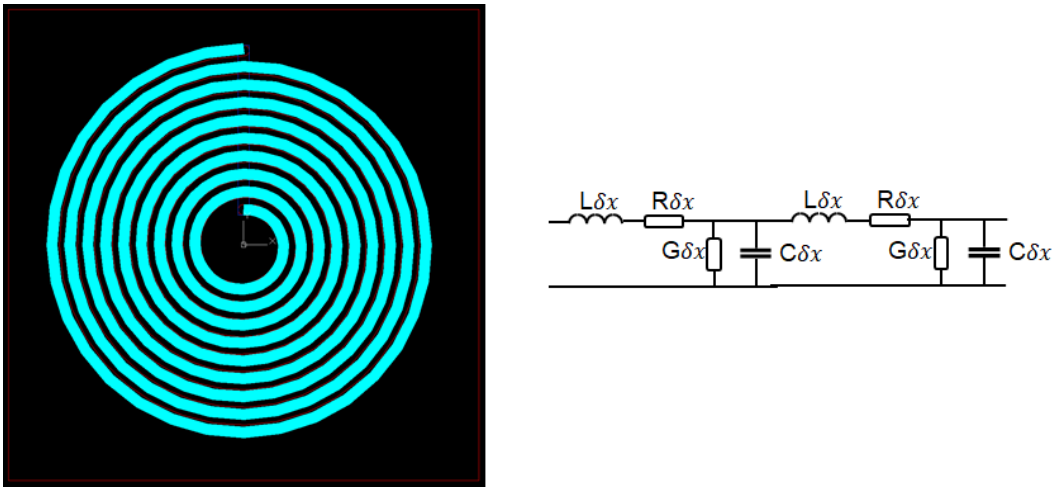


Figure 1.3: simulated spiral inductance - two elementary cell

The results of simulations at different frequencies (1KHz, 10KHz, 100KHz, 1MHz, 10MHz and 100 MHz) are shown in Figure 1.4 and Figure 1.5.

The simulations show that the losses caused by Eddy currents affect both the underlying silicon and the leadframe, in the latter, being metallic, the losses are already relevant at relatively low frequencies. Table in figure 1.6 shows that at 100 MHz the inductance is reduced from 71.4nH to 48.2nH.

In [12] to confine the magnetic field is poposed two layer spiral inductor, one in the upper and one in the lower face, thus reducing losses in the lead-frame.

Regarding the volume of silicon underlying the inductance, I proposed dividing the silicon into small isolated volumes by means of trenches, solution borrowed from the ferrite magnetic cores used in the high-frequency transformers [13].

This solution suggested a patent proposal.

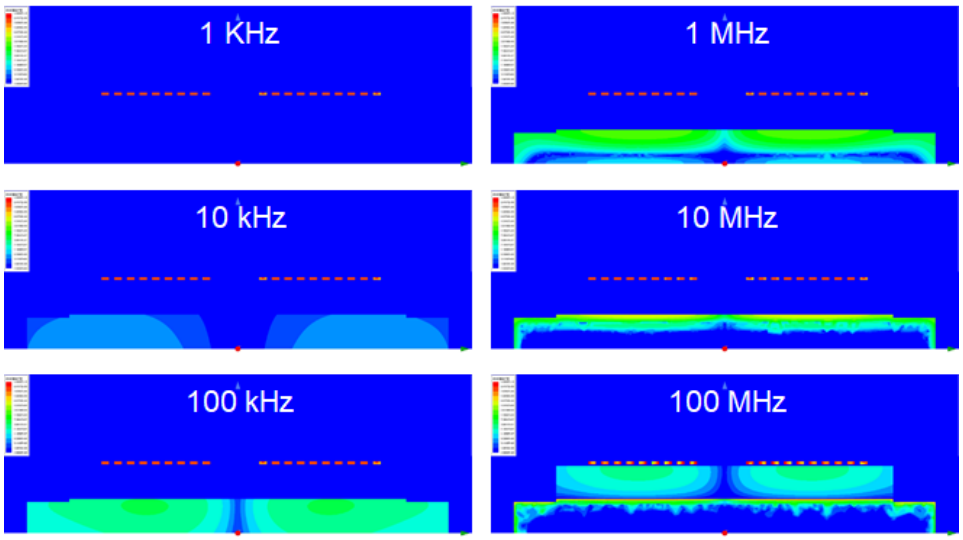


Figure 1.4: Simulated Losses at Several Frequencies - 1KHz, 10KHz, 100KHz, 1MHz, 10MHz, 100MHz

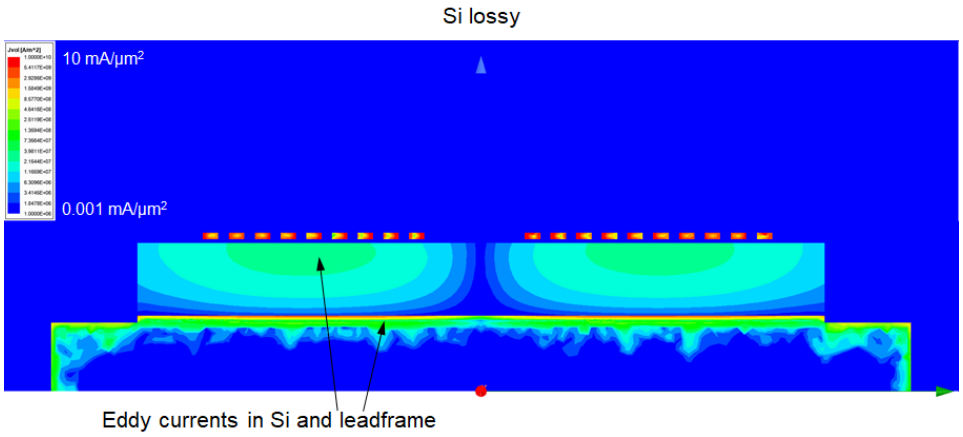


Figure 1.5: Losses Simulated at 100MHz

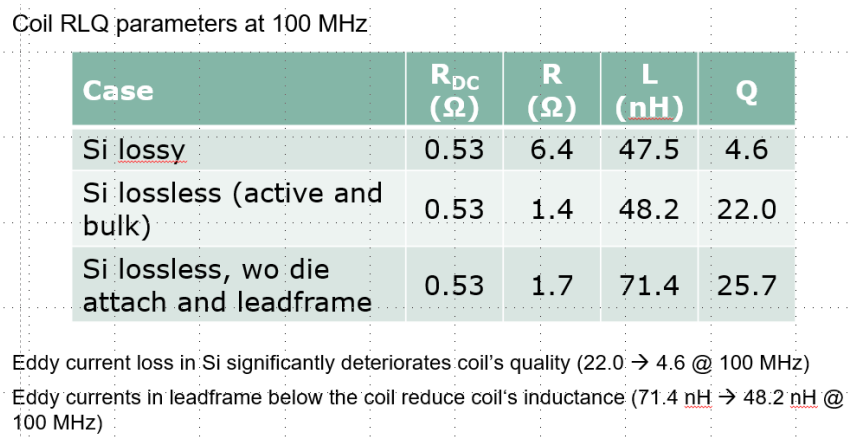


Figure 1.6: degradation of inductance at 100 MHz

Despite interesting developments, I had to abandon ongoing investigations as management opted to optimise development efforts and focus them in one direction by allowing only one development testchip for commercial products in BCD technology.

I was forced to abandon the BCD-Cap technology and develop the Buck Converter in BCD.

However, the work carried out so far remains an interesting input for possible and eventual developments given the interest aroused in the process group.

1.4 Design Target

As mentioned above, BCD technology will be used for the Buck-converter design. Thanks to its versatility allows the integration of a highly efficient vertical Power DMOS ideal for the implementation of High Side Switches. This BCD technology also allows on-chip current sensing and bootstrap diode integration.

This leads to a reduction of external components, a simplification of the system with related volume and overall cost savings (Table 1.1).

COMPONENTS	Integrated	External
DMOS	✓	-
Current sense	✓	-
Bootstrap Diode	✓	-
Bootstrap Capacitor	-	✓
Free Wheeling Diode	-	✓
Inductor	-	✓

Table 1.1: Buck Components.

In Figure 1.7 is shown the application consisting of the IC and the external components. The functions implemented in the IC are the minimum necessary as we are currently interested in testing the high-frequency core. This explains the few PINs available. In addition to the power supply "VCC" and the ground "GND" there is the input PIN "ON" with which we switch the system ON and OFF. The output PIN

"BOOT" connects the Bootstrap capacitor while the "Source" PIN is the connection between the Power DMOS and the external circuit.

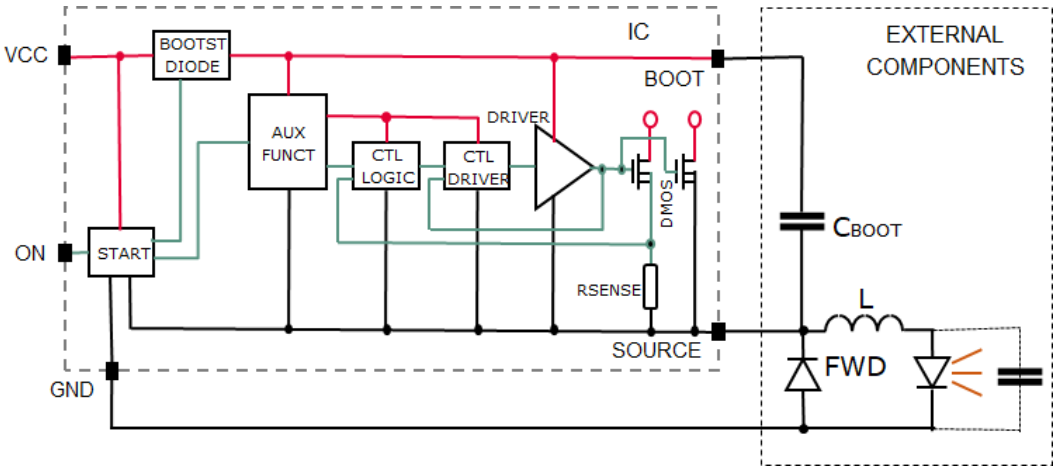


Figure 1.7: Buck Converter - IC with External Components

The three Buck converters developed all have the same architecture and only driver and t_{OFF} block have been adapted to different frequencies. In what follows, where not explicitly specified, reference will always be made to the Buck converter with the higher frequency.

1.5 Design Guidelines

Before starting the project, we defined the guiding specifications. This is actually an Infineon study with which we intend to verify the possibility of using the BCD technology to implement high-frequency converters, thus many functions needed in a commercial device are missing. Table 1.2 shows the guidelines we used to develop the converter.

Parameter	Symbol	min	typ	max	unit
Supply Voltage	VCC	7	13.5	18	V
Operating Temperature Range	T	-40	-	150	°C
Current Consumption (not Switching)	Ignd	-	-	1	mA
Current Consumption Standby	Istb	-	-	500	uA
Nominal Load Current	Iload	-	3A	-	A
Load Current Limitation	Ilim	-	6	-	A
Rds ON (25°)	Rds ON	-	80	-	mOhm
Rds ON (150°)	Rds ON	-	150	-	mOhm
Switching Frequency (Low freq)	fsw	-	1	-	MHz
Switching Frequency (Medium freq)	fsw	-	4	-	MHz
Switching Frequency (High freq)	fsw	-	10	-	MHz
Input Logic - High Level	Vih	2	-	-	V
Input Logic - Low Level	Vil	-	-	0.8	V
Input Logic Hysteresis		-	0.25	-	V

Table 1.2: Buck Converter Guidelines.

Being the high-frequency converters a topical subject, a literature research on high-frequency buck converter was carried out before starting the project. Indeed, there is a lot of material and several papers propose solutions at 10 MHz and above, all however based on Gallium nitride (GaN) technology, ([14], [15], [16]).

The GaN technology guarantees much higher switching speed than conventional silicon-based ones, and I am convinced that it will be the future for high-frequency converters. unfortunately, it is a technology currently under development that we do not have for commercial applications.

Another interesting solution is described in [17], in which a Dual Buck with a switching frequency of 25MHz based on a full differential current balance method is presented. This solution requires the measurement of the voltage at the ends of the two inductances and technology suitable for digital circuitry. It is therefore an expensive and complex system for our target and not suitable for the BCD technology we use.

In addition to literature, a market research was carried out to see what competition offers.

In Figure 1.8 are shown some Buck converter available in the market [18] [19] [20] [21] [22] [23] [24] [25] [26] [27] . Obviously they are not completely equivalent to what we are developing, mainly because these are commercial products that have to meet customer requirements, whereas our study is more exploratory for Infineon use. Another reason depends on the technology used, ours allows for more integration. In any case they can be considered a good comparison especially with regard to switching frequency and output current.

Figure 1.8 shows that only the best performing ones have switching frequencies of 2.0-2.5MHz, load currents of 2-2.5A and usually not simultaneously

The target we set ourselves, a switching frequency of 10MHz (in addition to the 1MHz and 4MHz Buck), the load current of 3A in the -40,150°C temperature range, is very aggressive and is considerably higher than the commercially available Buck converters. It should also be considered the R_{DSON}=80$m\Omega$ intentionally lower than necessary in anticipation of the development of step 3 (see Figure 1.1)

Wide VIN Step Down Devices

	Part No	I_{OUT} (A)	V_{IN} (V)	V_{OUT} (V)	F_{SW}	Synchronous	Features
	LM34919C-Q1	0.6	4.5 to 50	3.5 to 45	2.6 MHz		Ultra-small footprint
	LM5010-Q1/Q0	1	6 to 75	1.5 to 70	1.0 MHz		Available in Q1 and Q0 grades
PMIC, Sync	TPS65310A-Q1	1 / 2	4 to 40	0.8 to 5.5	0.98 MHz	✔	Supports up to 5 outputs
High efficiency	LM26001/03	1.5 / 3	3 to 38	1.25 to 35	500 kHz, Sync	✔	High-efficiency sleep mode
	LM25011-Q1	2	6 to 42	2.5 to 40	2.0 MHz		Adjustable Current Limit
DCDC + LDO	TPS65320-Q1	3.2	3.6 to 40	1.1 to 20	2.5 MHz		LDO input auto sourcing
High efficiency	TPS54340/540	3.5 / 5	4.5 to 60	0.8 to 58.8	2.5 MHz, Sync		Eco-mode
External MOS	LM(2)5119Q	N/A	5.5 to 65	0.8 to 64	750 kHz, Sync	✔	Dual-channel, dual-phase
External MOS	LM(2)5117-Q1	N/A	4.5 to 65	0.8 to 62	750 kHz, Sync	✔	Analog Current Monitor
External MOS	TPS40170-Q1	N/A	4.5 to 60	0.6 to 57	600 KHz	✔	Pre-biased output support

Single products or small families (1-3 products for each application)

Figure 1.8: Buck Converters Available in the Market

Figure 1.9 and Figure 1.10 show the first pages of the two devices datasheet that we consider to be the best performing, the TPS54340 and the TPS65320.

Even the devices mentioned are commercial buck converters, they are a good ref-

erence with regard to switching frequency and load current. In addition to frequency and output current, we also want to test the degree of integration achievable with our technology.

TEXAS INSTRUMENTS

TPS54340

SLVSBK0D – OCTOBER 2012 – REVISED MARCH 2017

TPS54340 42 V Input, 3.5 A, Step Down DC-DC Converter with Eco-mode™

1 Features

- 4.5 V to 42 V (45 V Abs Max) Input Range
- 3.5 A Continuous Current, 4.5 A Minimum Peak Inductor Current Limit
- Current Mode Control DC-DC Converter
- 92-mΩ High-Side MOSFET
- High Efficiency at Light Loads with Pulse Skipping Eco-mode™
- Low Dropout at Light Loads with Integrated BOOT Recharge FET
- 146 µA Operating Quiescent Current
- 1 µA Shutdown Current
- 100 kHz to 2.5 MHz Fixed Switching Frequency
- Synchronizes to External Clock
- Adjustable UVLO Voltage and Hysteresis
- Internal Soft-Start
- Accurate Cycle-by-Cycle Current Limit
- Thermal, Overvoltage, and Frequency Foldback Protection
- 0.8 V 1% Internal Voltage Reference
- 8-Terminal HSOP with PowerPAD™ Package
- –40°C to 150°C T_J Operating Range
- Create a Custom Design with WEBENCH Tools

2 Applications

12 V, 24 V Industrial, Automotive and Communications Power Systems

3 Description

The TPS54340 is a 42 V, 3.5 A, step down regulator with an integrated high side MOSFET. The device survives load dump pulses up to 45 V per ISO 7637. Current mode control provides simple external compensation and flexible component selection. A low ripple pulse skip mode reduces the no load supply current to 146 µA. Shutdown supply current is reduced to 1 µA when the enable pin is pulled low.

Undervoltage lockout is internally set at 4.3 V but can be increased using the enable pin. The output voltage start up ramp is internally controlled to provide a controlled start up and eliminate overshoot.

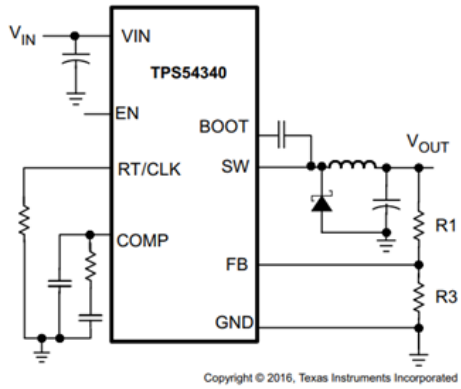
A wide switching frequency range allows either efficiency or external component size to be optimized. Frequency foldback and thermal shutdown protects internal and external components during an overload condition.

The TPS54340 is available in an 8-terminal thermally enhanced HSOP PowerPAD™ package.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TPS54340DDA	HSOP (8)	4.89 mm x 3.9 mm

Simplified Schematic



Efficiency vs Load Current

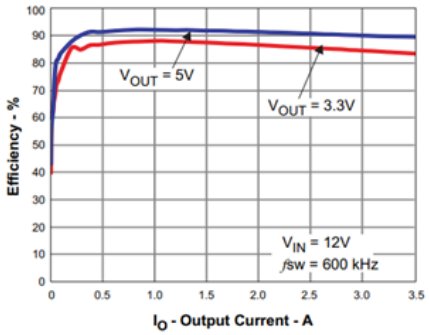


Figure 1.9: TPS54340 Datasheet

TEXAS INSTRUMENTS

TPS65320D-Q1

SLVSE56 – NOVEMBER 2017

TPS65320D-Q1 36-V Step-Down Converter With Eco-mode™ and LDO Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- One High-VIN Step-Down DC-DC Converter
  - Input Range of 3.6 V to 36 V
  - 250-mΩ High-Side MOSFET
  - Maximum Load Current 3.2 A, Output Adjustable 1.1 V to 20 V
  - Adjustable Switching Frequency 100 kHz to 2.5 MHz
  - Synchronizes to External Clock
  - High Efficiency at Light Loads With Pulse-Skipping Eco-mode™ Control Scheme
  - Maximum 140-µA Operating Quiescent Current
- One Low-Dropout Voltage (LDO) Regulator
  - Input Range of 3 V to 20 V, With Auto-Source to Balance Efficiency and Lower Standby Current
  - 280-mA Current Capability With Typical 35-µA Quiescent Current in No-Load Condition
  - Power-Good Output (Push-Pull)
  - Low-Dropout Voltage of 300 mV at I_O = 200 mA (Typical)
- Overcurrent Protection for Both Regulators
- Overtemperature Protection
- 14-Pin HTSSOP Package With PowerPAD™ Integrated Circuit Package

2 Applications

- Automotive Infotainment and Cluster
- Advanced Driver Assistance System (ADAS)
- Automotive Telematics, eCall

3 Description

The TPS65320D-Q1 device is a combination of a high-VIN DC-DC step-down converter, referred to as the buck regulator, with an adjustable switch-mode frequency from 100-kHz to 2.5-MHz, and a high-VIN 280-mA low-dropout (LDO) regulator. The input range is 3.6 V to 36 V for the buck regulator, and 3 V to 36 V for the LDO regulator. The buck regulator has an integrated high-side MOSFET. The LDO regulator features a low-input supply current of 45-µA typical in no-load, also has an integrated MOSFET with an active-low, push-pull reset output pin. The input supply of the LDO regulator auto-source from the output of the buck regulator when it is in operation. Low-voltage tracking feature enables TPS65320D-Q1 to track the input supply during cold-crank conditions.

The buck regulator provides a flexible design to fit system needs. The external loop compensation circuit allows for optimization of the converter response for the appropriate operating conditions. A low-ripple pulse-skip mode reduces the no-load input-supply current to maximum 140 µA.

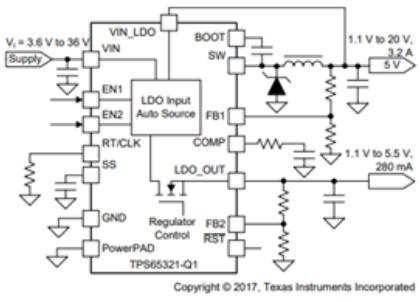
The device has built-in protection features such as soft start, current-limit, thermal sensing and shutdown due to excessive power dissipation. Furthermore, the device has an internal undervoltage-lockout (UVLO) function that turns off the device when the supply voltage is too low.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65320D-Q1	HTSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Buck Efficiency Versus Output Current

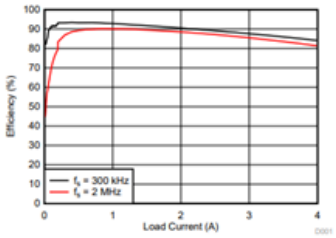


Figure 1.10: TPS65320 Datasheet

1.6 Integrated Development

In summary, the second step of our program consists of three Buck converters design and their layouts. The layouts will be placed on a shared test chip for prototyping. Prototypes will be measured in the laboratory by building appropriate test PCBs optimised to work at different switching frequencies. The number of PCB layers will

be minimised, and the definition of test-point positioning for prototype measurement will be optimised by simulations with appropriate development software.

The all development steps are shown in Figure 1.11.

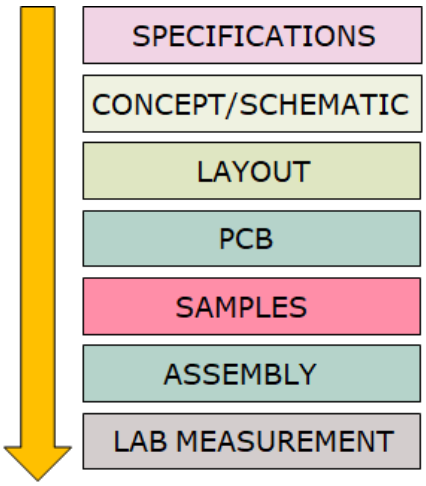


Figure 1.11: Process Flow Overview

Chapter 2

Buck Converter Architecture

2.1 Floating Control Logic

In Buck Converters the Power DMOS having Drain connected to V_{CC} and Source to the inductor floating side, floats between GND and V_{CC}. So must do the Driver that drives it, being fed between the Bootstrap capacitance and Source.

Therefore, one of the first topics addressed was the definition of the power lines architecture to be adopted in the IC. The often-used solution of low-side control and auxiliary circuits (Figure 2.1) has the simplicity of requiring supply lines referred to GND. Conversely, this architecture requires level shifters [28] [29] to transfer commands, feedback and protection signals from the circuits referred to GND to the circuits located between the Bootstrap and Source lines and vice versa. Level shifters take time to transfer signals and cause delays. Moreover parasitic capacitive couplings between the substrate 'n' connected to VCC and the 'p' pockets of the floating electrical components are cause of parasitic capacitive currents that dirty the transferred signals when they do not even overwrite them, causing the device to malfunction.

The other solution shown in Figure 2.2 requires for control and auxiliary circuits a power supply between VCC and a virtual ground few volts below VCC (very often 3V), but requires level shifters capable of transferring signals in two directions, to GND and to the power supply provided by the Bootstrap capacitance. This makes the situation described above even worse.

It was therefore decided for a different solution, preferring to have all the circuits controlling the Power DMOS floating (Figure 2.4) and fed between Bootstap and Source. This solution does not require level shifters, as all the monitoring and control signals access the switching parts directly, which speeds up the whole system.

In order to eliminate the effects of the capacitive currents to the substrate generated by the switching, all floating circuits are placed in a doped 'p' pocket (Figure 2.3), and polarised at the low-impedance Source node, which collects the parasitic capacitive currents and neutralises their effects. The circuits, fed between Bootstrap and Source are in parallel to the C_{BOOT} capacitor. This is comparable to a voltage supply and constitutes a short circuit for disturbances.

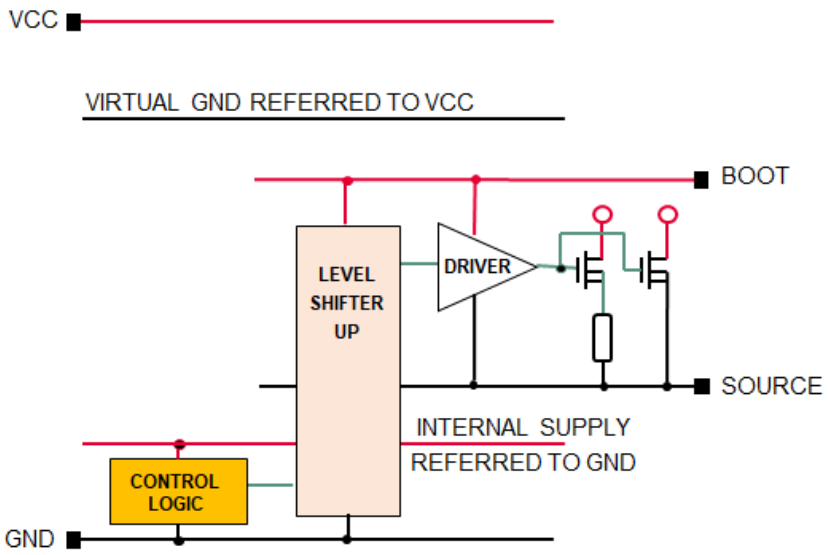


Figure 2.1: Control Logic GND Referred Plus UP Level Shifter

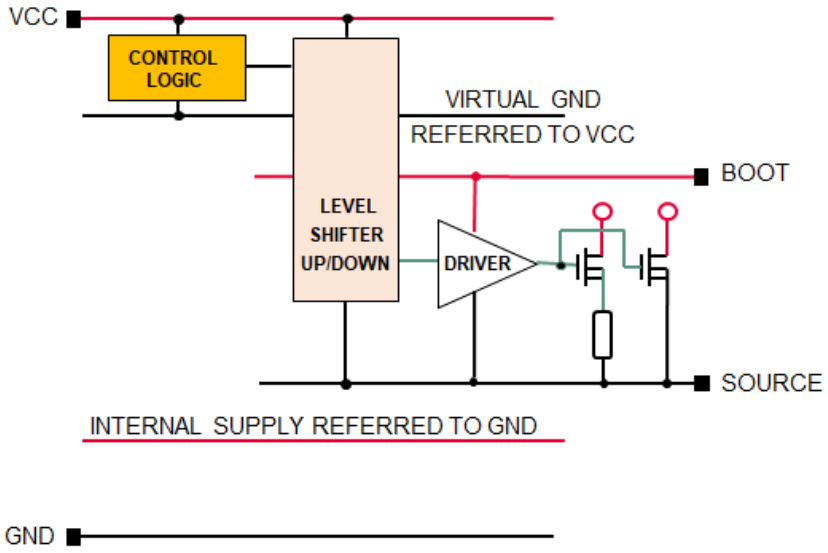


Figure 2.2: Control Logic VCC Referred Plus UP/DOWN Level Shifter

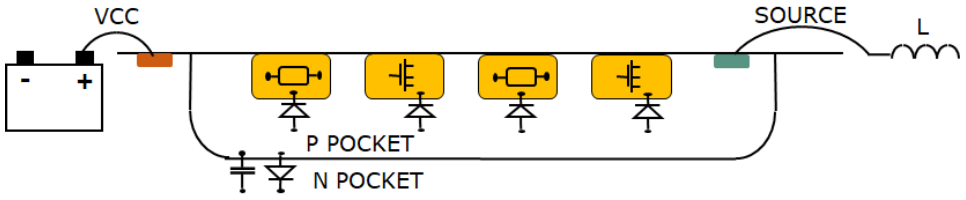


Figure 2.3: "p" Pocket Shield

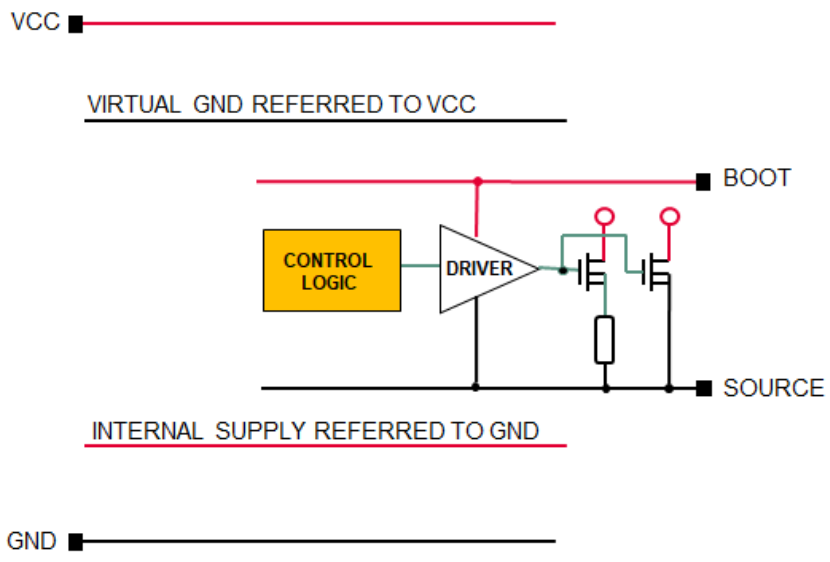


Figure 2.4: Floating Control Logic

2.2 Block Diagram

Having defined the power supplies, consider now the block diagram of the Buck Converter (Figure 2.5).

The battery via the VCC pin directly supplies the 'Start' block and the 'Bootstrap Diode' block.

The 'Start' block is the only one referred to GND and is interfaced with the outside via the 'ON' pin. Only if "ON" is high the converter is active. The "Start" block recognises the status of the "ON" pin and sends the power signal to the "Bootstrap Diode" block and the "Aux Functions" block.

"Bootstrap Diode" is responsible for charging the external capacitance C_{BOOT} to the desired voltage. C_{BOOT} is charged by the diode when the "Source" pin is close to GND, however, when "Source" rises towards VCC the diode is OFF because reverse polarised.

The 'Aux Functions' block is activated as soon as C_{BOOT} is loaded to the correct value. It consists of several sub-blocks, the main ones being "Internal Supplies" which generates the supply for the entire floating part, "References" which, thanks to the Band-gap, generates the voltage and current references, the "Under Voltage Shut-Down" which activates the entire floating part when the supplies, voltage and current references reach the required values.

The 'Control Logic' and 'Control Driver' blocks control system and driver for the correct operation of the buck converter.

The 'Driver' block switches the Power DMOS ON and OFF according to the signal provided by the previous blocks. In conventional solutions, the Driver is powered at the same voltage that has to be transferred to the Power DMOS Gate (often 3V). In this project, anticipating the Driver section, we power it at 6-7V in order to charge the Power DMOS gate to 3V faster. This requires a proper control, which explains the presence of the "Control Driver" block.

Finally, the Power DMOS with its current sense formed by a fraction of the Power-DMOS with the R_{SENSE} resistor in series. The voltage drop across R_{SENSE}

(a few tens of mV) constitutes the feedback of the Control Logic circuit.

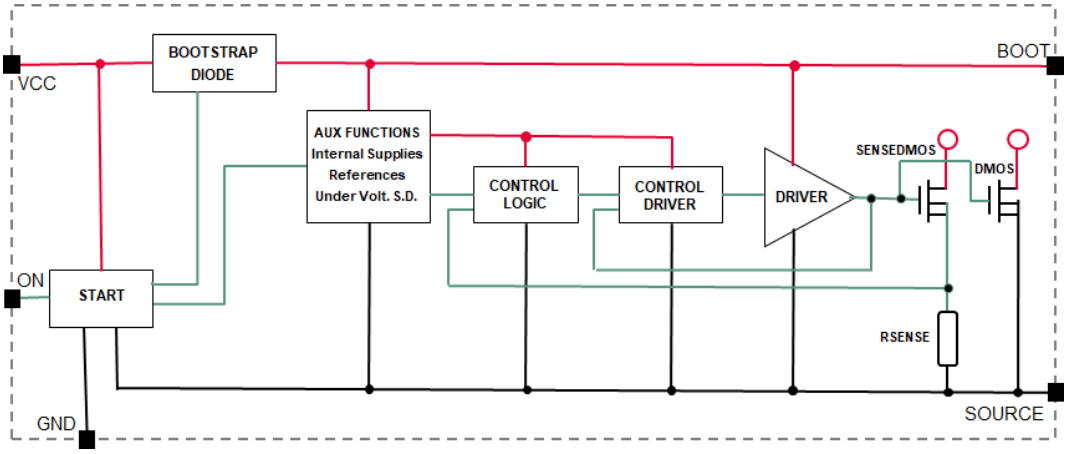


Figure 2.5: Buck Converter IC Block Diagram

2.3 Fixed t_{OFF}

Another point to be defined is the frequency control

Fixed frequency control [30] [31], [32] is the solution often used, the period $T = t_{ON} + t_{OFF}$ is constant. If a perturbation causes a variation Δt_{ON} the control will cause a variation $\Delta t_{OFF} = -\Delta t_{ON}$ so that the period remains constant. Normally in fixed-frequency controls, R_{SENSE} monitors the load current throughout the cycle. It is usually external and the voltage across it is the feedback signal. It is brought to the on-chip control circuit via a PAD.

A fixed-frequency DC-DC converter oscillates when the duty-cycle ($d = t_{ON}/T$) is less than 0.5. The Slope Compensation technique is used to eliminate the oscillations [30] [31], [33].

Other methods of controlling switching frequency are Fixed t_{ON} [34], [35], [35] and Fixed t_{OFF} [36], [37], [38], [39], [40].

Fixed t_{ON} and Fixed t_{OFF} are one the dual of the other. Preferring one or the other depends on the type of application.

In our case, as the current sensing is on-chip and the internal R_{SENSE} is necessarily placed in series with the Power DMOS, we can only measure the current during t_{ON} as during t_{OFF} the load current recirculates externally through the freewheeling diode and the control system is blind.

The choice of Fixed t_{OFF} control was forced. In addition, this choice minimise the PINs, reduce the external components and simplify the PCB.

(Figure 2.6) shows the difference between constant frequency and Fixed t_{OFF}. In case of constant frequency the control system reacts to load variations and disturbances by varying the duty-cycle, while in case of fixed t_{OFF} by varying t_{ON}.

In the cases of Fixed t_{OFF} and Fixed t_{ON} controls, one speaks of quasi constant frequency.

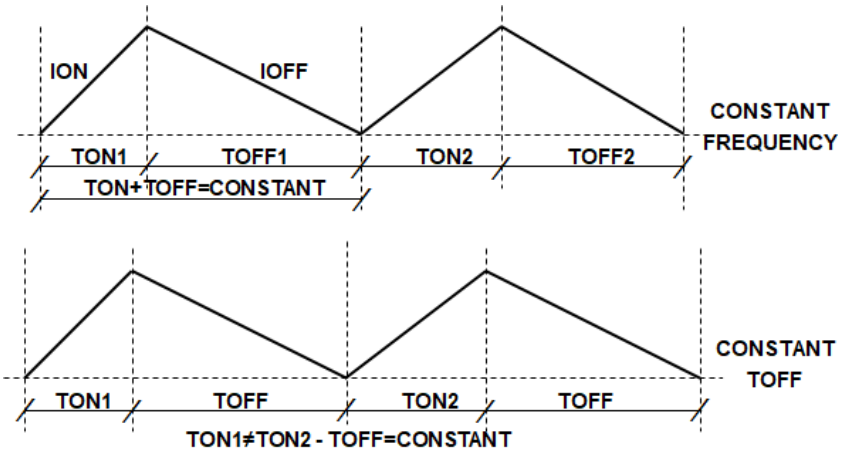


Figure 2.6: Fixed Frequency Versus Fixed t_{OFF}

Chapter 3

Start and Bootstrap Diode Blocks

3.1 Start Block

The Start and Bootstrap Diode blocks are the only ones connected to VCC.

The principle diagram of the Start block is shown in Figure 3.1. The ON pin is connected after the ESD protections to the HV (high voltage) switch M_1 which enables the current generator I_1. The current I_1 constitutes the drive signal for the bootstrap diode. Simultaneously with a similar circuit (M_2, I_2) the Feed Forward (FF) function is activated [41].

The Feed Forward function generates a signal proportional to the supply voltage VCC and changes the t_{ON} in presence of changes in VCC, so the work of the control loop is lightened accordingly and the stability of the output variable is increased, indeed recall that $V_{out} = V_{in}(t_{ON}/T) = V_{in}\,D$. The Start block is fed by PIN 'ON', while the connection to VCC is the feedback for the Feed Forward function.

When the PIN ON returns to GND, the information is purposely transferred with a certain delay (R,C) to the HV switch M3, which similarly to the previous cases, via I3, generates the shutdown signal for the entire system. The R-C delay is necessary both to avoid uncertainties during transitions and to give the control the necessary time to properly set the system for shutdown.

It should be noted that these are the only level-shifters in the Buck Converter and that the transmitted signals are in DC current as they are more immune to transitions between GND and VCC than voltage signals.

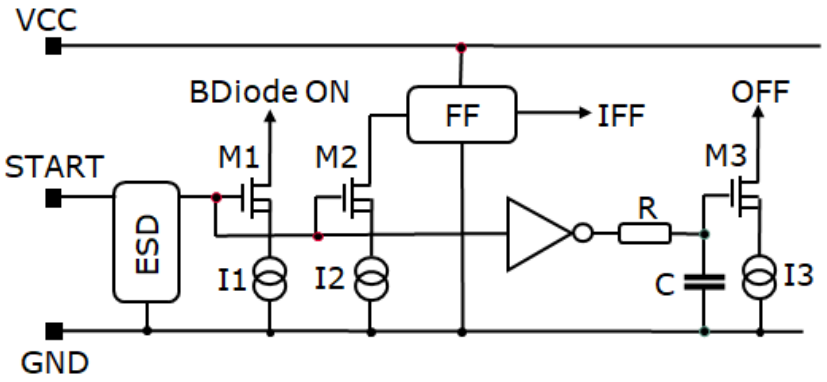


Figure 3.1: Start Block

3.2 Bootstrap Diode Block

When the Power DMOS is ON, its resistance is close to zero and brings the Source to a voltage value close to VCC. In this condition, all floating circuits are powered by the bootstrap capacitance loaded to a predefined value in the previous half-cycle. The bootstrap capacitance being of high value (from a few nF up to μF) constitutes for practical purposes a voltage supply.

In the discrete component solution, the implementation of the bootstrap capacitance charging circuit is quite simple (Figure 3.2). When the DMOS is OFF, the Source line is close to GND and the directly biased diode allows charging of the C_{BOOT} capacitance. The zener diode Z_{BOOT} defines the voltage of C_{BOOT} while the resistor R_{BOOT} limits the current drawn by VCC. When the DMOS is ON, the Source line is close to VCC and the inversely biased diode prevents the discharge of the C_{BOOT} capacitor.

This solution has some drawbacks, because more components are needed and more area is requested in the PCB, all of these translates into higher costs. Another drawback is the power consumption through Z_{BOOT} and R_{BOOT}, the latter of which must limit the current to rather high values in order to allow the system to function.

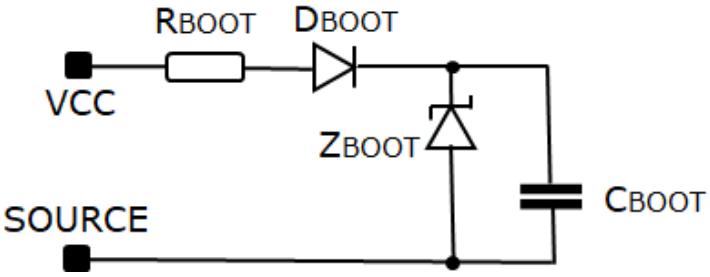


Figure 3.2: Bootstrap Diode, Discrete implemantation

The Bootstrap diode on chip realisation is necessarily different as no zener capable of carrying high currents is available and only reduced power dissipation is allowed. In Figure 3.3 is shown an outline schematic of the on chip Bootstrap Diode implementation [42].

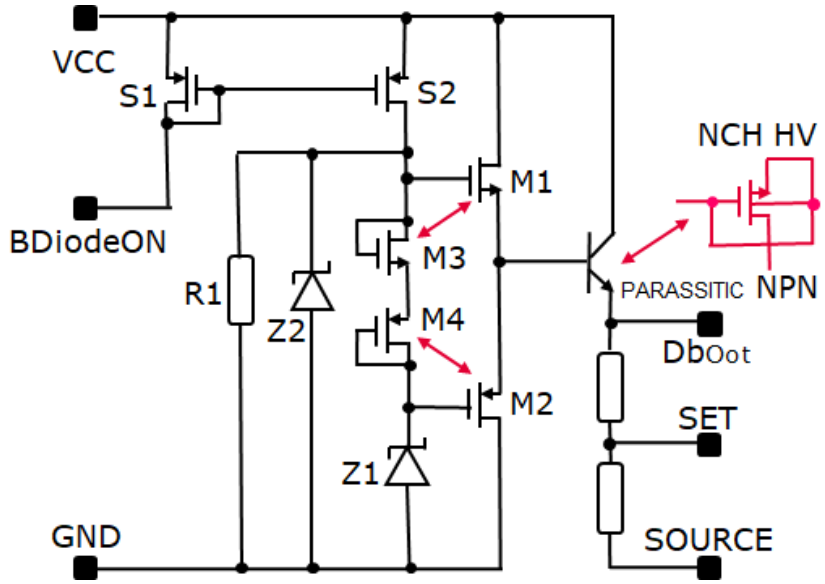


Figure 3.3: Bootstrap - Principle Schematic

The Diode-ON current signal activates via the current mirror S_1-S_2 the Bootstrap Diode bias circuit, this stage resembles the output of class AB amplifiers.

The output of the complementary pair M_1-M_2 feeds the npn-HV bipolar capable of delivering over a hundred mA to quickly charge the bootstrap capacitance. M_3 and M_4 coupled with M_1 and M_2 plus Z_2 settimg the base voltage of the npn, define the voltage of C_{BOOT} to approximately 7V. The zener Z_1 is a maximum voltage protection. The central point SET, of the resistive divider R_2-R_3, is the signal that enables the Buck Converter to function. When the bootstrap capacitance reaches 7V the bipolar Q_1 and the MOS M_1 are interdicted and the current drawn is reduced to that of the mirror S_1-S_2.

Unfortunately, the bipolar npn-HV component is not available in the technology. The nch HV parasitic npn was therefore used (Figure 3.4)

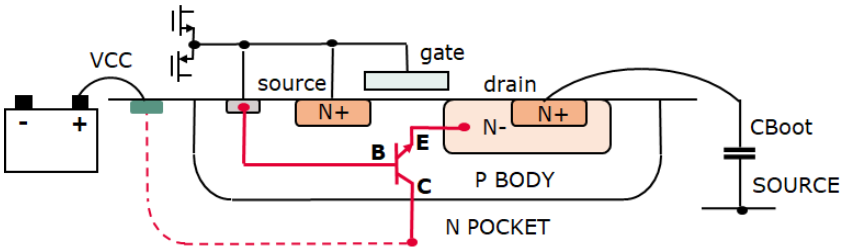


Figure 3.4: npn - Parassitic in High Voltage nch

The MOS nch HV having the gate, source and body short circuited is disabled. In Figure 3.4 the npn is shown in red, the substrate woks as collector, the pbody as base and the drain as emitter. The drain-emitter having the drain-extension has a breakdown voltage higher than the junction $N^+ PBody$ and is not damaged when the Power DMOS is ON and the voltage of the bootstrap capacity is about 7V above VCC.

Figure 3.5 shows the simulated behaviour of the bootstrap diode and the voltage across the bootstrap capacitance. It can be seen that during T_{OFF} as the diode is in

conduction the capacitance is charged, and during the T_{ON} pulse when the DMOS gate is charging shows a rapid drop in voltage. When 3V is reached at the gate, the charge transfer ceases and the voltage on the capacitance remains constant until the next T_{OFF}.

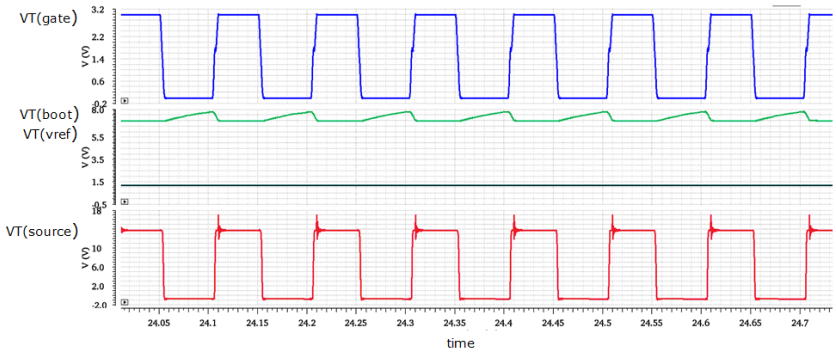


Figure 3.5: Bootstrap Diode behaviour

Chapter 4

Auxiliary Blocks

4.1 Introduction

In this chapter we describe the auxiliary circuits. The task of these circuits is to define the boundary conditions necessary for the proper functioning of the buck converter's control blocks.

The auxiliary blocks are 'Supply', 'Bandgap' and 'UVSD' (Under Voltage Shut Down), all of which are floating circuits, i.e. fed between Bootstrap capacitor and Source.

4.2 Supply Block

The 'Supply' block essentially performs two tasks, the first is to supply the voltages to the floating circuits, the second, once the supplies are present, is to give the 'Power ON' signal to the subsequent blocks. The schematic diagram is shown in Figure 4.1. "Supply" is necessarily powered by the Bootstrap capacitor (approx. 7V) as this is currently the only power supply available.

As soon as the block is energised, the two supplies, analogue (supA) and digital (supD), are generated independently. The supA power supply is dedicated to circuits that require current continuously, while supD supplies digital blocks that typically require pulsed currents. This reduces interference between the analogue and digital parts.

A set-reset flip-flop generates the "Power ON" signal. It is set by the "Set" signal generated in the "Bootstrap Diode" block. The "OFF" current signal from the "Start" block is converted into a voltage signal via resistor R_1, which resets the flip-flop and consequently switches off the Buck Converter. The voltages S_{UPA} and S_{UPD} are defined by a circuit represented for simplicity by zener Z_2. Being M_1, M_2 and M_3 matched they have the same V_{GS}, it follows that $S_{UPA} = V_{Z2} + V_{GSM1} - V_{GSM2}$ and similarly for S_{UPD}.

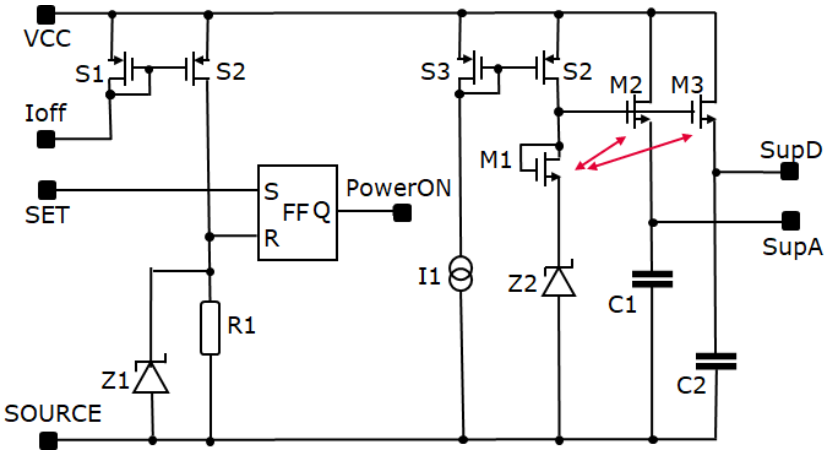


Figure 4.1: Supply - Principle Schematic

4.3 Bandgap Block

Voltage references are essential circuits in any electronic circuit, whether discrete or integrated. A reference circuit must be well-defined and insensitive to changes in temperature, power supply and load. In the past, the zener diode was often used as a voltage reference [42]. The zener breakdown voltage essentially involves two physical phenomena, ranging from the tunnel effect for low zener voltages with a negative temperature coefficient to the avalanche effect at high zener voltages with a positive temperature coefficient. In the intermediate range, the two phenomena coexist, and as the zener voltage increases, there is a gradual change from a negative to a positive temperature coefficient. The balance between the two generating a coefficient close to zero corresponds to a zener voltage of about 5V.

In integrated circuits, they are no longer used as a reference for several years, either because the zener values obtained is too high in relation to the circuit requirements or because they did not guarantee the required accuracy. Bandgap (BGR) circuits are universally used for voltage references [42]. Bandgap is usually used as a constant voltage reference. From the Bandgap, the reference voltages for the entire chip are generated.

Frequently, in the bandgap circuit starting from the reference voltage, a current references is also derived, but as $I_{REF} = V_{BANDGAP}/R$ the production spread and the thermal coefficient of R affect I_{REF}, which must at least be compensated in temperature. Trimming is used to correct the value. Unfortunately, the current bandgap does not exist.

The Bandgap core of implemented circuit is shown in Figure 4.2

The diodes D_1 and D_2, where $D_2 = nD_1$ play a fundamental role in the bandgap, values normally used for n are 8 or 10. In our case n=8 because this value allows the centroid layout, where the diode of multiplicity 1 stands in the centre.

Being the voltage on the diode

$$V_D = V_T \, ln(I_D/I_S) \qquad \text{where} \qquad V_T = KT/q \tag{4.1}$$

$$\text{results} \qquad V_{D1} - V_{D2} = \Delta V_D = V_T \, ln(I_{D1}/I_{S1} * I_{S2}/I_{D2}) \tag{4.2}$$

$$\text{since} \qquad I_{D1} = I_{D2} \qquad \textit{and} \qquad I_{S2} = nI_{S1} \tag{4.3}$$

$$\text{results} \qquad \Delta V_D = V_T\, ln(n) \qquad \text{for n=8 a 25°C} \qquad \Delta V_D = 52mV \tag{4.4}$$

There are also circuit symmetries: $P_1 = P_2$ and $N_1 = N_2$ form two current mirrors with a 1:1 ratio, $R_1 = R_2$, and as already mentioned $D_2 = 8D_1$.

The currents I_1 and I_2 are forced to be equal by the mirrors, also the voltages at the sources of N_1 and N_2 must be equal and equal to the voltage across D_1. It follows that $I_{R1} = I_{R2}$. From this we obtain the relation

$$I_{R1} = I_{R2} = V_{D1}/R_1 \tag{4.5}$$

V_{D1} has a thermal coefficient (NEGATIVE) of -2mV/°C - known as CTAT (Complementary To Absolute Temperature)

The voltage drop at the ends of R_2 is V_{D1}-V_{D2} = Δ_{VBE}. Hence the second relationship:

$$I_{D2} = \Delta V_{BE}/R_3 \tag{4.6}$$

DV_{BE} has a (POSITIVE) thermal coefficient proportional to KT, known as PTAT (Proportional To Absolute Temperature). Since

$$I_1 = I_2 = I_{R1} + I_{D1} = I_{R2} + I_{D2} \qquad \text{must be} \qquad I_{D1} = I_{D2} \tag{4.7}$$

I_1 and I_2 are the contribution of two terms proportional to CTAT and PTAT.

Now simply mix the curents $I_{R1} = I_{R2}$ and $I_{D1} = I_{D2}$ in the right proportion and complete the bandgap circuit as in Figure 4.3 into which mirror P_3 (mirror ratio 1:1) and resistor R_4 have been added. The resistors R_1, R_2, R_3 and R_4 are coupled and the same type to have equal thermal coefficient.

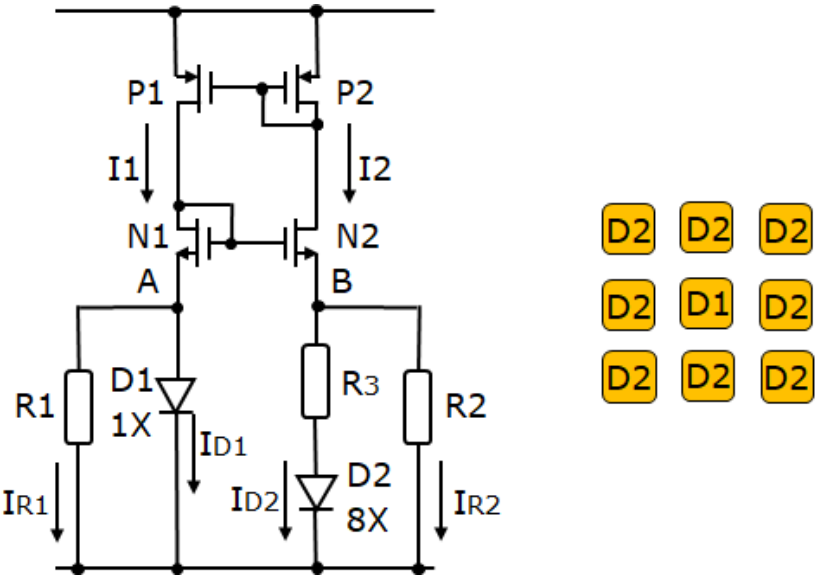


Figure 4.2: Implemented Bandgap Core

Since $I_1 = I_2 = I_3$ and since diodes in integrated circuits are always bipolars with base and emitter short-circuited, we shall henceforth denote V_D by (V_{BE}. We can therefore write

$$(V_{BE}/R_1 + \Delta V_{BE}/R_3) * R_4 = V_{ref} \tag{4.8}$$

If we set $R_3 = KR_1$ we obtain

$$(V_{BE}/R_1 + \Delta V_{BE}/KR_1) * R_4 = V_{ref} \tag{4.9}$$

$$\text{which becomes} \qquad (V_{BE} + \Delta V_{BE}/K) * R_4/R_1 = V_{ref} \tag{4.10}$$

K is not only the ratio between the resistances R_3 and R_1 but also the mixing factor of the terms CTAT and PTAT. By choosing it appropriately we can give to our voltage reference the slope we desire, not necessarily zero.

A curiosity, by properly choosing k, the currents I_{D2} and I_{R2} can be mixed so that the current I_2 is constant in temperature. However, it must be taken into account that is possible to pass from voltage to current only via a resistor which usually is affected by the production spread. The current reference will have the same spread despite having zero thermal coefficient.

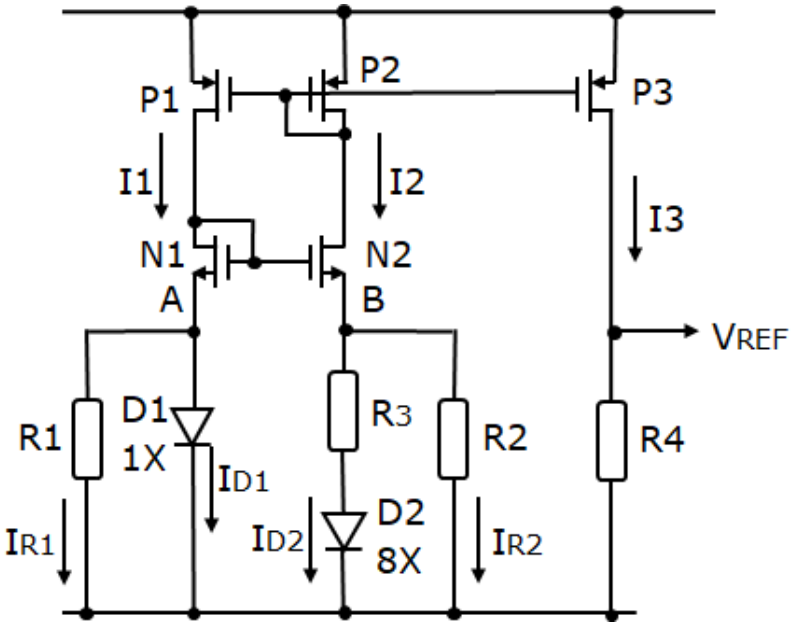


Figure 4.3: Bandgap core with reference voltage (V_{REF})

Figure 4.4 shows the contributions of the PTAT and CTAT currents. When poperly mixed the reference voltage is constant.

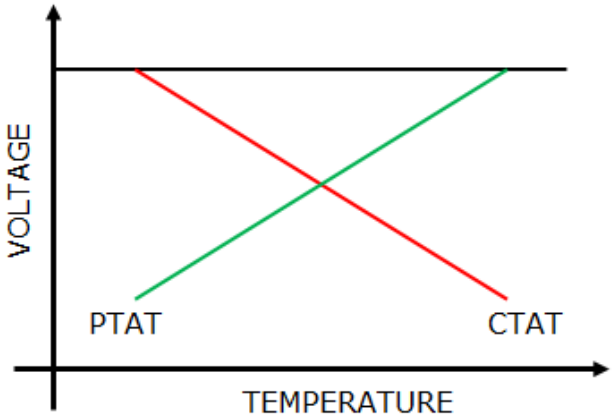


Figure 4.4: PTAT Vs CTAT

Figure 4.5 shows the PV (Process-Voltage) simulation over temperature of the implemented bandgap. The reference value is 1V and the simulated temperature range is (-40°C-150°C), typical automotive.

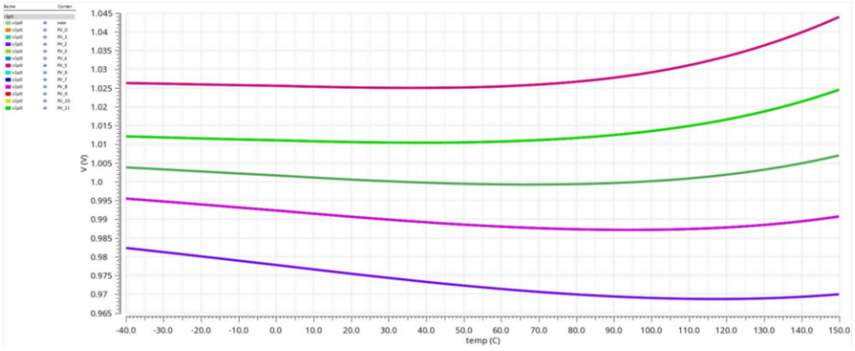


Figure 4.5: Voltage Reference - PV Simulation

The Monte Carlo simulation is shown in Figure 4.6. The mean value is 1.01V and sigma is 0.03%.

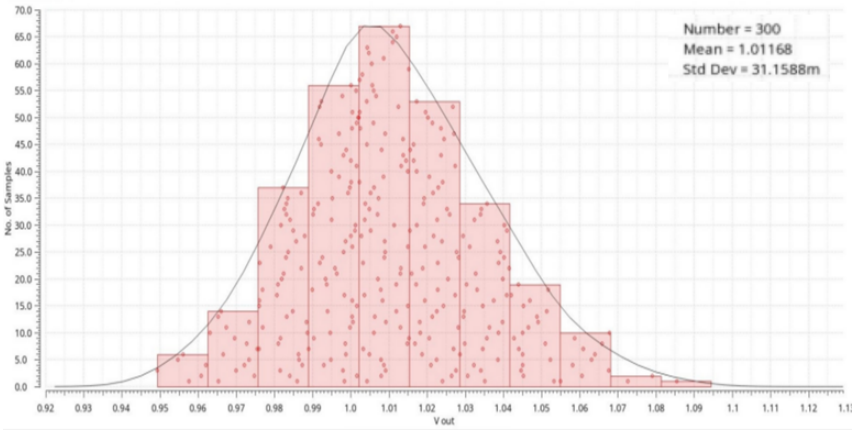


Figure 4.6: Bandgap - Montecarlo simulation

There is one last point to discuss, the 'Starter'. Bandgaps have multiple equilibrium points besides the working point and the Starter is the circuit that avoids unwanted equilibrium points and moves the Bandgap to the desired working point.

The Brokaw cell has two equilibrium points [42], one in the origin, which is unstable, and a second stable one which is the working point. Simply diverting the Brokaw cell from the equilibrium point at the origin is enough to make it evolve towards the stable equilibrium point.

Unfortunately, the Brokaw circuit requires too high supply voltage for many current requirements. Therefore, different circuit topologies are used, which are developed in "parallel" rather than "series" to reduce the supply voltage. We also use one of these in the Buck Converter.

Unfortunately, these have infinities plus 1 stable equilibrium points. In Figure 4.7 it can be observed from the I-V characteristics of the diode D_1 and the series $R_3 + D_2$ that $Vt_{D2} < Vt_{D1}$ and the current I_{R3+D2} due to the series resistance R_3 grows more slowly than the current I_{D1}. The two curves cross at the stable equilibrium point that we want as working point.

All other points in the segment O-Vt_{D2} are undesirable equilibrium points. In fact, in that segment, the currents I_{D2}=I_{D1} are zero and I_{R1}=I_{R2} even if different from 0 fulfil the conditions imposed by the circuit.

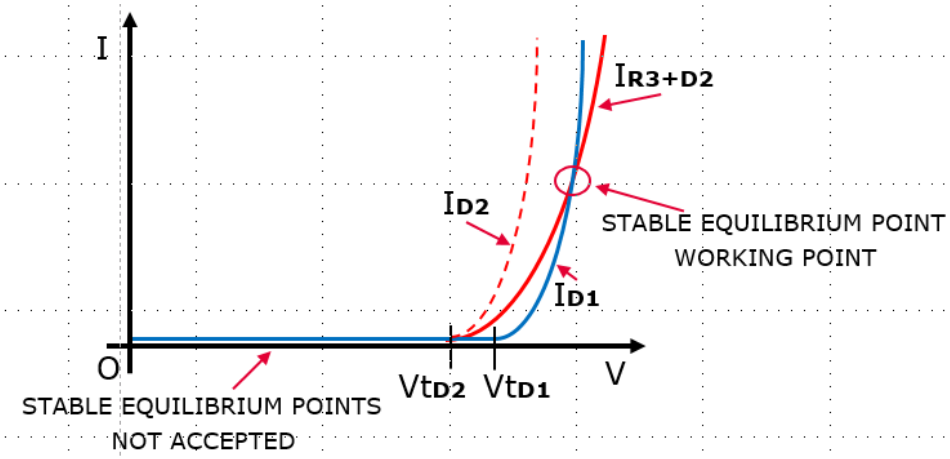


Figure 4.7: Bandgap Stable Equilibrium Points

We therefore need an appropriate 'Starter' that forces the bandgap to the desired working point. The one used in this Buck Converter is shown in Figure 4.8. The starter consists of a comparator with an intrinsic offset and inputs connected to the ends of R_3. Connected at the comparator output there are a switch N_3 with the current generator I_{OFFSET} in series.

In the segment O-Vt_{D2} the comparator inputs have the same null voltage, but due to the intrinsic offset (approx. 25_{mV}, 30_{mV}) the output of the comparator being high, enables the switch N_3 and the generator I_{OFFSET} starting a regenerative loop which ends only when a voltage equal to the intrinsic offset appears at the comparator inputs. At this point the offset is removed and the bandgap evolves to the working point.

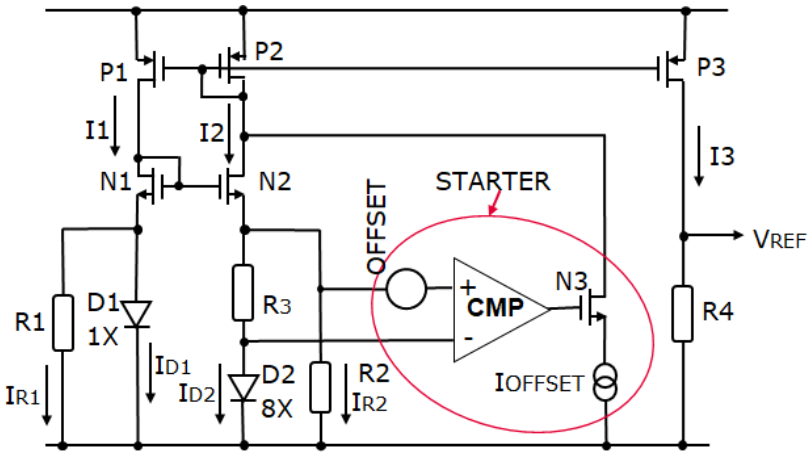


Figure 4.8: Bandgap Circuit Plus Starter Circuit

4.4 UVSD - (Under Voltage Shut Down) Block

The start-up moment of an integrated circuit is one of the most critical phases because at start-up, digital circuits, but also analogue ones, can assume states that do not guarantee a regular evolution of the device.

The UVSD is the block that gives the OK for the device to do what it was designed to do. This does not mean that before the OK the circuits are asleep. Quite the contrary, they are working on getting the circuits set up properly to allow a regular start. Let's take a digital and an analogue example. For a flip-flop, it is not equivalent to start with set or reset, the evolution can be completely different. Or for an OPA within a loop, starting with the compensation capacity unloaded or loaded to maximum voltage can make the difference between good operation or load failure.

The UVSD OK is not only dependent on the supply voltage of the various blocks, but also on the feedback from other blocks, e.g. the bgap-OK signal provided by Bandgap.

In the Buck converter design, in addition to monitoring the internal supply voltages, the UVSD is conditioned by feedback from bandgap and bootstrap voltage (Figure 4.9).

R_3 is in series with R_1 and R_2 or short-circuited depending on the output of the comparator CMP. When the relation

$$(H_{SUP} - L_{SUP}) \left(\frac{R_2 + R_3}{R_1 + R_2 + R_3} \right) \geq V_{REF} \tag{4.11}$$

together $BGAP_{OK}$ and $BOOT_{OK}$ the Buck converter is enabled.
When

$$(H_{SUP} - L_{SUP}) \left(\frac{R_2}{R_1 + R_2} \right) < V_{REF} \tag{4.12}$$

the Buck Conveter is disabled

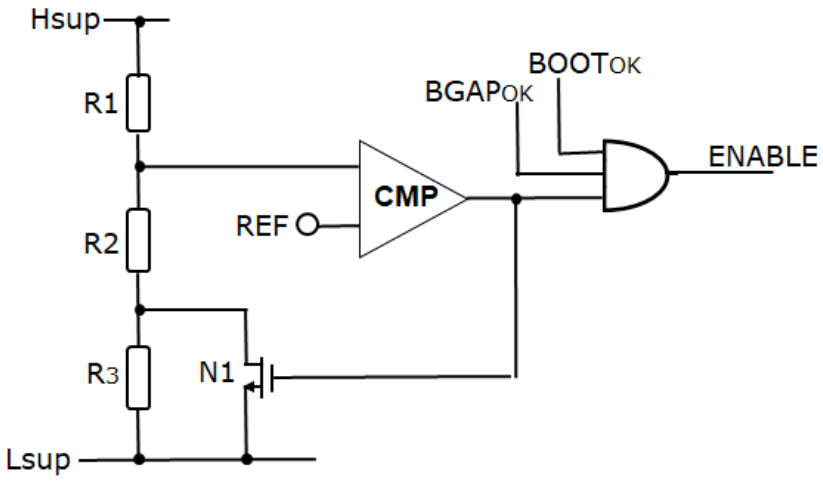


Figure 4.9: UVSD - Under Voltage Shut Down

Chapter 5

Control Driver

5.1 Introduction

In DC-DC converters the transfer of energy between input and output occurs with an intermediate storage of energy packets in the reactive components L and C. The storage is cyclic and is imposed by the switching frequency of the DMOS. It follows that the higher the frequency, the lower the energy stored in the single period in the L and C components. Therefore smaller reactive components, lower cost and lower volume required.

The driver plays a key role, as faster driver allows higher switching frequency with the advantages mentioned above.

A typical implementation is shown in Figure 5.1. Since the DMOS in ON condition has the source close to V_{CC}, the gate must be driven at a higher voltage. This voltage, provided by the bootstrap capacitor, is applied to the gate of the DMOS via the driver. Typically the driver is a series of trumpets as shown in figure.

If we call with Req the output resistance of the driver and approximate the input capacity of the DMOS with Ceq, we obtain the circuit in Figure 5.2. The time requested to charge Ceq is about 5 time constants, $5\tau = 5R_{eq}C_{eq}$.

It must be said that assimilating the charge of DMOS to the charge of capacity is a simplification. As explained in the Appendix, the capacitance between gate and drain C_{GD} plays a fundamental role in the charge of the DMOS

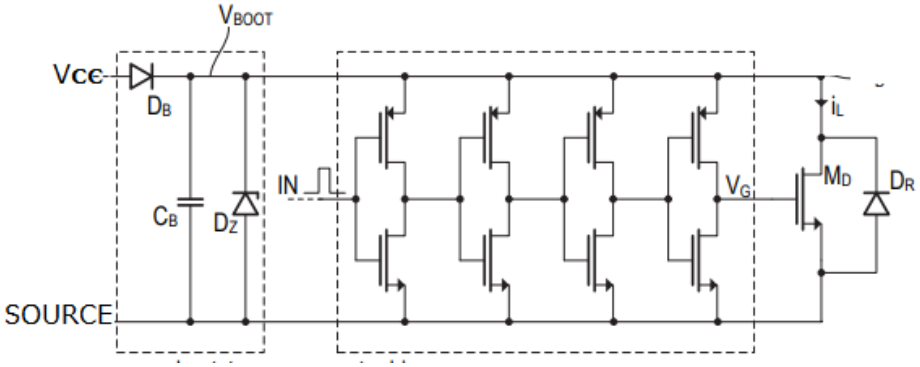


Figure 5.1: Example of Typical Driver Implementation

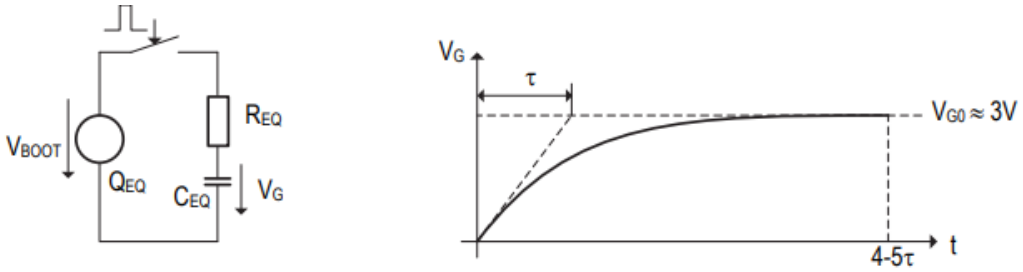


Figure 5.2: Driver Equivalent Circuit and Charging Capacitor Timing

5.2 High Speed Driver

An idea to increase the speed of the driver is to load the voltage of the Bootstrap capacitor with a higher voltage, in this way the Ceq capacity reaches the required voltage more quickly. The simulation of the DMOS gate charged with Bootstrap capacity loaded at 3V and 7V is shown in Figure 5.3, the time savings to charge the gate to 3V is dramatic .

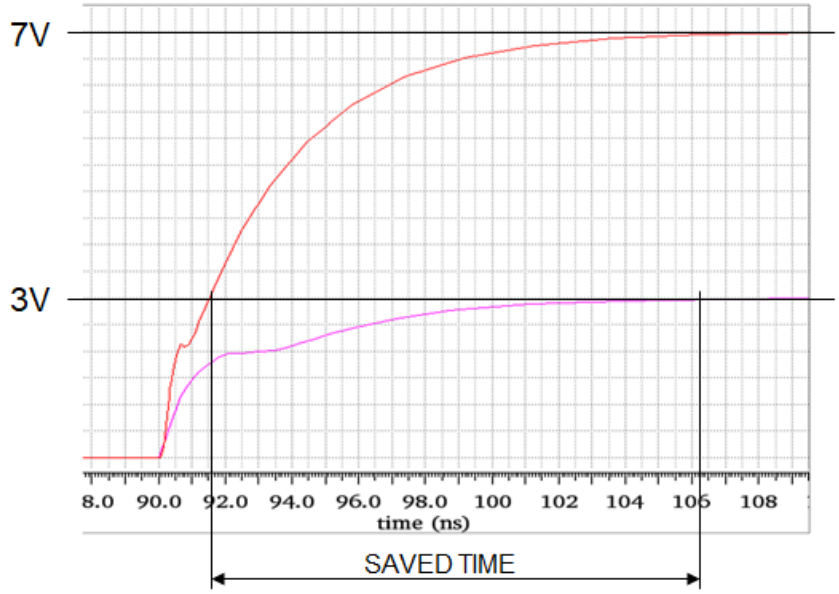


Figure 5.3: Difference in Charging DMOS with Bootstrap Voltage 3V and 7V

Observing the simulation it is also obvious that is required to stop immediately as soon as the gate reaches the allowed voltage otherwise the DMOS is destroyed. The solution of measuring the instant in which the gate reaches right voltage with a comparator can be accepted only for very low switching frequencies, i.e. only when the gate charge time is much greater than the comparator delay Figure 5.4.

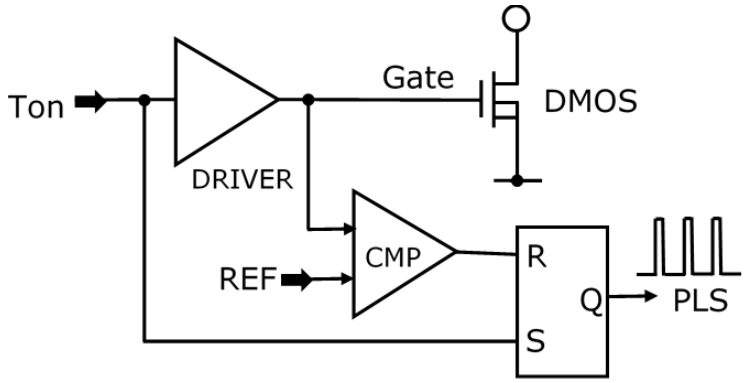


Figure 5.4: Gate Voltage Sensed with a Comparator

For high switching frequency a different approach is needed.

We can start by considering the Ton signal coming from the control circuit and the gate of the DMOS Figure 5.5, for convenience of explanation we divide the gate voltage into three parts, "turn ON" (1-2), "DMOS ON" (2-3) and "turn OFF" (3-4).

The turn ON is the real charging phase, the current supplied by C_{BOOT} through the driver charge the gate of the DMOS. In the next phase the DMOS is ON and is not loaded further.

Suppose to measure the turn-ON time (0-1) and from this generate the "PLS" pulse. The time interval between 1 and 2 define the "CLK" pulse. The sum of PLS and CLK is equal to T_{ON}. The interval (2-3) is the turn-OFF time.

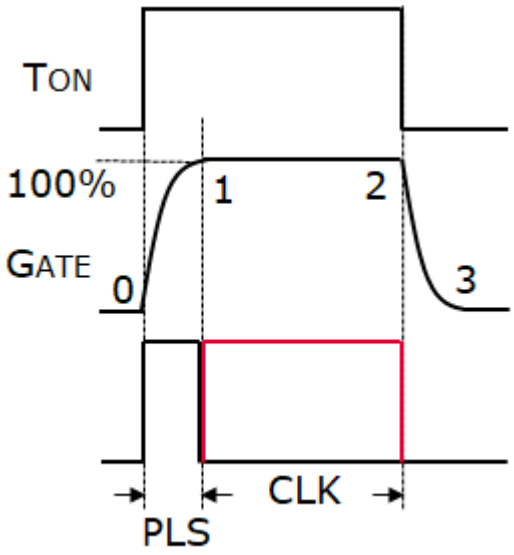


Figure 5.5: Relation Between Ton, PLS and CLK

Now let's do the opposite procedure. At the beginning of T_{ON} the PLS pulse is generated and with this the driver is activated, the driver is ON only during PLS, and during the rest of T_{ON}, that is CLK, it is OFF. We are thus sure that at the end of PLS the gate of the DMOS has reached the right value.

Now a method must be found to generate the PLS and CLK pulses.

The block circuit that implements the above mentioned control is shown in Fig-

ure 5.6. The pulse generator activated by T_{ON} sends the PLS pulse to the driver which loads the DMOS gate. Once PLS is finished, the CLK pulse begins and, by switching ON the synchronous switch, allows the C_{STORE} capacitor to store the gate voltage. The OPA compare the voltage across C_{STORE} with the voltage reference. The OPA_{OUT} output acts on the pulse generator to modulate PLS.

In other words, a feedback control, reading the gate voltage defines the driver switch-on time.

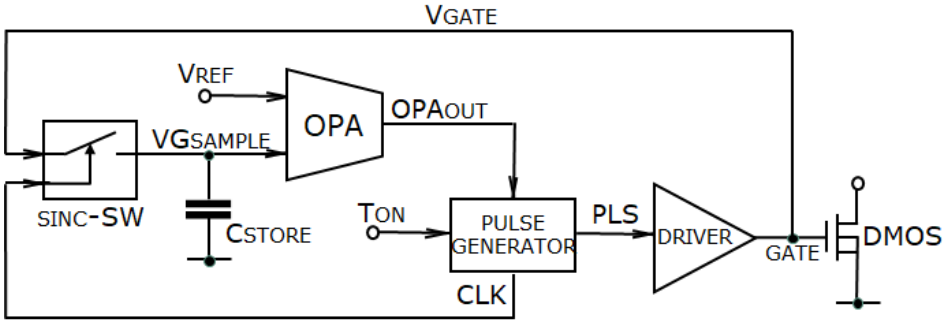


Figure 5.6: Circuit Loop that Generate PLS and CLK Pulses

Much attention must be paid at the start to avoid too long pulses. A Soft Start is therefore recommended. As soon as the DC-DC is turned on, a PLS pulse of minimum width is defined and not sufficient to reach the correct gate voltage, thus the closed loop control widens the pulse until the desired gate voltage is reached.

Figure 5.7 shows the block diagram of the circuit that generates the PLS and CLK pulses. Current I_{PLS} is the difference between the DC current I_0 and the current I_{OPA} delivered by the OPA. At the beginning of T_{ON} starts to loads the capacitance C_{PLS}. The "logic block" senses the capacitor voltage and depending on it defines the PLS and CLK pulses width. The current I_{PLS}, modulated by the OPA, charges C_{PLS} more or less quickly, thus defining PLS.

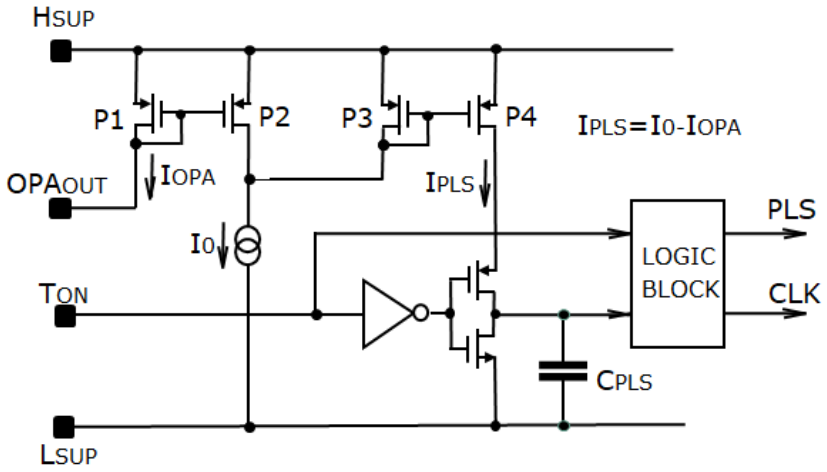


Figure 5.7: Pulse Generator Block

5.3 Driver Control Simulations

This paragraph shows some simulations of the Contol Driver related to the 10MHz Buck Converter.

In Figure 5.8 is shown the control driver loop stability. The Bode diagram reaches 0dB with 20dB/dec and shows a phase margin of about 75°.

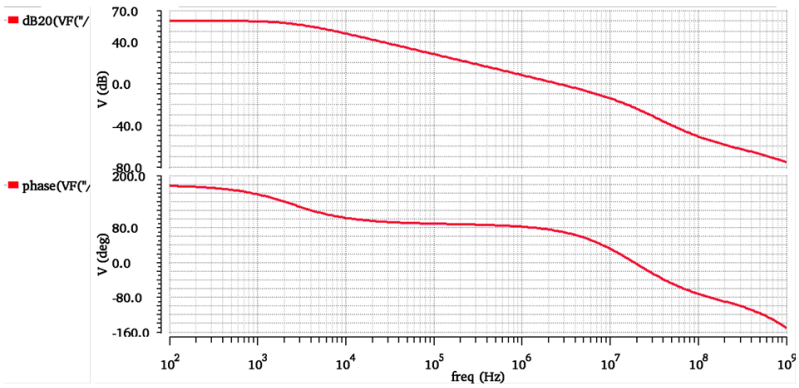


Figure 5.8: Control Driver Loop Stability

The Figure 5.9 shows for OPA a Gm at input balance of 0.05uA/mV.

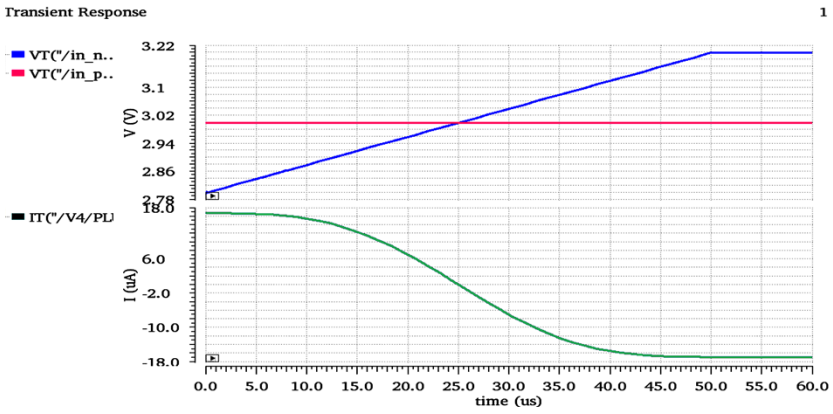


Figure 5.9: Control Driver - OPA Gm

The simulation in Figure 5.10 shows the generation of the PLS and CLK pulses. An input voltage of the OPA causes an output current, which modulates the PLS pulses depending on its value. The CLK pulses are the difference between Ton and PLS.

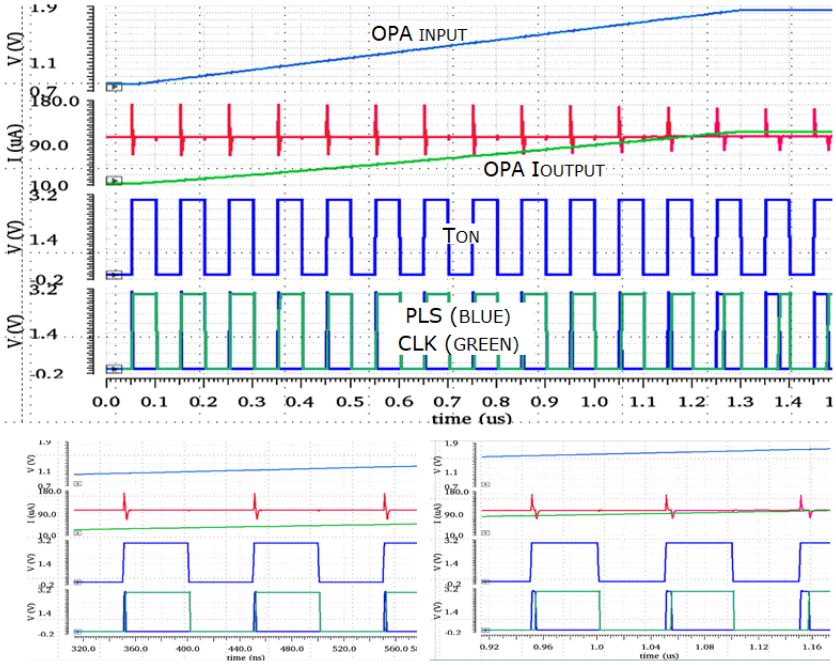


Figure 5.10: Control Driver - PLS Generator Block Simulation

Figure 5.11 shows the simulation of the PLS soft start. At the beginning the pulses, too tight to effectively drive the driver, gradually grow thanks to the closed loop control. The simulation frequency is 10MHz.

In Figure 5.12 a more detailed simulation of Inductor Current, PLS and CLK Pulses, T_{ON} and DMOS gate voltage. It is interesting to observe how the gate voltage of the DMOS reaches 3V before being abruptly stopped.

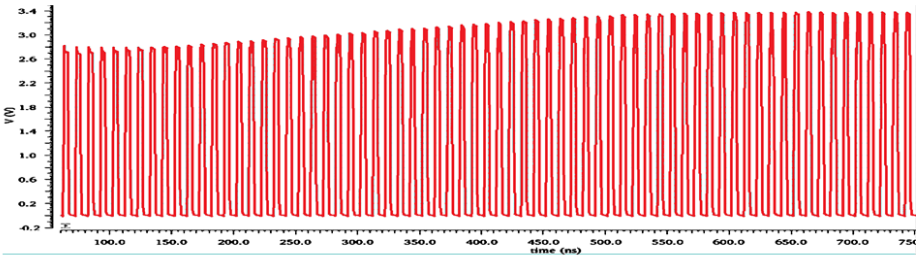


Figure 5.11: PLS Pulses Soft Start - 10 MHz Frequency

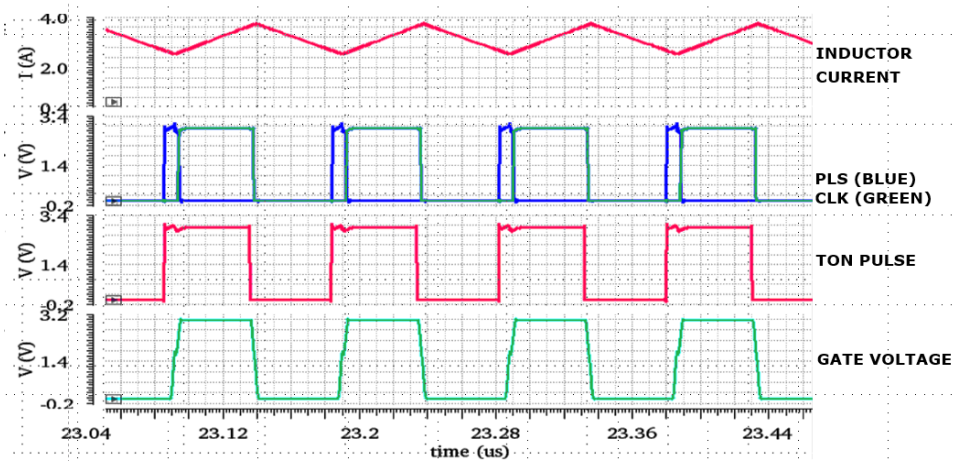


Figure 5.12: PLS and CLK Pulses - 10 MHz Frequency

Chapter 6

Current Sense and Control Logic - PVT Simulations

6.1 Current Sense

Knowing the load conditions is essential in all applications. In DC-DC Converters normally at least the load voltage and/or the load current informations are brought to the control circuit. In this Buck Converter, having to power a LED, we only need to know the current.

To monitor the current, an external Sense Resistor referred to ground and in series with the load is normally used. The voltage drop across it is the feedback signal for the control circuit. This solution is simple and has the advantage of monitoring the current throughout the all period, but this clearly maximizes the power consumption, especially when dealing with a high current LED (e.g. 3A). It also increases the complexity of the board in terms of components, connections, assembly.

When the sense resistor is connected to Ground, additional disadvantages especially in automotive arise from the fact that the LED won't be directly grounded.

For these reasons and thanks to the Infineon technology it was decided to integrate the current sense. The sensing used is shown in Figure 6.1.

The "Power DMOS" is divided into two DMOS of different sizes. The smallest (SenseDMOS) with the Rsense in series is the effective current sensing as the voltage drop across the resistor constitutes the feedback for the control circuit. The Rsense must therefore have a value such as to generate a measurable signal for the control circuit, and at the same time limit the voltage drop with respect to the Vds of the SenseDMOS in order to find a good compromise between the feedback signal and the current splitted in the two DMOSes as close as possible to the ratio of their areas.

If with K we indicate the ratio between the sensing current I_S and the total current $I_L = I_S + I_M$, we can write in the ideal case taking into account that the area of D_S in the developed Buck Converter is 15% of the total DMOS:

$$K_I = I_S/I_L = \frac{A_S}{A_M + A_S} = \frac{1/R_{DSS}}{1/R_{DSS} + 1/R_{DSM}} = \frac{0.15}{0.15 + 0.85} = 0.15 \qquad (6.1)$$

In the real case in series to M_S there is the resistance R_S , and this causes a deviation from the Ideal case. Thus

$$K_R = I_S/I_L = \frac{1/(R_{DSS} + R_S)}{1/(R_{DSS} + R_S) + 1/R_{DSM}} \tag{6.2}$$

The Current Sense values at ambient temperature are:

$$R_{DSM} = 90m\Omega \qquad R_{DSS} = 510m\Omega \qquad R_S = 100m\Omega \tag{6.3}$$

$$K_R = I_S/I_L = \frac{1/(510m\Omega + 100m\Omega)}{1/(510m\Omega + 100m\Omega) + 1/90m\Omega} = 0.128 \tag{6.4}$$

Because the resistance R_S, K_R is affected by a deviation of 15% and this systematic error must be taken into account during the design.

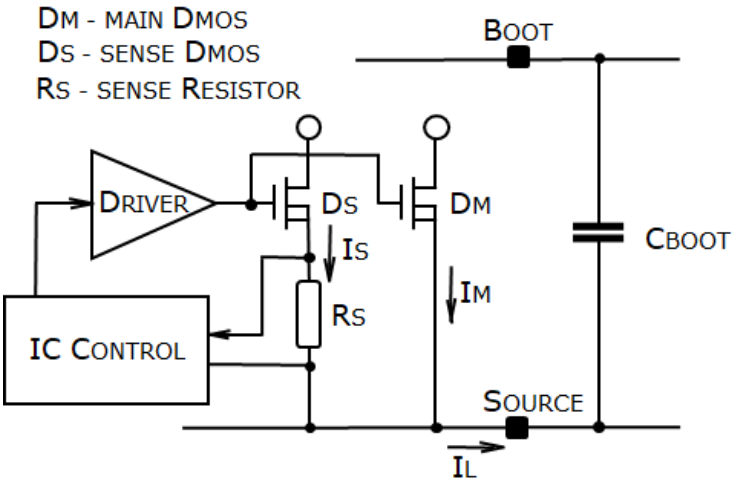


Figure 6.1: Current Sense

Looking at the Figure 6.1 this structure has the drawback that being Rs in series with Ds, the Gate charging current flows through Rs generating a high peak current that causes an error in the measurement of the load current (Figure 6.2). To avoid a wrong feedback this peak has to be masked.

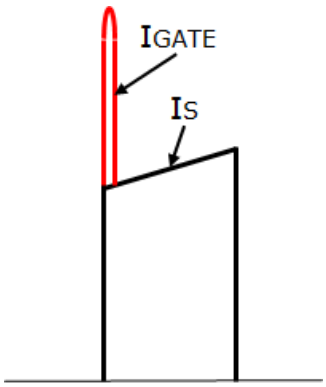


Figure 6.2: Peak Gate Current Superimposed on Is

With the current sense in series to the DMOS it is possible to read the current only during T_{ON}, and during T_{OFF} the circuit is blind. For this reason it has been adopted a control topology based on the fixed T_{OFF}. Even reading the current during T_{ON} only, the Control Circuit developed allows to control the average load current regardless of the duration of T_{ON} and T_{ON}.

The Main DMOS consists of four equal fingers coupled two by two with the Sense DMOS and Rsense in between. Since the sense DMOS is central and his size is comparable with a DMOS finger, a good matching is guaranteed (Figure 6.3)

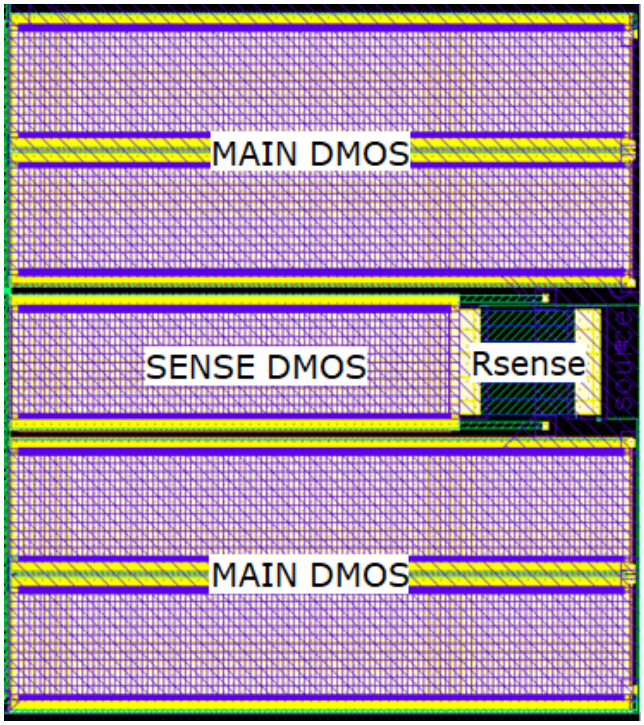


Figure 6.3: DMOS and Current Sense Layout

6.2 Control Logic

The purpose of the developed buck converter is to control the average current supplying the LED. The control circuit loop is shown in Figure 6.4. The 'CTL Driver' and 'Driver' blocks are shown in dotted line as they are described in the previous chapter.

The signal provided by the R_{SENSE} can be considered the control input, it consists as already mentioned of the voltage signal generated by the current flowing in D_S with superimposed the peak of the D_S gate charging current. This pulse is fundamental for the operation of the circuit, but for the LED current control it represents a source of error and must be removed. Another risk is the tripping of current protection. Since the gate current spike is in phase with PLS pulse, the complementary CLK pulse generated by the "CTL Driver" block is used to synchronise the sampling switch and remove the spike.

The voltage signal across R_{SENSE}, sampled through "Sinc-SW" and cleaned of the gate spike, becomes a trapezoidal signal proportional to the current in the load during T_{ON}. The load current during T_{OFF} cannot be read with the implemented

Current Sense, but must necessarily be trapezoidal in shape with the base length defined by the $FixT_{OFF}$ block, and it connects two successive T_{ON} trapezoids.

The trapezoidal signal at the switch output passes through the "Low Pass Filter" Block and is transformed into the DC signal $I_{L-AVERAGE}$ representing the average current through the LED

$I_{L-AVERAGE}$ is compared by OPA with the load current reference R_{EF} to generate the comparator first input. The other input is a triangular ramp modulated by VCC via the "Feed Forward" function. The comparator transition determines the T_{ON} end and the beginning of T_{OFF}.

The "CTL Driver" block provides the CLK and PLS signals with which the Driver is driven.

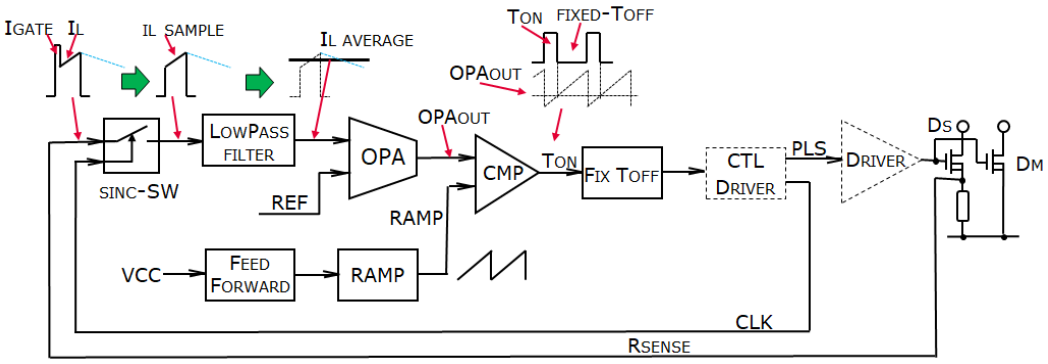


Figure 6.4: Buck Converter Control Loop

6.3 10 MHz Buck Converter Simulations

This section shows some simulations of the 10MHz Buck Converter version. The 1MHz and 4MHz versions show similar behaviour.

The DMOS gate soft start is shown in Figure 6.5. The effect of the closed loop control in the Control Driver block is evident. the PLS pulse starts with a very narrow pulse and is widened until the DMOS gate reaches 3V.

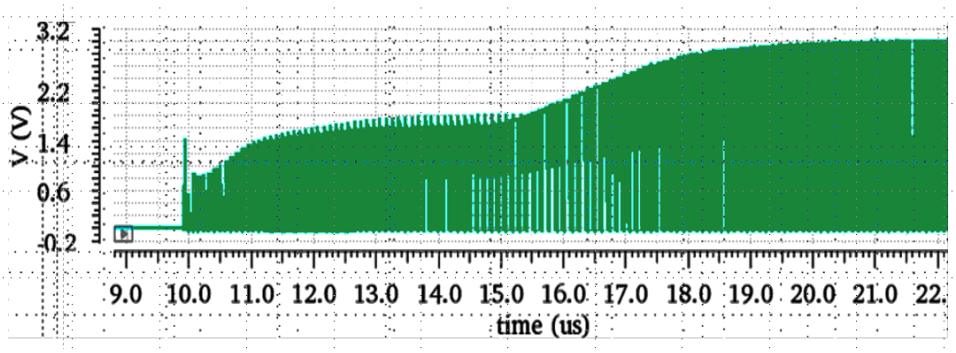


Figure 6.5: DMOS Gate Voltage Soft Start

In Figure 6.6 are shown the T_{ON} pulse generated by the Control Driver and its division into PLS and CLK pulses. The last row is the voltage across R_{SENSE} where the peak of the gate charge is clearly visible.

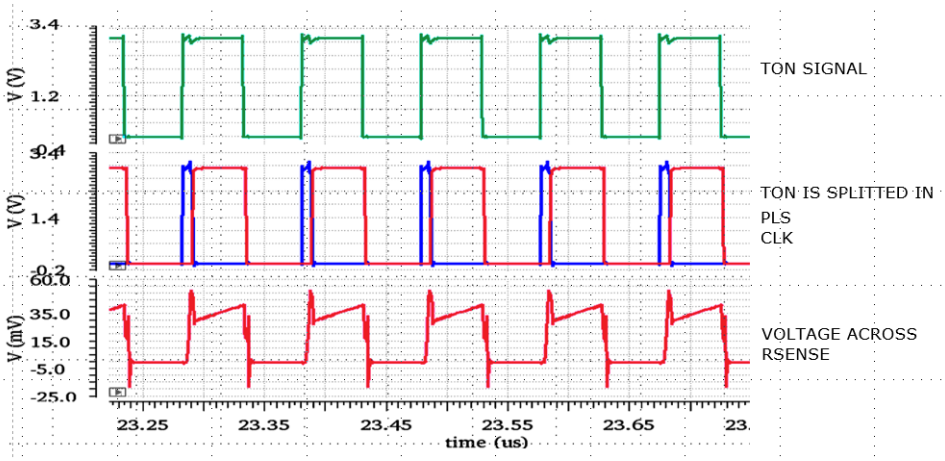


Figure 6.6: T_{ON}, PLS, CLK Pulses and R_{SENSE} Voltage

In Figure 6.7 the inductor current is compared with the R_{SENSE} current appropriately scaled

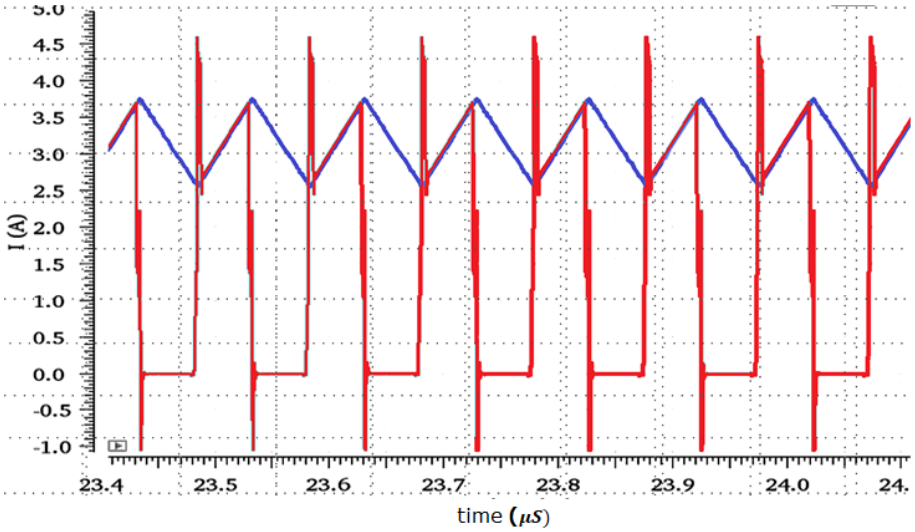


Figure 6.7: Inductor and R_{SENSE} Current (Scaled)

In Figure 6.8 several control circuit signals are shown.

The first row compares the voltage across R_{SENSE} with the I_L signal at the output of the Low Pass filter. Even though the current is read only at the T_{ON}, a signal proportional to the average load current is obtained.

In the second row there is the comparison between the triangular ramp and the OPA OUT. The intersection of the two curves defines the start of T_{OFF} whose duration is 60nS (third line). The last line shows the total current of the two DMOSes.

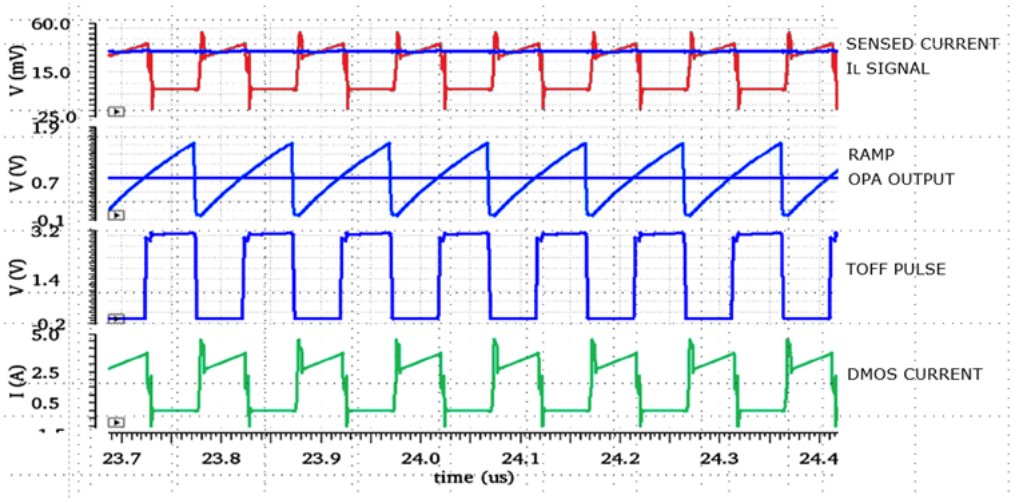


Figure 6.8: R_{SENSE} voltage versus I_L, Ramp Signal Versus OPA_{OUT}, T_{OFF} Pulse, DMOS Current

6.4 4 MHz Buck Converter PVT (Process, Voltage, Temperature) Simulations

Since the 4MHz switching frequency device is the most commercially attractive, we show PVT simulations of the device in the complete buck conveter system, including load and discrete elements (Figure 1.7).

Figure 6.9 shows the load current, the t_{ON} pulse and the V_{GS} on DMOS in typical case: V_{CC}=12V, ambient tempeature and load current 3A.

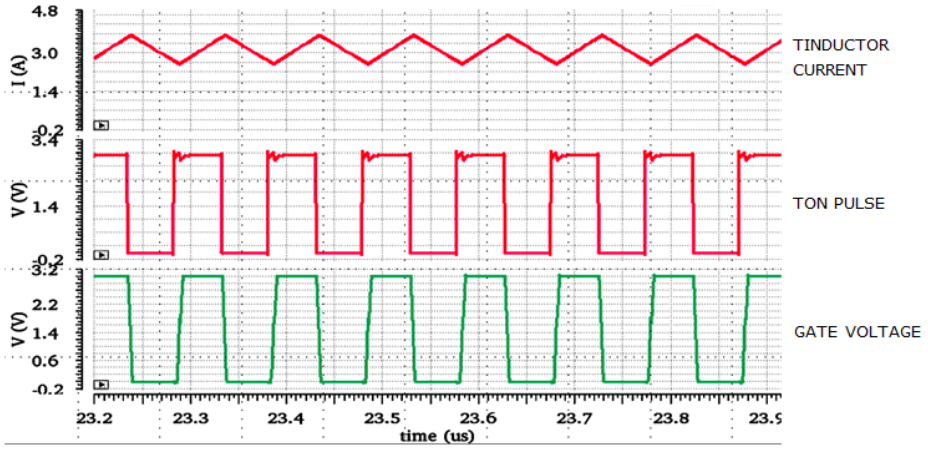


Figure 6.9: 4 MHz Simulation - Typical Case

The DMOS V_{GS} shape is fundamental as it represents a summary of the correct operation of the closed loop driver proposed in this work.

It is thanks to this innovative driver that the DMOS gate reaches 3V an order of magnitude faster than conventional drivers, allowing high switching frequencies.

PVT simulations are performed by crossing extreme operating conditions: battery voltage (7V/12V/18V), temperature (-40°C/27°C/150°C) and process (min/max/max-min/min-max).

Figure 6.10 shows an overview of the PVT simulations of V_{GS}. It can be seen how the V_{GS} reaches the value of 3V almost in a straight line and then abruptly stopped.

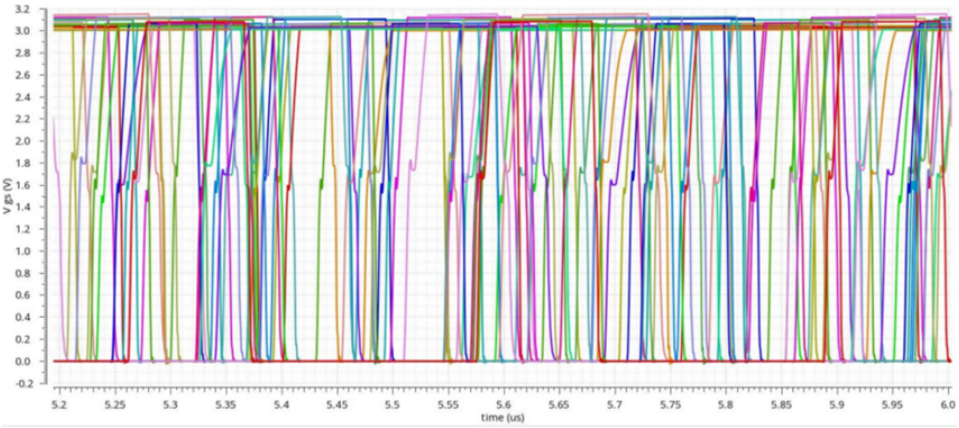


Figure 6.10: 4 MHz PVT Simulation - V_{GS}

Figure 6.11 shows an overview of the PVT simulations of the square wave voltage on Source PIN.

V_{SOURCE} and V_{GS} are correlated in that a fast DMOS switch-on implies a fast transition of the Source pin between GND and VCC. In Figure 6.11 in addition to the quick transition the three simulated supply voltages (7V,12V,18V) are evident.

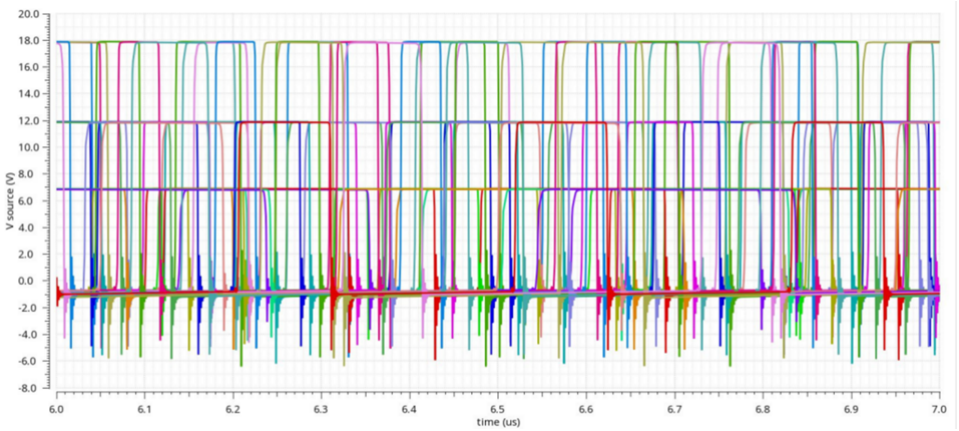


Figure 6.11: 4 MHz PVT Simulation - V_{SOURCE}

In figure 6.12 and figure 6.13 five of the previous simulations are shown to better highlight the transitions of V_{GS} and V_{SOURCE}

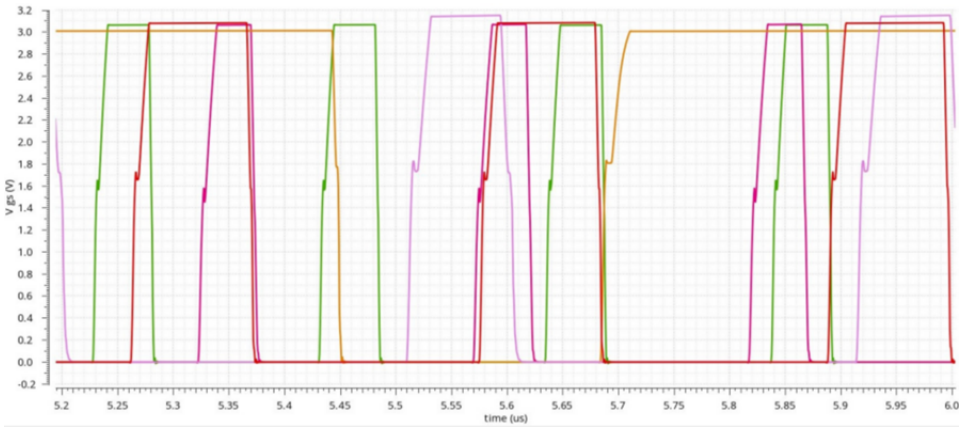


Figure 6.12: 4 MHz PVT Simulation Zoom - V_{GS}

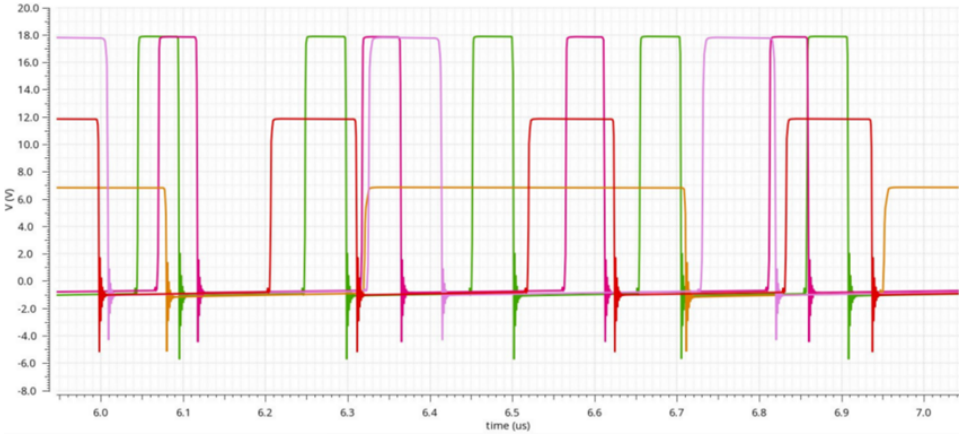


Figure 6.13: 4 MHz PVT Simulation Zoom - Source

Chapter 7

Layout

7.1 Buck Converters Layout

Since a small silicon rectangle has been reserved for us in a development silicon lot we want to diffuse the three Buck Converters, assemble and measure them in the laboratory, we therefore layouted the three devices. For reasons of practicality and time, we first designed the 10MHz version and then derived the 1MHz and 4MHz versions with a limited number of changes.

The layout is shown in Figure 7.1. It is clearly visible that this is a prototype as development time prevailed over area optimisation. In fact, not being a production device where saving area is essential, care was taken to do it within the assigned time. In a development lot, it is crucial to keep to the schedule as different groups come in to test their ideas, hypotheses, circuits, etc., and a delay becomes a delay for everyone.

Looking at the layout Figure 7.1, the Power DMOS with the sensing is on the right, while the control and auxiliary circuitry are in the left half. The PADs are outside the circuitry and not embedded in it as is usual in the production chips. In the lower part are the PADs 'lsup' (GND), 'on-pin' (ON) and 'supply-hv' (signal VCC). In the upper part there are 6 PADs divided into groups of three. The three on the right are in parallel and connected to the Main DMOS Source and the R_{SENSE} resistor. At the top left are the three PADs 'Boot1', 'Boot2' and 'Boot3'. Externally they are all connected to Bootstrap capacity, while internally they feed different circuits so that disturbances from the noisiest circuits do not affect quieter circuits.

The power VCC is the package lead-frame to which the substrate is connected. The substrate coincides with the DMOS Drain.

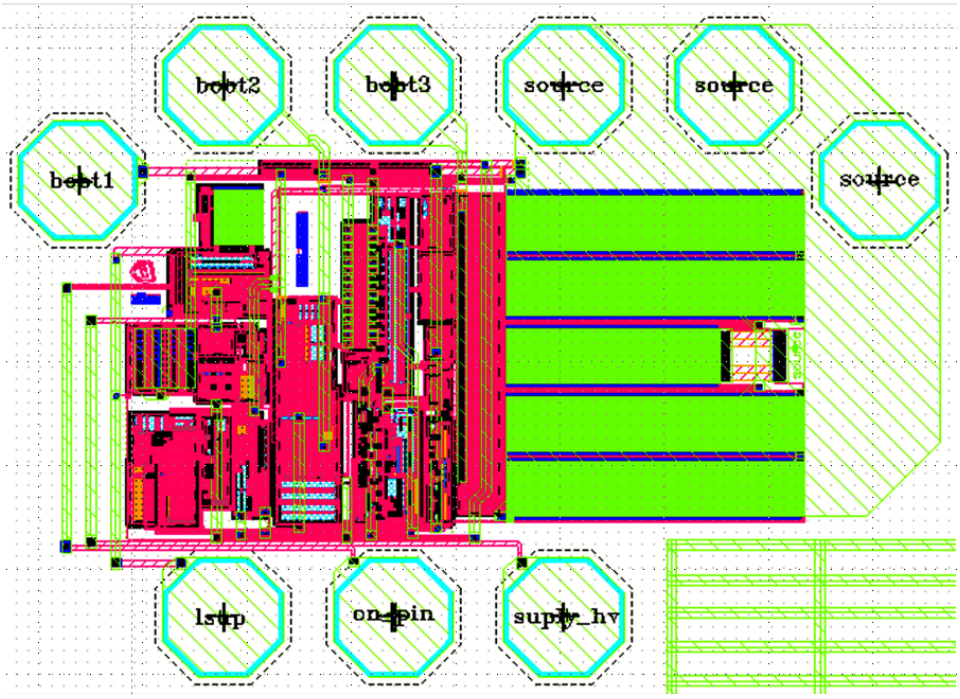


Figure 7.1: 1MHz, 4MHz, 10MHz Buck Converter Layout

Unfortunately, the silicon area assigned to us is not sufficient to place all three layouts, so it was decided to place two in this "development lot" and the third in the next one.

In this run, the 1MHz and 4MHz versions were chosen, however, it was necessary to reduce the Bootstrap PADs from three to two and to change their position. The Figure 7.2 shows the layout of our silicon rectangle.

In addition to the silicon layout, the Bonding Diagram layout for the plastic and ceramic packages of both devices must also be prepared (Figure 7.3 and Figure 7.4).

The packages of devices in production are almost always plastic, so it is essential to test the device in its final environment. It is in fact the device in the plastic packaging subjected to reliability tests, and this requires assembly in the production lines, often located in Far East. Clearly, this is not a fast process and the time required for their availability is often a couple of months.

For initial measurements, ceramic packages are therefore used, which are frequently inferior in performance, but as they are assembled on site they are available in a couple of days or so.

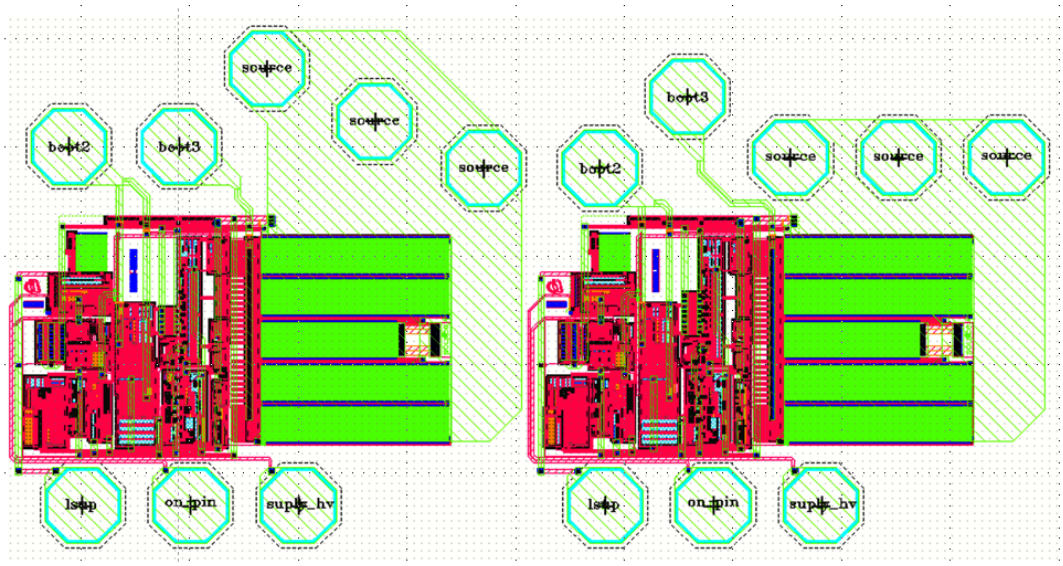


Figure 7.2: 1MHz, 4MHz, Buck Converter Layout in Silicon Test Chip

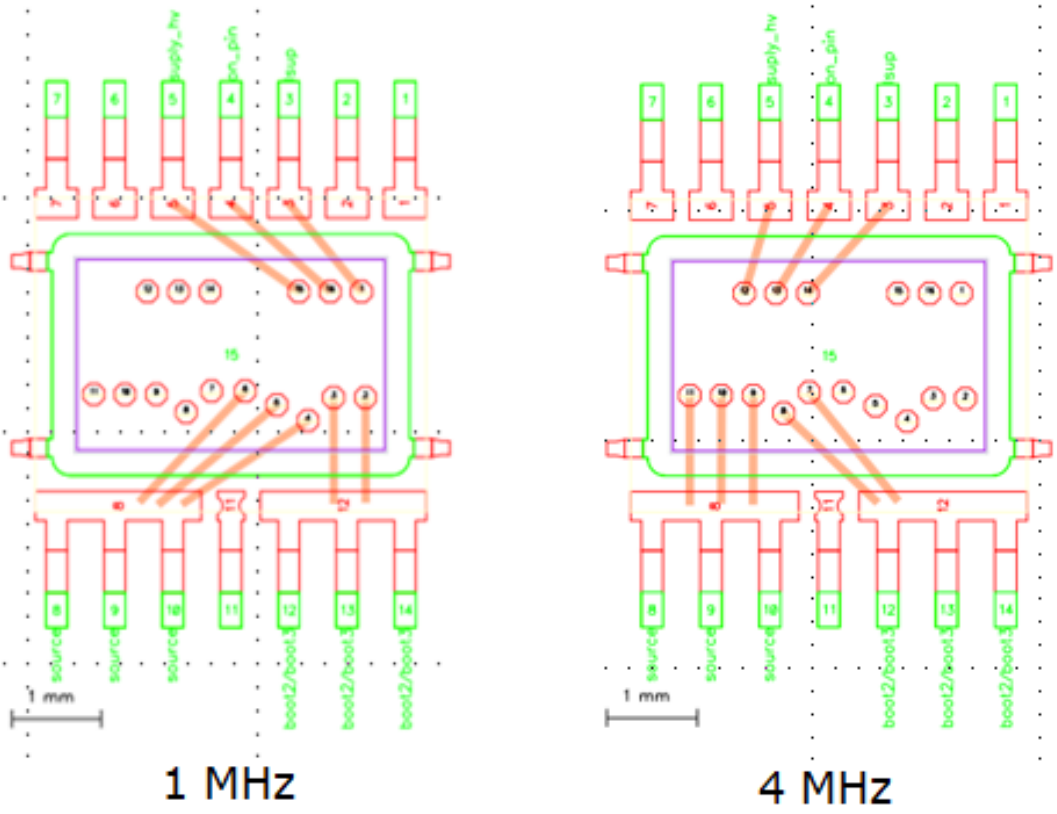


Figure 7.3: 1MHz, 4MHz, Plastic Package Bonding diagram

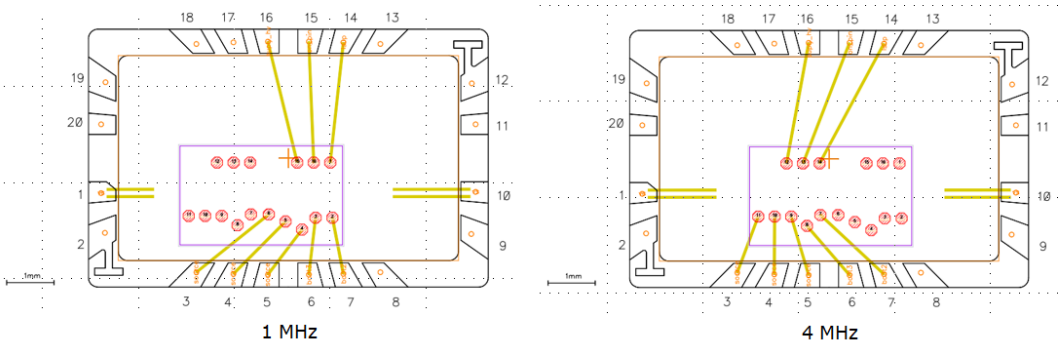


Figure 7.4: 1MHz, 4MHz, Ceramic Package Bonding Diagram

At the time of writing, the two devices are in diffusion. Wafer out is planned for February 2023.

Chapter 8

PCB Design

8.1 Introduction

While the devices are under diffusion, the PCB for testing the devices in laboratory must be prepared. This phase also requires the use of the simulator. It is, however, a simulator oriented towards the development of printed circuit boards, which is necessarily different from those used for the development of integrated circuits.

The PCB is designed considering the complete system, so the top view of the device including bonding wires and Spice models of the external components are used (Figure 8.1 and Figure 8.2)

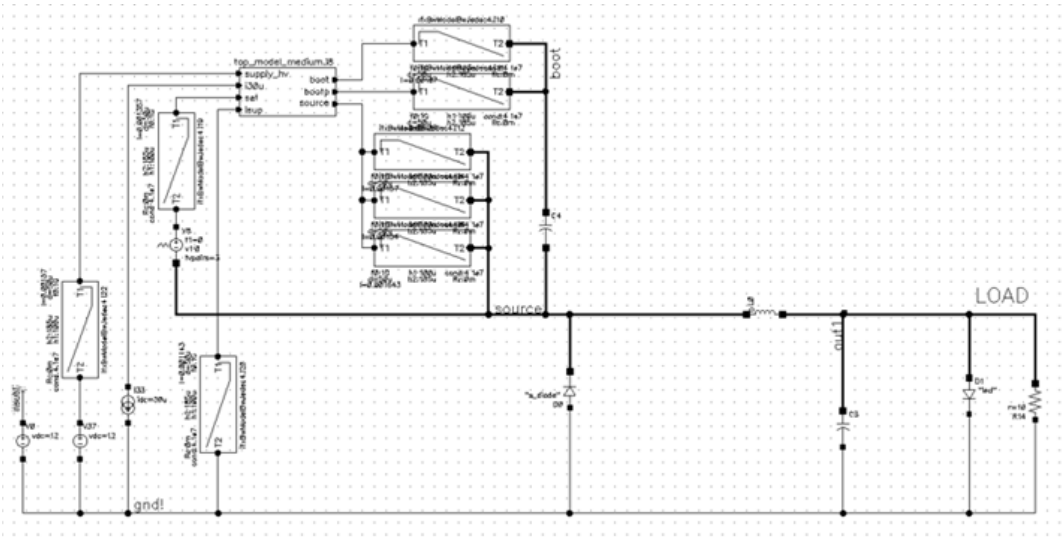


Figure 8.1: PCB Schematic with Real Components

CAPACITOR MODEL
subckt C1206C105K5RACTU 1 6
//Temp = 25°C, Bias = 0VDC, Center Frequency = 10000 Hz
//KEMET Model RLC Cerm
R1 (3 4) resistor r=0.264628827571869
R2 (2 5) resistor r=2.54999995231628
R3 (1 6) resistor r=1000000000
L1 (1 2) inductor l=3.35000027718024E-11
L2 (2 3) inductor l=6.36500052664246E-10
C1 (4 6) capacitor c=9.63658521868638E-07
C2 (5 6) capacitor c=1.67999994754791E-12
ends

INDUCTOR MODEL
subckt LL123 1 5
//Temp = 27°C, Bias = 0VDC, Frequency = 4000000 Hz
//KEMET Model RLC Cerm
R2 (1 2) resistor r=0.024
Rv2 (2 5) resistor r=1380
Rv1 (2 4) resistor r=0.706
R1 (3 5) resistor r=20
L1 (4 5) inductor l=1.133E-6
C (2 3) capacitor c=0.00000000000151
ends

DIODE MODEL
subckt s_diode 1 2
d1 1 2 dm
r1 1 2 resistor r=4.936E+7
simulator lang=spice
.MODEL dm D
+ IS = 1.656E-6
+ N = 1
+ BV = 44
+ IBV = 0.001
+ RS = 0.03034
+ CJO = 5E-10
+ VJ = 0.3122
+ M = 0.4761
+ FC = 0.5
+ EG = 0.69
+ XTI = 2
simulator lang=spectre
ends

LED MODEL
subckt led 1 2
dx 1 2 dled
simulator lang=spice
.MODEL dled D IS=2a RS=0.3 N=0.1
simulator lang=spectre
ends

BONDING MODEL
Bonding spec for all=>
Conductivity: 4.1e7 (Gold)
Die height: 185u
Loop height: 100u
Length [m]:
Supply_hv: 0.00157
Set: 0.001357
Gnd: 0.001143
Source1: 0.00157
Source2: 0.00154
Source3: 0.001643
Boot1: 0.00107
Boot2: 0.00107

Figure 8.2: External Components Model

8.2 PCB Simulations and Development

The PCB was developed for the 1 MHz and 4 MHz devices currently in diffusion, and for reasons of practicality, a single board was developed that is suitable for both chips. The PCB simulations show that the complete application with real components is in good agreement with what was seen in the simulations for the silicon development.

Figure 8.3 and Figure 8.4 show the startup phase, while Figure 8.5 and Figure 8.6 show the two applications under stationary conditions.

The printed circuit board suitable for both devices is shown in Figure 8.7

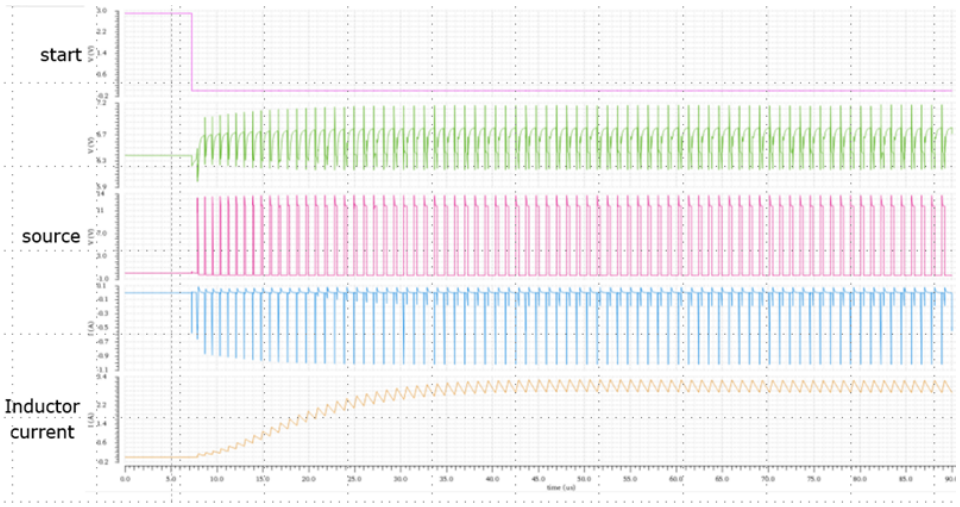


Figure 8.3: PCB Startup Simulation - Frequency 1 MHz

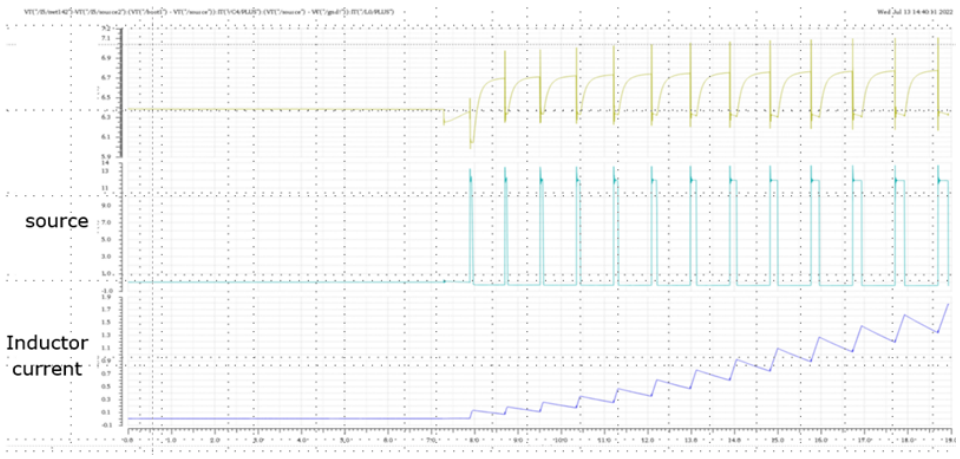


Figure 8.4: PCB Startup Simulation - Frequency 1 MHz - Zoom

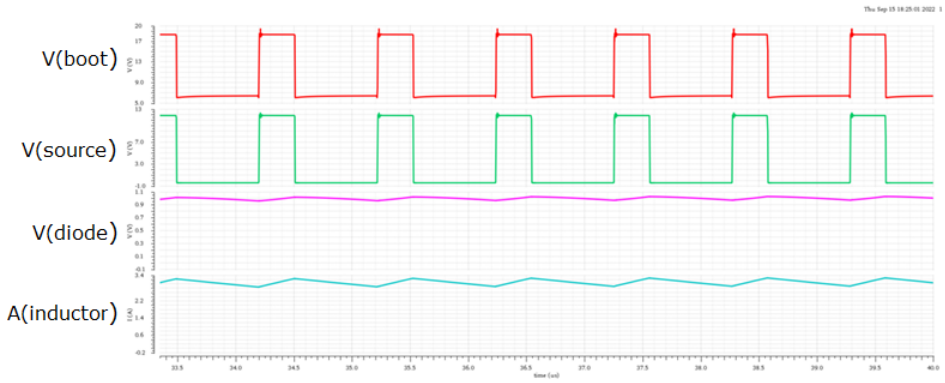


Figure 8.5: PCB Steady State Simulation 1 MHz

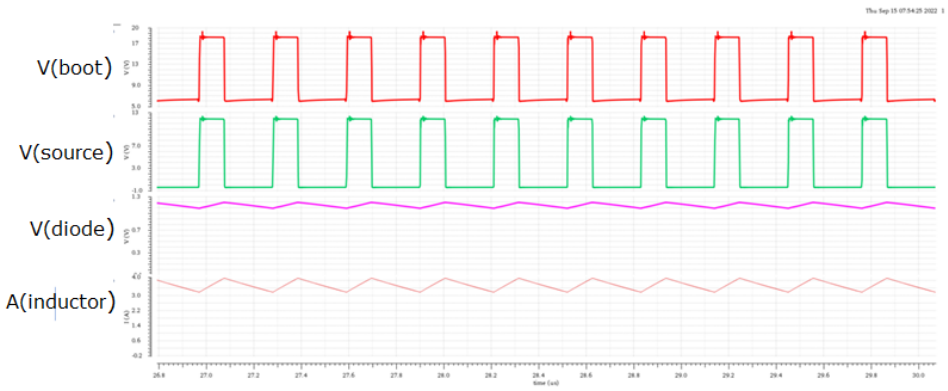


Figure 8.6: PCB Steady State Simulation 4 MHz

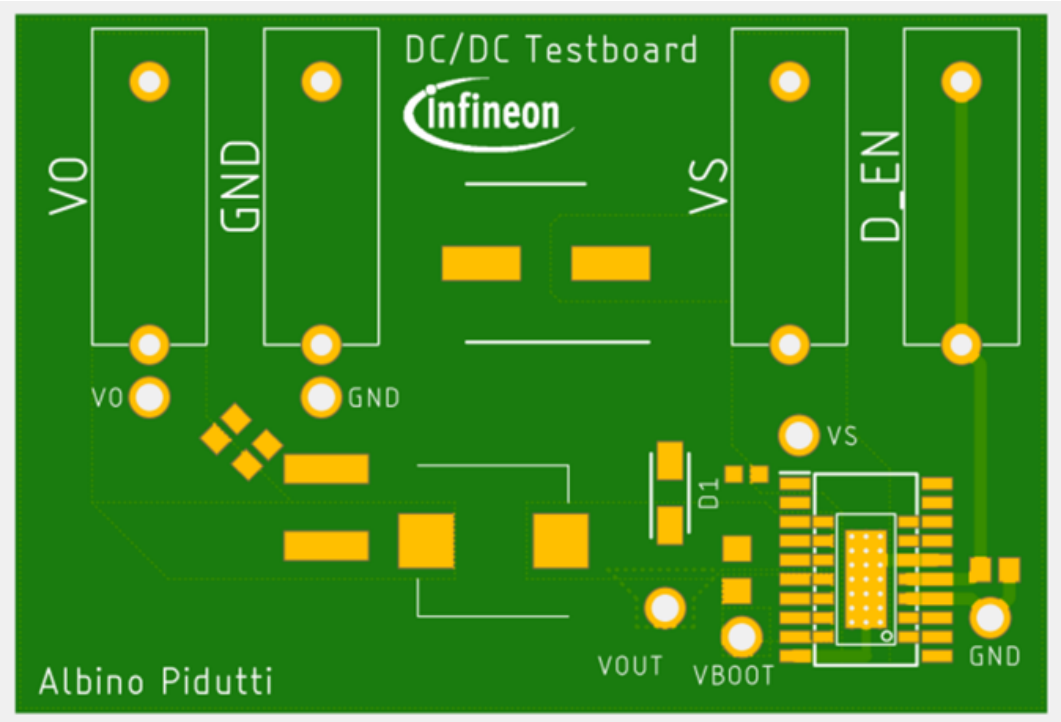


Figure 8.7: PCB - Test Board

Appendix

Considerations About Bandgap

Probably the first Bandgap structure widely used in Integrated Circuits was the one based on the Brokaw cell (Figure A.1) [42].

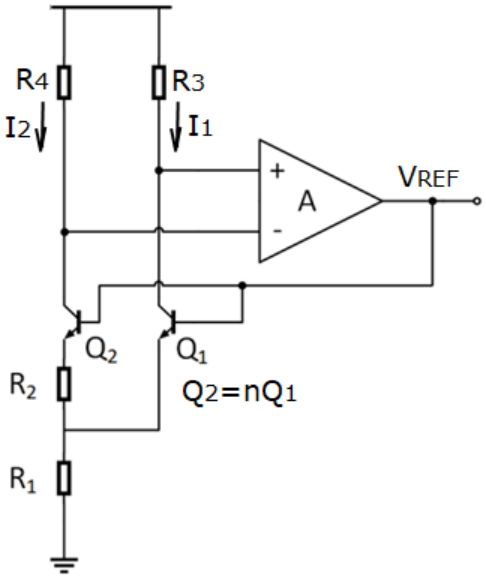


Figure A.1: Brokaw Cell

The amplifier forces the equality of the voltage drops on the resistance R_3 and R_4, so that the two branches have the same current I_1=I_2=I . Being $Q_2 = n\,Q_1$ and having the same base voltage between the emitters Q_1 and Q_2 there will be a voltage equal to

$$\Delta V_{BE} = V_T\, ln(n) \qquad \text{for n=8 at 25°C} \qquad \Delta V_{BE} = 52mV \tag{A.1}$$

$$\text{from the Figure A.1} \qquad 2R_1 I + R_2 I + V_{BE} = V_{REF} \tag{A.2}$$

$$= (2R_1/R_2\, + 1)\, \Delta V_{BE} + V_{BE} = V_{REF} \tag{A.3}$$

The voltage V_{REF} is a combination of V_{BE} and ΔV_{BE} The similarity with the formula obtained in chapter 4 and reiterated here is evident.

$$(V_{BE} + \Delta V_{BE}/K) * R_4/R_1 = V_{ref} \tag{A.4}$$

Both circuits by suitably mixing the PTAT and CTAT part obtain a constant temperature reference.

The Brokaw cell has two equilibrium points, one unstable at the origin and one table at the working point. So just move from the origin to automatically end up on the stable equilibrium point (Figure A.2).

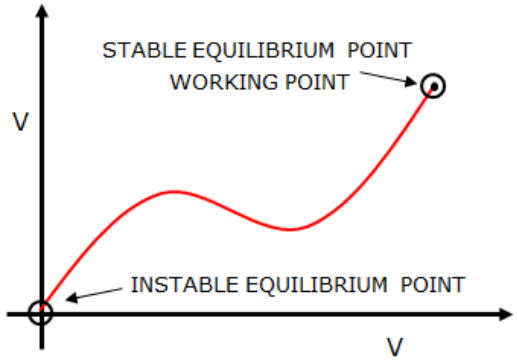


Figure A.2: The Two Equilibrium Points in Brokaw Cell

Often in integrated circuits the Bandgap structure shown in Figure A.3 is preferred. The bandgap based on the Brokaw cell having a telescopic structure requires a power supply voltage higher than a parallel structure like the circuit of Figure A.3.

As shown in chapter 4, in the parallel topologies the points on the line $(0 - Vt_{D2})$ are points of stable equilibrium. Often the starter is a timed circuit activated at the IC start-up that brings the bandgap beyond the operating point and then naturally returns to it.

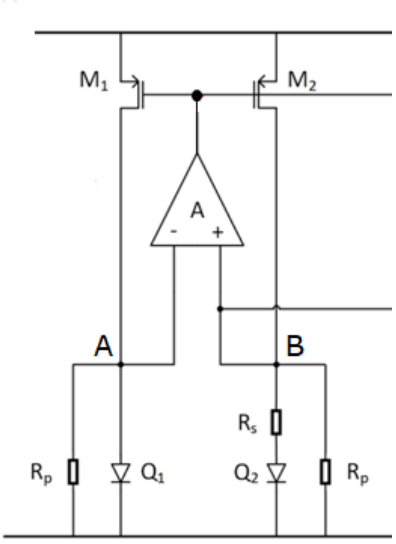


Figure A.3: Often Used Bandgap Structure

Frequently the parallel structures make use of OPAMP to balance points A and

B. This implies the use of a compensation network and relative stability study.

In this work we propose the Bandgap shown in the Chapter 4 "Auxiliary Blocks - Bandgap" which for convenience we replicate in Figure A.4.

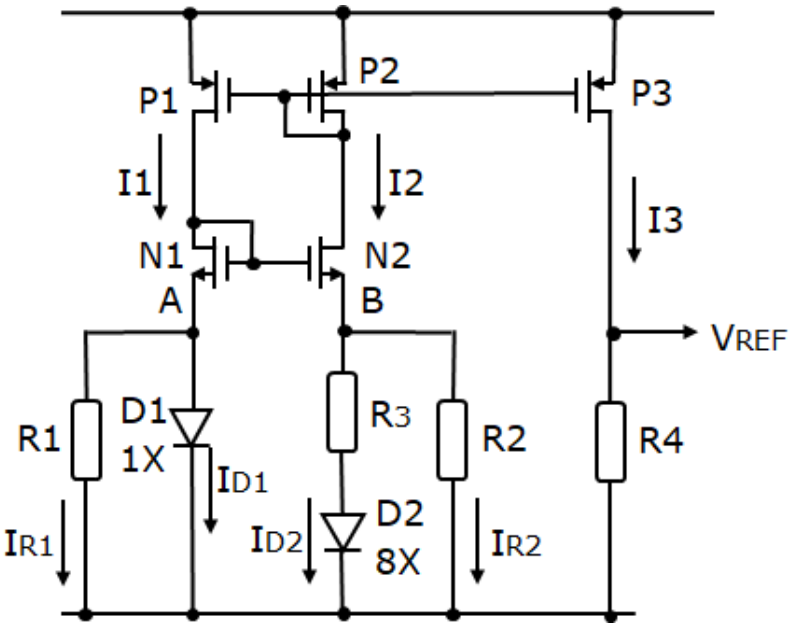


Figure A.4: Buck Converter Bandgap

This is also a parallel topology but does not use OPAMPs to define points A and B, being this topology intrinsically stable as demonstrated below.

To calculate the stability we need to open the loop composed of N2-P2-P1-N1 as shown in Figure A.5. Let's call $Z_1 = R_1 \parallel D_1$ e $Z_2 = R_2 \parallel (R_3 + D_2)$. Considering the DMOS simplified equivalent circuit we write

$$V_2 = V_{i2} + V_{z2} = \frac{I_2}{G_{m2}} + I_2 Z_2 = I_2 \left(\frac{1}{G_{m2}} + Z_2\right) \tag{A.5}$$

$$I_2 = \frac{V_2}{1/G_{m2} + Z_2} \tag{A.6}$$

with the same procedure for the left half circuit we obtain

$$I_1 = \frac{V_1}{1/G_{m1} + Z_1} \tag{A.7}$$

and being $I_1 = I_2$

$$\frac{V_1}{1/G_{m1} + Z_1} = \frac{V_2}{1/G_{m2} + Z_2} \qquad \text{from which} \qquad \frac{V_2}{V_1} = \frac{1/G_{m1} + Z_1}{1/G_{m2} + Z_2} \tag{A.8}$$

$$\text{because} \qquad G_{m1} = G_{m2} = G_m \qquad R_{D1} = R_{D2} = I_C/V_T = R_D, \qquad R_1 = R_2 = R \tag{A.9}$$

$$Z_1 = R \parallel R_D \qquad \text{and} \qquad Z_2 = R \parallel (R_D + R_3) \tag{A.10}$$

$$\text{at the end results} \qquad \frac{V_2}{V_1} = \frac{1/G_m + R \parallel R_D}{1/G_m + R \parallel (R_D + R3)} < 1 \tag{A.11}$$

Since the open loop gain is always <1 this topology is inherently stable.

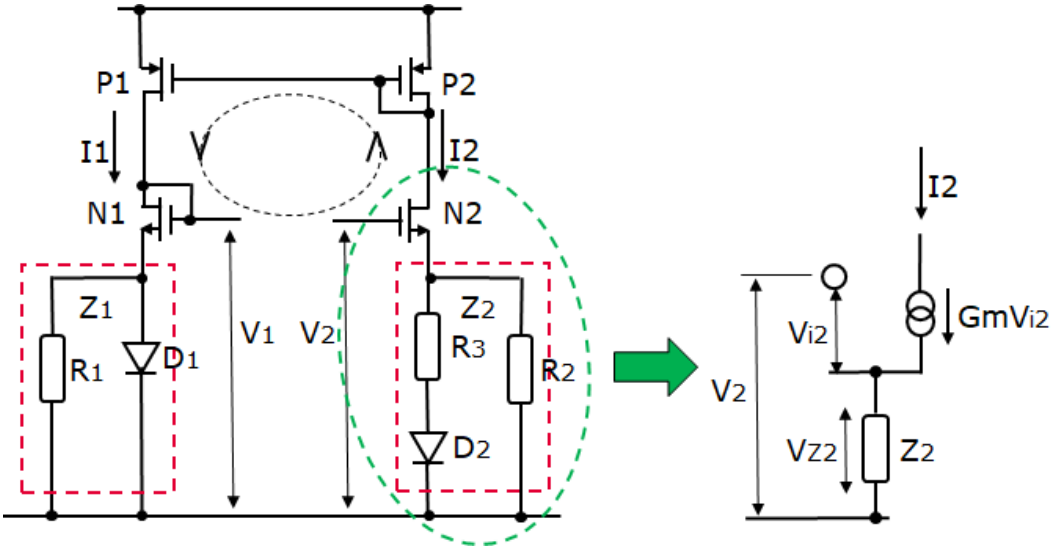


Figure A.5: Bandgap Open Loop and Equivalent Circuit of N2 Plus Z1

The bandgap data we use in the Buck Converter are:

$$G_m = 255\mu\,, I_D = 8.2\mu\,, R_D = 25mV/8.2\mu = 3.05k\,, R_1 = 60K\,, R_3 = 6.5K \tag{A.12}$$

substituting these values in the formula we have $A = V_0/V_1 = 0.56$.
whose logarithm is

$$A = 20\log_{10} 0.56 = -5.03\,dB \tag{A.13}$$

In good agreement with the Bode simulation from which results $A = -5.42\,dB$ (Figure A.6)

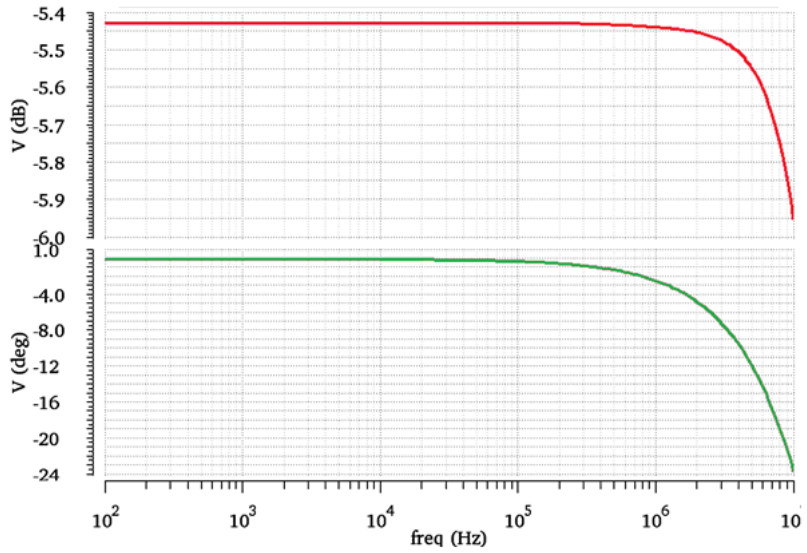


Figure A.6: Bandgap Bode Diagram

In the fourth chapter the start-up circuit of the bandgap has already been shown and for convenience is repeated in Figure A.7.

The comparator has an intrinsic offset of approximately 25 mV. Assuming that at the start-up no current flows through resistor R3, due to the offset the comparator output is high and enables the current Ioffset. The effect of this current is to shift the I-V curve of D2 up (Figure A.8) eliminating the infinite equilibrium points of the segmant $(0 - Vt_{D2})$, and forcing the circuit to move towards the only remaining equilibrium point. When the voltage drop across resistor R3 equals the offset, the comparator switches and removes the offset.

This starter does not need a trigger signal and intervenes immediately whenever the Bandgap moves from the point of equilibrium. The potential risk that a possible disturbance move the operation from the desired working point to a point on the segment $(0 - Vt_{D2})$ and from there it doesn't move is avoided.

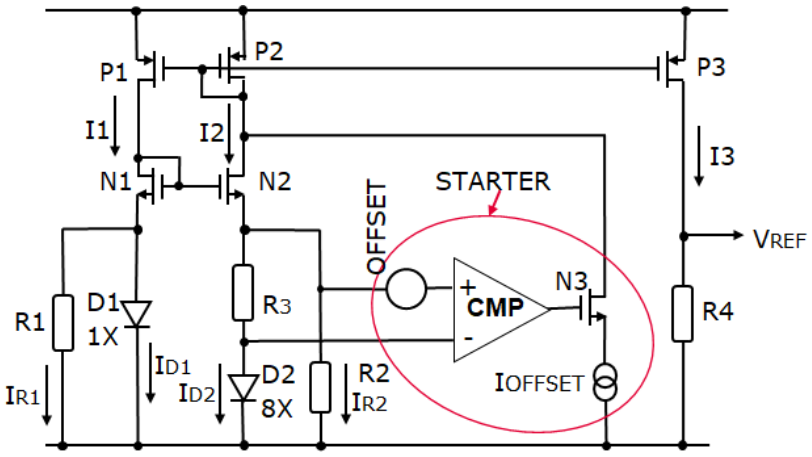


Figure A.7: Bandgap Circuit Plus Starter Circuit

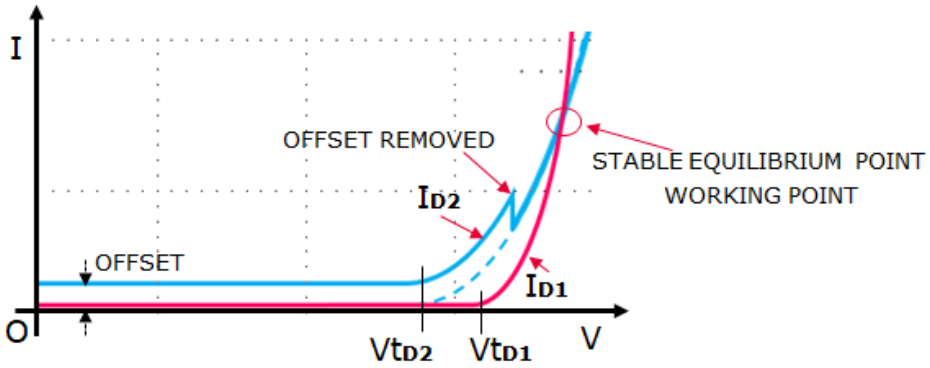


Figure A.8: Bandgap - Effect of the Starter

DMOS as Power Switch

The DMOS is frequently used as a switch, consequently it works between the ON and OFF states. A characteristic parameter is the RdsON, ie the resistance between Drain and Source when completely ON. Other fundamental parameters are the gate source capacitor C_{GS} and the gate drain capacitor C_{Gd}, both necessary for a correct Driver design . The capacitor C_{DS} is the capacitor between Drain and Source.

The Figure A.9 shows the cross section of a vertical DMOS with n substrate. The current path starts from the lead frame, crosses the substrate n^+, the Body p and is collected by the Sources. The substrate represents the preponderant part of the path and is heavily doped to reduce the series resistance.

In (Figure A.10) is shown the DMOS equivalent circuit.

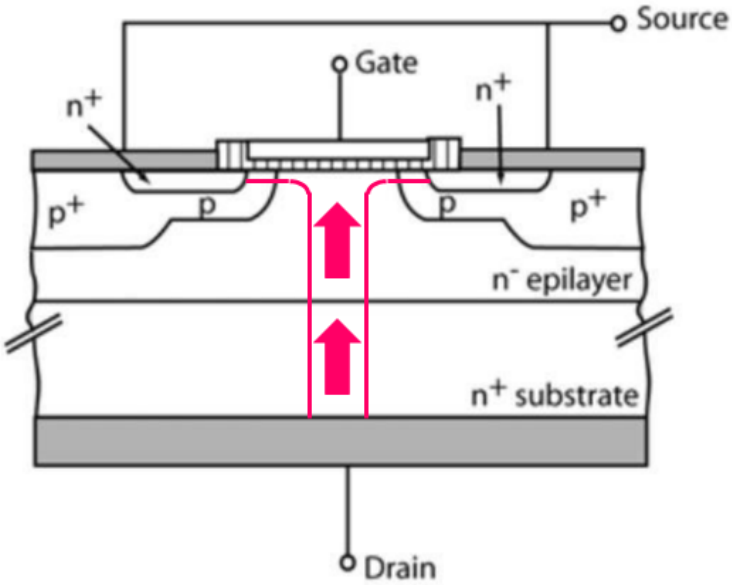


Figure A.9: Power DMOS Cross Section

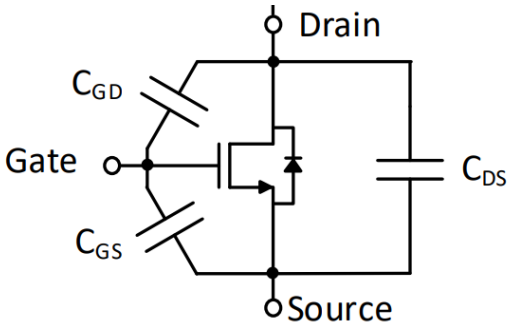


Figure A.10: DMOS - Equivalent Circuit

It is important to consider the DMOS when switching. We explain it in a simplified way using Figure A.11. To the equivalent circuit of the DMOS a resistive load is connected to the source and the gate is powered by the current generator Io.

In the time interval t_0-t_1 the current Io loads the capacitance C_{GS}. Because the value of the capacitance C_{GD} depends on the voltage across it and in this time being the voltage across it practically equal to V_{CC} its value is negligible in the parallel C_{GS} C_{GD}.

At the instant t_1 the Gate reaches the threshold voltage V_t, the DMOS begins to conduct and the Source grows with respect to GND. However, this is only possible if the capacity C_{GD} is charged thanks to the current Io. Consequently in the interval t_1-t_2 Io stops charging C_{GS} which will consequently keep a constant value and Io will flow only in C_{GD}. The flat part is called Miller Plateau.

When the Source is close to Vcc, the voltage across C_{GD} is close to zero, the Miller Plateau ends and the current Io restart flowing in the parallel C_{GS} C_{GD}. Now C_{GD} cannot be neglected since the voltage across it is relatively small and its capacitive value is relevant. The voltage on Gate reaches its maximum value in t_3 with a much lower slope than in the t_0-t_1 segment.

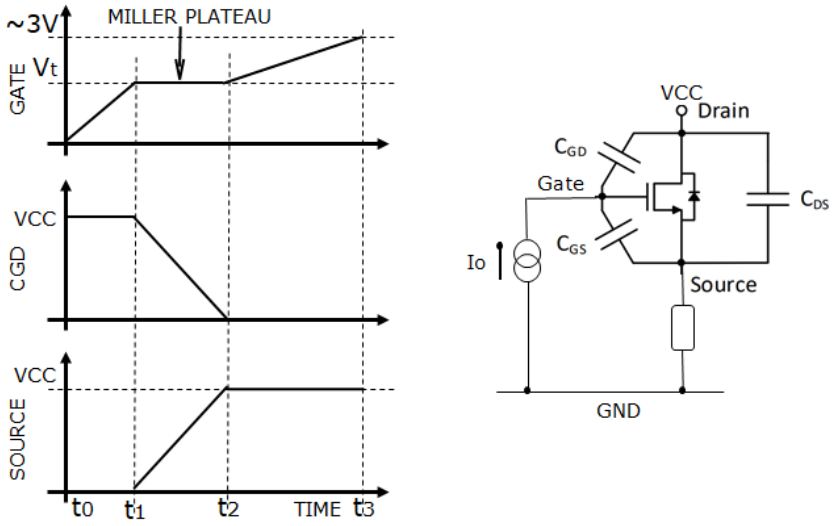


Figure A.11: DMOS Switching Behavior

During the Miller plateau the Source voltage completes the $0 - V_{CC}$ transaction.

The time required, called Switching Time, is an index of the system speed. It is possible to estimate as

$$d_t = (C_{GD}/I_0)d_V \qquad \text{integrating} \qquad t_2 - t_1 = 1/I_0 \int_0^{V_{CC}} C_{GD}\, dV \tag{A.14}$$

Figure A.12 shows the Miller Plateau simulation of the Buck Converter DMOS

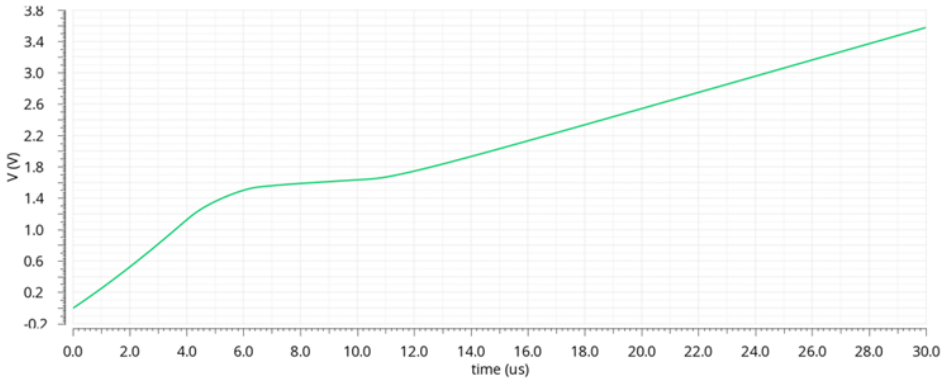


Figure A.12: $80m\Omega$ DMOS - Miller Plateau Simulation

Patent Proposals

Some innovative ideas were developed during the PhD work, which led to four patent applications:

- **Patent proposal 1**, High Speed Driver for High Frequency DC-DC Converter - PENDING
- **Patent proposal 2**, Intelligent Semiconductor Switch with Integrated Current Measurement Function - PENDING
- **Patent proposal 3**, A Method for Detecting Degradations of DMOS and its Driver in Real Time - PENDING
- **Patent proposal 4**, Reduce Eddy Currents Method for On-Chip Coils - pending claims discussion with the European Patent Office

HIGH SPEED DRIVER FOR HIGH FREQUENCY DCDC CONVERTER

[0001] This application claims the benefit of German Patent Application No. 102021116029.4, filed on June 21, 2021, which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] This disclosure relates to the field of gate driver circuits. Embodiments described herein particularly relate to driver circuits used to drive the gate of a MOS transistor which may be used, for example, in a switching converter.

BACKGROUND

[0003] A large variety of gate driver circuits for Metal-Oxide-Semiconductor (MOS) transistors is known. Generally, gate driver circuits (or short gate drivers) can be optimized with regard to a specific desired switching behavior. In some applications a short switching time (i.e., a fast switching) is an important design goal for gate drivers.

[0004] In switching power supply applications such as, for example, in DC/DC switching converters a higher switching frequency allows to reduce the size of the reactive circuit components (capacitors and inductors), which may be desirable for various reasons (size, costs, etc.). A high switching frequency requires a correspondingly high-speed switching of the power transistors used in the switching converters, wherein the gate driver is crucial for the achievable switching speed. This disclosure deals with improved driver circuits that allow a fast switching of MOS transistors.

SUMMARY

[0005] A gate driver circuit is described herein. In accordance with one embodiment the circuit includes a pulse generator that is configured to receive an input signal and to generate a pulse signal in response to a switch-on command included in the input signal. The pulse signal

has a pulse with a pulse length that is dependent on a level of a pulse control signal. The circuit further includes a sampling circuit that is configured to sample an output voltage subsequent to the pulse and to store a respective sampled value and a controller that is configured to receive the sampled value of the output voltage and a reference voltage and to update the level of the pulse control signal based on the sampled value and the reference voltage. A driver circuit is configured to generate the output voltage based on the pulse signal.

[0006] Another embodiment relates to a method for driving a transistor gate. Accordingly, the method includes generating a pulse signal in response to a switch-on command included in an input signal, wherein the pulse signal has a pulse with a pulse length that is dependent on a level of a pulse control signal. The method further includes generating an output voltage based on the pulse signal using a driver circuit, sampling the output voltage subsequent to the pulse and storing a respective sampled value. The level of the pulse control signal us updated based on the sampled value and a reference voltage value.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] In the following detailed description, reference is made to the accompanying drawings. The drawings form a part of the description and, for the purpose of illustration, show examples of how the invention may be used and implemented. It is to be understood that the features of the various embodiments described herein may be combined with each other, unless specifically noted otherwise.

[0008] Figure 1 illustrates one common implementation of a gate driver circuit for driving a high-side transistor;

[0009] Figure 2(a) illustrates an equivalent circuit of the driver circuit and a timing diagram, Figure 2(b) illustrates the charging process of the transistor gate;

[0010] Figure 3 illustrates, in a schematic timing diagram, the charging process of a transistor gate when using a driver circuit according to the embodiments described herein;

[0011] Figure 4 illustrates one approach that might be obvious but that will not work in practical applications;

[0012] Figure 5 illustrates timing diagrams illustrating, by way of example, the operation principle of the embodiments described herein;

[0013] Figure 6 illustrates one example implementation of a gate driver circuit in accordance with one embodiment;

[0014] Figure 7 illustrates one exemplary implementation of the pulse generator used in the example of Fig. 6 in more detail; and

[0015] Figure 8 illustrates one exemplary application of the gate driver circuit of Fig. 6.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0016] Figure 1 illustrates one common implementation of a gate driver circuit for driving a high-side transistor. In the present example, the high-side transistor is a power transistor (e.g., a DMOS transistor) denoted as M_D. The diode D_R coupled in parallel to the transistors drain-source current path represents the transistor's intrinsic body diode, which is always present in most semiconductor fabrication technologies. The gate driver circuit 11 includes a series of CMOS inverter circuits, wherein the input signal IN, applied to the input of the driver circuit is a logic signal, which is basically forwarded to the power transistor's gate electrode. When the power transistor M_D is switched on, the source voltage V_S (at circuit node N_S) will be close to the drain voltage V_B of the transistor M_D and, therefore, the supply voltage V_{BOOT} for the gate driver 11 needs to be shifted to a voltage level higher than the drain voltage V_B applied to the power transistor M_D. This is usually accomplished by a so-called boot-strap circuit.

[0017] In the present example the boot-strap circuit 10 includes a series circuit composed of rectifier diode D_B and capacitor C_B, wherein the series circuit is coupled between a circuit node providing the supply voltage V_B and circuit node N_S. The capacitor C_B is charged while the transistor M_D is off and the circuit node N_S is pulled to lower voltage levels (e.g., close to ground). The capacitor C_B is charged up to a voltage V_{BOOT} which is limited by the Zener voltage of Zener diode D_Z coupled in parallel to the capacitor C_B. When the transistor M_D is switched on, the circuit node N_S is pulled close to the supply voltage V_S and the rectifier diode D_B becomes reverse biased (and blocking) which the capacitor C_B still can provide the supply voltage V_{BOOT} to the gate driver 11. Various implementations of boot-strap circuits are known and are thus not further discussed herein.

[0018] Figure 2(a) illustrates an equivalent circuit of the gate driver circuit and the transistor gate connected thereto. The transistor gate is represented by the capacitance C_{EQ}, which is basically determined by the gate capacitance of the power transistor M_D. The resistor R_{EQ} coupled in series to the capacitor C_{EQ} represents the effective output resistance of the gate driver circuit 11, and the voltage source represents the voltage V_{BOOT} provided by the capacitor C_B shown in Figure 1. For further discussion, we assume the capacitor C_{EQ} is discharged. When the switch SW is closed, the voltage V_{BOOT} is applied to the series circuit of resistor R_{EQ} and capacitor C_{EQ} causing the capacitor C_{EQ} to be charged. Figure 2(b), illustrates a timing diagram of the voltage V_G across the capacitor C_{EQ}, which corresponds to the gate-source voltage in the circuit of Figure 1. The equivalent circuit of Figure 2(a) is a first-order low pass having a time constant of $\tau=R_{QE}C_{EQ}$. It takes usually a time of 4τ to 5τ to charge the gate capacitance C_{EQ} to a level V_{Go} (approximately 3V in the current example) that is sufficiently high to drive the transistor into its low-ohmic state (on-resistance R_{ON} of transistor M_D). The level V_{Go} basically corresponds to the bootstrap voltage V_{BOOT}. The embodiments described herein aim at shortening the charging time to significantly shorter time spans.

[0019] The timing diagram in Figure 3 illustrates how the charging curve if Figure 2(b) changes if the bootstrap voltage V_{BOOT} is increased from V_{G0} to V_{G1}, which is approximately 8 V in the present example. Due to the higher bootstrap voltage V_{BOOT}, the gate voltage V_G reaches the target level of V_{G0} in significantly less time. In the depicted example, the level V_{G0} is reached in a charging time of T_{CH} which can be significantly lower than the time constant τ. The problem with increasing the bootstrap voltage to, e.g., 8 V is that the charging process must be reliably interrupted as soon as the target level of 3V is reached. Otherwise the gate oxide of the power transistor may be destroyed.

[0020] One straight-forward approach to limit the gate voltage to a target voltage V_{G0} significantly lower than the bootstrap voltage V_{BOOT} is illustrated in Figure 4. The circuit of Figure 4 basically corresponds to the circuit of Figure 1 with an additional comparator 12, which is configured to compare the gate voltage V_G present at the transistor's gate electrode with the desired target voltage V_{G0} (wherein $V_{G0} < V_{BOOT}$) and detect the gate voltage V_G reaching the target level V_{G0}. If this is the case, the comparator triggers disables the gate driver 11 thus stopping the charging process of the gate capacitance. Unfortunately, in practice, the approach shown in Figure 4 will not work for most applications because of the comparator delay and the propagation delay within the gate driver 11. During this delay time, the gate voltage will rise to levels above the target voltage which can damage the gate oxide of the power transistor M_D.

[0021] The embodiments described below use an approach different from the approach illustrated in Figure 4 to reliably limit the gate voltage V_G to the desired target voltage V_{G0} while using significantly higher bootstrap voltages (e.g., 8 V or higher). The concept is first explained using the timing diagrams of Figure 5. The first diagram (top) of Figure 5 illustrates the control signal IN, which can be regarded as the input signal of the gate driver circuit. The signal IN is a logic signal indicating (e.g., by a high signal level for a time interval T_{ON}) the desired switching

state of the power transistor M_D. The rising edge of the signal IN triggers the process of charging the gate capacitance of the power transistor M_D.

[0022] However, the gate capacitance is not charged for the whole time interval T_{ON} but only for a short time interval T_{CH}, which is indicated by a high level of signal IN' (see third diagram (from the top) of Figure 5). The time intervals T_{ON} and T_{CH} begin at the same time instant, wherein T_{CH} is only a fraction of T_{ON}. As can be seen in the second diagram of Figure 5, the gate voltage V_G rises during the time interval T_{CH} (as the charge stored in the gate capacitor increases), whereas the gate voltage V_G remains basically constant after the time interval T_{CH} during the remaining part of the time interval T_{ON}. At the end of the time interval T_{ON} (on-time) the gate capacitor is discharged (e.g., by connecting the gate electrode to the source electrode of the power transistor by a low-ohmic current path and, consequently, the transistor is switched off.

[0023] The time T_{CH} is adjustable and is initially set to a default value small enough to ensure that the gate voltage V_G will not exceed the target value V_{Go} even if the combination of the actual parameters V_{BOOT}, R_{EQ} and C_{EQ} (cf. Figures 2(a) and 2(b)), which may vary due to tolerances, represent a worst case (bootstrap voltage at the higher end and the time constant $R_{EQ}C_{EQ}$ at the lower end). At the end of the charging time T_{CH} the actual voltage level at the gate electrode is sampled, e.g., using a sample and hold circuit. The sampling time instant is determined by the rising edge of the signal SMP, which may immediately follow after the falling edge of the signal IN' (see fourth (bottom) diagram of Figure 5). The time T_{CH} can then be adjusted based on the sampled gate voltage level. If the sampled value is lower than the target value V_{Go}, then the time T_{CH} is increased by a specific amount so that, in the next switching cycle, the gate is charged to a somewhat higher level as in the preceding cycle. Conversely, if the sampled value is higher than the target value V_{Go}, then the time T_{CH} is decreased. If the sampled value equals the target level V_{Go}, then the time T_{CH} may remain unchanged.

[0024] On exemplary implementation of the concept explained above is illustrated in Figure 6 (gate control circuit 100). Figure 6 shows the power MOS transistor M_D whose drain-source current path is coupled between the circuit nodes N_D (connected to drain) and N_S (connected to source). The supply voltage V_B is applied to the node N_D. An impedance (load, not shown) may be connected between node N_S and a reference potential (e.g., ground). Similar to Figure 1, the gate driver 11 is supplied by the bootstrap voltage V_{BOOT}, wherein the floating potential at node N_S is the reference potential for the gate driver circuit 11. Different from the circuit of Figure 1, the pulse signal IN' is supplied to the input of the gate driver 11, which produces a corresponding output signal. As shown in Figure 5, the signal IN includes, in each switching cycle, a short pulse with an adjustable pulse length T_{CH}. According to the example of Figure 6, a pulse generator 20 is configured to receive the input signal IN (cf., Figure 5) and to generate the pulse signal IN' in response to a rising edge if the input signal IN, wherein the pulse length T_{CH} is dependent on a level of a pulse control signal S_{CH}. It is noted that, in the present example, the rising edge of the input signal IN serves as a switch-on command, which initiates the process of switching-on the transistor M_D. Other types of switch-on commands (e.g., a falling edge, a specific digital word received via a serial communication link, etc.) may be used dependent on the actual application.

[0025] The example of Figure 6 further includes a sampling circuit 21 that is configured to sample the gate voltage V_G generated by the gate driver 11 subsequent to the pulse (i.e., after the time interval T_{CH}, see Figure 5) and to store a respective sampled value V_{SMP}. A controller 22 is configured to receive the sampled value V_{SMP} and a reference voltage V_{REF} (that represents the desired target gate voltage) and to update the level of the pulse control signal S_{CH} based on the sampled value V_{SMP} and the reference voltage V_{REF}. In the depicted embodiment, the controller is basically a difference amplifier which amplifies the difference V_{REF}-V_{SMP}. This means basically a P-controller. However, other types of controllers may be used in other embodiments. If, in one switching cycle, the gate voltage V_G – and thus the sampled value V_{SMP} – is lower than the

reference value V_{REF}, then the pulse control signal S_{CH} will be adjusted to increase the time T_{CH} in the next switching cycle, which will result in a higher gate voltage V_G. Similarly, if the gate voltage V_G – and thus the sampled value V_{SMP} – is higher than the reference value V_{REF}, then the pulse control signal S_{CH} will be adjusted to decrease the time T_{CH} in the next switching cycle, which will result in a lower gate voltage V_G. In steady state with continuously repeating switching cycles, the gate voltage V_G will approximately be equal to the reference voltage value V_{REF}.

[0026] Before being updated for the first time, the level of the pulse control signal S_{CH} is at a predetermined initial level. The initial level may be used to generate the first pulse in response to the first switch-on command after a startup (power-on) of the circuit.

[0027] Figure 7 illustrates one example implementation of the pulse generator circuit 20 in more detail. In the depicted example, it is assumed that the controller 22 has a current output like, for example, a transconductance amplifier. The controller 22 sinks a current i_{CH} at its output, wherein the current i_{CH} depends on the difference V_{REF}-V_{SMP}. The higher the difference V_{REF}-V_{SMP}, the higher the current i_{CH} at the output of controller 22. The current i_{CH} is “mirrored” to another current path by a first current mirror CM_1. That is the current i_{CH} passes though the input path of current mirror CM_1 that is coupled to the output of the controller 22, wherein the output current path of current mirror CM_1 provides the mirrored current, which may be equal to the current in the input path. A current sink Q_1 is connected to the output of the current mirror CM_1 and configured to sink a constant DC current i_{DC}. Further, the input path of a second current mirror CM_2 is connected to the output of the first current mirror CM_1. Following Kirchhoff's current law, the current i_o passing through the input path of the second current mirror CM_2 must equal i_{DC} minus i_{CH} (i_o=i_{DC}-i_{CH}). The input current i_o of current mirror CM_2 is mirrored to the output of the current mirror CM_2.

[0028] An inverter INV_2 is supplied by the output current i_o of the second current mirror CM_2 and accordingly, the current $i_o=i_{DC}-i_{CH}$ is the maximum output current of the inverter INV_2 when the inverter output is at a high level. Another inverter INV_1 is connected ahead of the inverter INV_2. Accordingly, the inverter chain INV_1 and INV_2 does not change the logic state of the input signal IN supplied to the inverter INV_1 in a steady state, but the output current of the inverter chain is limited to the current level i_o. A capacitor C_{CH} is coupled to the output of inverter INV_2. Accordingly, upon with a rising edge in input signal IN the capacitor C_{CH} is charged with the current i_o. The resulting capacitor voltage V_{CH} will ramp up until it reaches approximately the supply voltage of the inverter INV_2 (approximately V_{BOOT} minus the voltage drop in current mirror CM_2).

[0029] The capacitor voltage V_{CH} (voltage ramp) is compared with a reference voltage V_X by comparator CMP, which is configured to signal (e.g., by a low level at its output) that the capacitor voltage V_{CH} has exceeded the reference voltage V_X. The comparator output voltage is used to blank the input voltage IN using an AND gate which receives, as input signals, the input signal IN and the comparator output signal. The output signal of the AND gate is denoted as IN' (see also Figure 5). The signal IN' follows the input signal IN before it is blanked by the comparator output signal a time T_{CH} after the rising edge of the input signal. The time T_{CH} depends in the current i_o and the capacitance C_{CH}, wherein the current i_o depends on the controller output current i_{CH}. If the controller output current i_{CH} increases, the current i_o will decrease and, consequently, the capacitor C_{CH} is charged more slowly and the time T_{CH} increases. The time T_{CH} is the pulse length of the pulse in signal IN' triggered by a (rising edge in input signal IN, see Figure 5). The inverted comparator output signal (inverter INV_3) is provided as output signal SMP that triggers the sampling circuit 21 as explained above. Accordingly, the pulse length T_{CH} is determined by the controller output current i_{CH} and thus by the sampled voltage value V_{SMP}, wherein at the end of the pulse a new value is samples.

[0030] It is noted that Figure 6 illustrates a concept for charging the gate capacitance in order to switch the power transistor M_D on. The circuitry for discharging the gate capacitance in order to switch the power transistor M_D off is not shown in order to keep the drawings simple. However, known concepts may be used to switch off the power transistor M_D such as, for example, an electronic switch (e.g., another transistor) configured to electrically connect gate and source electrode of the power transistor M_D in response to a falling edge of the input signal IN. Of course, gate and source electrode of power transistor M_D need to be disconnected at or before the next rising edge of the input signal IN in order to allow another switch-on.

[0031] Figure 8 illustrates one exemplary application of the gate control circuit 100 of Figures 6 and 7. In essence, Figure 8 illustrates a buck converter circuit. The gate control circuit 100 and the high-side power transistor 100 have already explained with reference to Figure 4. An inductor L is connected between the source terminal of power transistor M_D and an output circuit node, at which the output voltage V_{OUT} is provided. A capacitor C_{OUT} is connected between the output node and ground GND. Further, a free-wheeling diode D_F is connected between the source terminal of transistor M_D and ground GND. A low side DMOS transistor may be used instead of the diode D_F. Embodiments of the gate control circuit 100 described herein allow a faster switching and thus a reduction of the inductance and, consequently, a reduction of the inductor size.

[0032] Although the invention has been illustrated and described with respect to one or more implementations, alterations and/or modifications may be made to the illustrated examples without departing from the spirit and scope of the appended claims. For example, inverted logic levels can be used, and logic operations such as AND, NAND, OR, etc. can generally be replaced by different logic operations using commonly known concepts. In particular regard to the various functions performed by the above described components or structures (units, assemblies, devices, circuits, systems, etc.), the terms (including a reference to

a “means”) used to describe such components are intended to correspond – unless otherwise indicated – to any component or structure, which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure, which performs the function in the herein illustrated exemplary implementations of the invention.

WHAT IS CLAIMED IS:

1. A circuit comprising:

a pulse generator configured to receive an input signal and to generate a pulse signal in response to a switch-on command included in the input signal, the pulse signal having a pulse with a pulse length that is dependent on a level of a pulse control signal;

a sampling circuit configured to sample an output voltage subsequent to the pulse and to store a respective sampled value;

a controller configured to receive the sampled value of the output voltage and a reference voltage and to update the level of the pulse control signal based on the sampled value and the reference voltage; and

a driver circuit configured to generate the output voltage based on the pulse signal.

2. The circuit of claim 1,

wherein the pulse control signal has a predetermined initial level before being updated for a first time.

3. The circuit of claim 2,

wherein the initial level is set to such a level, that a resulting pulse length is short enough that the generated output voltage is below a predefined maximum voltage value.

4. The circuit of claim 1,

wherein the driver circuit operably receives a supply voltage that is higher than a predetermined maximum voltage value.

5. The circuit of any of claim 1,

wherein the driver circuit includes an output resistor.

6. The circuit of claim 1,

wherein the pulse generator uses the updated level when generating a subsequent pulse in response to a subsequent switch-on command included in the input signal.

7. The circuit of claim 1,

wherein the sampling circuit is configured to store the sampled value in a first capacitor, the sampled value being represented by a respective capacitor voltage.

8. The circuit of claim 1,

wherein the controller comprises a differential amplifier configured to output, as pulse control signal, a signal representing a difference between the sampled value and the reference voltage.

9. The circuit of claim 1,

wherein the pulse control signal is a control current, and

wherein the pulse generator is configured to generate a ramp signal with a steepness depending on the control current, the pulse length being determined by a time at which a level of the ramp signal reaches a reference value.

10. A switching converter comprising:

a power transistor having a gate electrode and a load terminal coupled to an inductor,

wherein the gate electrode is coupled to the circuit of claim 1 so that the output voltage of the circuit is applied to the gate electrode.

11. A method comprising:

generating a pulse signal in response to a switch-on command included in an input signal, the pulse signal having a pulse with a pulse length that is dependent on a level of a pulse control signal;

generating an output voltage based on the pulse signal [using a driver circuit (11)];

sampling the output voltage subsequent to the pulse and storing a respective sampled value; and

updating the level of the pulse control signal based on the sampled value and a reference voltage.

12. The method of claim 11, wherein generating the pulse signal comprises:

generating a ramp signal with a steepness depending on the pulse control signal, the pulse length being determined by a time at which a level of the ramp signal reaches a reference value.

ABSTRACT

HIGH SPEED DRIVER FOR HIGH FREQUENCY DCDC CONVERTER

A gate driver circuit includes a pulse generator that receives an input signal and generates a pulse signal in response to a switch-on command included in the input signal. The pulse signal has a pulse with a pulse length that is dependent on a level of a pulse control signal. The circuit further includes a sampling circuit that samples an output voltage subsequent to the pulse and stores a respective sampled value, and a controller that receives the sampled value of the output voltage and a reference voltage and updates the level of the pulse control signal based on the sampled value and the reference voltage. A driver circuit generates the output voltage based on the pulse signal.

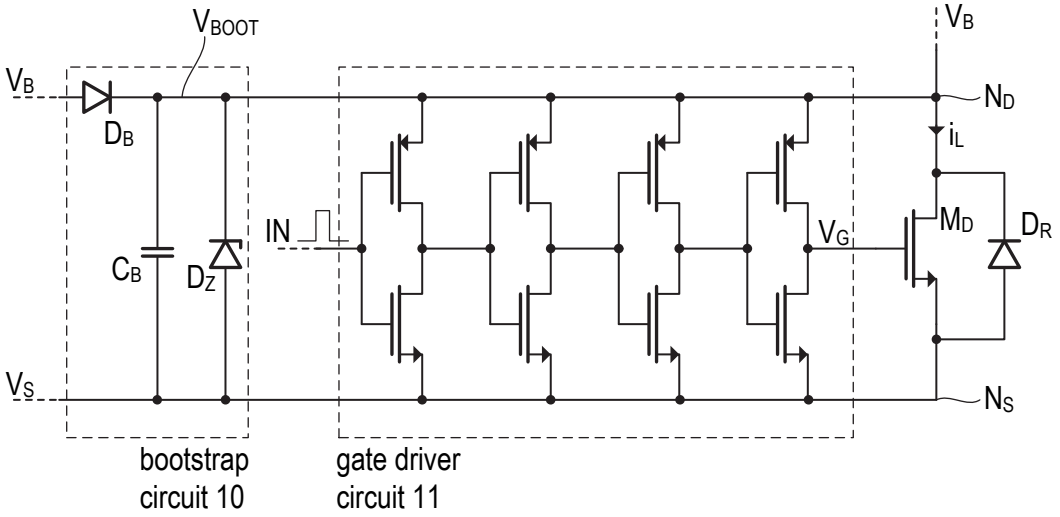


Fig. 1

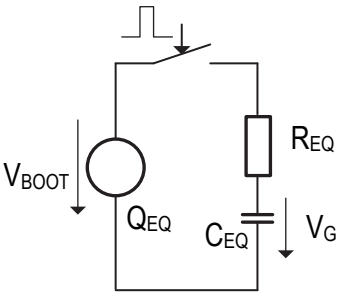


Fig. 2(a)

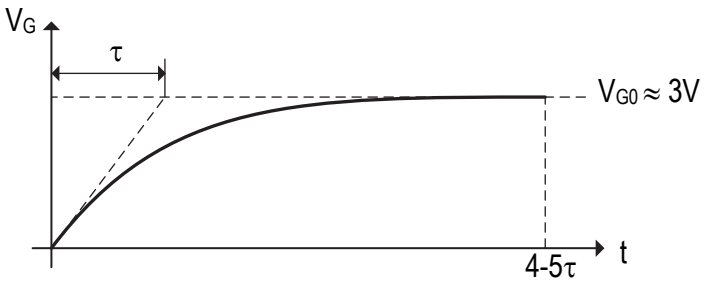


Fig. 2(b)

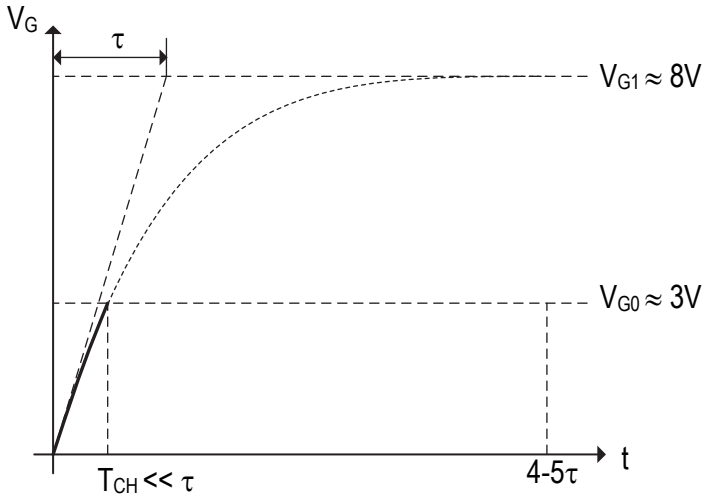


Fig. 3

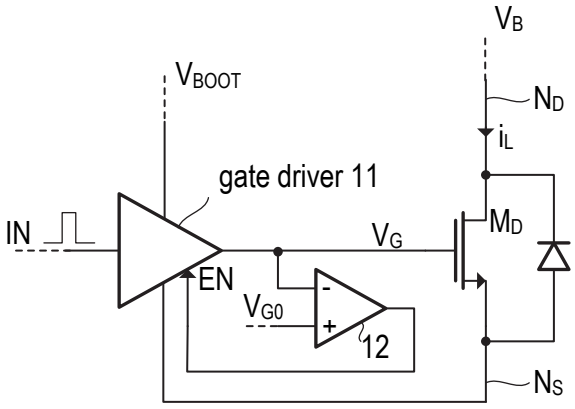


Fig. 4 (will not work due to comparator delay)

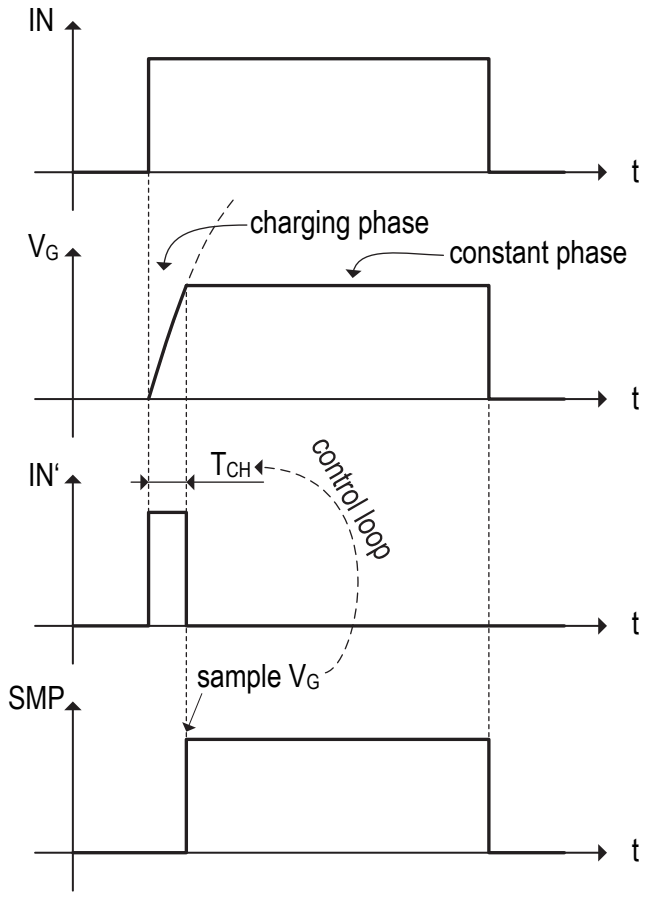


Fig. 5

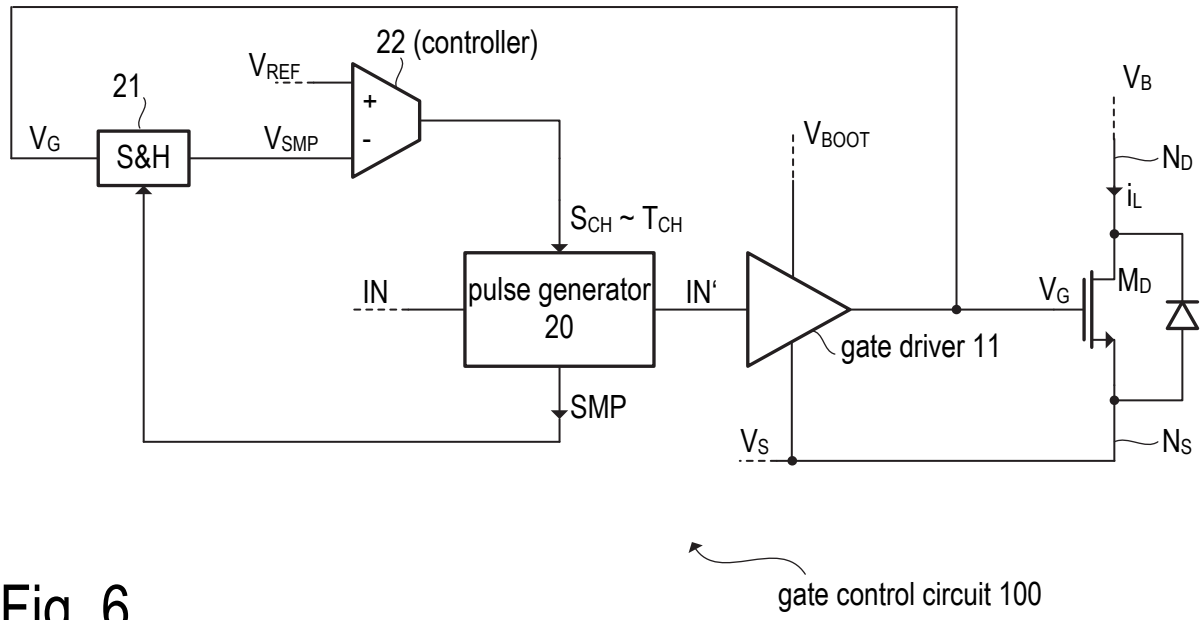

22 (controller)
V_{REF}
21
V_G
S&H
V_{SMP}
V_B
V_{BOOT}
N_D
i_L
S_{CH} ~ T_{CH}
IN
pulse generator 20
IN'
V_G
M_D
gate driver 11
SMP
V_S
N_S
gate control circuit 100

Fig. 6

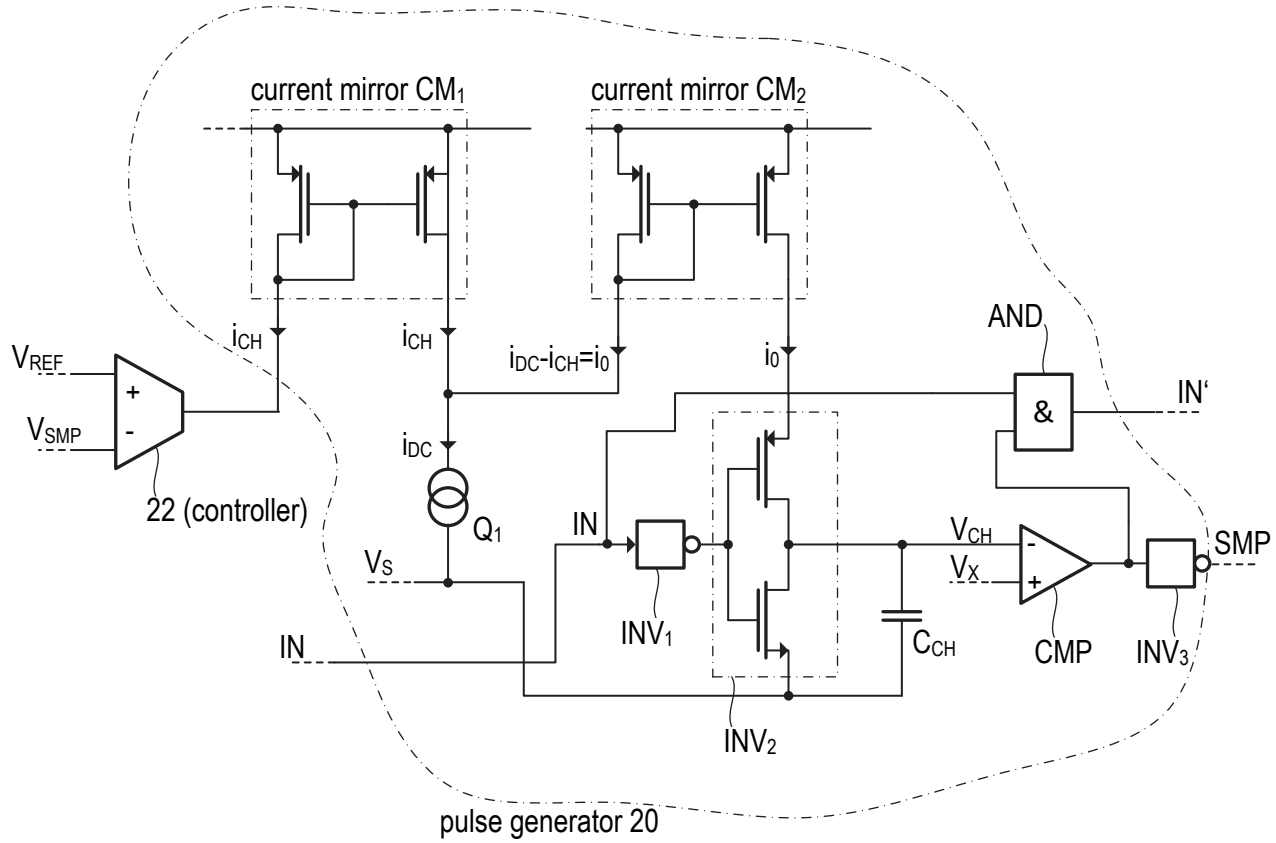

current mirror CM_1
current mirror CM_2
i_{CH}
i_{CH}
i_{DC}-i_{CH}=i_0
i_0
AND
IN'
&
V_{REF}
V_{SMP}
22 (controller)
i_{DC}
Q_1
IN
V_S
V_{CH}
V_X
SMP
INV_1
C_{CH}
CMP
INV_3
IN
INV_2
pulse generator 20

Fig. 7

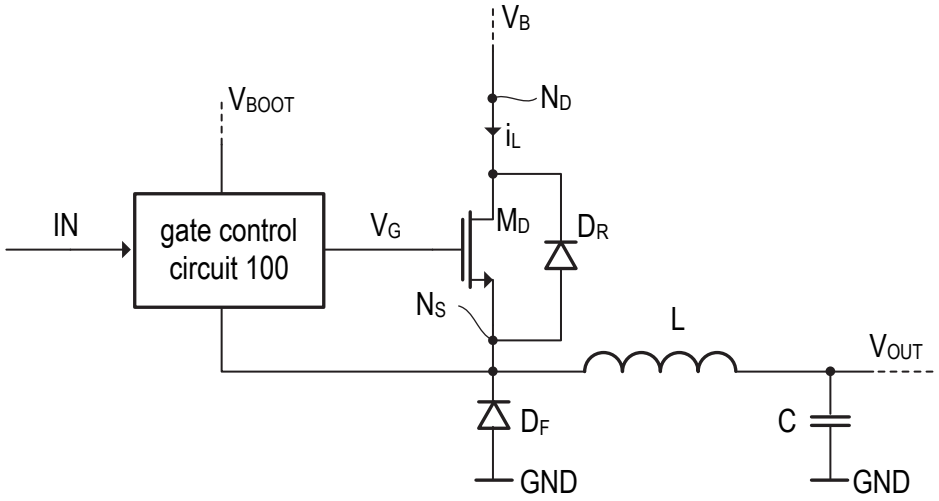

V_B
V_{BOOT}
N_D
i_L
IN
gate control circuit 100
V_G
M_D
D_R
N_S
L
V_{OUT}
D_F
C
GND
GND

Fig. 8

INTELLIGENT SEMICONDUCTOR SWITCH WITH INTEGRATED CURRENT MEASUREMENT FUNCTION

TECHNICAL FIELD

[0001] The present disclosure relates to the field of intelligent semiconductor switches, in particular to an integrated semiconductor circuit including a transistor as switching device and a current measurement circuit. The present disclosure further relates to the field of switching converters for voltage conversion in which one or more intelligent semiconductor switches can be used.

BACKGROUND

[0002] Intelligent semiconductor switches are increasingly replacing “normal” power transistors in various applications. Switching converters, such as buck converters which may be used to supply various electric loads, are one such example. In illumination applications, for example, light emitting diodes (LEDs) can be supplied using a buck converter.

[0003] Current sensing is an important capability for controlling the function of the circuit in switching converters. In switching converters, current sense resistors are commonly used to obtain information about the inductor current which passes through the switching converter’s inductor. The information concerning the inductor current is used to implement a so-called load current control.

[0004] A current sense resistor, which needs to be coupled to the inductor, is a separate circuit component and requires a dedicated input pin at the integrated control circuit of the switching converter. In order to increase the level of integration, the external current sense resistor and the power transistor, as well as some of the control circuitry, may be integrated in one semiconductor device. However, an integrated current sense circuit is only capable of delivering current information while the power transistor is active (switched on). When the power transistor is inactive (switched off), the inductor current cannot be measured.

SUMMARY

[0005] A method for current measurement in a switching converter is described herein. In accordance with one embodiment, the method includes switching a first transistor on and off in accordance with a logic signal, wherein a load current passes through the first transistor while it is switched on. The method further includes providing – by means of a second transistor – a sense current that is indicative of the load current, wherein the second transistor

is coupled to the first transistor such that the first and the second transistors are switched on and off simultaneously. Furthermore, the method includes determining an end of a switch-on phase of the second transistor, and providing a current sense signal that represents the sense current between a first time instant, which corresponds to the determined end of the switch-on phase, and a second time instant, at which the logic signal signals a switch-off of the first transistor (TL).

[0006] Further, a circuit for use in a switching converter controller is described herein. In accordance with one embodiment, the circuit includes a first transistor configured to provide a load current in accordance with a logic signal, a sense transistor coupled to the first transistor and configured to provide a sense current that is indicative of the load current, and a control circuit that is configured to: determine an end of a switch-on phase of the sense transistor and to provide a current sense signal that represents the sense current between a first time instant, which corresponds to the determined end of the switch-on phase, and a second time instant at which the logic signal signals a switch-off of the first transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The embodiments, which are described in the following, can be better understood with reference to the following drawings and descriptions. The components in the figures are not necessarily to scale; instead emphasis is placed upon illustrating the principles of the embodiments described herein. Furthermore, in the figures, like reference numerals designate corresponding parts.

[0008] Figure 1 illustrates one example of a buck converter with a power transistor, current measurement and control circuitry integrated in one semiconductor chip.

[0009] Figure 2 illustrates the charging phase of the transistor’s gate capacitance when the transistor is switched on.

[0010] Figure 3 illustrates an example of a circuit which may be used to determine the duration of the charging phase of the gate capacitance.

[0011] Figure 4 illustrates an example of a circuit which is configured to determine a measured value representing an average load current for the control of a switching converter.

[0012] Figure 5 includes timing diagrams illustrating the function of the circuit of Fig. 4.

[0013] Figure 6 is a flow chart illustrating an example of a method described herein which may be performed by a controller of a switching converter.

DETAILED DESCRIPTION

[0014] Fig. 1 illustrates one example of a buck converter with a power transistor, current measurement and control circuitry integrated in one semiconductor chip, referred to as controller chip 10. As can be seen in Fig. 1, the only discrete circuit components are the inductor L_O, a free-wheeling element (diode D_F), a capacitor C_B and, naturally, the electric load 20, which is a LED in the present example.

[0015] The controller chip 10 includes a power transistor T_L having a load current path (drain-source current path) that is coupled between a supply pin VS and an output pin OUT of the controller chip 10. During operation, a supply voltage V_S is applied at the supply pin VS. The inductor L_O is connected between one terminal of the load 20 (e.g. anode of the LED) and the output pin OUT. The other terminal of the load 20 (e.g. cathode of the LED) may be connected to ground potential. The diode D_F is connected between the output pin OUT and the ground potential. In some applications, the diode D_F is replaced by a second power transistor. In some embodiments the diode D_F (or, instead, a transistor) may be integrated in the controller chip. In this context, the term “pin” refers to any common chip contact. Accordingly, “pin” may designate a solder pin or a solder ball for the surface mounting of the chip onto a circuit board. Alternatively, the pins may be configured for through-hole mounting.

[0016] The controller chip 10 further includes a so-called sense transistor T_S. The drain electrodes and the gate electrodes of the two transistors T_S and T_L are interconnected, wherein a current sense resistor R_S is connected between the source electrode of the sense transistor T_S and the output pin OUT. In contrast thereto, the source electrode of the power transistor T_L is directly connected to the output pin OUT. In the present example, the current passing through the power transistor T_L is denoted as i_L (load current) while the current passing through the sense transistor T_S and the resistor R_S is denoted i_S (sense current). While the transistors are active (switched on, time interval T_{ON}), the inductor current i_{OUT} equals the sum of the transistor currents i_L+i_S. When the transistors are off, the inductor current i_{OUT} passes through the free-wheeling diode D_F.

[0017] The two transistors T_S and T_L may be implemented in the same transistor cell array, wherein the number of cells N_L, which compose the power transistor T_L, is much higher than the number of cells N_S, which compose the sense transistor T_S. As the two transistors T_S and T_L are operated in approximately the same operating point, the ratio i_L/i_S is approximately equal to the ratio $k=N_L/N_S$. Thus the load current i_L may be inferred from the current sense

signal V_{SENSE} according to the equation $i_L = k \cdot i_S = k \cdot V_{SENSE}/R_S$. The output current i_{OUT} equals $(k+1) \cdot i_S$.

[0018] The gate voltage V_G applied to the gate electrodes of transistors T_L and T_S is generated by the gate driver circuit 11, which is configured to generate the gate voltage V_G (or a gate current i_G resulting in a respective gate voltage) in accordance with a logic signal ON. The logic signal ON is a control signal indicating the desired switching state (on or off) of the transistor T_L. In the present example, the logic signal ON is provided by a control circuit 12, which is configured to generate the logic signal ON based on the current sense signal V_{SENSE} and other parameters. The control of switching converters, in particular of a buck converter, is as such known and thus not further discussed herein.

[0019] The above-mentioned equation $i_L = k \cdot V_{SENSE}/R_S$ is not exactly valid during a switch-on process of the transistors T_L and T_S, because during the switch-on of transistor T_S the displacement current passing through the gate-source capacitance C_{GS} of the sense transistor T_S also flows through the sense resistor R_S and contributes to the voltage drop V_{SENSE} across the sense resistor R_S, which may cause a measurement error. It is noted that this source of systematic measurement errors is a consequence of the current sense resistor R_S being integrated in the controller chip 10. Using an external current sense resistor in series with the inductor L_O would not cause such a systematic error. This situation is further explained with reference to Fig. 2.

[0020] Fig. 2 includes three timing diagrams illustrating, by way of example, a switch-on process of the transistors T_L and T_S. The top diagram of Fig. 2 illustrates an example of the logic signal ON, the middle diagram illustrates a corresponding example of the gate voltage V_G, and the bottom diagram illustrates a pulse, the length of which corresponds to the length of the switch-on process of the transistors T_S and T_L. As can be seen in Fig. 2, the control circuit 12 sets the logic signal ON to a High Level at time instant t_0 (indicating that the transistors T_L and T_S are to be switched on) and back to a Low Level at time instant t_2 (indicating that the transistors T_L and T_S are to be switched off). However, the transistors T_L and T_S cannot instantaneously become conductive. In the depicted example, it takes from time instant t_0 to time instant t_1 to charge the gate-source capacitance. As the gate-source capacitance is being charged, the gate-voltage ramps up to a value needed to fully switch on the transistors T_S and T_L. In the example of Fig. 2, the duration of this switch-on process is denoted as $T_{GCP} = t_1 - t_0$.

[0021] In order to obtain a precise current measurement, the time interval T_{GCP} is blanked out in accordance with the concept described herein. However, the time interval T_{GCP} is not constant and may vary dependent on different parameters (e.g. temperature, aging, etc.), as well as on tolerances of the manufacturing process. Fig. 3 illustrates one example of a circuit which can be used to determine the time interval T_{GCP} and to adaptively adjust it during operation of the controller chip 10.

[0022] Fig. 3 illustrates the gate driver 11 and part of the control circuit 12 (see also Fig. 1). The pulse generator 20 generates the logic signal ON from the signal S_{WPM} (which may be a pulse-width modulated, PWM, signal) and also outputs a signal PLS with a pulse with length T_{GCP} as shown in the timing diagrams of Fig. 2. The signal ON is basically a copy of the signal S_{PWM}. Accordingly, the rising edges of a pulse in the logic signal ON and of a corresponding pulse in the signal PLS are practically coincident. The length T_{GCP} of the pulse PLS depends on the input signal S_{GCP} supplied to the pulse generator 20. That is, the input signal S_{GCP} determines the duration T_{GCP} of the currently generated pulse in signal PLS.

[0023] The signal PLS is supplied, as a control signal, to a control input of a sample and hold circuit 21, which receives the gate voltage V_G as input signal and provides the signal V_{SMP} as output signal. In the present example, the output signal V_{SMP} is equal to the input signal V_G as long as the control input “sees” a High Level, whereas the output signal V_{SMP} remains at its current level when the control input changes to a Low Level. In other words, the sample and hold circuit 21 samples the gate voltage V_G at the time instant at which a pulse signal PLS exhibits a falling edge (see Fig. 2, time instant t_1).

[0024] The circuit of Fig. 3 also includes a controller 22, which receives the sampled voltage V_G and a reference voltage $V_{G,REF}$ (set point) and generates, as output signal, the control signal S_{GCP}. The controller 22 may be a difference amplifier, which operates a P-controller (P meaning “proportional”). As mentioned, the control signal S_{GCP} is supplied to the pulse generator 20, wherein the level of the control signal S_{GCP} determines the pulse lengths T_{GCP} pf the pulses PLS.

[0025] As can be seen from Fig. 3, the depicted circuit implements a control loop which iteratively adjusts the pulse length T_{GCP} until the sampled gate voltage V_{SMP} corresponds to the reference value $V_{G,REF}$. When the circuit is powered on, an initial value of T_{GCP} may be used that is at the lower end of its possible range, as a result of which T_{GCP} initially tends to be too short, whereby the control loop will adjust T_{GCP} to its correct value within one PWM cycle. As a result, each pulse PLS indicates the duration of the gate charge period, i.e. the

duration between the time instant t_0, at which the signal ON indicates a switch-on, and the time instant t_1, at which the transistor T_L actually switches on (see also Fig. 2).

[0026] As mentioned above, during the gate charge period T_{GCP}, the current sense resistor R_S basically "sees" the displacement current passing through the gate-source capacitance C_{GS} (see Fig. 1). Therefore, according to the embodiments described herein, the time interval T_{CGP} is blanked out for the purpose of current measurement, which is done with the help of the current sense resistor R_S.

[0027] Fig. 4 illustrates an example of a circuit which can be used to control the buck converter of Fig. 1. The circuit of Fig. 4 may be regarded as part of the control circuit 12 of Fig. 1. According to Fig. 5, the circuit receives the current sense signal V_{SENSE} as input signal (voltage drop across the resistor R_S) As indicated in Fig. 4, the current sense signal V_{SENSE} is a superposition of a first portion, which corresponds to the gate current i_G (during the time interval T_{GCP}), and a second portion, which corresponds to the load current i_L passing through the load transistor T_L (after the time interval T_{GCP} as long as signal ON is High, see Fig. 2). The current sense signal V_{SENSE} is provided to a pass filter 111 via a switch 110.

[0028] The switch 110 is closed as long as the logic conjunction ON & $\overline{\text{PLS}}$ is true. That is, the switch 110 is closed when the signal ON (or S_{PWM}) indicates a switch-on of the power transistor T_L provided that the time interval T_{GCP} has already lapsed. In essence, the switch 110 is switched on at the falling edges of the pulses PLS (i.e. when the inverse signal $\overline{\text{PLS}}$ transitions from High to Low at time instant t_1, see Fig. 2). As a consequence, the filter 111 sees, as input signal, a trapezoidal waveform, which is the current sense signal with the first portion (which corresponds to the to the gate current i_G) blanked out.

[0029] The filter 111 is configured to provide a signal V_{AVG} at its output, which approximately corresponds to the average of the input signal (signal V_{SENSE}) during the time interval during which the switch 110 is closed (i.e. from t_1 to t_2, see Fig. 2). The filter may be implemented, for example, as a low pass filter, in particular as a simple first order RC lowpass filter (e.g. resistor R_F, capacitor C_F). As can be seen from Fig. 4, the low pass filter 111 does, in essence, average the (switched) current sense signal V_{CS} over the time interval from t_1 to t_2 (see Fig. 2) which is T_{ON}-T_{GCP}. During the time interval T_{OFF} (see Fig. 5), i.e. when the switch 110 is open, the averaged signal V_{AVG} remains basically constant as the charge stored in the capacitor C_F of the low-pass filter 111 remains constant (assuming the error amplifier 112 has a high input impedance). Due to the approximately trapezoidal waveform of the load current

during the on-time and the off-time, and due to the constant clock frequency, the average current value is the same during the on-time and the off-time.

[0030] An error amplifier 112 receives the average current sense signal V_{AVG} and a reference signal $V_{REF,}$ which represents the current set-point / desired load current. The error amplifier 112 is basically a difference amplifier and generates an output signal (error signal V_E) which is based on (e.g. proportional to) the difference V_{AVG}-V_{REF}. The error signal V_E and a triangular signal V_{RAMP} (e.g. a sawtooth / ramp signal) are provided to the inputs of a comparator 114, which is configured to compare the error signal V_E and the ramp signal V_{RAMP} and to generated the PWM signal S_{PWM} at its output. As shown in Fig. 4, the PWM signal S_{PWM} provided by the comparator 114 is at a High level when the ramp signal V_{RAMP} is lower than the error signal VE, and at a Low level otherwise.

[0031] The ramp generator 113, which provides the ramp signal V_{RAMP}, usually operates at a fixed frequency f_{PWM}. That is, the start of a PWM period (time instant t_0 in Fig. 2) is triggered by (e.g. a rising edge of) a clock signal CLK (see Fig. 5, not shown in Fig. 4), wherein the end of the on-time T_{ON} is determined by the comparator 114. It is noted that the concept of generating a PWM signal for controlling a switching converter by using an error amplifier and a ramp generator is as such known and thus not explained herein in more detail. However, different from known approaches, the example of Fig. 4 allows the controlling of the output current i_{OUT} of a switching converter without actually measuring the output current i_{OUT} passing through the load, but instead only the load current i_L passing through the power transistor T_L during the on-time T_{ON}, which is possible with an integrated current sense resistor R_S.

[0032] Fig. 5 illustrates timing diagrams further illustrating the function of the circuit of Fig. 4. The top diagram of Fig. 5 illustrates an exemplary waveform of the mentioned clock signal CLK. The middle diagram of Fig. 5 illustrates the load current i_L and the current iF passing through the free-wheeling diode D_F during the off time T_{OFF}, and the bottom diagram illustrates the resulting signal ON (which corresponds to S_{PWM}). As can be seen in Fig. 5, the average i_{AVG} of the current i_L during the on-line T_{ON} is equal to the current i_F during the off-time T_{OFF} and also equal to the total output current i_{OUT} during a PWM cycle period T_{PWM} = T_{ON}+T_{OFF}. The time period T_{GCP}, which is blanked out for current measurement as explained above, is shaded gray in Fig. 5.

[0033] The concept described herein will be summarized below by way of example. It is understood that the following is not to be understood as an exhaustive listing of technical

features but rather as an exemplary summary. According to one embodiment, a controller chip for a switching converter includes a first transistor (power transistor T_L), configured to provide a load current in accordance with a logic signal (see Figs. 1 and 3, signal S_{PWM} and signal ON), and a second transistor (sense transistor T_S) coupled to the first transistor and configured to provide a sense current that is indicative of the load current. The controller chip further includes a control circuit (see Fig. 1, control circuit 12) that is configured to determine an end of a switch-on phase (see Fig. 2, falling edge of pulse PLS at time t_1) of the sense transistor, and to provide a current sense signal (see Fig. 5, signal V_{SENSE}) that represents the sense current between a first time instant (see Fig. 2, time t_1), which corresponds to the determined end of the switch-on phase, and a second time instant (see Fig. 2, time t_2) at which the logic signal signals a switch-off of the first transistor.

[0034] The control circuit may include a low pass filter configured to filter the current sense signal (see Fig. 4, filter 111), and an error amplifier configured to generate an error signal (see Fig. 4, error amplifier 112 and signal V_E) representing a difference between the filtered current sense signal and a reference value. A ramp generator is configured to generate a periodic signal (see Fig.5, ramp generator 113) which comprises a triangular pulse in each period. A comparator is configured to compare the periodic signal with the mentioned error signal (see Fig. 5, comparator 114), wherein the control circuit is configured to generate the logic signal (see Fig. 3, signal ON) based on an output signal (see Fig. 4, PWM signal S_{PWM}) of the comparator.

[0035] In order to form a buck converter, an inductor is connected to the first transistor, so that the load current passes through the inductor while the first transistor is switched on (see Fig. 1, inductor L_O, and Fig. 5, load current i_L), and a free-wheeling element (see Fig. 1, diode D_F) is coupled to the inductor, so that an inductor current can pass though the free-wheeling element while the first transistor is switched off (see Fig. 5, diode current i_F). An electric load, which may be a light emitting diode (or a series circuit of light emitting diodes), is coupled to the first transistor (see Fig. 1, power transistor T_L) via the inductor.

[0036] A further embodiment relates to a method that may be used in a switching converter. The method is also represented by the flow chart of Fig. 6. Accordingly, the method includes switching a first transistor (see Fig. 1, power transistor T_L) on and off in accordance with a logic signal (Fig. 6, box S1) so that a load current (see Fig. 1, current i_L) passes through the first transistor while it is switched on. The method further includes: providing a sense current (see Fig. 1, current i_S), indicative of the load current by a second transistor (see Fig. 1, sense

transistor T_S), that is coupled to the first transistor such that the first transistor and the second transistors are switched on and off simultaneously (Fig. 6, box S2), thus determining an end of a switch-on phase of the second transistor (Fig. 6, box S3), and providing a current sense signal (see Fig. 5, signal V_{SENSE}) that represents the sense current between a first time instant (see Fig. 2, time t_1), which corresponds to the determined end of the switch-on phase, and a second time instant (see Fig. 2, time t_2) at which the logic signal signals a switch-off of the first transistor (Fig 6, box S4).

[0037] In one embodiment, the method may include filtering the current sense signal using a low-pass filter (see Fig. 4, filter 111). An error signal may be generated that represents a difference between the filtered current sense signal and a reference value (see Fig. 4, error amplifier 113, error signal V_E). The method may further include generating a periodic signal, which comprises a triangular pulse in each period (see Fig. 4, ramp signal V_{RAMP}), and comparing the periodic signal with the error signal using a comparator (see Fig. 4, comparator 114).

[0038] The mentioned logic signal may be generated based on an output signal of the comparator. Further, in one embodiment the logic signal is a modulated signal indicating on-times and off-times (see Fig. 5, T_{ON} and T_{OFF}) of the first transistor, wherein the begin of each on-time triggers a respective switch-on phase (see Fig. 3, pulse PLS) of the second transistor.

[0039] In order to determine the end of the switch-on phase of the second transistor, the method may comprise modifying a time value (see Fig. 2 and 3, time interval T_{GCP}), indicating the end of the switch-on phase, based on a voltage value of the gate voltage of the first transistor, sampled at the end of a preceding switch-on phase, and a reference value (see Fig. 3, sampled voltage value V_{SMP}, and reference voltage $V_{G,REF}$).

Although the invention has been illustrated and described with respect to one or more implementations, alterations and/or modifications may be made to the illustrated examples without departing from the spirit and scope of the appended claims. In particular regard to the various functions performed by the above described components or structures (units, assemblies, devices, circuits, systems, etc.), the terms (including a reference to a “means”) used to describe such components are intended to correspond – unless otherwise indicated – to any component or structure, which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure, which performs the function in the herein illustrated exemplary implementations of the invention.

CLAIMS

1. A method comprising;

switching a first transistor (T_L) on and off in accordance with a logic signal (ON), with a load current (i_L) passing through the first transistor (T_L) while it is switched on;

providing a sense current (i_S) that is indicative of the load current (i_L) by means of a second transistor (T_S) that is coupled to the first transistor (T_L) such that the first and the second transistors (T_L, T_S) are switched on and off simultaneously;

determining an end of a switch-on phase of the second transistor (T_S);

providing a current sense signal (V_{SENSE}) that represents the sense current (i_S) between a first time instant (t_1), which corresponds to the determined end of the switch-on phase, and a second time instant (t_2), at which the logic signal (ON) signals a switch-off of the first transistor (T_L).

2. The method of claim 1, further comprising:

filtering the current sense signal (V_{SENSE}) using a low-pass filter.

3. The method of claim 2, further comprising:

generating an error signal (V_E) representing a difference between the filtered current sense signal (V_{SENSE}) and a reference value (V_{REF}).

4. The method of claim 3, further comprising:

generating a periodic signal (V_{RAMP}) which comprises a triangular pulse in each period;

comparing the periodic signal (V_{RAMP}) with the error signal (V_E) using a comparator; and

generating the logic signal (ON) based on an output signal (S_{PWM}) of the comparator.

5. The method of any of claims 1 to 4,

wherein the logic signal (ON) is a modulated signal indicating on-times (T_{ON}) and off-times (T_{OFF}) of the first transistor (T_L), the begin of each on-time (T_{ON}) triggers a respective switch-on phase of the second transistor (T_S).

6. The method of any of claims 1 to 5, wherein determining the end of the switch-on phase of the second transistor (T_S) comprises:

modifying a time value (T_{GCP}), indicating the end of the switch-on phase, based on a voltage value (V_{SMP}) of the gate voltage of the first transistor (T_L), sampled at the end of a preceding switch-on phase, and a reference value ($V_{G,REF}$).

7. A circuit comprising:

a first transistor (T_L) configured to provide a load current (i_L) in accordance with a logic signal (ON);

a sense transistor (T_S) coupled to the first transistor (T_L) and configured to provide a sense current (i_S) that is indicative of the load current (i_L);

a control circuit (10) that is configured to:

determine an end of a switch-on phase of the sense transistor (T_S); and

provide a current sense signal (V_{SENSE}) that represents the sense current (i_S) between a first time instant (t_1), which corresponds to the determined end of the switch-on phase, and a second time instant (t_2) at which the logic signal (ON) signals a switch-off of the first transistor (T_L).

8. The circuit of claim 7,

wherein the control circuit (10) comprises a switch (110) configured to blank out the current sense signal (V_{SENSE}) from a time instant (t_0), at which the logic signal (ON) signals a switch-on of the first transistor (T_L), and the first time instant (t_1).

9. The circuit of claim 7 and 8, wherein the control circuit (10) comprises:

a low pass filter (111) configured to filter the current sense signal (V_{CS}).

10. The circuit of claim 9, wherein the control circuit (10) further comprises:

an error amplifier (112) configured to generate an error signal (V_E), representing a difference between the filtered current sense signal (V_{CS}), and a reference value (V_{REF}).

11. The circuit of claim 10, wherein the control circuit (10) further comprises;

a ramp generator (113) configured to generate a periodic signal (V_{RAMP}), which comprises a triangular pulse in each period;

a comparator (114), configured to compare the periodic signal (V_{RAMP}) with the error signal (V_E),

wherein the control circuit (10) is configured to generate the logic signal (ON) based on an output signal (S_{PWM}) of the comparator (114).

12. The circuit of any of claims 1 to 10, further comprising:

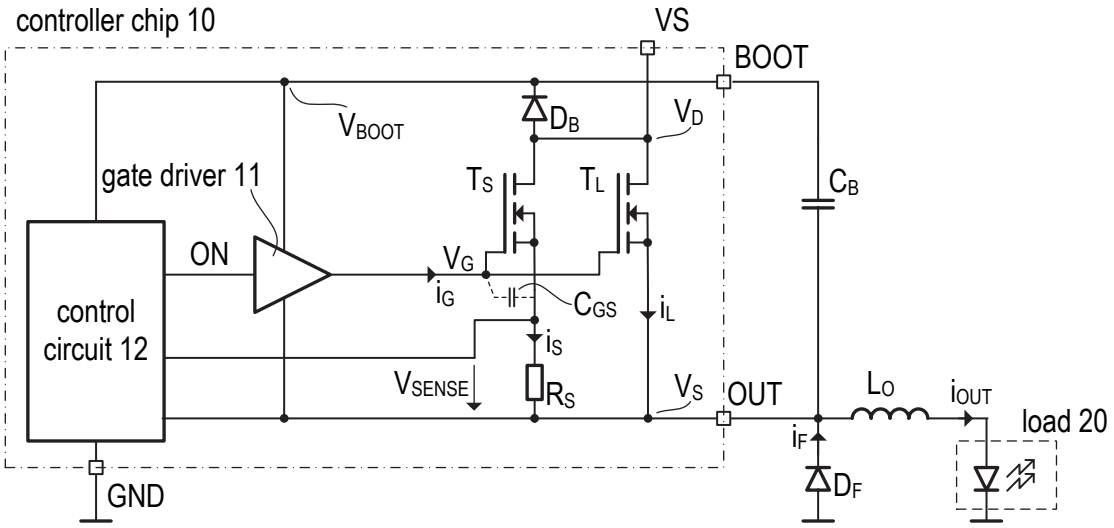
an inductor connected to the first transistor (T_L) such that the load current (i_L) passes through the inductor (L_O) while the first transistor (T_L) is switched on;

a free-wheeling element (D_F) coupled to the inductor (L_O) such that an inductor current can pass though the free-wheeling element (D_F) while the first transistor (T_L) is switched off; and

an electric load (20) which is coupled to the first transistor (T_L) via the inductor (L_O).

ABSTRACT

[0040] A method for current measurement in a switching converter is described herein. In accordance with one embodiment, the method includes switching a first transistor on and off in accordance with a logic signal, wherein a load current passes through the first transistor while it is switched on. The method further includes providing – by a second transistor – a sense current that is indicative of the load current, wherein the second transistor is coupled to the first transistor so that the first and the second transistors are switched on and off simultaneously. Further, the method includes determining an end of a switch-on phase of the second transistor, and providing a current sense signal that represents the sense current between a first time instant, which corresponds to the determined end of the switch-on phase, and a second time instant, at which the logic signal signals a switch-off of the first transistor (TL).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VS
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D_B
V_D
gate driver 11
T_S
T_L
C_B
ON
V_G
i_G
C_{GS}
i_L
control
circuit 12
i_S
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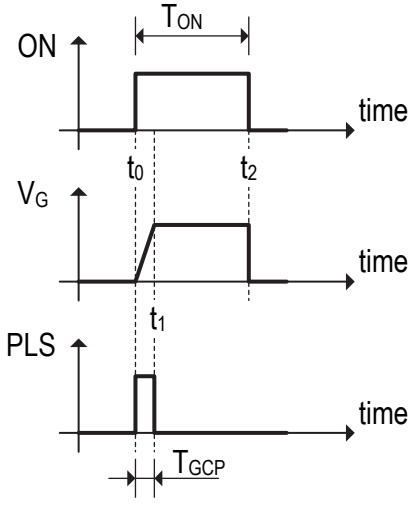
R_S
V_S
OUT
L_O
i_{OUT}
load 20
i_F
D_F
GND

Fig. 1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ON
time
t_0
t_2
V_G
time
t_1
PLS
time
T_{GCP}

Fig. 2

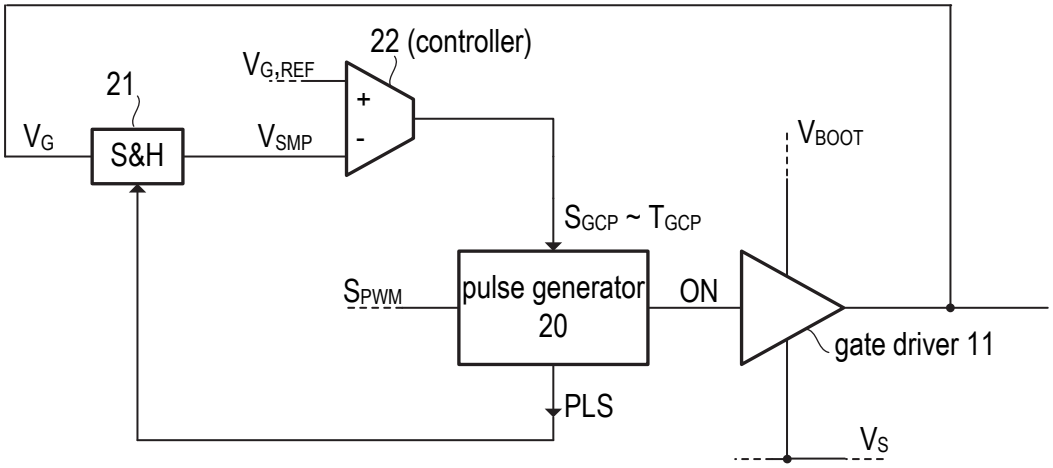

Fig. 3

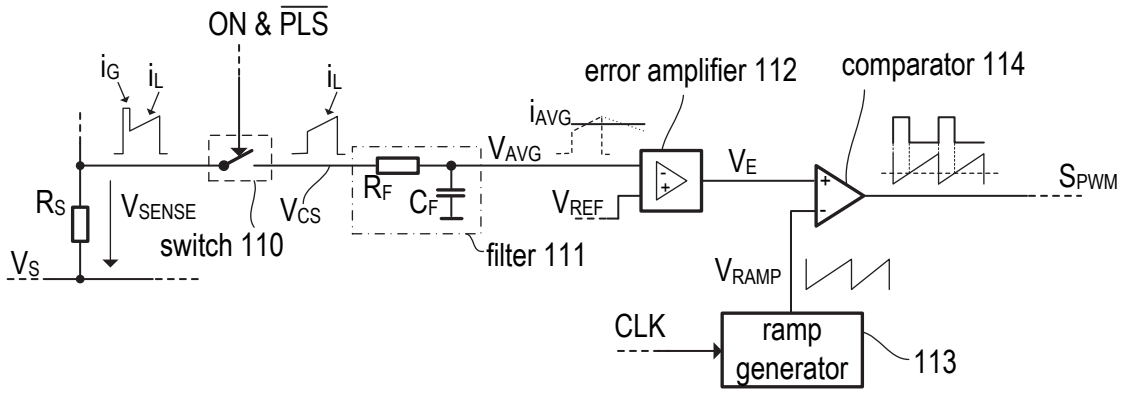

Fig. 4

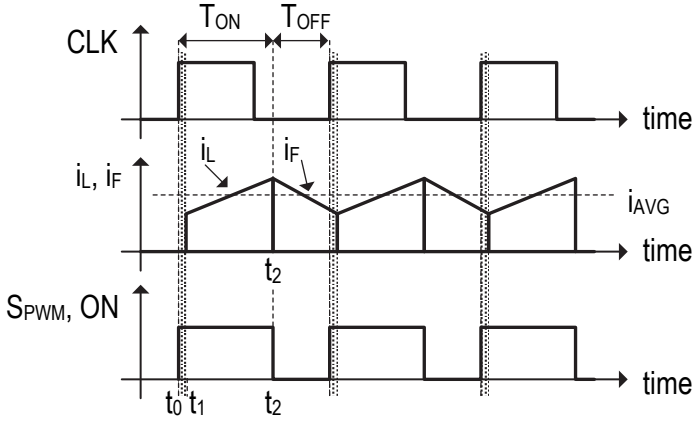

Fig. 5

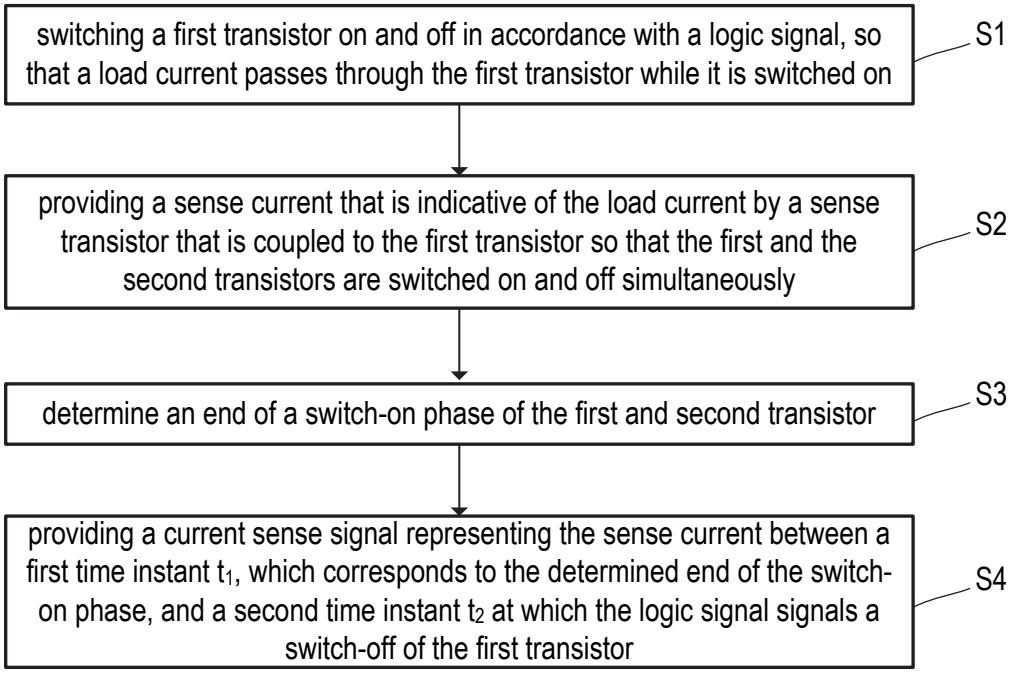
switching a first transistor on and off in accordance with a logic signal, so that a load current passes through the first transistor while it is switched on
S1
providing a sense current that is indicative of the load current by a sense transistor that is coupled to the first transistor so that the first and the second transistors are switched on and off simultaneously
S2
determine an end of a switch-on phase of the first and second transistor
S3
providing a current sense signal representing the sense current between a first time instant t_1, which corresponds to the determined end of the switch-on phase, and a second time instant t_2 at which the logic signal signals a switch-off of the first transistor
S4

Fig. 6

Conclusions and Future Works

Conclusions

Main targets of this PhD work is to verify the suitability of the proprietary BCD technology for the possible manufacture of high-frequency DC-DC converters in the automotive field.

The study presented here is part of a research agreement between Infineon and University of Milano Bicocca developed with the relevant contribution of PhD students at the university.

As explained in Chapter 1, it is divided into three steps. In the first step, an investigation was made about the suitability of the technology with regard to the manufacture of DC-DC devices. In the second step, developed here, the aim is to investigate the feasibility of switching DC-DC from 1 to 10 MHz and load current of at least 3A using the technologies at our disposal . In the third part, the intention is to build a prototype with constant output voltage and characteristics closer to market requirements.

My work started with a literature search of the state of the art.

Indeed, there are several studies and proposals to increase the switching frequency of DC-DC converters. Most of these proposals are based on switches in GaN technology.

Solutions based on this technology, which are still in the development phase, also require specific drivers which, having to follow the development of GaN switches, have not yet reached a stable topology.

Although they represent the future of DC-DC, we do not currently have adequate GaN technology to develop commercial devices.

Research was also carried out on the Buck devices available on the market as knowledge of devices on the market is essential.

In Figure 1.8 on chapter 1 the devices that we consider to be the state of the art from a commercial point of view are listed. Only the best performing ones have switching frequencies of 2.0-2.5MHz, load currents of 2-2.5A and usually not simultaneously

For our device, we designed three Buck Converters with switching frequencies of 1MHz, 4MHz and 10MHz in their essential parts. In chapter 1 are indicated on table 1.2 the guidelines.

It's evident the very aggressive target we set ourselves, in particular switch at 10MHz a typical 80mOhm Power DMOS with currents in the order of 3A.

This investigation was carried out by investigating multiple fields, circuital and technological, depending on available technologies available in the company.

Initially, the BCD-cap technology was considered. This technology, that I consider very promising, would have allowed the integration of large capacitors, even

several tens of nF. This would have made it possible to integrate bootstrap capacitance as well as Power DMOS, current sense and bootstrap diode. The absence of bonding wires in the switching part would have eliminated the inductances and capacitances associated to the bonding and related pins.

I also started some investigations to check whether make sense to integrate an inductance of a few tens of a few tens of nH into the silicon.

Despite interesting developments, I had to abandon the ongoing investigations due to management's decision to reduce costs.

Anyway the study led to a patent proposal.

The development of the Buck therefore turned to classic BCD technology.

To increase the switching frequency, I had to think of new solutions.

First, I eliminated operations that would have taken time without being directly involved in signal processing. For example, the transfer of signals using level shifters, because even a few nS at high frequencies are heavy.

This led to a device architecture in which all circuits are floating, being fed between Bootstrap (power supply) and Source (virtual ground). Since all circuits, references, protections, control, drivers, DMOS, current sense, are in the same domain, signal transfers and processing are faster. Bootstrap capacitor in parallel to all circuits is another advantage as it is a short-circuit for switching disturbances.

Fundamental to achieving high frequencies is the innovative closed-loop driver (patented), which allows the DMOS gate to be loaded an order of magnitude faster than conventional drivers.

Another interesting point is the high-side control of the average load current.

Thanks to these innovations, the goal was achieved.

The three Buck Converters operating at 1MHz, 4MHz and 10MHz were designed and layouted.

The simulations were performed with a slightly more conductive DMOS ($70m\Omega$) to take production spreads into account. In Figure C.1 the simulation at 10MHz, show the internal signal T_{ON}, the 3A load current and the DMOS gate voltage. It is interesting to note that to switch the $70m\Omega$ DMOS from 0 to 3V, 5nS are enough. A $140m\Omega$ DMOS could have been used with a more conservative choice and the switching time would be reduced to about 2.5nS.

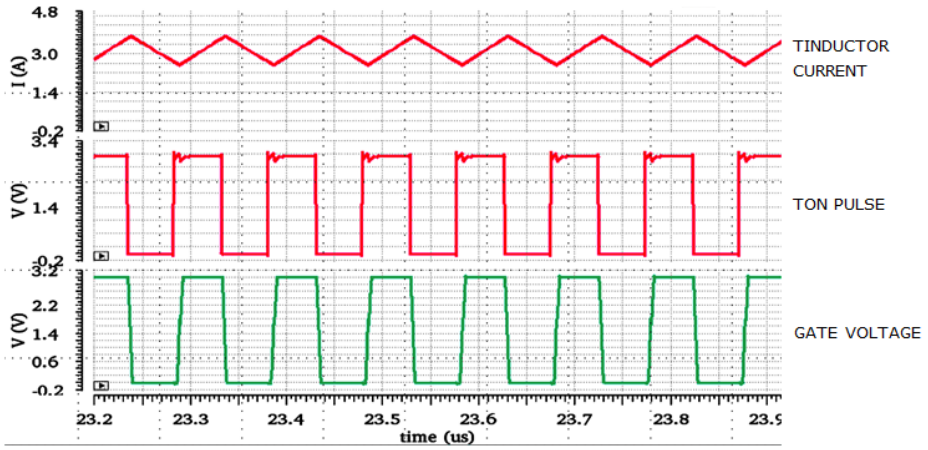

Figure C.1: 10MHz Buck Converter Simulation

At the time of writing, the 1MHz and 4MHz devices are in diffusion. Wafer out is planned for February 2023. The 10MHz device was not included in this development lot because the silicon area at our disposal was insufficient to hold all the three devices. It will however be included in the next test chip.

A total of four patent applications were submitted

In the end I would like to mention the study done on the bandgap topology described in Chapter 4 and in Appendix. Figure C.2 compares a commonly used bandgap topology and the one proposed in this PhD work. It is immediately evident from the topology shown on the right that the error amplifier and its compensation network are missing because the proposed topology is inherently stable.

A new start-up circuit has also been proposed that does not require a trigger signal and intervenes independently each time the bandgap moves from the operating point, avoiding the risks of an accidental circuit shutdown.

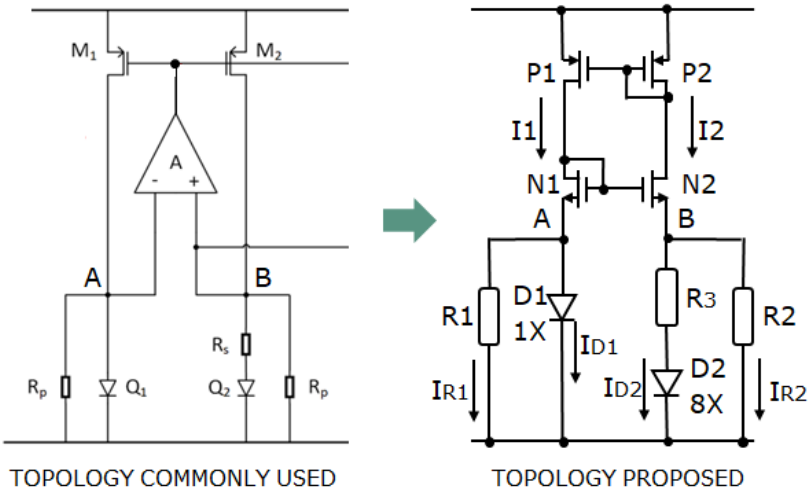

Figure C.2: Bandgap Topology Comparison

Future Works

In the near future, as soon as we have prototypes of the two versions in diffusion, there will be the lab characterization, while the 10MHz version already layouted will be put on the next test chip. Any minor changes will be evaluated following measurements of the 1MHz and 4MHz versions. Perhaps the 10MHz PCB will have to be revised as the higher frequency will most likely require some adaptation. Obviously, lab characterization will also follow for this version.

One aspect neglected in this phase is the on-chip free wheeling diode. It will in fact be considered in the third phase and more possibilities will be investigated, external, integrated and synchronous diodes.

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