SCUOLA DI DOTTORATO
UNIVERSITÀ DEGLI STUDI DI MILANO-BICOCCA

Dipartimento di / Department of

Fisica 'G.Occhialini'

Dottorato di Ricerca in / PhD program FISICA E ASTRONOMIA Ciclo / Cycle XXXV

INTEGRATED READOUT SYSTEMS FOR PARTICLE DETECTORS

Cognome /Surname Shah Nome / Name Syed Adeel Ali

Matricola / Registration number 863653

Tutore / Tutor: Marcello De Matties

Supervisor: Andrea Baschirotto

Coordinatore / Coordinator: Stefano Ragazzi

ANNO ACCADEMICO / ACADEMIC YEAR 2022/2023

.

.

Contents

List of Figures

List of Tables

Abstract

Increasing demand for high rate detectors in modern High-Energy-Physics (HEP) experiments is generating many technological challenges. Particularly, the particle detectors utilized in HEP experiments requires efficient readout electronics systems that can cope with the challenges faced due to the upgrade in HEP experiments. CMOS integrated circuits, widely used technology, is a common choice for readout chip based on reliability, cost reduction and performance improvement factors.

In this thesis, a general information of the experiment along with the upcoming challenges due to expected upgrade in the experiment are presented and a new readout electronic system, targeting a significantly power efficient, are efficient design, with a promising performance targetting to replace the existing readout electronics is presented. The first part of this thesis presents the LHC experiment information and the classical readout electronics, fabricated in CMOS 130nm, used for it.

Chapter 2 and 3 of this thesis presents the new readout chip, Front End Electronics for Monitored Drift Tube in a long sustainable technology, 65nm CMOS. This readout system has been specifically designed for Muon Drift Chambers matching the performance parameters of the existing readout electronics design. After theoretical analysis of the signal processing technique, the implementation of design is presented in detail. The simulations and measurement results are reported in Chapter 4 and 5.

1 Chapter 1: Introduction

The main goal of High-Energy Physics (HEP) experiments, carried out at CERN is to study the fundamental constituents of matter in terms of elementary charge particles, their interactions and their secondary products. Part of these phenomena have already been studied and are used to define the Standard Model of matter. In 2012, after 40 years of search, a subatomic particle with the expected properties of the missing paricle, was discovered in 2012 by the ATLAS experiment at CERN. The new discovered particle was later-on confirmed to match the expected properties of a Higgs bosons. The discovery of the Higgs bosons was a major milestone in particle physics. It is considered as the end of decades-long journey of exploration and the start of a new era of studies of this very special particle. The further challenges of CERN project is targeted to provide more details on the new charged particles as Higgs Bosons and neutrinos.
The Large Hadron Collider, world's largest and most powerful particle accelerator, at the CERN works every day for this purpose. It has a superconducting magnetic ring structure able to guide two high-energy particle beams. The high energy particle beams have opposite directions and they travel at light speed. Charged particles are generated from collisions of beams and they are accelerated toward a proper detector. Different detectors are located in different points of the collider. They are organized in shell structures and are designed to detect few topology of particles. Typically, the parameters useful to identify a charged particle are electrical charge, momentum, energy, distance and time of flight.
Detectors design is important but it is performance depends upon efficient electronic read-out systems, to collect and provide the correct required information. A big experiment requires a hard work of scientists, engineers and technicians.
In the last decade, electronics design have become more and more efficient and compact. CMOS integrated solution are preferred because of reliability, cost reduction and performance improvement. Proper and efficient readout electronics design is challenging but not impossible. Some characteristics are directly dependent from the electronic designer and their capability to manage the external parasitic effects, which are unavoidable factors in the experiment, as the parasitic capacitance of the connected detector.

1.1 The Large Hadron Collider

The Large Hadron Collider (LHC) at CERN [1] is the most powerful accelerator and collider in terms of luminosity and beam energy upto date. It is located in the same 26.7 km long tunnel as the Large Electron Positron Collider (LEP) which was shut down and decommissioned in 2000.
The tunnel is ring-shaped, consisting of eight arcs and eight straight sections, and is located 45m to 170m below the surface on slightly inclined plane. Two transfer tunnels, 2.5 km long, connect it to the rest of the CERN accelerator complex (see Figure 1) which is used for beam injection.
As a proton–proton collider, the LHC contains two separate vacuum pipes with oppositely oriented magnetic fields for the counter-rotating beams. A "twin bore design" was chosen for the superconducting dipole magnets that keep the beams on circular orbits. In this compact design, the two rings are integrated into the

superconducting magnets in the same cryostat. The dipole magnets generate a field strength of up to 8.33 T allowing for a maximum proton beam energy of 7 TeV. The proton beams are divided into 2808 bunches of 1.15.10 ^{11} protons each with 25 ns spacing resulting in a collision rate of 40 MHz at design operation of the LHC.
Of the eight straight sections of the LHC, four of them house the big experiments named as: ALICE, ATLAS, CMS and LHCb. ATLAS [2] and CMS [3] are multi-purpose detectors, which contributed in the discovery of the Higgs Boson particle, designed to operate at the design centre-of-mass energy of 14 TeV and luminosity of up to L=1.10^{34}cm^{-2}s^{-1}.
Main LHC machine parameters are presented in Table 1.

Table 1: Nominal design machine parameters of the Large Hadron Collider.

Parameter	**Value**
Circumference	26659 m
Center of Mass Energy	14 TeV
Luminosity	10^{34}cm^{-2}s^{-1}
Emittance	3.75 μm rad
β	0.55 m
Bunch Spacing	25 ns (7.5 m)
No. protons per bunch (at start)	1.5×10^{-11}
Collision crossing angle	300 μrad
Average crossing rate	31.6 MHz
RF Voltage (at 7 TeV)	16 MV
Number of RF Cavities	8
Number of Dipoles	1232
Number of Quadrupoles	858
Dipole operating temperature	1.9 K
Peak Dipole Field Strength	8.33 T
Stored beam energy	360 MJ
Stored energy in magnets	11 GJ
Typical beam lifetime	10 h
Synchrotron radiation per beam	6 kW

After the achievement of the main goal, the discovery of the Higgs boson in 2012 [4,5] as the last missing particle of the Standard Model, the experiment aims to search for any accessible physics beyond the Standard Model and to perform measurements of the properties of the Higgs boson like coupling strengths to bosons and fermions, total decay width and CP quantum numbers.

LHCb [6] experiment is dedicated to b-hadron physics designed to operate at a lower luminosity of L=1.10^{2}cm^{-2}s^{-1}. It performs precision measurements of CP-violation that may help to explain the matter–antimatter asymmetry in the universe and searches for rare B meson decays.
In addition to protons, the LHC can collide lead ions (^{208}Pb^{+82}) in lead–lead and lead–proton operating modes at a centre-of-mass energy of $\sqrt{s}$ = 2.76 TeV per nucleon. At the high energy densities reached in lead–lead collisions, quarks and gluons are expected to form a colourdeconfined state called quark–gluon plasma. The ALICE experiment [7] is devoted to the study of heavy ion collisions at a luminosity of L=1.10^{27} cm^{-2}s^{-1}.

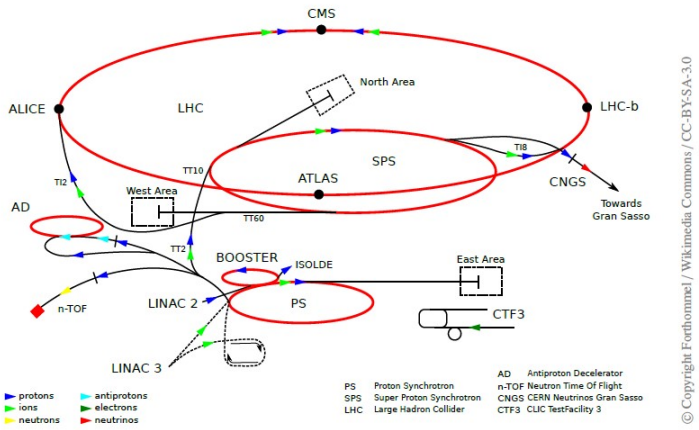


Figure 1: The CERN accelerator complex.

The four big LHC experiments, mentioned above, share their interaction points with three smaller experiments known as: LHCf, TOTEM and MoEDAL. LHCf [8] consists of two detectors 140m from the interaction point on both side of the ATLAS detector and aims to understand the origin of ultra-high-energy cosmic rays. TOTEM [9] shares the interaction point with CMS and consists of detectors 147m and 220m from the collision point. It is designed for the measurement of the total proton–proton interaction cross section and elastic and diffractive scattering processes. MoEDAL [10], which got approval in 2010, is the newest of the LHC experiments. Its goal is the search for magnetic monopoles and other strongly ionising massive particles.

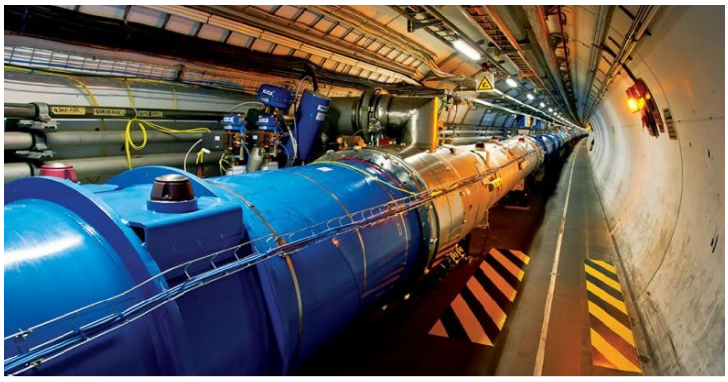


Figure 2: Large Hadron Collider (form CERN [1]).

1.2 The ATLAS Experiment

The ATLAS detector is a multipurpose detector designed to explore a wide range of physics topics. The unprecedented energy and luminosity of the LHC allow for both precision measurements of the Standard Model and searches for any credible new physics processes beyond the Standard Model.
The high interaction rate and luminosity, however, demands for high performance readout electronics in-terms of radiation tolerance, spatial and time resolution. The production cross-sections of most interesting processes are smaller by many orders

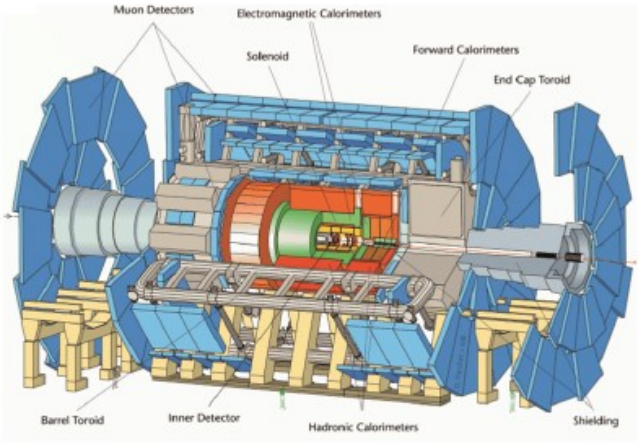


Figure 3: Scheme of complex ATLAS Detector[2].

of magnitude than the total inelastic proton–proton cross-section of about 80 mb which is dominated by dijet production. At design luminosity, crossing rate of 40 MHz, each interesting event is accompanied by on average, further, 23 inelastic events. Highly granular, radiation hard detectors and electronics are needed to cope with the high radiation levels and track density to control the effects of overlapping events. As the read-out and storage capacity is limited, a very selective, robust and efficient trigger system is required to arrive at a manageable data volume, without discarding interesting rare events.
High resolution electromagnetic calorimetry is essential for efficient electron and photon detection and precise energy measurement. Hermetic hadronic calorimetry is important for accurate jet and missing transverse energy measurements which are fundamental for many studies.

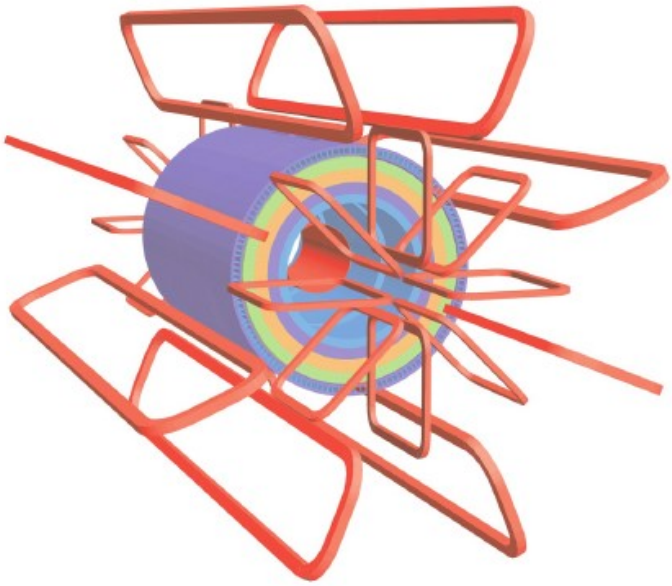


Figure 4: The superconducting solenoid (blue) and toroid (red) magnet coils [2].

The ATLAS detector scheme shown in Figure 3, is forward–backward symmetric with respect to the interaction point. The individual sub-detectors are arranged in

a cylindrical pattern, around the beam pipe in the central barrel region and in discs, in the so-called end-caps, typical for different collider experiments.
The superconducting magnet system consists of a thin solenoid coil. It surrounds the inner tracking detector with a diameter of 2.5m and a length of 5.3m and three large air-core toroids (one for the barrel and one for each end-cap) in the Muon Spectrometer. The layout of the magnet system is shown in Figure 4.
The ATLAS design uses a right-handed coordinate system. Its origin is at the nominal interaction point, in the centre of the detector, and the z-axis along the beam line. The y-axis is directed upwards and the x-axis points from the interaction point to the centre of the LHC ring. Cylindrical coordinates (r, θ, Φ) are used in the transverse plane. Φ is the azimuthal angle around the beam line, θ the polar angle and r the radius measured from the beam line. Transverse observables (index τ) are projections into the x–y plane perpendicular to the beam line.

1.2.1 Detector Components

This section briefly describes the sub-detectors of the ATLAS experiment.

The Inner Tracking Detector:
When a p=p collision occurs, around 1000 particles emerge at the LHC, which leads to a high density of tracks in the detector. ATLAS uses a combination of three technologies in the Inner Detector (ID): silicon pixel, micro-strip (SCT) detectors and a Transition Radiation Tracker (TRT) — to achieve the required momentum and vertex resolutions. The ID is immersed in a 2 T magnetic field created by the central solenoid. The design layout of the ID is shown in Figure 5.
The innermost component is the Pixel Detector, and is arranged around the interaction point in three concentric cylinders in the barrel region and the disks perpendicular to the beam line in the end-cap regions. The spatial resolution provided by the Pixel Detector is 10 µm in the transverse plane and 115 µm in the longitudinal direction with respect to the beam line. The innermost detector layer is at a distance of only 5 cm from the beam line and is of especial importance for the measurement of decay vertices needed for b-quark and τ-lepton identification as well as for searches for new long-lived discovered particles. The Pixel Detector has a large number of readout channels, approximately 80.4 million.
In a similar pattern but with four layers, the Semiconductor Tracker SCT (Semiconductor Tracker) surrounds the Pixel Detector. It uses silicon micro-strip sensors with an average strip pitch of 80 µm assembled back-to-back with a stereo angle of 40 mrad in each layer to measure track coordinates with a resolution of 17 µm in transverse and 580 µm in longitudinal direction. Both the Pixel and the SCT detectors cover the pseudo-rapidity range $|\eta| < 2.5$.

The outermost component of the ID is the TRT. It consists of a 4mm diameter straw drift tubes, made of 35 µm thick Kapton with 31 µm diameter gold-plated tungsten anode wires operated with Xenon/Carbon dioxide/oxygen (70/27/3) gas at 5 to 10 mbar over-pressure. For every track, The TRT provides on average 36 coordinates with a resolution of 130 µm in transverse direction over a pseudo-rapidity range of η=2.
Transition radiation photons from electrons traversing the polypropylene fibres and

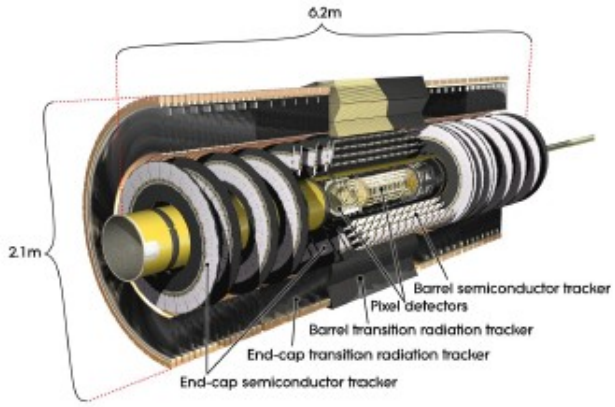


Figure 5: The ATLAS Inner Detector [2].

foils with which the straws are interleaved, ionize the enclosed Xenon gas yielding much larger signals than minimum-ionizing particles and thus providing electron identification. The large number of hits per track allows for robust pattern recognition.

Calorimeter:

The ATLAS calorimeter system consists of electromagnetic and hadronic sampling calorimeters covering the pseudo rapidity range $\eta < 4.9$. The total thickness of the electromagnetic calorimeters is more than 22 radiation lengths. Approximately 11 nuclear interaction length of the whole calorimeter system suffciently reduce the punch-through into the Muon Spectrometer.
The high containment of hadrons together with the large η-coverage enables high jet and missing transverse energy resolution which are crucial for a hadron collider experiment. An overview of the calorimeter system is given in Figure 6.

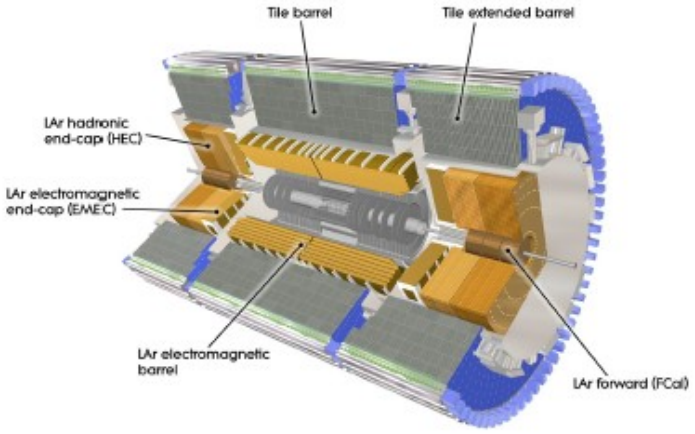


Figure 6: The ATLAS calorimeter system [2].

Electromagnetic Calorimeters:

The electromagnetic calorimeter uses liquid argon (LAr) as active medium and

lead absorber material in a barrel part and two end-cap parts. The barrel part shares the vacuum vessel with the superconducting solenoid magnet it surrounds minimising the amount of dead material which deteriorates the energy resolution. Each end-cap consists of two coaxial wheels. All parts consist of radially accordion-shaped lead absorber plates and Kapton electrodes. The accordion geometry provides homogeneous azimuthal response and electronics connections at the outer diameter. The absorber plate thickness is optimised for energy resolution as a function of η. For $\eta < 2.5$, the electromagnetic calorimeter is segmented into three sections in depth, while in the more forward regions there are only two sections in depth and also the lateral granularity is reduced. In the range $\eta < 1.8$, a highly segmented LAr pre-sampler is used to correct for energy loss upstream of the calorimeter.

Hadronic Calorimeters:

The hadronic calorimeter consists of a barrel and two end-cap parts augmented by a forward calorimeter. The barrel Tile Calorimeter with its extensions uses steel as absorber and scintillating tiles as active medium and covers the ranges $\eta < 1.0$ and $0.8 < \eta < 1.7$, respectively. Both the barrel and the extended barrels are segmented into 64 modules azimuthally and three sections in depth. The scintillating tiles are read out on two sides by photomultiplier tubes via wavelength shifting fibres. The hadronic end-cap LAr calorimeter is located directly behind the electromagnetic end-cap calorimeter and shares the same cryostat.
It consists of two wheels on each side, each consisting of 32 wedge-shaped modules. Copper plates, 25mm thick in the inner and 50mm thick in the outer wheel, are used as absorber material, separated by 8.5mm wide LAr gaps.
The forward calorimeter shares the cryostats with the end-cap calorimeters and covers the range $3.1 < \eta < 4.9$. It is recessed by about 1.2m with respect to the front of the electromagnetic calorimeter in order to reduce neutron albedo into the inner detector. It also utilizes LAr as the active medium and consists of three modules in longitudinal direction. The innermost module enhanced for electromagnetic measurements uses copper absorbers, the other two enhanced for measurements of hadronic interactions use tungsten absorbers. A matrix of longitudinal channels filled with LAr as active medium is embedded into the absorber materials.

The Muon Spectrometer:

The distinctive part of the ATLAS detector is the Muon Spectrometer which defines the overall size of the detector. It has a length of 44m and diameter of 25m. It measures the deflection of muon tracks in the magnetic field generated by large superconducting air-core toroid magnets and is designed to provide a highly efficient muon trigger and high-precision muon momentum measurement up to the TeV scale. It utilizes a position-sensitive detector that records tracks of charged particles, and a magnetic field so that charge and momentum can be recorded from the track curvature. The air-core magnet design minimises the degradation of the momentum resolution due to multiple scattering. An overview of the Muon Spectrometer is given in Figure 7.
The Muon Spectrometer is subdivided into the barrel part ($\eta < 1.4$), where the toroidal magnetic field is provided by the eight 20m long superconducting coils and two end-caps ($1.6 < \eta < 2.7$), where the magnetic field is provided by two separate superconducting toroid magnets. In the transition region between the barrel and

the end-caps ($1.4 < \eta < 1.6$), there is a superposition of the barrel and end-cap toroid fields. While the eight barrel toroid coils are housed in individual cryostats assembled symmetrically around the beam line, the end-cap toroid coils on either side of the detector share a common cryostat. The eight end-cap toroid coils are rotated by 22.5θ with respect to the barrel toroid coils in order to provide radial overlap and improve the bending power in the transition region (see Figure 1.3). The magnetic field is mostly perpendicular to the muon trajectories and provides a bending power in the range from 1 to 7.5 Tm.
Dedicated detectors for precision tracking and triggering are arranged in three cylindrical layers around the beam axis in the barrel and in three wheels in the end-cap regions. The majority of the precision tracking chambers are Monitored Drift Tube (MDT) chambers which are described in detail in the following chapter as they form the framework of this thesis.

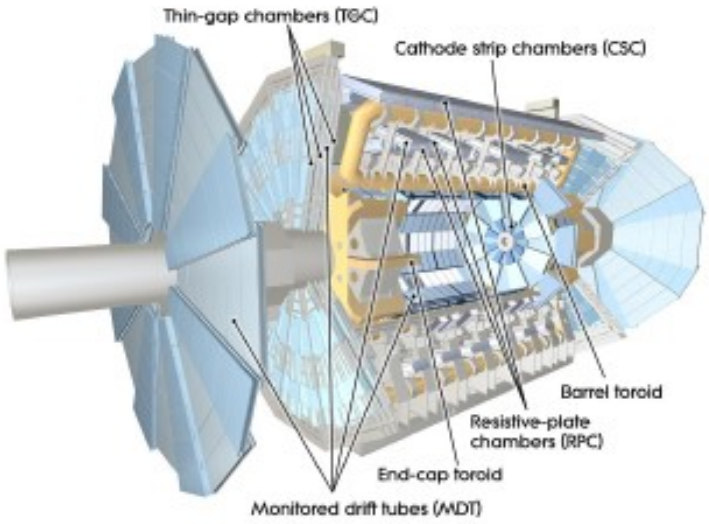


Figure 7: The ATLAS Muon Spectrometer [2].

Only in the inner end-cap layer at large pseudo-rapidity ($2.0 < \eta < 2.7$), where the particle flux is too high for the MDT chambers, Cathode Strip Chambers (CSC) with higher granularity and faster response are used. In total, 1150 MDT chambers with 350 000 drift tubes and 32 CSCs with 31 000 channels cover the pseudorapidity range $\eta < 2.7$. Resistive Plate Chambers (RPC) are used as trigger detectors in the barrel region while. Thin Gap Chambers (TGC) are used in the end-caps. Besides providing a fast trigger decision, the trigger chambers provide bunch crossing identification and measurement of the second coordinates of the muon tracks in the direction of the drift tubes of the MDT chambers. The spatial resolution is only on the order of 1 cm.

1.2.2 Trigger and Data Acquisition System

ATLAS uses a three-level trigger system to minimize the event rate from the 40MHz bunch crossing rate to almost 200 Hz written to tape. The first trigger level (L1) is designed in custom-made electronics. The second (L2) and third (Event Filter)

levels utilizes commercial computer farms. The L1 trigger as shown in Figure 8, takes decisions in a very minute time frame, 2.5µs and reduces the event rate to about 100 kHz. It searches for electrons,high transverse momentum muons, photons, jets and

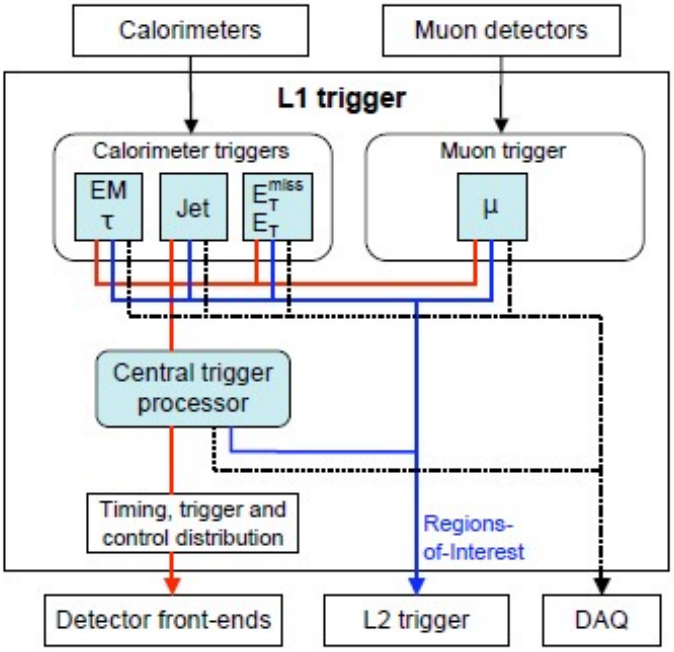


Figure 8: Schematic of the first level (L1) trigger [2].

τ-leptons decaying into hadrons as well as for events with large transverse energy. The L1 decision is taken by the Central Trigger Processor (CTP) which also provides selection criteria like passed thresholds and regions-of-interest (RoI) information to the L2 trigger.
The L2 trigger uses the regions-of-interest information provided by the L1 trigger as a starting point for the processing of the full detector information with simple reconstruction programs within the regions-of-interest. It reduces the event rate to about 3.5 kHz with an average processing time of 40ms.
Finally, the last event selection is performed by the third stage, the "Event Filter", which uses the full ATLAS event reconstruction software. It reduces the event rate to 200 Hz with a typical processing time of four seconds per event. With an average event size of 1.3MB, the average output bandwidth is almost 300MB/s.

1.2.3 Data Taking and Analysis

During the first period of operation from 2010 to 2012, now called Run 1, the LHC has delivered integrated luminosity of L = 5.5 fb^{-1} at a centre-of-mass energy of $\sqrt{s}$ = 7 TeV and of L = 22.8 fb^{-1} at $\sqrt{s}$ = 8 TeV to the ATLAS and CMS experiments [11].
With these recorded sets of data, the Standard Model (SM) of particle physics has been confirmed in the new energy regime culminating in the discovery of the last missing SM particle, the Higgs boson, in 2012 [4, 5] with a mass of mH ≈ 125.5 GeV [12, 13] and rate compatible with the SM prediction.

Researchers have searched alot but no evidence for physics beyond the Standard Model could be confirmed in first period of operation. Second Run of ATLAS experiment is happening at increased centre-ofmass energy of 13 TeV and the search for Physics beyond the standard model is still in process.
An increase of the integrated luminosity is desirable,, not only to discover new physics, but also to study the still open questions of the Standard Model like the naturalness or hierarchy problems or the origins of dark matter and of the matter–antimatter asymmetry

Figure 9: CERN LHC and HL-LHC schedule [15].

1.3 Towards Higher Luminosity

1.3.1 LHC Upgrade

During Run 2, which was planned to last from mid 2015 to mid 2018, the LHC reached its target the design luminosity and energy. After the so-called Phase-I upgrades of the LHC with improvements to the injectors including a new linear accelerator LINAC4 [14] replacing the current LINAC2, the instantaneous luminosity is be doubled to 2.10^{34} cm^{-2} s^{-1}. In this configuration, the LHC will be operated until 2023 and deliver at least 300 fb^{-1} of proton–proton collisions to the ATLAS and CMS experiments.
After Phase-II upgrades from 2023 to 2025, the LHC will reach an instantaneous luminosity of 7.10^{34} cm^{-2} s^{-1} (High-Luminosity LHC or HL-LHC) and deliver 3000 fb^{-1} within the following ten years.

1.3.2 ATLAS Upgrade Projects

With the increase of the instantaneous luminosity beyond the design value and extended running time, the LHC experiments need to adjust with the higher demands on rate capability, particle multiplicities, radiation hardness and trigger selectivity in order to take advantage of the higher luminosity.
This section gives an overview of planned ATLAS upgrade projects in the coming decade. The goal of the upgrades is to at least maintain and even improve upon the design performance at the higher luminosity.

Detector Consolidation Phase-0 The biggest upgrade project during the first long LHC shutdown (2013–2014) was the installation of the "Insertable β-Layer"

(IBL), a fourth layer added inside the present pixel detector on a new beam pipe [16]. The IBL enhances the decay vertex reconstruction and hence the b-hadron and τ-lepton identification and compensates for deterioration of present pixel detector due to radiation damage.
Another significant upgrade project is the installation of additional muon tracking chambers to improve the momentum resolution in a so far poorly instrumented region of the barrel Muon Spectrometer [17]. A new type of smaller diameter drift tube (sMDT) chambers is used.

Phase-I Upgrades The Phase-I upgrades of the Muon Spectrometer in 2018–2019, Figure 9, anticipate necessary improvements for HL-LHC [18]. The main project was the replacement of the inner end-cap layer of the Muon Spectrometer, the so-called Small Wheel, by the New Small Wheel (NSW) using detector technologies with higher rate capability and spatial trigger detector resolution [19].

Phase-II Upgrades The Phase-II upgrades are planned for 2022–2024 which will enable efficient operation at HL-LHC conditions for additional ten years to collect collision data corresponding to 3000 fb^{-1} [20].
Entire replacement of the inner tracking detector, which reaches the end of its lifetime after 400 fb^{-1}, is required. The new tracker has to deal with a much higher track multiplicity from up to 200 interactions per bunch crossing and tolerate more than an order of magnitude higher radiation doses.
To limit the trigger rate without missing interesting events, the selectivity of the L2 trigger has to be reached already at L1. With trigger latencies above 30 µs, inner detector track reconstruction information can be incorporated into the L1 trigger and combined with more complex calorimeter and muon triggers [21]. The low-momentum muon trigger rate can be suppressed by higher momentum resolution of the L1 muon trigger using the high spatial resolution of the MDT chambers [22, 23].

1.4 Electronic for the physical experiments

The most important discoveries on the matter components has been developed in the CERN laboratory at Geneva exploiting the world's largest and most powerful particle accelerator, known as Large Hadron Collider (LHC). The collider takes time in range of nanoseconds to create high-energy proton-proton collisions at speeds close to light speed.
Two opposite beams are accelerated in a ring with superconducting magnets and accelerating structures. The temperature of the system is very low (around 271.3 °C) limiting the loss energy and conductivity. For this reason, the accelerator temperature is controlled by distribution system of liquid helium [1].
Groups of physics and engineering collaborate with the main goal to organize overall experiments, from events generation and detection up to the final data analysis. Different detectors interface with the LHC to analyze the particles produced by the collisions. They are organized in a shell-structure and each of them is able to detect a specific range of charged particles. For each detectors, there is an associated experiment. ATLAS (A Toroidal Lhc ApparatuS) and CMS (Compact Muon Solenoid) are the biggest ones because they investigate the large range of physics particles. The first is thought to posses information about experiments happening

up to 14 TeV energy. CMS experiment is very useful for Standard Model studying, including Higgs bosons, muons, photons and electrons. Both of these experiments contributed in the discovery of the Higgs Boson particle, in 2012, and are further utilized to investigate other particles that could make up dark matter.
Physics experiments without electronic control doesn't exist. In the years, detectors and search methodology of the particles have been developed with the main target to search for more particles and understand the existing particles more clearly. At the same time, this advancement implied a major attention on the electronic parts, on their efficiency and reliability. These requirements led to replace an electronics based on discrete components with integrated circuits, because of the remarkable advantages. The costs have been drastically reduced although a different number of prototype must be produced before to have optimal performance. CMOS technology allows designing mixed-signal circuits, named ASIC, able to work in different worlds, i.e. digital and analog. A high performance analog part is closer to a dense digital logic with considerable benefits of efficiency for unit of area and driving. Integrating a complete mixed-signal circuit in a die, interface and load managing issues are reduced. The ASIC development depends on scaling down technology. Performance, sizing, resolution and number of components, integrable in the same, area are substantially increased with more work by electronic designers.

1.4.1 State Of The Art MDT AFE

As a result of the proton-proton collision, at center-of-mass energies of up to 14 TeV, some charged and neutral particles are generated. Muons are the most penetrating charged particles emerging from proton–proton collisions. In order to determine the energy and direction of the secondary particles emerging from the collision, readout electronics are utilized.
The actually mounted state-of-the-art MDT readout circuit is realized in a 130nm CMOS technology[24,25,26], and operates from a single 3.3V supply voltage. It performs a charge-to-voltage conversion by a Charge-Sensitive-Preamplifier (CSP). The CSP is followed by a three stage shaper design to implement Bipolar shaping scheme is chosen to avoid deterioration of efficiency due to baseline fluctuations due to high signal rates in MDT chambers (up to 400 kHz/tube). A pre-discriminator is also attached to adjust the analog channel sensitivity (that is voltage output for an input charge pulse) at the input of discriminator. The analog channel is followed by a Discriminator and WADC (Wilkinson ADC) to perform Analog to Digital conversion. Two modes of operations are provided:

- Time over Threshold (ToT) mode: The length of the Discriminator output corresponds to the time of the input signal above threshold and encodes information about input charge.
- WADC mode: The length of the circuit output corresponds to the charge, contained in a time window of 8-16 ns after threshold crossing which represents an approximate measure of the peak amplitude of the incoming signal.

The channel can be programmed by the external FPGA board, before operating, to operate in wither ToT mode or WADC mode. In ToT mode the rising edge of signal represents the charge arrival time where as the length of the signal gives information the amount of charge being arrived.The Wilkinson ADC (WADC) [26] performs an

approximate measurement of the amplitude, by charging and discharging the holding capacitor, of the incoming signal in the time window shortly after the signal was triggering the discriminator. Knowing this amplitude allows for a correction of the raw trigger time for time slewing and in addition it also provides diagnostics for monitoring the gas gain of the chamber. To suppress multiple threshold crossings for a single track passing a tube, a "dead time" (DT) is introduced, disabling the discriminator for a programmable time after a threshold crossing. The Dead-Time can be selected in the range 150-750 ns.
For a 60pF detector capacitance, classical readout electronics (ASD) features a sensitivity of 8.9mV/fC at the output of Analog chain, 15ns nominal Peaking Time Delay (i.e. PTD, the front-end capability to quickly detect charge arrival time) and low-noise enabling 5fC minimum detected charge at 10dB Signal-to-Noise-Ratio (i.e. SNR).
In the process of renewing the MDT readout electronics, one of the main objectives is to make a significant low-power and area-efficient design using long-term sustainable technology, along with achieving all the functional parameters of MDT-ASD [24,25,26].
This Thesis presents a new readout electronics circuit designed in 65nm CMOS technology, highly optimized in terms of area and power efficiency along with achieving the same performance. The power consuming components are identified and are carefully designed by selecting the right topology and design parameters to minimize the power consumption without deteriorating the performance parameters. The design incorporates a two-stage shaper to implement bipolar shaping of the input signal. This design has a single mode of operation, time over- threshold. The W-ADC mode, used for signal charge measurement and time-slewing corrections in the reference model, has become unnecessary due to the larger gain observed at the unchanged input-referred noise level of the new-generation chips, so it has been eliminated. To avoid bulky capacitors, as used in the three-stage shaper of the previous design, the sizing of passive components has been optimized to minimize RC component sizes, resulting in a 4x area shrinking factor in the shaper stage w.r.t. to the previous design. SLVS drivers have been designed to provide an interface for the FEE system to TDC, which is the subsequent stage of the readout chain.

2 Chapter 2: FEE Design Overview

2.1 Front End Electronics Design

High-Energy-Physics (HEP) experiments developed in the last decades [27]-[28]-[29]-[30] target to describe the high energy particle interactions.
The main target of High-Luminosity Large-Hadron-Collider (LH-LHC) ATLAS experiments is to search the elementary particle of the Standard Model, studying a broad spectrum of physics processes, and to study physics beyond the Standard Model. For this purpose, it requires a complex detection system as that shown in Figure 10.
According to [33] [34], muons measurement uses two completely independent systems called Inner Tracker and Muon Spectrometer [35]. The Inner Tracker is surrounded by a superconducting coil which generates a magnetic field parallel to the beam axis where there are three different sensor systems. It performs the measurements of direction, momentum and charge of electrically charged particles produced in each proton-proton (p-p) collision. The muons emerging from the primary collision, being the most penetrating charge particle component, are able to transverse the Calorimeters and to reach the Muon spectrometer, the outermost shell of the ATLAS detector. The Muon Spectrometer (MS) surrounds the calorimeters and consists of three large air-core superconducting magnets providing a toroidal field (each with eight coils); a system of precision tracking chambers and fast detectors.
A proper readout electronic circuit is designed for each part to detect and record the useful information. This chapter, presents a read-out front-end, dedicated to the Monitored Drift Tube (MDT) chambers.

The MDT chambers are the main components of the precision tracking system [32]. The tubes have 29.970mm of diameter and they are organized in six layers arranged [36], a cross section of MDT tube is shown in Figure 11. They are connected to electronics containing the readout electronics as represented in Figure 12. An impedance matching network avoids reflections and losses of charge detected. About that, each wire operates with Ar/CO2 gas (93/7) at 3 bar and it is terminated with the equivalent transmission line impedance of the tube (383). In addition, all contacts between the chamber and the hedgehog board are gold plated to ensure a long-term connectivity.
A section of the MDT tube is reported in figure 12. Electrons generated by muons in the gas-filled pressurized MDT tubes are drifted to the central wire of the tube, where their time-of-arrival is used to determine the distance of the track from the wire (RMIN in Figure 11). The main operating parameters of the MDT are summarized in Table 2.

As the muon usually passes through a large number of drift tubes, the position of the muon track can be reconstructed from a combination of measurements in the tubes along the muon trajectory. The specific details on ATLAS experiment and setup can be found in [36]. Considering a simplified MDT readout scheme (Figure 12), the small charge signals, coming from the wires, are sent to the 'mezzanine board' where the readout circuit is placed. Each 'mezzanine board' contains 24 channels organized in 3 Octal groups and it is connected to a single 24-channel Time-to-Digital Converter (TDC) and to a proper control circuitry [19].

The monolithic readout chip senses, shapes and converts the signal coming from the tubes, providing time-domain voltage pulses, whose duty cycle is proportional

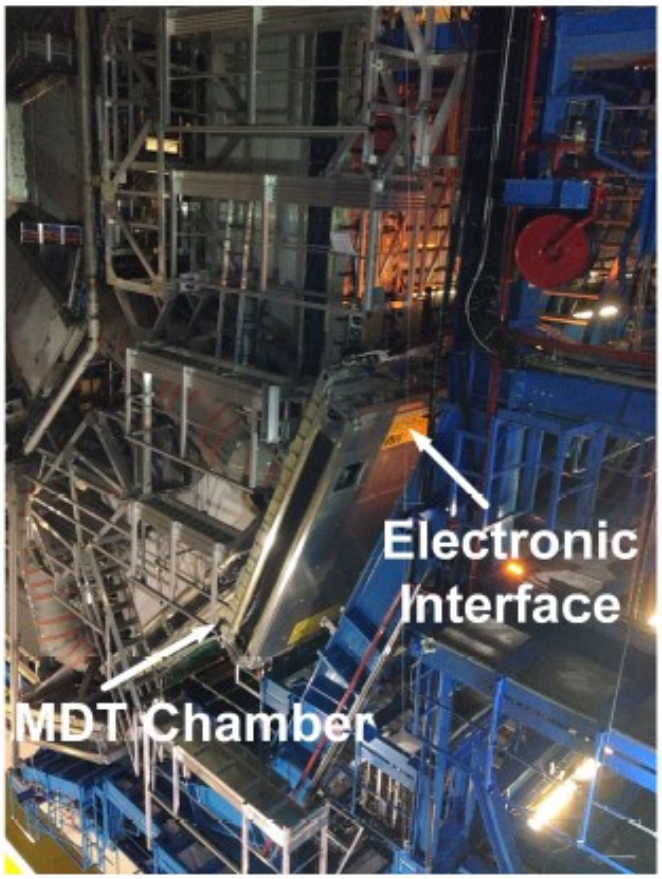


Figure 10: Photo of ATLAS Detection System[2].

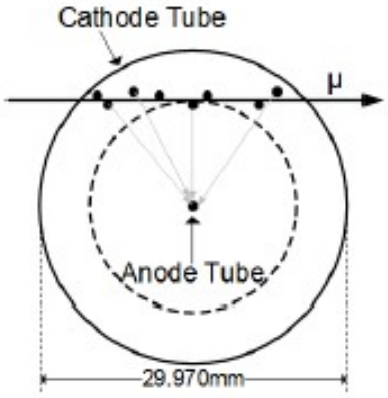


Figure 11: Section of MDT tube.

to the amount of charge at the circuit input. The output signal of the discriminator is triggered when the voltage pulse crosses a programable predefined and adjustable threshold, and is subsequently sent to an, off-chip, TDC, which forwards the recorded information to data acquisition chain for recording and track reconstruction.
Before moving on to analyze the most important requirements for MDT read-out channel, it is important to point out that the choice of the ionizing gas has been done for its favorable aging properties in the LHC environment [19]. Unfortunately, it is

Table 2: Operating parameters of MDT chambers with large and small tubes.

Parameter	**Large Tubes**	**Small Tubes**
Length	1.5 to 6 m	1.5 to 2.50 m
Diameter	30 mm	15 mm
Wire diameter	50 um	idem
Wire resistance	44 Ω	idem
Impedance	380 Ω	340 Ω
Termination	380 Ω in series with 470 pF	340 Ω with 470 pF
AC coupling	470 pF	idem
Drift gas	Ar/CO2 (93%/7%)	idem
Maximum hit rate	500 Hz/cm2	30 kHz/cm2
Nominal operating voltage	3000 V	2730 V
Electron avg. drift velocity	20 m/ns	42 m/ns
Maximum drift time	750 ns	180 ns

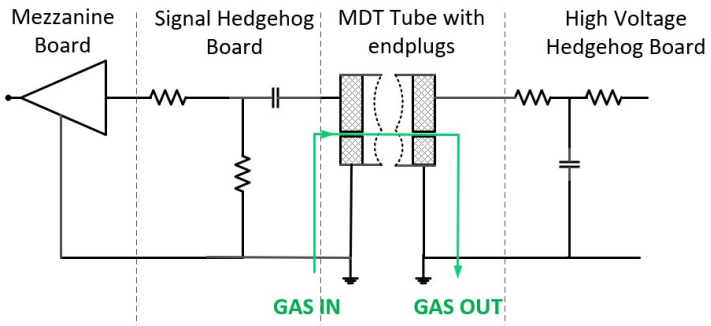


Figure 12: Simplified Scheme of Muons Detection system[32].

a non-linear drift gas and from this situation results difficult track reconstruction solving with a programmable dead-time up to the total drift time.

2.2 Channel Architecture

The FEE65nm is a four channel CMOS design which has been optimized for the ATLAS MDT chambers. It is an advance version of ASD130nm [24,25] which is an Ultra-Low-power and area efficient design, in a long sustainable technology, with the same performance parameters as the reference design. The efficiency is achieved by optimizing the architecture of every block of its precedent model without effecting the performance parameters. It has a single Mode of operation, Time-Over-Threshold, eliminating W-ADC Mode which performs an approximate measurement of the amplitude of the incoming signal in the time window shortly after the signal was triggering the discriminator. Time-Over-Threshold measurement gives us enough information to know the charge arrival time and the amount of charge being detected as a result of proton-proton collision.
For the CSP, a large bandwidth, single-ended two stage amplifier is used. Since the input signal comes from a single source, the single ended topology is utilized keeping in view its power efficiency benefits as compared to fully differential topology. The three-stage shaper of ASD130nm, utilized to implement the bipolar shaping

scheme, is replaced by a differential two-stage design and the Pre-Discriminator stage is eliminated. The bipolar shaping scheme is implemented to avoid baseline variation error.

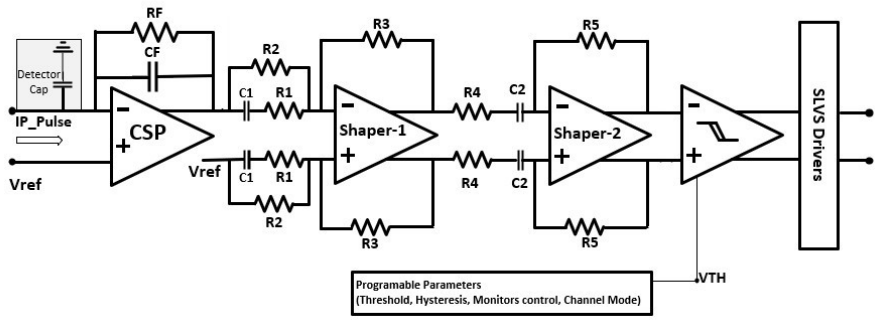


Figure 13: ASD Single Channel Schematic.

Each channel, as shown in Figure 13, consists of a single ended Charge Sensitive Preamplifier (CSP) and differential two stage shaper (SH1-SH3), to implement bipolar shaping, followed by a discriminator. The discriminator compares the incoming signal to a programable threshold value and output a digital pulse.
The CSP amplifies the input charge, generating an amplified voltage signal which is further amplified and shaped in the Shaper stages. The conversion of Analog chain from single ended to differential, in Analog channel, is for the purpose of Noise immunity and high-power supply rejection ratio while bipolar shaping is selected to reduce the effects of baseline shift at high signal rates [37][38][39]. Negative terminal of CSP is connected to the signal source of the MDT tube (i.e. the central wire), while the positive one is fixed with an internal resistor divider to a proper bias voltage. A capacitor of up to 60pF is attached to negative terminal, assuming the parasitic capacitance.
For each of the four channels, the output of the shaper stage is fed directly into the discriminator stage, unlike the previous design in which the output was fed into pre-discriminator stage and W-ADC. The discriminator stage compares the output of shaper with a programmable threshold (DISC1 threshold). At the moment of threshold crossing, the (digital) outputs of a discriminator change polarity, going from LOW to HIGH, thus defining the "leading edge" of the ASD output. This leading edge corresponds to arrival time of charge. Whereas the width of the Digital output gives a time measurement of the amount of charge being arrived.
For storing and processing the digital content (binary word to program the chip) of design, a novel design is used for shift registers. Unit cells based on parallel arrays of Serial-In-Parallel-Out (SIPO) and Parallel-In-Serial-Out (PISO) blocks are used to confirm the correctness of data loaded to design.
At the output the FEE65nm the output is available as both, low voltage differential signal, with a voltage swing from 200mV to -200mV , and digital CMOS Level signal, with high level as 1.2V and low level with 0V.

2.3 Analog Chain

Overall FEE65nm is a mixed signal design, comprising of both Analog and Digital section. The Analog section of the design consists of Preamplifier and two stage Shaper. The negative input of the CSP (Figure-13) is connected to the signal source of the MDT tube, that is, the central wire. The CSP amplifies the input charge, generating a proportional voltage signal which is amplified and shaped in the subsequent stages whereas the two-stage shaper implements the Bipolar shaping.

2.3.1 Charge Sensitive Preamplifier

The Charge Sensitive Preamplifier, shown in Figure 14, is the first stage of Analog Chain. It is designed using two-stage amplifier topology as shown in Figure 15. The input signal is attached to the negative terminal of CSP. A capacitor of 60pF, assuming the detector capacitance, is attached to this node. The positive input has been fixed by a resistor divider (Rb1 and Rb2) to 700 mV, generated on chip. To suppress the substrate noise, a capacitor of 16pF is attached to the positive terminal on Board.

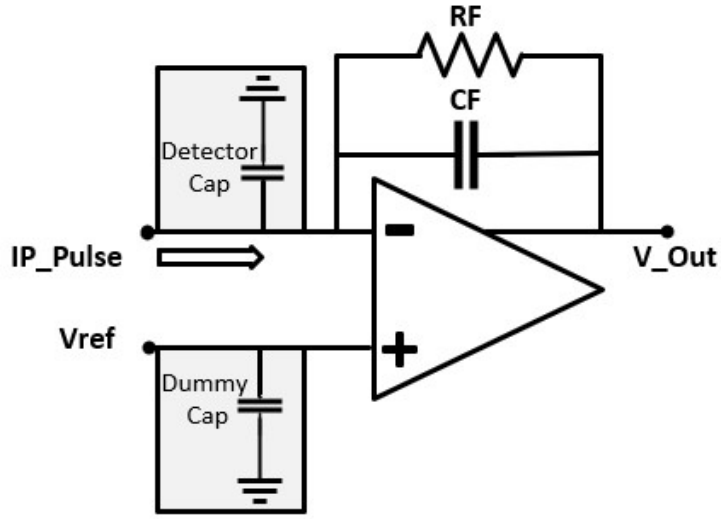


Figure 14: Scheme of a Charge Sensitive Preamplifier.

CSP design is very critical as it defines allot of key functional parameters of the system. Performance and functional specifications such as signal rise-time, overall power consumption, noise, is largely defined by this block. Along with the high specification criteria, the performance of this block is adversely affected by very large value of CD, parasitic capacitance, due to the PCB parasitic and the long wires of connection between the ASD and the tubes. This high parasitic capacitance affects the closed-loop-gain bandwidth, sensitivity, and signal rise time of the CSP. Key design parameters for CSP performance are minimum noise generation, minimum power consumption and high rise-time. To achieve these specifications, it is designed with a very high trans-conductance value of 25mA/V for input Mosfets.

This is in accordance to target the design for minimum noise generation. This technique however has a trade-off of an increase in power consumption as high the transconductance is, more is the current it consumes. The currents IA+IB, IC

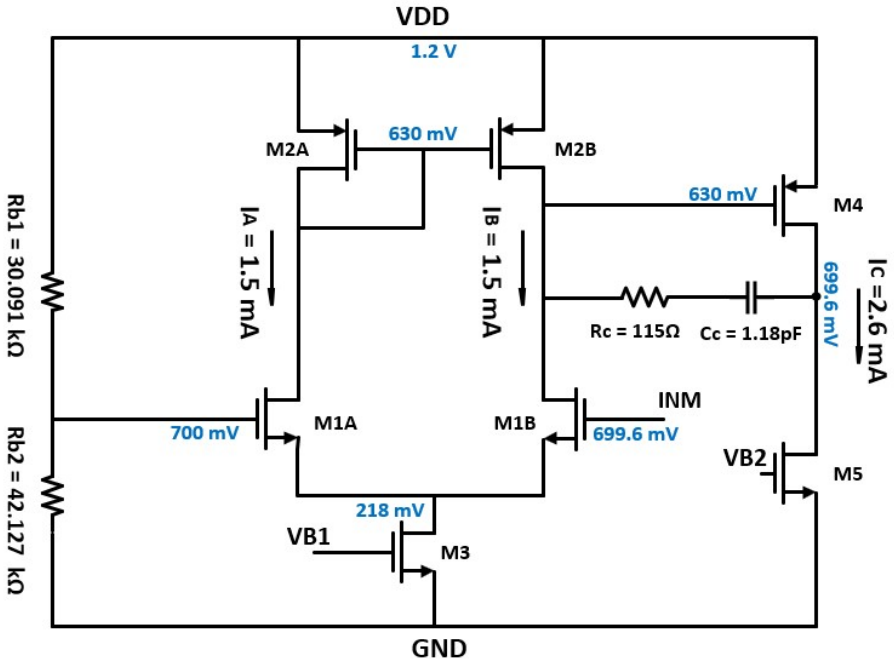


Figure 15: Scheme of OpAmp used.

shown in Figure 15, are implemented through a current mirror from a reference current source. To compensate for the excessive power consumption, first very large size mosfets, W/L = 580u/330nm, are used and are operated in sub-threshold region. Along with that, as the input comes from a single source (Anode wire of Tube) a single ended topology is used and hence saving a current of 2.7mA in the outer stage of amplifier and eliminating the use of common-mode feedback circuit, in like-manner. Apart from this, the overall stages in design are reduced to make it an Ultra-Low-Power design. To make the CSP faster, as requirement for high rise-time, the OP-Amp is designed with a very high gain bandwidth 0f 2.4GHz with a phase margin of 60 degree, ensuring good stability of CSP. With these open loop characteristics, the CSP shows a very fast peaking time of 4ns without the detector capacitor and 10.5ns with the large (60pF) detector capacitor. The values of currents, voltages, dimensions of passive/active components are reported in Figure 15 and in Table 3. The load impedance of CSP stage is the input impedance of Shaper-1 and 2. It is, a parallel combination of a Resistor, Rs1 with a series of Resistor and Capacitor, Rs2 and C1 respectively, shown in Figure-13. The CSP transfer function depends on the feedback network (parallel network of RF and CF), the transconductance of the input transistor (M1AB), the output impedance (ZL) and the detector capacitance (CD). It can be approximated by:

$$T(s) = \left(\frac{-R_F(1 - \frac{sC_F}{gm_{M1}})}{(1 + sC_F R_F(1 + \frac{C_D}{C_F}\frac{1}{gm_{M1}Z_L}))} \right) \tag{1}$$

Similarly, the input impedance transfer function is approximately given by Eq. 2:

$$Zin = \left(\frac{T(s)}{gm_1 Z_L} \right) \tag{2}$$

It is almost constant (ZIN 44) at low frequencies and below 63 all in-band frequencies.

Table 3: CSP W/L and Trans-conductance value.

MOS	W/L	Gm
M1A	580um/330nm	25mA/V
M1B	580um/330nm	25mA/V
M2A	340um/200nm	19mA/V
M2A	340um/200nm	19mA/V
M3	180um/200nm	31.45mA/V
M4	600um/200nm	33mA/V
M5	30um/200nm	27.4mA/V

2.3.2 Shaper

The Preamplifier stage is followed by a two-stage shaper, Figure 16-17, to implement bipolar shaping of pulse, to avoid deterioration of efficiency due to baseline fluctuations. Each stage of shaper is based on two stage fully differential amplifiers as shown in Figure-18.

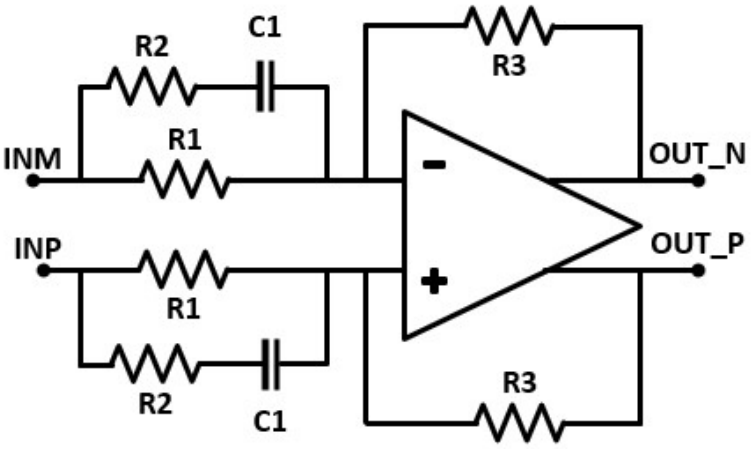


Figure 16: Shaper 1.

The choice of two stage differential topology is due to the reason of being more robust to load and high output swing. Since we are operating from a 1.2V supply now, two stage topology is the best choice to achieve a maximum linear qwing at the output of shaper. The transconductance value of Input mosfets is 2.5mA/V and it consumes a current of 104uA in each of inner stage, Ia Ib, and 418uA in each of outer stage as shown in Figure 18. The Outer stage mosfets are designed with an overdrive voltage of less than 100mV to have the maximum linear sensitivity, for full range of input charge up to 100fC. To set the common mode feedback voltage a separate common-mode-feedback CMFB network is designed whose W/L value is half as that of main amplifier input stage, to save current consumption. The CMFB network is attached to main amplifier through a common-mode level sensing network, consisting

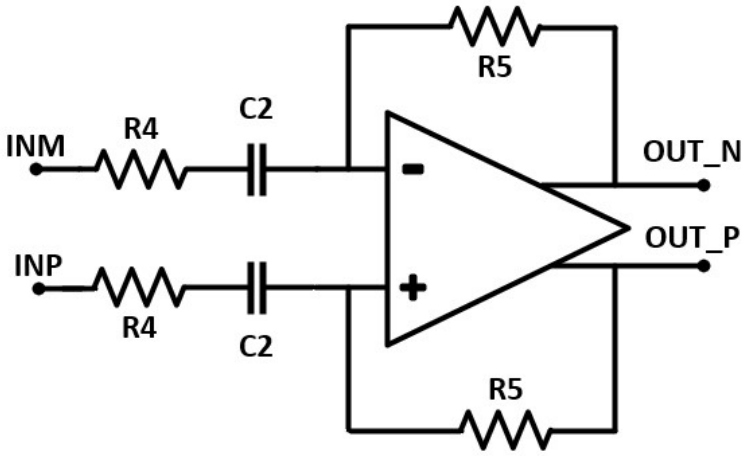


Figure 17: Shaper 2.

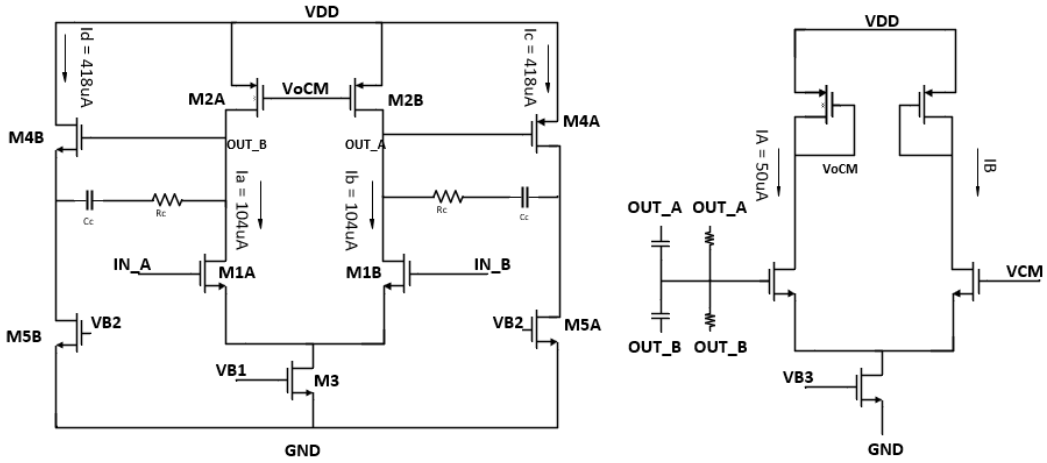


Figure 18: Scheme of OpAmp used.

of a pair of resistors with capacitor in parallel for better performance at higher frequency.

Each stage of the shaper (shaper 1–2) has an input impedance network and a resistive feedback loop, as shown in Figure [16,17]. The poles and zeroes used to implement the bipolar shaping are the same as in ASD130 [24,25,26], selected to cancel the very long time constant component of the positive ion MDT pulse, however, the values Z-RC are greatly changed, shrunk by almost a factor of four, with the aim of an area-efficient design. The values of impedance network components are given in Table 4.
The transfer function of each shaper stage depends on the input impedance and feedback network. Equations (3) and (4) show the transfer function of shaper-1 and shaper-2, respectively.

$$T(s) = \frac{R3}{R1}\left(\frac{1 + sC_1(R_1 + R_2)}{1 + sC_1R_2}\right) \tag{3}$$

$$T(s) = \left(\frac{sC_2R_5}{1 + sC_2R_4} \right) \tag{4}$$

Table 4: Shaper Impedance Network components value.

Stage	Component	Value
Shaper-1	R1	9.8 kΩ
Shaper-1	C1	10.2 pF
Shaper-1	R2	10.1 kΩ
Shaper-1	R3	9.8 kΩ
Shaper-2	R4	9.8 kΩ
Shaper-2	C2	11.5 pF
Shaper-2	R5	37.8 kΩ

2.3.3 Discriminator

The Bipolar output signal of Analog Chain is passed into comparator stage where it is compared with a threshold value. Coupling capacitors are utilized to separate the discriminator from the Analog section
The comparator is designed using two stage single ended amplifier topology, without compensation as shown in Figure 19. It is a high gain amplification stage, followed by a series of inverters to give the output as High or Low depending on input signal and threshold value.
Transient noise is always present in CMOS design and causes fluctuation when it comes to threshold crossing. For this reason a Hysteresis Block is added to comparator to unbalance the current in main differential amplifier by a programmable value. Its significance is to remove glitches in the output of comparator because of noise. The hysteresis can be varied from 0 - 50mV using 3-bit programmable code and can be set into eight different values in range of 0-50 mV.

The Threshold value for main comparator is set deferentially, i.e varying the baseline voltage at both terminals of comparator by same amount, across the baseline voltage of the channel. Two sets of 8-Bit string DAC and 3-To-8 bit Decoders are used to set the threshold values which are programable up to 256mV across the common mode voltage with LSB of 2mV. String DAC is a collection of resistors in series, acting as voltage divider circuit, with switching points or tap nodes between each of the resistors. Each string-DAC is composed of main string and sub-string to divide the reference voltage and give output voltage with LSB of 1mV. Complementary switches are designed for selecting required output voltage to set threshold value.

2.3.4 SLVS Driver

Modern experiments in high-energy physics contain a huge number of data processing events in channels. Therefore, reducing power consumption and increasing data transmission speed of each individual front-end ASIC is an important task.
The front-end electronics aim to achieve high levels of performance in terms of resolution and accuracy. This performance is limited by the system intrinsic noise,

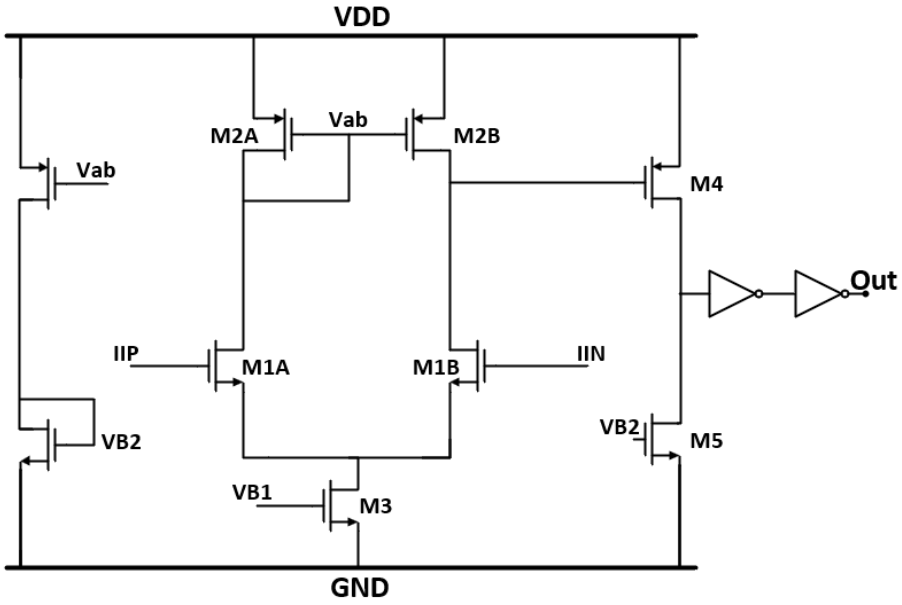


Figure 19: Scheme of OpAmp used.

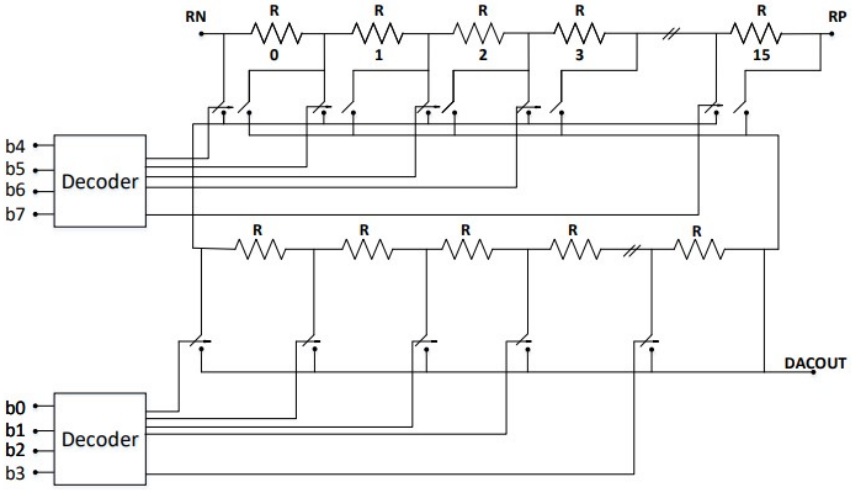


Figure 20: String DAC and Decoder.

therefore electrical links should be designed to minimize cross-talk and power supply noise. For these reasons, using a low-power, low-voltage-swing signaling standards become a very popular in particle physics applications in recent years.
Since a low-power, low-voltage-swing signaling standards is very important in particle physics, for these reasons along with CMOS level signal at output for testing purpose, SLVS driver is designed. The SLVS standard is defined in [40] and describes a differential current-steering electrical protocol with a voltage swing of 200 mV on a 100 load and a common mode of 200 mV. The differential voltage is therefore 400 mV. The output current is 2 mA, with a power consumption at the load of 0.4 mW.

Block diagram of SLVS driver is presented in Figure-21, this is composed of a

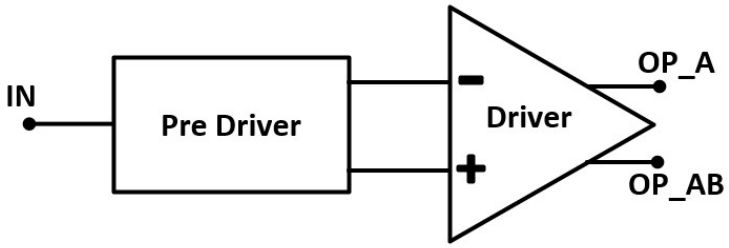


Figure 21: SLVS Block Diagram.

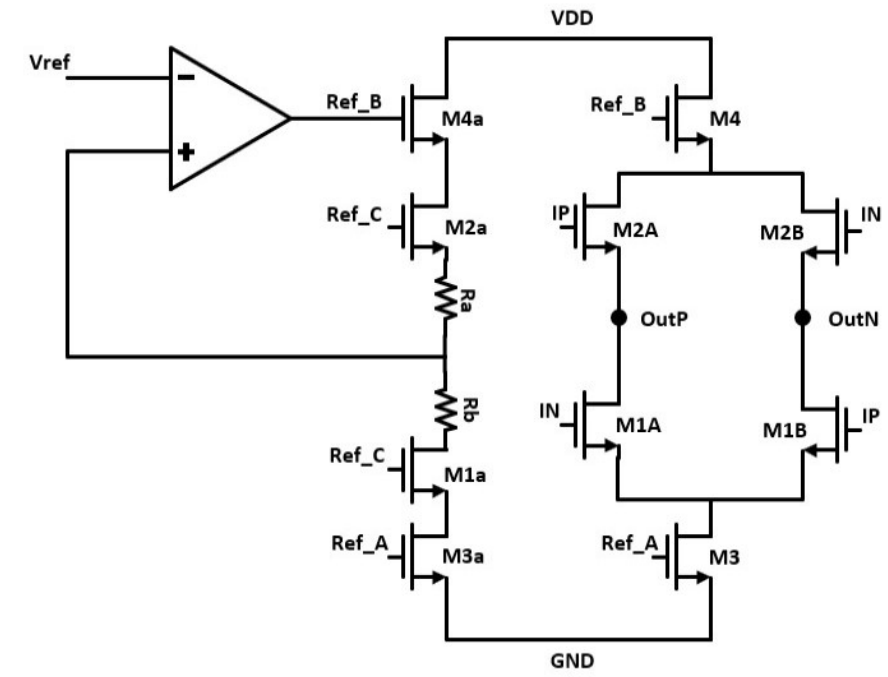


Figure 22: SLVS Transistor Schematic.

pre-driver and a transmitter (Tx). The pre-driver takes the input from the comparator and convert it into differential signals with opposite phase. A typical SLVS transmitter operates as a current source with switched polarity [41,42]. The output current flows through the load resistance, external to chip, establishing the correct differential output voltage swing. The proposed transmitter circuit, presented in Figure-22, uses the configuration with four MOS switches in H-Bridge configuration, implemented with the M1-M2(AB) NMOS transistors. The operation of this circuit is described in the following. When M1A and M2B transistors are switched on, the polarity of the output current is positive together with the differential output voltage. On the contrary, when M1B and M2A transistors are switched off, the polarity of the output current and voltage is reversed.

2.4 Programmable Functional Parameters

For proper functioning of FEE65nm chip, some functional parameters can be setup or vary in pre-run time. It includes threshold voltage, hysteresis control, channel mode control. A 55-bit digital word is transmitted to the chip using a simplified JTAG protocol, serial interface, based on a chain of register, transmits the word code to its target block in the chip. Table 5 gives a summary of the Programmable parameters together with the number of bits, corresponding range, and resolution/LSB. Programmable parameters manage channel/chip operation and functioning.

Table 5: Programable Parameter of FEE Chip.

Parameter	**Range**	**Unit**
Disc Threshold	-255 to 255	mv
Disc Hysteresis	0 – 50	mV
Dead Time	50 – 500	ns
Channel Mode	HI, ON, LOW	

Discriminator control:

The Discriminator Stage compares the output of Analog Section with a threshold voltage (VTH) and uses a hysteresis to avoid multiple threshold crossings due to noise.
VTH is applied at the AC coupled input of the Discriminator stage and is generated by two complementary 8-bit String resistor DACs. By setting the reference voltage, two mirror voltages are generated across the common mode voltage to establish the threshold voltage. The final differential output threshold can vary from – 255 mV to + 255 mV with an LSB of 2 mV.

Hysteresis control:

It was demonstrated that the option of a wide-range adjustable hysteresis for the timing discriminator is a useful feature to reduce the probability of multiple threshold crossings in the tail of the MDT signal[37,38].
It also improves the system reliability by removing ambivalent output states of the comparator due to signals or signal fluctuations close to the threshold level. Hysteresis is applied through a scaled-transistor current source with a resolution of 3 bits. The range of the hysteresis is 0 - 50mV variation.

Channel Mode:

For diagnostic purpose, to check if the channel is working or no, it is be useful to force the SLVS output to a logic HIGH or LOW. One of the following channel operation modes can be selected:

- ON MODE: default working setting; the output depends on input signal;.
- HI MODE: the output is forced to HIGH or ‘Logic 1’.
- LO MODE: the output is forced to LOW or ‘Logic 0’.

Dead Time:

Dead Time is the time interval in which any threshold crossing of discriminator will not produce any output. It is the time between the leading edge of one output to the leading edge of consecutive next output.
This feature of the chip allows to suppress multiple threshold crossings. This time interval is controlled by a 4-bit digital code. DT circuit is made up of a series of RC Delay elements with controlled switches, thus able to produce configurable deadtime interval once activated by the edge of TOT output. Selectable range of deadtime is from 50ns to 500ns in steps of 30ns. Figure-20 presents the response of dead time vs. 4-bit code.
The deadtime window is added to the output pulse, thus a minimum deadtime is always present (the time of the output pulse itself).

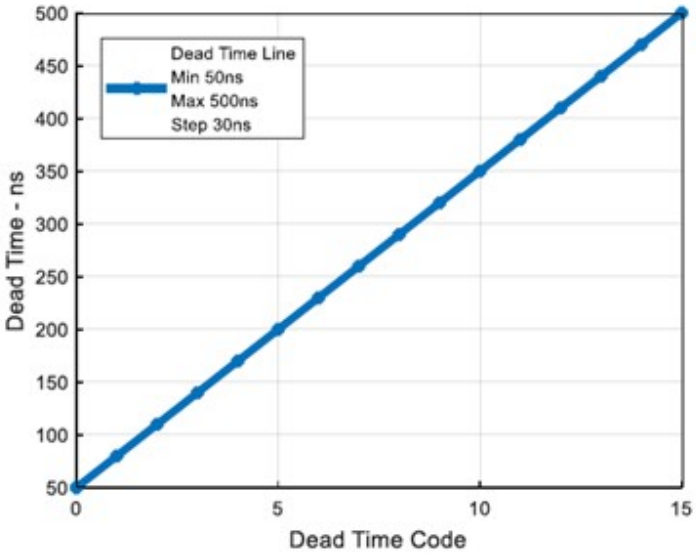


Figure 23: Dead Time VS Dead Time code

2.5 Serial data I/O and programmable parameters

It was found advantageous to be able to control or tune certain analog and functional parameters of the MDT-ASD, both at power-up/reset and during run time. Rather than applying external currents or voltages, it was chosen to send the control signals as digital data to the chip, where they are converted into physical quantities by custom Digital-to-Analog Converters (DACs) as required. A serial I/O data interface was implemented in the circuit, containing digital I/O ports, shift registers and the required control logic. The data as well as the control signals and the shift register clock are generated by an FPGA off the chip and are transmitted to the chip using a JTAG like protocol.

ASD serial data interface The selected FEE serial data interface architecture utilizes separate shift and working registers. The shift register is connected directly to digital input and output pads respectively. Its length is designed to hold a complete set of control bits (55). The data can be uploaded any time to the

shadow registers, which control the DACs, multiplexers etc. The architecture allows downloading the whole set of active bits from the shadow to the shift register in order to send them back to the controller for diagnostic or monitoring purposes. This can be done any time and does not interfere with the normal operation of the chip.
The interface, for each data bit, consists of the shift register-cell, implemented as a static master-slave D flip flop. And a shadow register cell, realized as a static transparent latch and also 2 two-in-one multiplexers as shown in Figure 24.
The protocol requires 2 data lines (TO and FROM chip), 3 control lines (LOAD, HOLD, DOWN) and one clock line as shown in Table 6. The configuration allows extensive control over the data flow.

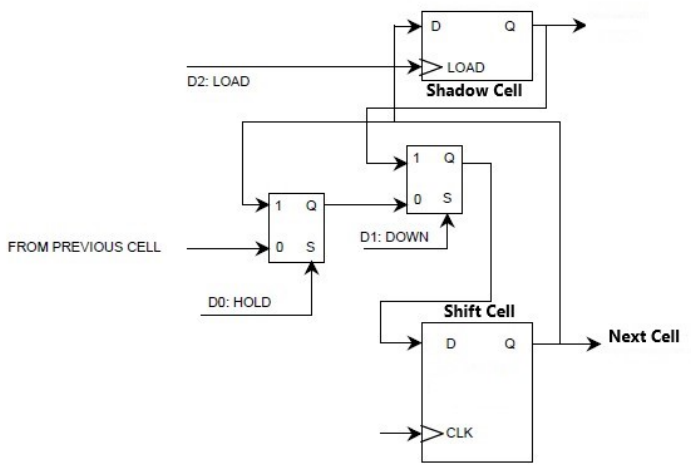


Figure 24: Serial Data Interface

- HOLD mode keeps the data in the shift register by feeding back each cell with its own content.
- SHIFT mode shifts data right at the rising edge of the clock. LOAD active copies the bits in the shift register to the shadow register at any time (asynchronous).
- DOWN active copies the contents of the shadow registers to the shift register at the next rising clock edge (overrides SHIFT - HOLD).

The FEE serial input expects the data to be stable at the rising edge of the clock. The circuit will change data bits at the falling clock-edge. Thus data are stable at the input for the entire clock period with the sensitive rising edge in the middle. Data bits at the ASD serial data output also change state at the falling edge of the clock. Shift and shadow registers have a length of 55 bits, where 54 are actual data bits. The last shift register cell is clocked with an inverted clock, making the output change at the falling edge of the clock. A DOWN instruction causes the last cell to perform a HOLD operation.

Table 6: Serial interface signal lines.

Parameter	Function
DATA IN	Data line from controller to ASD shift register input
DATA OUT	Data line from ASD shift register output to controller
CLK	Clock line
D[0:2]	Register control lines

Table 7: Serial interface instruction encoding.

Instruction	Do	D1	D2	Operation
SHIFT	0	0	X	Shift right at rising edge of CLK
HOLD	1	0	X	Keep shift register contents (self feedback)
DOWN	X	1	X	Copy to shift register @ rising edge of CLK
LOAD	X	X	1	Load shadow registers @ rising edge of CLK

2.6 Front End Electronics Design- V2

Although in the measurements, shown in chapter 5, promising results have been reported as compared to simulation results, however, following the chip testing two modifications were proposed for the FEE-V2:

- Improving response-time of SLVS Pads
- Test point monitors at output of CSP and Shaper

The response time of SLVS drivers as shown in simulations, is slow, have a rise time of 10ns. The phenomena is even further deteriorated in measurements due to parasitic effects. Along with that, adding test point monitor buffers at output of CSP and Shaper can provide a window to inside the channel to visualize the signal in different stages of the channel.

2.6.1 New SLVS Design

The basic principle of a new SLVS driver [43] are explained with the help of idealized model as shown in Figure. It consists of four devices that can be represented by by resistor-switch pairs. At a time, either the pair of branches containing R1a and R1b resistors or the pair of branches containing R2a and R2b resistors is connected through the switches to the load resistance RL. The RL resistance is off-chip and is equal to 100, while the other four resistances should be equal to 50 .
With such a circuit configuration, the the VON node potential is equal to 1/4VS, while the VOP node potential is equal to 3/4VS , which results in ±1/2VS voltage swing across RL resistance. The value of VS=400mV, so it results in swing is equal to ±200mV. The resulting eye diagram for the described case is shown in Figure 2.
The resistors in ideal model mentioned above, are replaced with NMOS as shown in Figure. With appropriate in put voltages (IN-IP) the mosfets are turned ON or OFF to make the circuit work as explained for idealized.

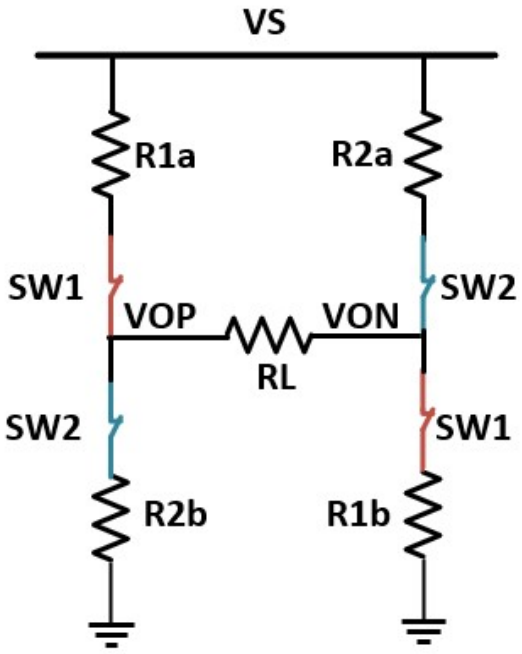


Figure 25: SLVS Block Diagram

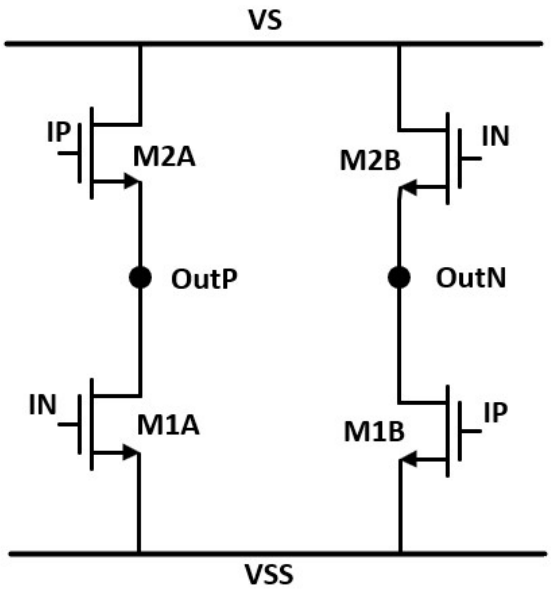


Figure 26: SLVS Schemaitc

2.6.2 Test Point Monitors

Test Point Monitors are designed to visualise the signal inside the Analog chain. They are connected at the output of CSP and Shaper and are connected only in channel four.
The Monitors are based on common drain topology topology with a load resistance equal to 800 ohms as shown in Figure. The amplifiers shows a gain of 0.75, lower sensitivity then the actual is observed at output, but since it is only

for signal monitoring purpose so a gain lower then unity does not make any difference. When the test point monitors are connected, the sensitivity of that particular channel is decreased due to loading effect of the buffer. For this purpose cmos switches are connected that can turn off the monitor-buffers when not in used. The switches are controlled by digital signal programmed from external board.

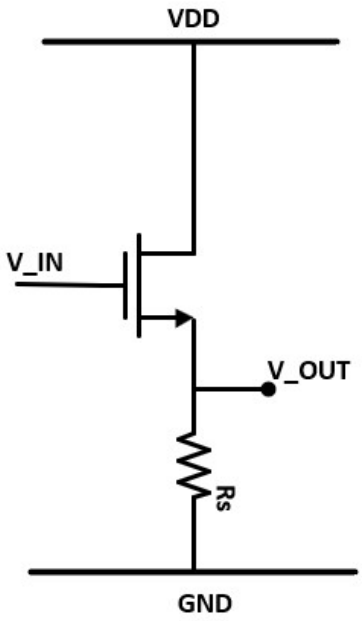


Figure 27: Test Point Buffer

3 Chapter 3: Design Layout

This section is dedicated to the layout of four channel front-end-electronic design. The layout is the final design step after which it is send for chip fabrication. Schematic designed is translated in a drawing form using metal layers provided from foundry to realize the chip.

The layout design consists of following blocks:

- a Pad-ring (with 100 pads, cover area of 2mm*2mm)
- Four Channels Front-End-Electronics design (with single channel area of about 0.4 mm^2)
- a Common Bias Block
- Two array of SIPO, PISO memory unit cells

Channel Layout:
The layout design of every block, CSP, Shaper etc, is done separately, first, and its performance is tested through post-layout simulations. By connecting the independent blocks layout, the channel layout is completed as shown in Figure 28. Each channel, shown in Figure 28, occupies an area of 0.235 mm^2.

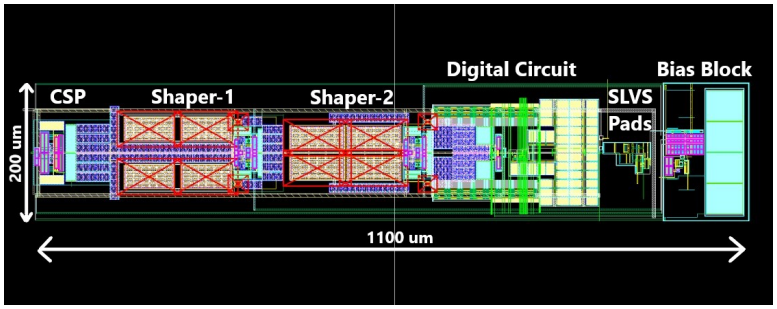


Figure 28: Channel Layout.

Pad-ring Layout:
The four channels, which are similar design, are placed symmetrically in the pad-ring. The pad-ring consists of 100 I/O pads which cover an area of 2mm by 2mm. The pads provide a connection to the off-chip world. Pad circuits are defined by the foundry which includes a bond-pad contact and diodes for protection, for the reason to avoid on-chip circuit damage due to external electrical discharges, etc.
The pad-ring includes pads for analog signals, digital signals and power signals. The pads for analog signal are placed at left side and bottom-left of the chip from where the input signal is inserted into the chip and the analog output of SLVS drivers is connected, respectively. The input charge pulses are generated off-chip and are connected to input pads, eight pads, placed on left side of the chip. The eight pads for SLVS driver output are placed at bottom of the pad ring. For uniform power distribution, different power and ground pads are distributed on four sides of the chip. The digital Pads are placed on right and top-right of the chip, where the

output signal of discriminator is connected and the JTAG signals are connected, respectively. Figure 29 shows the pad-ring diagram.
Finally, as regards supplies/grounds, they are divided to separate analog and digital worlds. In particular, there are:

- Analog supply AVDD and analog groung AVSS
- Digital supply VDD! and Digital groung VSS!

The analog and digital supplies are kept separate on chip to minimize the noise due to digital circuitry as in CMOS design the digital circuits are more noise due to level fluctuation. The AVDD and VDD! are connected to different external power supplies, externally, however the analog and digital grounds are connected on-board.

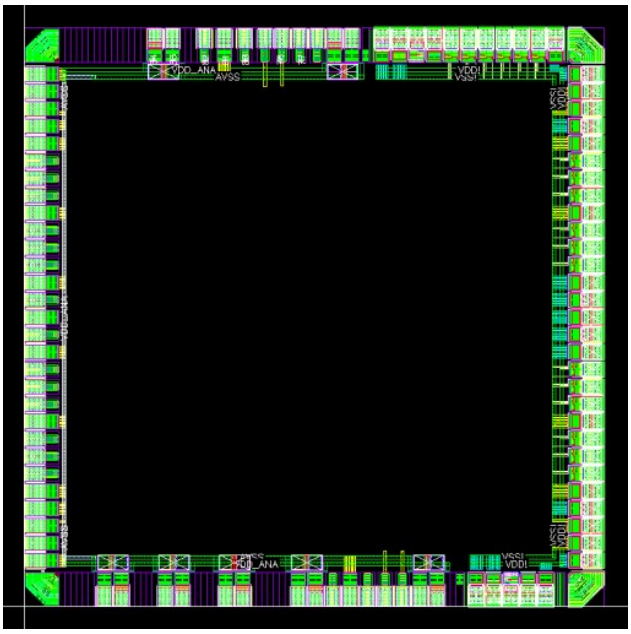


Figure 29: Pad Ring.

Core Layout:

The Core layout includes the entire four channel, bias block, memory unit cells of FEE chip except the Pad-ring shown in Figure 30
With in the pad-ring the four channels are placed symmetrically. For power symmetry the central bias block is in center of the Pad-ring and different power,ground connections are provided on four sides of the the pad-ring. The SIPO-PISO array, of area, are placed in right corner, close to the digital pads connecting the SIPO-PISO blocks to external FPGA Board.
Finally the floor plan is completed, using M1-M9 metal scheme, connecting the core layout and pad ring to complete the chip layout as shown in Figure 31.

Package:

The chips size is 2mm*2mm and consists a total of 100 pads on its four sides.The pads are very small,closely packed and is impossible to connect the individual pads to external boards, in the lab. For this purpose, QFN100 12mm by 12mm, width,

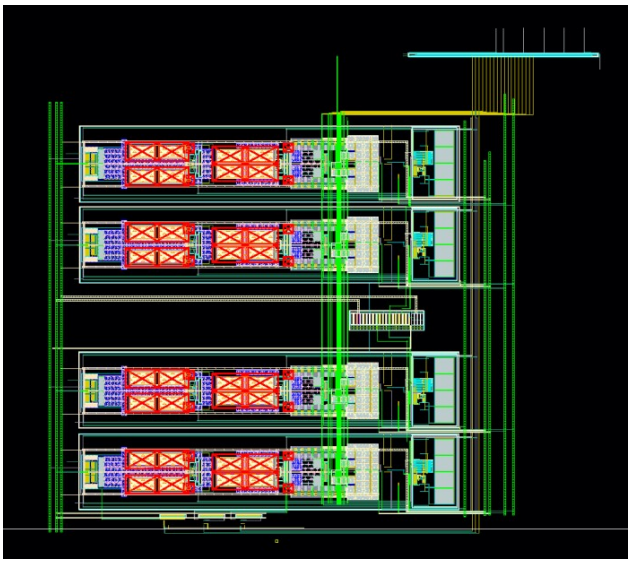


Figure 30: Core Layout

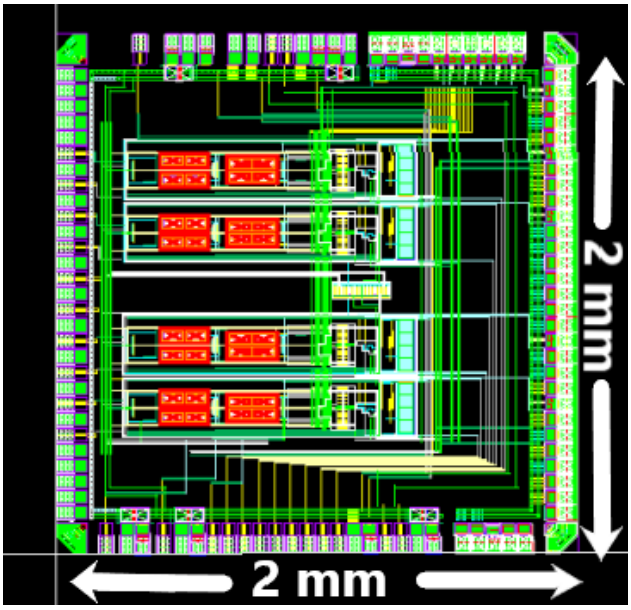


Figure 31: Chip Layout Design.

0.4 mm pin pitch, package is selected. Main Parameters of package are listed in Table 8. The FEE design is placed in center of the package and is connected to pads of package through metal layer Y4. Th package has symmetrical, 25 pins on each of its four sides
The final design is as shown in Figure 33.

Table 8: Main Parameters of Package

Parameter	**Value**
Package	QFN100 12*12mm^2
Number of Pins	100
Pad-Pitch	0.4mm
Die Material	Silicon
Lid Type	Sealed
Wafer Thickness	11mils

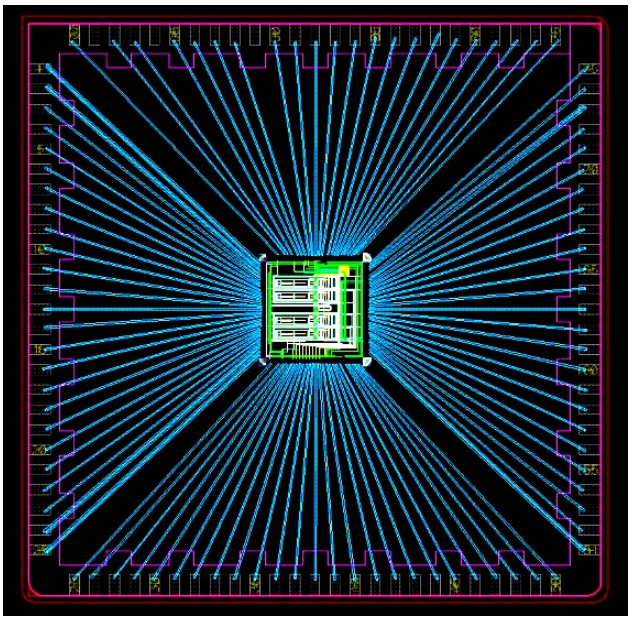


Figure 32: FEE package Layout Design.

4 Chapter 4: Simulations Results

In this chapter results from post layout simulation of FEE channel are presented. First, some results from simulations of fundamental blocks will be presented. After that, results of simulations to verify full channel functionality will be presented.

4.1 Simulations in the Time Domain

The performance of FEE channel is validated by simulating it with charges in the entire band of input charges 5 - 100 fC. The design is simulated with the dirac-delta pulse of different amplitude. Schematic and post layout simulations are carried out using cadence tools.
Cadence tools also allow to investigate the chip performance with respect to Process/¬Voltage/-Temperature (PVT) variations with the aim to,detect potential mismatch among devices of identical design. Our result w.r.t. process variations was that the variation of transistor parameters (e.g. threshold voltage, transconductance, output impedance) and resistor and capacitor values may cause performance variations within ± 20 percent for parameters like peak voltage, peak time, width of the ToT output and dead time.

Simulation was based on the following sets of parameters and five different processes of fabrication:

- a temperature range between – 40° and 120°
- typical – TT
- slow slow – SS
- fast fast – FF
- slow fast – SF
- fast slow – FS
- supply voltage variation of 10

CSP is designed for an input range from 5fC to 100fC. The input charge has been simulated in presence of large parasitic capacitance of 60 pF in parallel to an ideal current pulse (IPULSE). The current pulse has a duration of 2ns and an amplitude equal to QIN/QTime. In simulations, CSP exhibits a linear sensitivity of 1.1 mV/fC for entire range of input charges and a peaking time of 11ns as shown in Figure 33 - 34. The fast peaking time is as a result of clever design of the CSP with a very high unity gain bandwidth of 2.4 GHz, yet, maintaining the stability of the system.
The Shaper stage amplify and shape, the output of the CSP pulse, as a bipolar signal as shown in Figure 35. The bipolar signal has an overshoot followed by an undershoot of the same area as the overshoot.
Simulation shows that at the output of shaper the transient signal varies from 40 fC to 800 fC for an input charge range of 5 - 100 fC as shown in Figure 35. The sensitivity of shaper is 8mV/fC as shown in Figure 36. Again thanks to the right

choice of the amplifier topology, the design is able to achieve a linear sensitivity upto 800mV when operated from a 1.2 V supply.
The discriminator compares the output of shaper to a programable threshold value and gives the output with a High level of 1.2 volt and Low level of 0 volt as shown in Figure 37. The ToT, which is the useful information, is obtained from Discriminator. The variation of ToT with input charge is displayed in Figure 37. As can be seen the Time over threshold has a wide range to distinctly distinguish different input charges based on ToT information.
For higher speed and better power optimization SLVS drivers are designed as explained in Chapter 2. It generates an additional information along with the discriminator ToT output. The output of SLVS pads swings from 0 - 400 mV as shown in Figure 38.

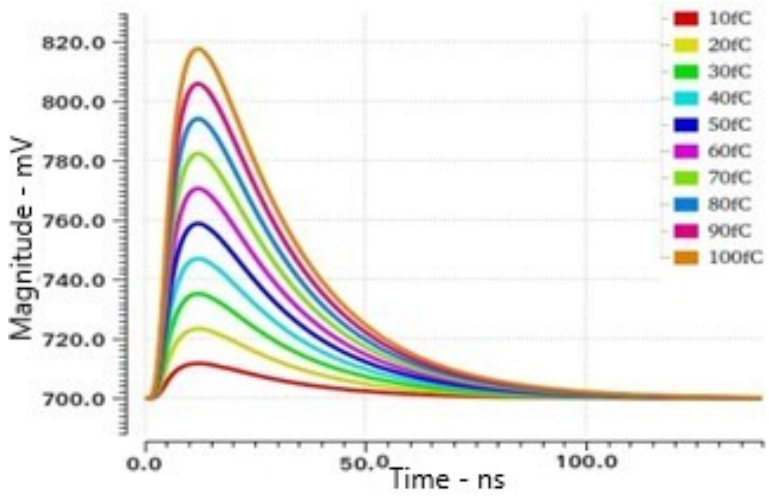


Figure 33: CSP Transient Response

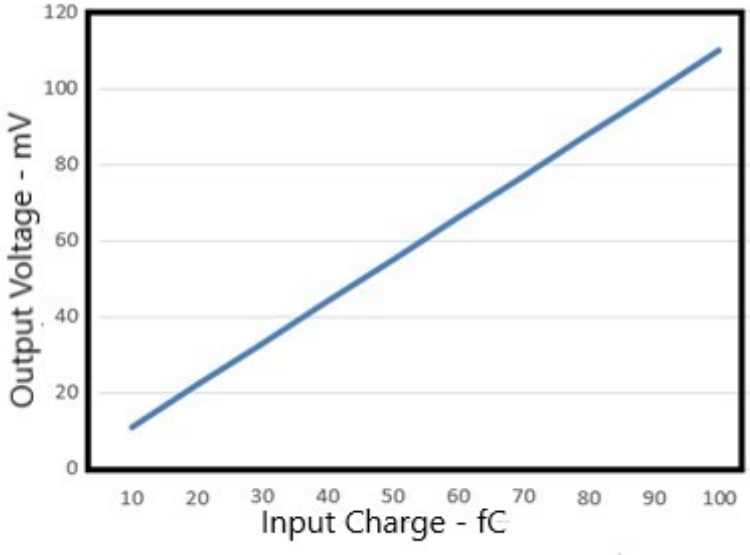


Figure 34: CSP Sensitivity

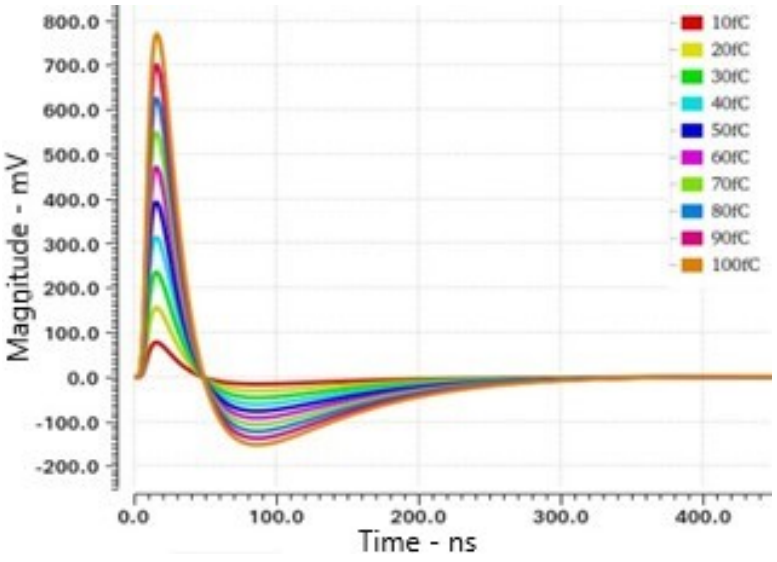


Figure 35: Shaper Transient response

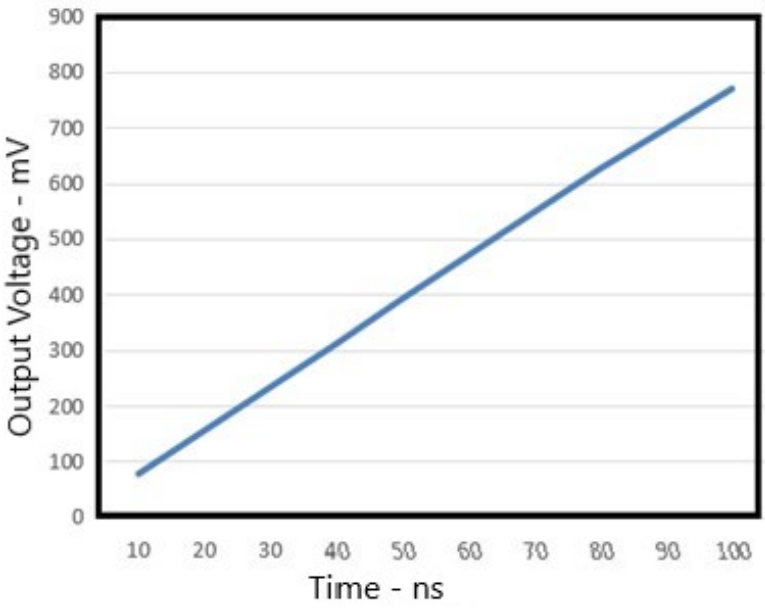


Figure 36: Shaper Sensitivity

4.2 Simulations in the Frequency Domain

The AC characteristics of the CSP and Shaper stage are shown in Figure 39-43. Topology for CSP is two-stage single-ended amplifier. The DC gain of op-amp is 57 dB. The unity gain frequency of CSP is 2.4 GHz with a phase margin of 60 degree for stability of design. This large unity gain bandwidth is set to make the CSP response faster to an Input charge pulse and achieve a peaking-time-delay of 11ns at CSP output. With feedback resistor and capacitor the Close-loop gain of preamplifier is 55 dB, as in Figure 39-40.

The SH1-SH2 serve both as gain and as shaping stages. The amplifier topology for both shaper amplifiers is identical chapter 2, while the input and feedback net-

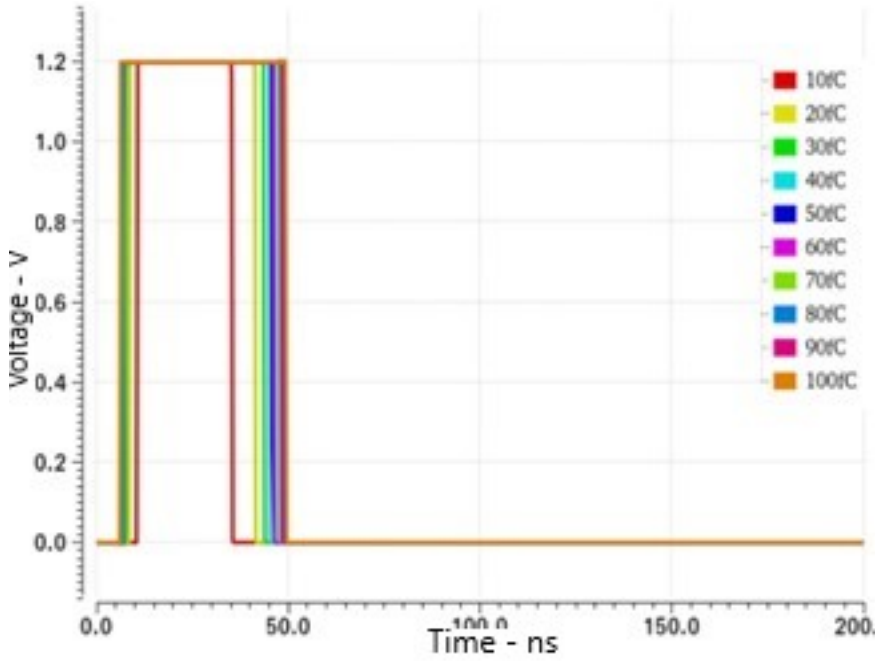


Figure 37: Discriminator Response

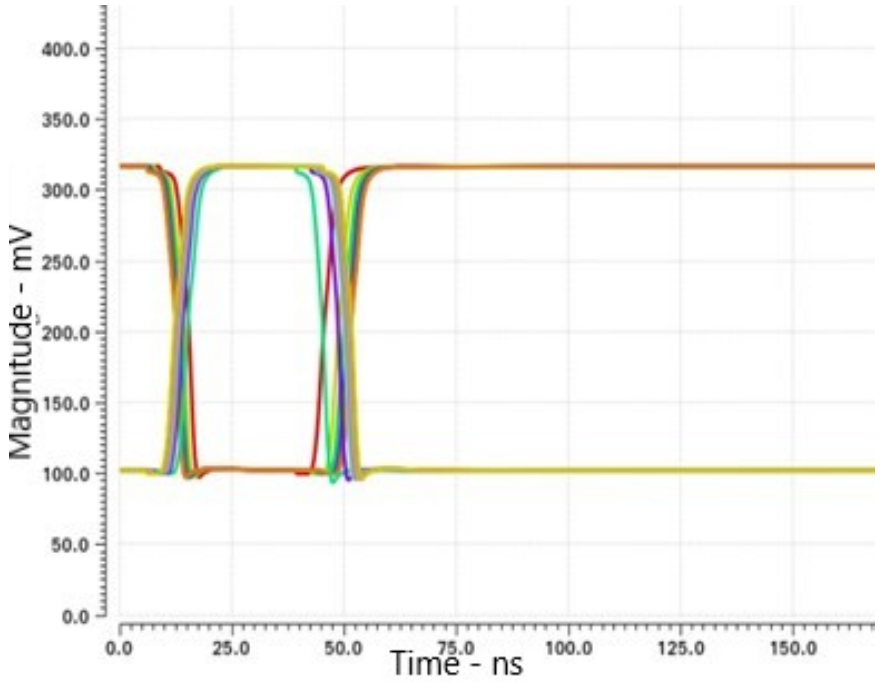


Figure 38: SLVS Drivers Response

work differ according to the desired frequency characteristics and the corresponding values of the feedback elements Z1 and Z2 (Table 4). The dc gain of op-amp is 52 dB with a unity gain bandwidth of 500 MHz. The maximum gain of SH-1 is 5.7 dB with a pass and of 1.05 MHz - 168.82 MHz. SH-2 stage has a maximum pas-band gain of 11.55 dB in the range 1.8 MHz – 74.4 MHz, Figure 42-43. The Two-Stage Shaper implement the intended bipolar shaping with a pass band gain of equal to 17.2dB.

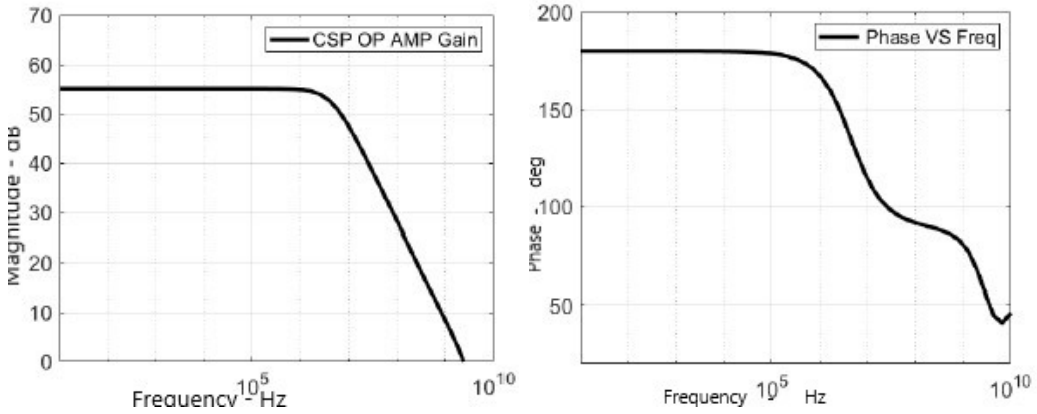


Figure 39: CSP OP-Amp Frequency Response.

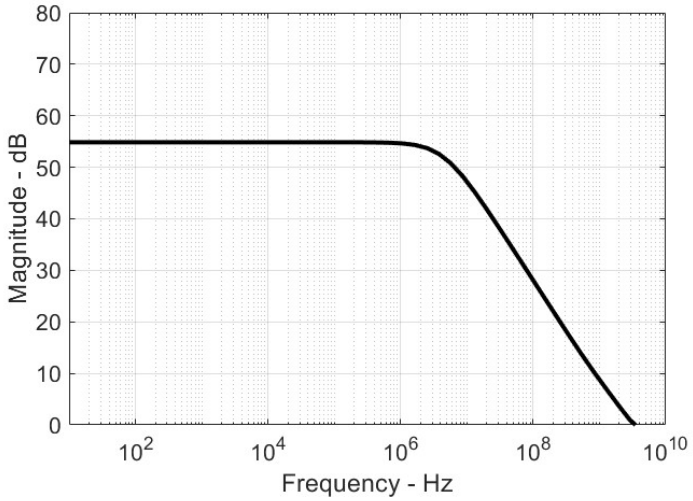


Figure 40: CSP close loop frequency response.

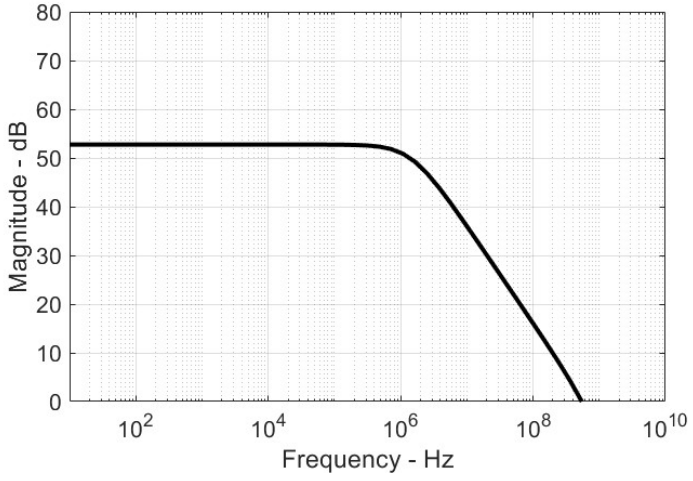


Figure 41: Shaper OP-Amp Frequency Response.

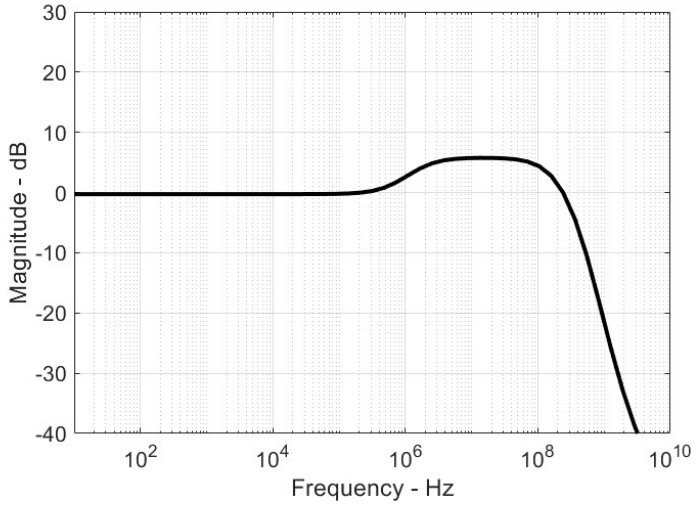


Figure 42: Shaper-1 close loop frequency response.

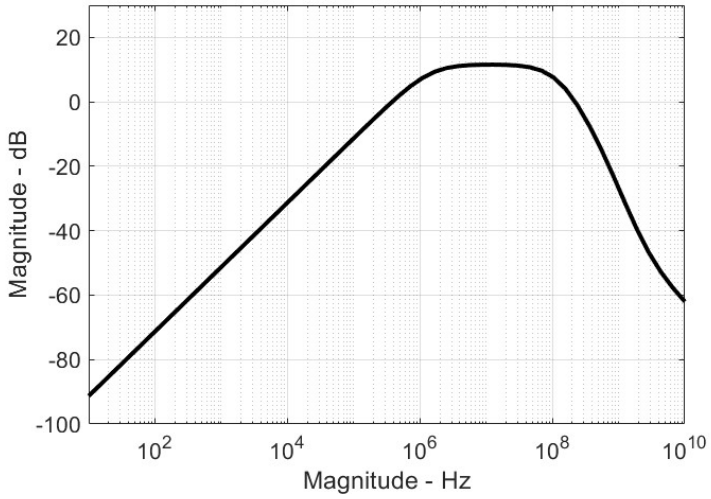


Figure 43: Shaper-2 close loop frequency response.

5 Chapter 5: Measurements

Four channel, read out electronics chip has been designed and realized with the final target to replace Octal MDT-ASD [24] currently used in ATLAS experiments for Muons detection. The replacement is necessary with the HL-LHC Phase II Upgrade but it will be done only when the proper tests will confirm that the performance of the presented chip matches with the reference model. For this purpose, a complete electrical characterization has been carried-out by realizing a similar experimental environment in the lab.
The 4xFEE chip presented in this paper has been realized in 65nm TSMC technology and is placed in QFN100 package. The package is soldered on a test PCB board, on which the reference voltages and currents are generated, to carry out the complete electrical characterization. The four channels are placed and routed in order to guarantee symmetrical paths to the reference voltages and central bias block. Each channel occupies 0.235mm^2. The total area of the design is 4mm^2. The design is validated by performing measurements with different equivalent input charge (QIN) in the full input range 5fC÷100fC as shown in Figure 44. Output signal gives information of charge arrival time and amount of input charge. The dead time measurement, hysteresis, threshold variation, channel mode selection has been tested and validated in measurements phase. The channel mode, described in chapter 2, was the first point to be tested by forcing the output signal into High or Low and thus confirming the design is working.

5.1 Time-Over-Threshold

The chip is designed for the purpose of detecting and measuring input charges in range of 5-100 fC. The performance of the chip is validated by performing measurements with an input charge pulse, diract delta, in entire input charge range. The ToT signal, which is output of the discriminator, encodes the information of charge arrival time and amount of charge been detected. The leading edge of ToT signal is representation of arrival of time where as the width of the pulse represents the amount of charge been detected. As the input charge is varied from 25-100 fC the Discriminator output varies as shown in Figure 44. An important factor in the ToT pulse is to have enough of ToT pulse width that it can be differentiated for different input charges. Again, as can be seen in Figure 44, from ToT pulses different input charges can be clearly differentiated. The ToT pulse varies from 30-45 ns for 5-100 fC of input charge.

5.2 Channel Mode Selection

As explained in Chapter-2 the design has a feature known as channel mode selection in which it can force the chip output to be either high, low or to depend on the normal operation of the channel. In measurement phase, this option is very helpful as a first point to check if the chip is working or no.
This was the first step of our measurement, in which we are able to force the output of our signal into desire level, for testing purpose.

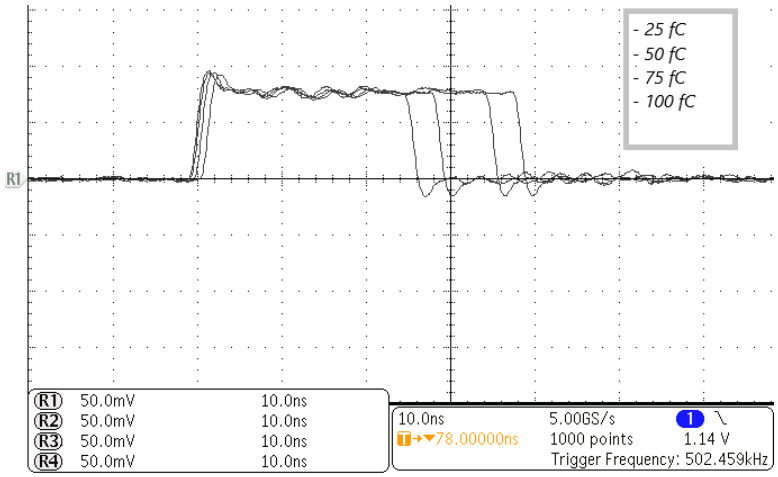


Figure 44: Time Over Threshold

5.3 Dead Time Measurement

Dead Time is the time interval in which any threshold crossing of discriminator will not produce any output. It is the time between the leading edge of one output to the leading edge of consecutive next output. The dead time block is designed using a series of RC delay blocks. The performance of dead time design is validated by changing the digital code from 0000-1111 to check for entire range. Measurement shows a very linear dead time performance for all four channels as shown in Figure 45. In measurements, the dead-time varies (by 50 ns maximum)as compared to simulation results but the variation due to RC elements is acceptable.

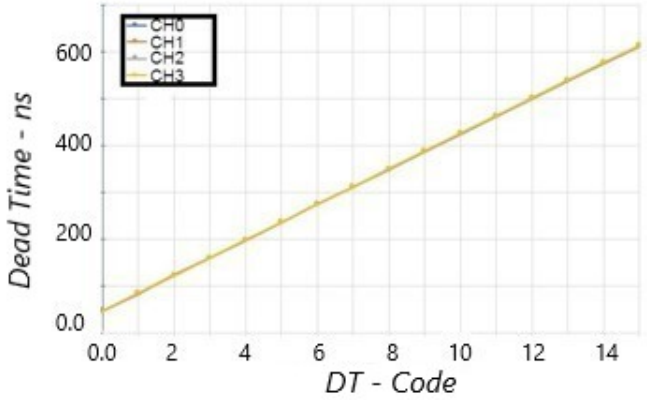


Figure 45: Dead Time measurement

5.4 Threshold Scans

The following procedure was used to measure the noise of readout circuit channel. A pulse with constant amplitude was injected into the input of the FEE with a constant frequency, 10 kHz, while the frequency of the discriminator output was recorded as a function of the programmed threshold. Figure 46 shows results for all

channels of the FEE. Scanning the pulses by threshold steps from high to low, the output frequency is changing from zero to 10 kHz. At 5 kHz recorded rate, half of the hits is below and half above the applied threshold. The width of the S-curve corresponds to the noise on top of the test pulses, which is mainly due to the noise of the CSP and the rest of the analog chain.
Along with that the effect of Hysteresis has also been confirmed via threshold scan. As can be seen, when the Hysteresis code is varied from 0 to 7, the variation in threshold scan for that particular channel is reported in Figure 47.
The chip photo is shown in Figure 48.

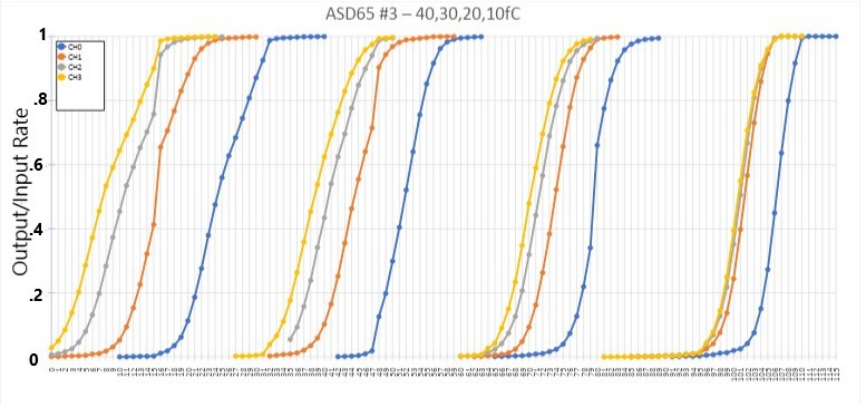


Figure 46: Threshold scan for channels of FEE chip

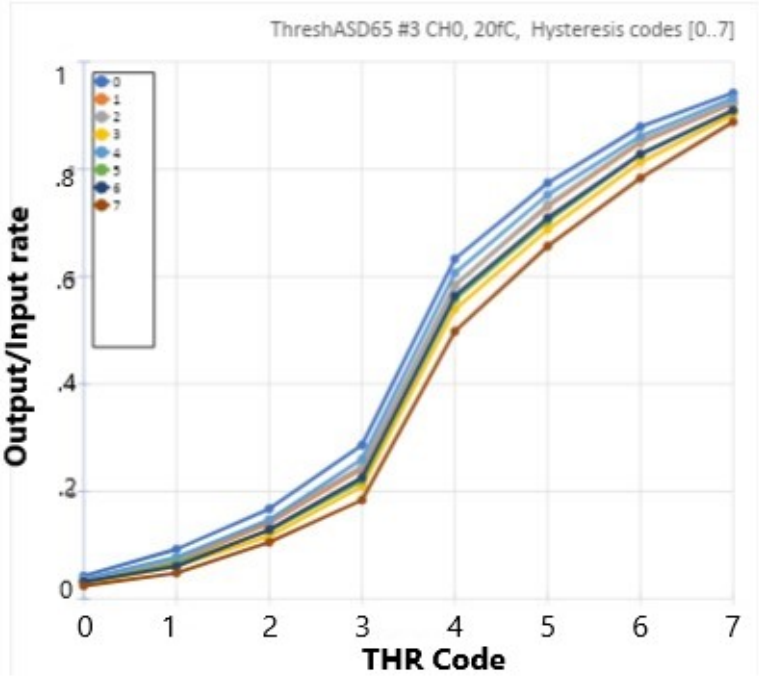


Figure 47: Threshold scan and effect of Hysteresis

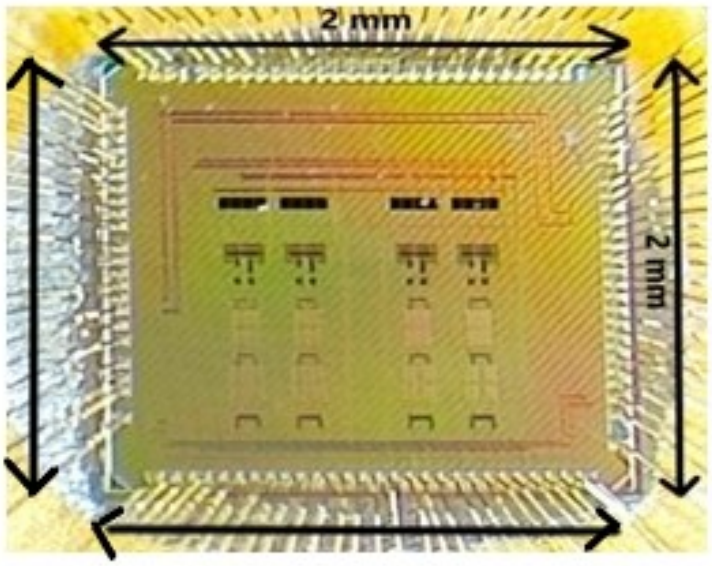


Figure 48: FEE chip

6 Chapter 6: Paper

6.1 Paper

6.1.1 A 4-Channel Ultra-Low Power Front-End Electronics in 65nm CMOS for ATLAS MDT Detectors

6.1.2 A 4-channel front-end electronics for muon drift tubes detectors in 65 nm CMOS technology

electronics

MDPI

Article

A 4-Channel Ultra-Low Power Front-End Electronics in 65 nm CMOS for ATLAS MDT Detectors

Syed Adeel Ali Shah [1,*], Marcello De Matteis [1], Hubert Kroha [2], Markus Fras [2], Oliver Kortner [2], Robert Richter [2] and Andrea Baschirotto [1]

[1] Physics Department 'G. Occhialini', Milano-Bicocca University, 20126 Milan, Italy; marcello.dematteis@unimib.it (M.D.M.); andrea.baschirotto@unimib.it (A.B.)
[2] Max-Planck-Institute for Physics, 80805 Muenchen, Germany; kroha@mpp.mpg.de (H.K.); fras@mpp.mpg.de (M.F.); kortner@mpp.mpg.de (O.K.); richterr@mpp.mpg.de (R.R.)
* Correspondence: s.shah4@campus.unimib.it

Abstract: A 4-channel front-end electronics (4 × FEE) system for the muon drift tube in the ATLAS detector in the High-Luminosity LHC is presented. The overall channel architecture is optimized to reduce the power and area of the design. Each channel comprises a charge-sensitive preamplifier (CSP), shaper, discriminator and differential low-voltage signaling drivers. The proposed channel operates with a 5–100 fC input charge and exhibits a linear sensitivity of 8 mV/fC for the entire input charge range. The peaking time delay of the analog channel is 14.6 ns. At the output, the time representation of the input signal is provided in terms of the CMOS level and in scalable low-voltage signal (SLVS). The FEE consumes a current of 10.6 mA per channel from a single 1.2 V supply voltage. The full 4 × FEE design is realized in TSMC 65 nm CMOS technology and its die-area is 2 mm × 2 mm.

Keywords: read-out channel; front-end electronics; ATLAS experiment; monitored drift tube

Citation: Shah, S.A.A.; De Matteis, M.; Kroha, H.; Fras, M.; Kortner, O.; Richter, R.; Baschirotto, A. A 4-Channel Ultra-Low Power Front-End Electronics in 65 nm CMOS for ATLAS MDT Detectors. *Electronics* **2022**, *11*, 1001. https://doi.org/10.3390/electronics11071001

Academic Editors: João Paulo Pereira do Carmo, Subhanshu Gupta and Kunhee Cho

Received: 15 February 2022
Accepted: 22 March 2022
Published: 24 March 2022

1. Introduction

The upgrade of the Large Hadron Collider (LHC) to discover novel physics particles creates new challenges for the readout electronics. After a decade of successful operation, the ATLAS experiment, including the muon spectrometer, has to be upgraded to cope with the high data and radiation rates in High Luminosity LHC operation [1,2]. The luminosity of the Large Hadron Collider (LHC) accelerator at CERN will be upgraded by a factor of about seven compared to its previous performance. Muon drift tube (MDT) detectors are the main precision tracking detectors of the muon spectrometer in the ATLAS experiment in the Large Hadron Collider (LHC) [1]. The sense wires of the drift tubes are connected to the channels of an ASD chip [2] to process the signals generated by the ionization electrons created by muons traversing the tubes filled with an argon:CO2 (93:7) gas mixture.

To cope with the new challenges of a high data rate and high luminosity, a new state-of-the-art version of the ASD chip [3–5] has been designed in 130 nm CMOS technology. Its analog chain includes a charge-sensitive preamplifier (CSP) and a three-stage shaper. It is operated in dual mode, either with a signal charge measurement using a Wilkinson ADC (W-ADC) or in time-over-threshold (ToT) mode. With a detector capacitance of 60 pF, it features a sensitivity (voltage-to-charge ratio) of 14 mV/fC, 15 ns peaking time delay, and 15 dB signal-to-noise ratio (SNR) for minimum input charge. Each channel consumes a power of 33 mW from a 3.3 V supply.

In the process of renewing the MDT readout electronics, one of the main objectives is to make a significant low-power and area-efficient design using long-term sustainable technology, along with achieving all the functional parameters of MDT-ASD [3]. In this design the technology is scaled down from a 130 nm to a 65 nm TSMC CMOS process and the circuit is operated from a single 1.2 V supply voltage (down from 3.3 V). With the

key target of power and area efficiency optimization, the full analog channel architecture is changed, and each block of the analog channel is designed accordingly with the new architecture and, as a consequence, with new specifications. Each channel starts with a single-ended CSP, which converts the incoming charge signal to a voltage pulse. The signal in the analog channel is converted into a pair of differential signals in later stages to improve the power supply rejection ratio. The design incorporates a two-stage shaper to implement bipolar shaping of the input signal. This design has a single mode of operation, time-over-threshold. The W-ADC mode, used for signal charge measurement and time-slewing corrections in the reference model, has become unnecessary due to the larger gain observed at the unchanged input-referred noise level of the new-generation chips, so it has been eliminated. To avoid bulky capacitors, as used in the three-stage shaper of the previous design, the sizing of passive components has been optimized to minimize RC component sizes, resulting in a 4x area shrinking factor in the shaper stage w.r.t. to the previous design. SLVS drivers have been designed to provide an interface for the FEE system to TDC, which is the subsequent stage of the readout chain.

The power consumption of each channel is 12.8 mW, which is 61.2 percent lower than in the previous design. Each channel occupies an area of 0.235 mm^2, which is only 58.75 percent of the previous design. These significant savings are achieved while guaranteeing a performance level in terms of a 14.6 ns peaking time of the analog channel and a 15 dB minimum SNR, as in the previous design. The design displays a linear sensitivity of 1.1 mV/fC and 8 mV/fC, for an input charge range of 5–100 fC, at the output of the CSP and analog channel, respectively.

2. ATLAS Experiment

ATLAS is one of two general-purpose experiments at CERN which contributed in the discovery of the Higgs Boson particle in 2012, and it is further used to investigate other particles that could make up dark matter [6]. As a general-purpose experiment, it is designed to study hard proton–proton collision processes at center-of-mass energies of up to 14 TeV. As a result of these collisions, some charged and neutral particles are generated. Muons are the most penetrating charged particles emerging from proton–proton collisions. In order to determine the energy and direction of the secondary particles emerging from the p–p collisions, a sequence of specialized detectors are used for the detection. The majority of tracking detectors are monitored drift tubes (MDTs) [2], which consist of gas-filled aluminium tubes with a central anode wire. The muons pass through the gas-filled pressurized tubes and ionize the gas molecules. The free electrons drift towards the centre anode wire, due to the electric field. The time of arrival of these charges at the wire is used to measure the distance of the track from the wire. Detailed information about MDT ATLAS readout electronics is provided in [1,2,6].

3. Implementation of the MDT-FEE Circuit

The architecture of a single-channel FEE is shown in Figure 1. The complete design is composed of four similar channels. The design has been realized in TSMC 65 nm CMOS technology. The input signal of each channel is a current pulse coming from the sense wire of the detector. The input signal is converted into a voltage pulse by the charge-sensitive preamplifier (CSP). The CSP's output pulse is amplified and shaped by the two-stage bipolar shaper (SH1, SH2). The CSP and shaper together constitute the analog signal processing chain of the design, which is connected with the discriminator through coupling capacitors. Two programmable DACs are used to set the threshold value for the discriminator. The discriminator compares the bipolar signal with the threshold value to yield the output, time-over-threshold. SLVS drivers are designed to provide an interface for the individual FEE channels with the subsequent TDC chip. Test-point buffers are added at the output of CSP and the shaper for diagnostic purposes. A central bias block has been designed, which mirrors the current to each channel from a reference source of 50 µA.

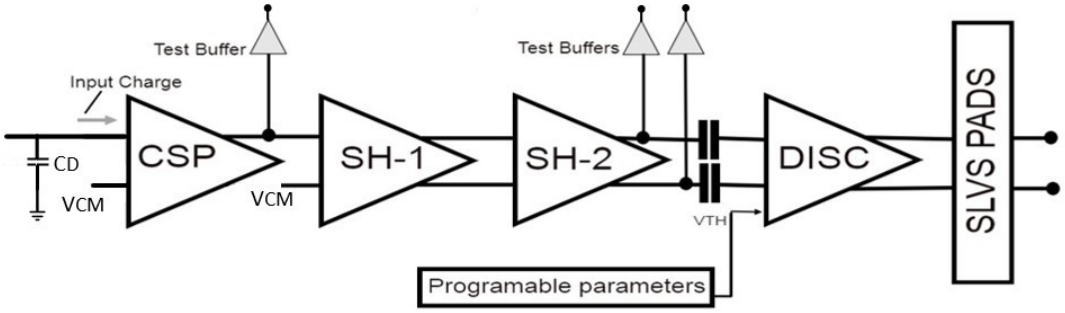


Figure 1. Generic block diagram of one channel of the FEE chip.

3.1. Charge-Sensitive Preamplifier

In the MDT-FEE design, the performance parameters of the CSP are of key importance. The design involves a two-stage, single-ended amplifier topology, as shown in Figure 2. The input signal, coming from the sense wire of the tube, is connected to the negative terminal of the CSP. A large parasitic capacitance (C_D = 60 pF) is connected between the CSP input node and ground, which is which is mainly due to the capacitance of the tube-wire system and the signal routing on the PCB. The positive input has been fixed by means of a resistor divider (Rb1 and Rb2) to 700 mV, implemented on-chip for better matching. To suppress the substrate noise, a capacitor of 16 pF is attached to the positive terminal of the CSP on-chip. The feedback network of the CSP is a parallel combination of a resistor R_F = 25 kΩ and a capacitor C_F = 920 fF in parallel.

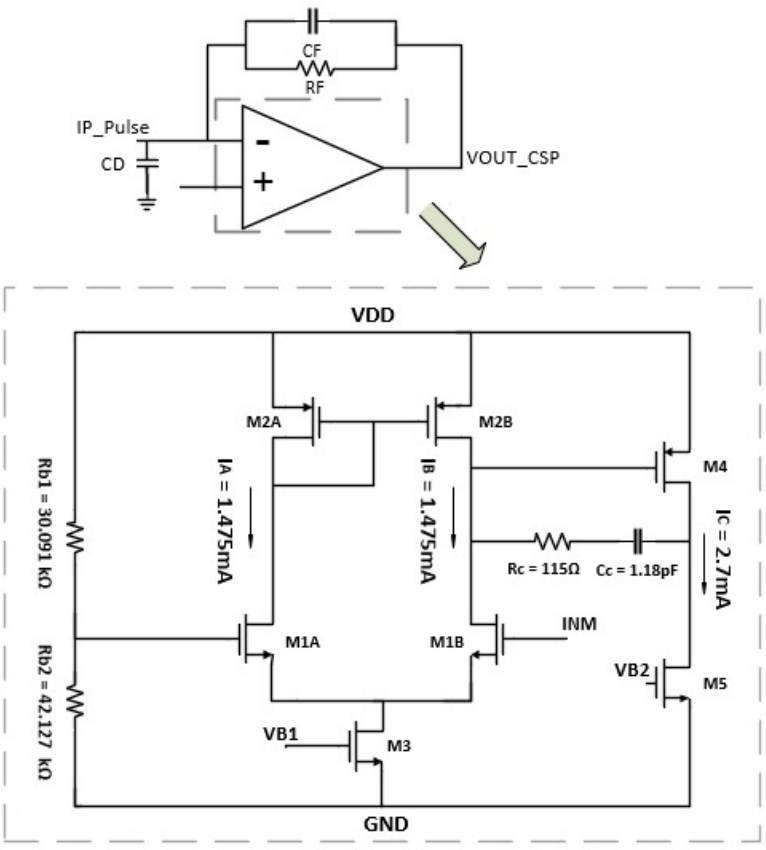


Figure 2. CSP and operational amplifier transistor-level scheme.

The CSP design is critical as it defines several key functional parameters of the design, such as signal rise-time, overall power consumption, and noise. Along with the high specification criteria, the functionality of this block is adversely affected by the large value of the detector capacitance. It has a highly deteriorating effect on the closed-loop-gain, bandwidth, sensitivity, and signal peaking time delay.

The most important performance parameters of the CSP in our design are the peaking time delay and signal-to-noise ratio. The peaking time delay is important for the precise determination of the arrival time of the signal, given the wide range of signal amplitudes as they occur in the experiment. CSP noise and the speed of response are optimized by using a suitable input device transconductance (gm1). The differential input transistors (M1A–M1B), of size W/L = 580 um/330 nm, operate in moderate inversion (to mitigate the increase in power consumption) with a nominal current of 1.475 mA in order to have very large transconductance, gm1 = 25 mA/V. This is in accordance with the minimum thermal noise requirement. The input charge pulse for the FEE comes from a single source (the sense wire of the tube); thus, a single-ended topology has been chosen for the CSP, hence saving a current of 2.7 mA in the output stage of the amplifier, as shown in Figure 2. In this way, the use of common-mode feedback circuit is also eliminated. To minimize the peaking time delay, the OpAmp is designed with a very high unity-gain bandwidth of 2.4 GHz, with a phase margin of 60 degree, ensuring good stability. With these open-loop characteristics, the CSP exhibits a very fast peaking time of 4 ns without the detector capacitor and 11 ns with the large (60 pF) detector capacitor, as shown in Figure 3.

The load impedance of the CSP stage is the input impedance of shaper-1. It is a parallel combination of a resistor, R_1, and a series connection of a resistor and a capacitor—R_2 and C_2, respectively. The CSP transfer function depends on the feedback network, the transconductance of the input transistor (M1A–B), the load impedance Z_L and the detector capacitance C_D. The CSP transfer function can be approximated by Equation (1).

$$T(s) = \left(\frac{-R_F(1 - \frac{sC_F}{gm_{M1}})}{(1 + sC_{FRF}(1 + \frac{C_D}{C_F}\frac{1}{gm_{M1}Z_L}))} \right) \quad (1)$$

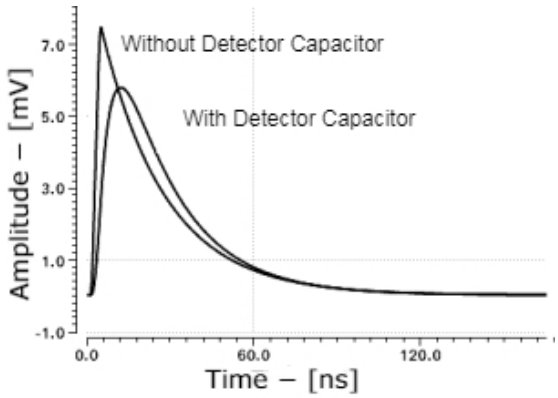


Figure 3. Transient response of CSP with and without a detector capacitor.

Similarly, the input impedance transfer function is given approximately by Equation (2). It is almost constant (Z_{IN} = 44 Ω) at low frequencies and below 73 Ω for all in-band frequencies, as shown in Figure 4.

$$Z_{IN} = \left(\frac{T(s)}{gm_1 Z_L} \right) \quad (2)$$

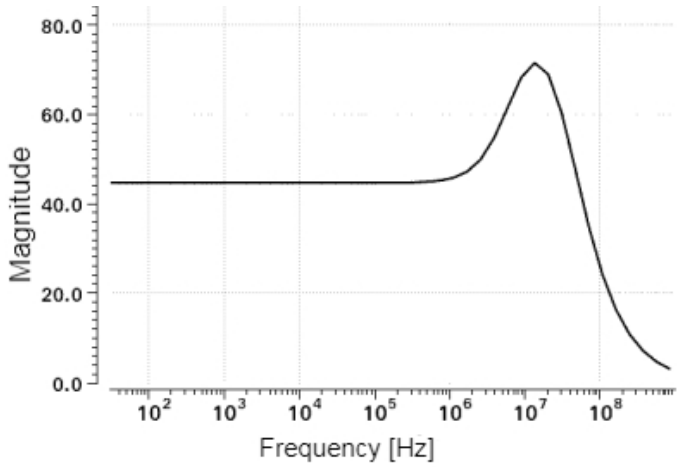


Figure 4. Input impedance of charge-sensitive preamplifier.

3.2. Shaper Section

The Preamplifier stage is followed by a two-stage shaper section to implement bipolar shaping of the pulse in order to mitigate signal pile-up at high signal rates. Each stage of the shaper is based on two-stage differential amplifiers, as shown in Figure 5. The two-stage differential topology is more robust to the load and allows for a higher output voltage swing. The transconductance value of input MOSs is 2.5 mA/V and sinks a current of 104 uA in each input stage (Ia and Ib) and 418 uA in each output stage, as shown in Figure 5. The output-stage MOSs have been designed with an overdrive voltage of 70 mV (i.e., moderate inversion) to maximize the output swing range, and to achieve a linear sensitivity for the full range of input charges up to 100 fC. To set the common-mode voltage a separate common-mode feedback (CMFB) network has been designed. The W/L values of the CMFB network are half of those of the main amplifier input stage in order to reduce the current consumption. The CMFB network is attached to the main amplifier through a sensing network, consisting of a pair of resistors with capacitors in parallel for better performance at higher frequencies. The values of currents are given in Figure 5.

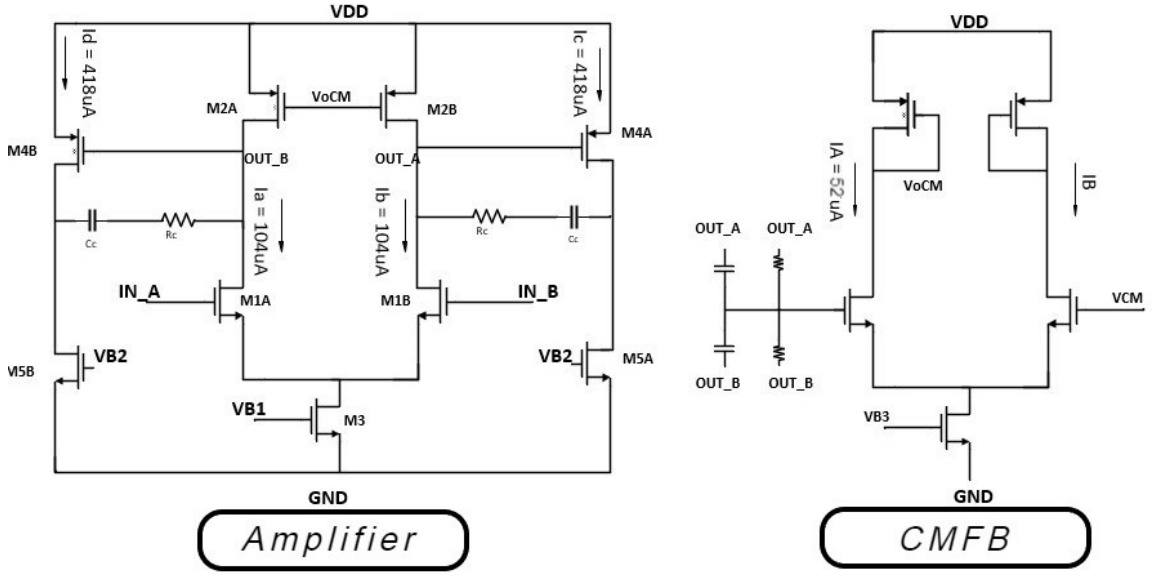


Figure 5. Shaper operational amplifier transistor-level scheme.

Each stage of the shaper (shaper 1–2) has an input impedance network and a resistive feedback loop, as shown in Figure 6. The poles and zeroes used to implement the bipolar shaping are the same as in ASD, at 130 nm [3], selected to cancel the very long time constant component of the positive ion MDT pulse [2]; however, the values Z-RC are greatly changed, shrunk by almost a factor of four, with the aim of an area-efficient design. The values of impedance network components are given in Table 1.

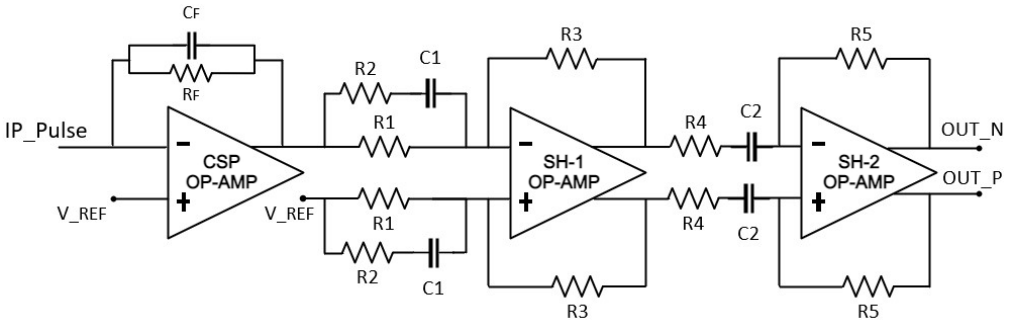


Figure 6. Analog signal-processing chain.

The transfer function of each shaper stage depends on the input impedance and feedback network. Equations (3) and (4) show the transfer function of shaper-1 and shaper-2, respectively.

$$T(s) = \frac{R_3}{R_1}\left(\frac{1 + sC_1(R_1 + R_2)}{1 + sC_1R_2}\right) \tag{3}$$

$$T(s) = \left(\frac{sC_2R_5}{1 + sC_2R_4}\right) \tag{4}$$

Table 1. Shaper Impedance network component values.

Stage	Component	Value
Shaper-1	R_1	9.8 kΩ
Shaper-1	C_1	10.2 pF
Shaper-1	R_2	10.1 kΩ
Shaper-1	R_3	9.8 kΩ
Shaper-2	R_4	9.8 kΩ
Shaper-2	C_2	11.5 pF
Shaper-2	R_5	37.8 kΩ

The open-loop gain and unity-gain-bandwidth of the shaper amplifier are 50 dB and 500 MHz, respectively. With these open-loop characteristics, the closed loop-gain values of shaper 1–2 vary by less than 4 percent as compared to ideal amplifiers. The pass-band gain is given by the ratio between Z2 and Z1, whereas the bandwidth is fixed by the resistive and capacitive loads. The frequency response of each stage of the analog channel is plotted in Figure 7. The shaper features a pass-band width of 1.06–172.6 MHz and a pass-band gain of 17.6 dB.

At the output of the CSP and the shaper, test-point buffers have been designed, for diagnostic purposes, using a common-drain topology as shown in Figure 8. The buffer's load resistance of 800 Ω is placed off-chip, on a PCB board.

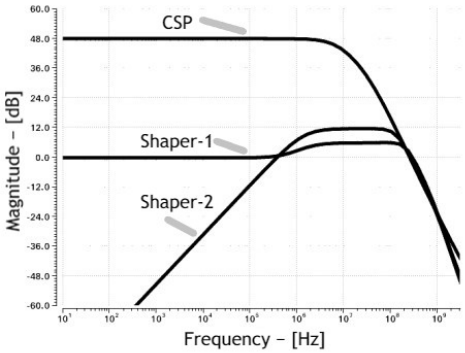


Figure 7. CSP and shaper stage (1–2) frequency response.

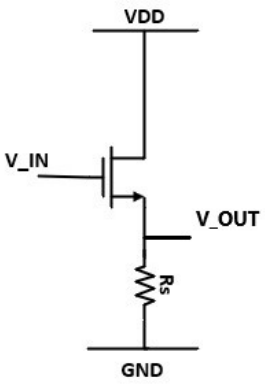


Figure 8. Test-point buffer.

3.3. Digital Circuit of FEE System

The output signal of the analog signal-processing chain is fed into the discriminator through coupling capacitors, where it is compared to a programable threshold value, which ultimately yields the digital ToT output pulse.

The comparator has been designed using a two-stage single ended amplifier topology without compensation, as shown in Figure 9. It consists of a high gain amplification stage, followed by a series of inverters to produce the output, referred to as high or low, depending on the input signal and threshold value. The threshold value for the main comparator is set differentially. Two sets of 8-bit string-DACs and 3-to-8 bit decoders are used to set the threshold values, which are programable up to 256 mV across the common mode voltage with an LSB of 2 mV. Each string-DAC is composed of a main-string and a sub-string to divide the reference voltage and give the output voltage with an LSB of 1 mV. Complementary CMOS switches were designed for selecting the required output voltage to set the threshold value.

A hysteresis block is added with the comparator to unbalance the current in the main differential amplifier (M1A-M1B) according to a programmable value. Its significance is to remove glitches in the output of the comparator, which arise due to noise. The hysteresis can be varied from 0–50 mV by means of the programable digital word set externally at run-time.

A dead-time block is used to introduce a delay in the discriminator response up to 500 ns, programmable in steps of 30 ns, thus allowing a large set of dead-time options. To set all these programmable and channel parameters, a digital word carried by a 50 bit shift register is used. A new design approach, as compared to the reference design [3], of using parallel arrays of serial-in-parallel-out (SIPO) and parallel-in-serial-out (PISO) blocks is utilized in the design of the shift register. The digital word is shifted serially into the SIPO block from an external board. At the instance of loading the digital word from the SIPO block to the channel, it is loaded into the PISO block as well. At the output pad, the

contents of the PISO block can be visualized to verify the data loaded into the channel. The digital word is passed from an external board through a JTAG interface.

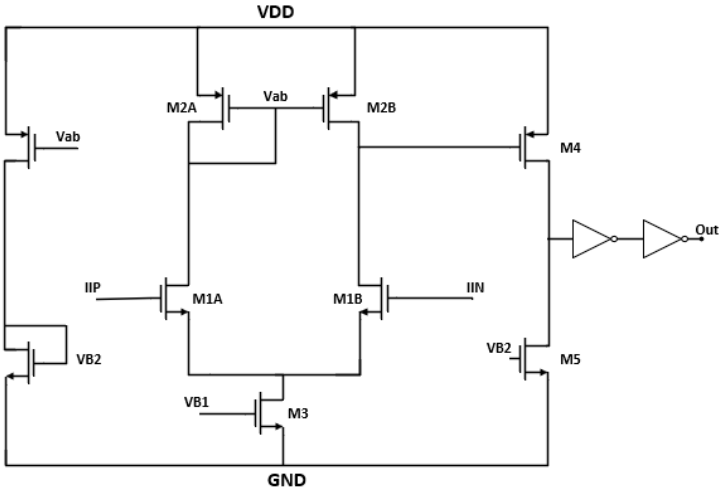


Figure 9. Comparator transistor-level scheme.

3.4. SLVS Output Drivers

Modern experiments, such as ATLAS, consist of large number of data-processing channels. Consequently, decreasing power consumption and improving the data transmission rate of readout electronics is important. For these reasons, along with providing the CMOS-level signal at the output, SLVS drivers are designed for connecting the FEE channels with the external components of the TDC. The SLVS standard is defined in [7] and describes a differential current-steering protocol. It has a voltage swing of 200 mV, across a common mode voltage of 200 mV. The load resistor on the receiver end is of the value of 100 Ω. At the output, the differential voltage is 400 mV and a current of 2 mA flows through the load resistor. The SLVS transmitter operates as a current source with switched polarity. The output current flows through the load resistance, external to the chip, building the differential output voltage swing of 400 mV. The proposed transmitter circuit, presented in Figure 10, uses the arrangement of four MOS switches in the H-bridge configuration [8,9], implemented with the M1–M2 (AB) NMOS transistors.

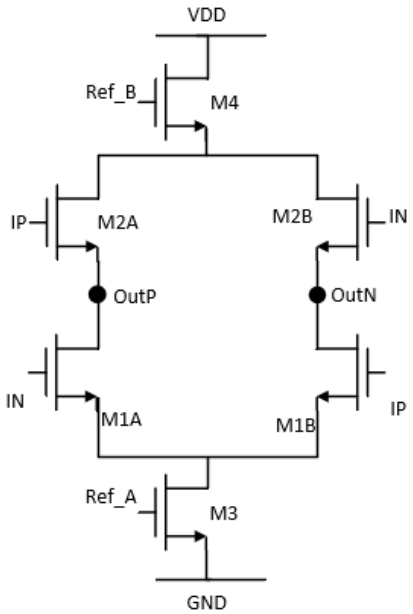


Figure 10. SLVS driver H-bridge transistor-level scheme.

4. Simulation Result

The FEE system has been designed in TSMC 65 nm CMOS technology. The four channels in the layout design are arranged and connected in order to guarantee the symmetry of paths with respect to the bias circuit, placed in the center region of the design. Each channel occupies an area of 0.235 mm^2. The total area of the design is 4 mm^2. Each channel consumes a current of 10.6 mA from a single 1.2 V supply voltage.

In post-layout simulations, the design was validated for different input charges (QIN) in the entire input range of 5–100 fC. The analog section output voltage ranged from 40 mV up to 800 mV for an input charge of 5–100 fC, as shown in Figure 11. Figure 12 shows that the analog chain exhibited a linear sensitivity (i.e.the peak-voltage of the curves vs. the input charge) of 8 mV/fC for the entire range of input charges. The design performance was also tested with respect to process, voltage, and temperature (PVT) variations to check for the robustness of the design. In PVT simulations, the design performance was tested with respect to different process corners (tt,ff,ss,fs,sf), a 10% variation in voltage supply, and a temperature range of 0–120 fC. In the worst case, the CSP exhibited a minimum sensitivity of 0.97 mV/fC and a maximum PTD of 14 ns.

When the test point buffers in channel 4 were switched on, the sensitivity of this channel was reduced to 6 mV/fC due to the loading effect of the buffers. However under normal operation conditions, when the buffer switches were off, all the channels exhibited a uniform sensitivity. The analog chain had a constant peaking time delay of 14.6 ns for the entire range of input charges. The baseline recovery time, complete time duration of overshoot and undershoot, of the bipolar signal was almost 400 ns for the full input range of 5–100 fC. At the output pads, the time representation of the input signal is provided as both the CMOS level with a voltage level of 0–1.2 V and the low-voltage differential signal with a voltage swing of 200 mV across a 200 mV common mode voltage, as shown in Figure 13. The complete layout design is shown in Figure 14. Table 2 summarizes the most important performance parameters of the presented FEE for the MDT-ATLAS-read-out, compared with our reference design [3].

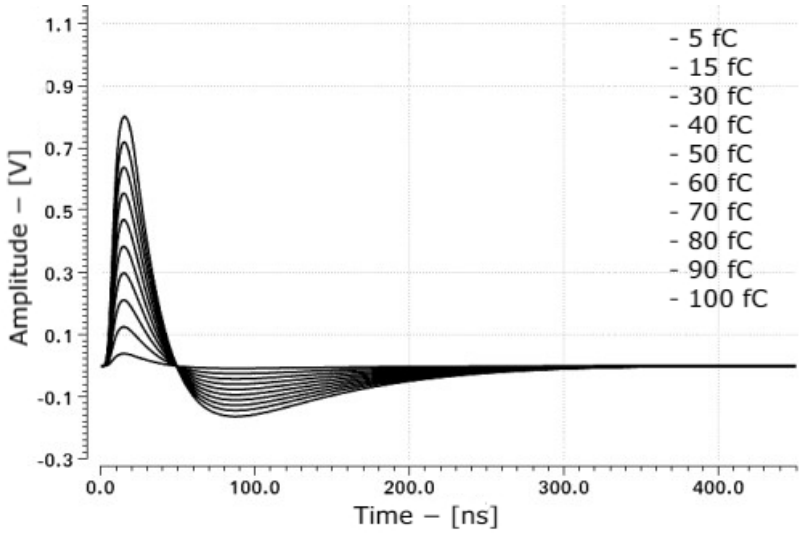


Figure 11. Analog channel output signal vs. input charge (5 fC–100 fC).

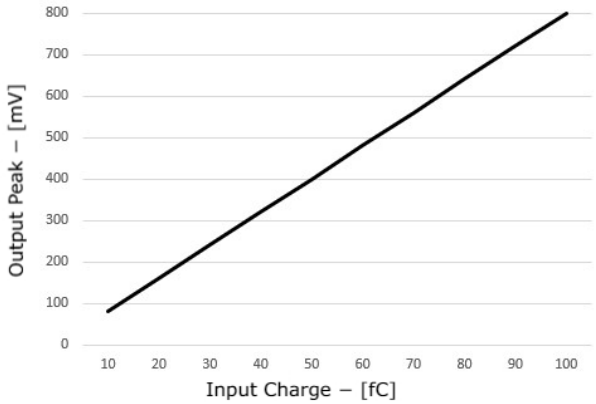


Figure 12. Sensitivity (Vout/Qin) at the output of the analog section.

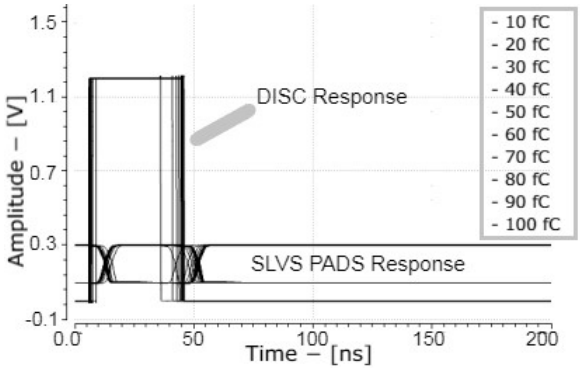


Figure 13. Comparator and SLVS drivers post-layout simulation results vs. input charges.

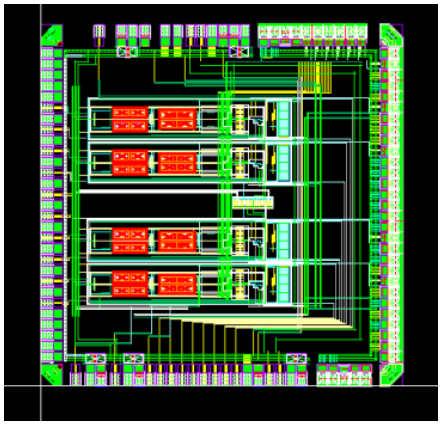


Figure 14. Four-channel FEE design layout.

5. Conclusions

A 4-channel FEE design for MDT ATLAS detectors at CERN LHC has been presented. The design has been realized in TSMC 65 nm CMOS technology, aiming for a power- and area-efficient design, matching the same performance parameters as that of the ATLAS MDT detectors [3]. As seen in Table 2, by scaling the technology to 65 nm CMOS and changing the design architecture of each block, the FEE channel is 61.3% more power efficient and utilizes 58.75% of the area as compared to the previous version. The key performance parameters—signal quality (SNR), peaking time and input signal dynamic range—are the same as for the previous design.

Table 2. State-of-the-art comparison.

Parameter	FEE 65 nm	ASD 130 nm
Technology	65 nm	130 nm
Channel Area	0.235 mm^2	0.4 mm^2
Supply Voltage	1.2 V	3.3 V
Channel Power	12.8 mW	33 mW
Detector Capacitance	60 pF	60 pF
Shaping Function	Bipolar	Bipolar
Input Charge	5–100 fC	5–100 fC
Signal Peaking Time	14.6 ns	15 ns
Sensitivity	8 mV/fC	14 mV/fC
SNR	15 dB	15 dB

Author Contributions: Conceptualization, A.B., M.D.M., H.K., M.F., O.K. and R.R.; methodology, A.B.; software, S.A.A.S.; formal analysis, S.A.A.S. and M.D.M.; writing—original draft preparation, S.A.A.S. and A.B.; writing—review and editing, M.D.M., H.K. and R.R.; supervision, A.B.; project administration, A.B. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

LHC	Large Hadron Collider
MDT	Monitored Drift Tube
FEE	Front-End Electronics
CSP	Charge-Sensitive-Preamplifier
PTD	Peaking Time Delay
SNR	Signal-to-Noise-Ratio
ASD	Amplification–Shaper–Discriminator
TDC	Time-to-Digital Converter
BLR	Baseline Recovery
LSB	Least Significant Bit
ToT	Time-over-Threshold
SIPO	Serial-In-Parallel-Out
PISO	Parallel-In-Serial-Out

References

1. ATLAS Collaboration; Aad, G.; Abat, E.; Abdallah, J.; Abdelalim, A.A.; Abdesselam, A.; Abdinov, O.; Abi, B.A.; Abolins, M.; Abramowicz, H.; et al. *The ATLAS Experiment at the CERN Large Hadron Collider*; JINST 3 S08003; CERN: Meyrin, Switzerland, 2008.
2. Arai, Y.; Ball, R.; Brandenburg, G.; Chapman, J.; Hazen, E.; Oliver, J.; Posch, C. On-chamber readout system for the ATLAS MDT muon spectrometer. *IEEE Trans. Nucl. Sci.* **2004**, *51*, 2196–2200. [CrossRef]
3. De Matteis, M.; Resta, F.; Richter, R.; Kroha, H.; Fras, M.; Zhao, Y.; Abovyan, S.; Baschirotto, A. An Eight-Channel 0.13-µm-CMOS Front End for ATLAS Muon Drift-Tube Detectors. *IEEE Sens. J.* **2017**, *17*, 3406–3415. [CrossRef]
4. Kroha, H.; Abovyan, S.; Baschirotto, A.; Danielyan, V.; Fras, M.; Mueller, F.; Nowak, S.; Resta, F.; De Matteis, M.; Richter, R. Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC. *arXiv* **2016** arXiv:1603.09093.
5. De Matteis, M.; Resta, F.; Richter, R.; Kroha, H.; Fras, M.; Zhao, Y.; Danielyan, V.; Abovyan, S.; Baschirotto, A. An 8-channels O.13 µm-CMOS front-end for ATLAS MDT-detectors. In Proceedings of the 2015 IEEE SENSORS, Busan, Korea, 1–4 November 2015.
6. ATLAS Collaboration. *Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*; CERN-LHCC-2017-017; CERN: Meyrin, Switzerland, 2017.
7. *JEDEC Standard JESD8-13*. Scalable Low-Voltage Signaling for 400 mV (SLVS-400). Solid State Technology Association: Arlington, VA, USA, 2001.

Journal of Instrumentation

PAPER

A 4-channel front-end electronics for muon drift tubes detectors in 65 nm CMOS technology

To cite this article: S.A.A. Shah *et al* 2022 *JINST* **17** C07012

Published by IOP Publishing for Sissa Medialab

Received: *October 24, 2021*
Revised: *March 4, 2022*
Accepted: *April 6, 2022*
Published: *July 7, 2022*

Topical Workshop on Electronics for Particle Physics 2021
20–24 September, 2021
Online

A 4-channel front-end electronics for muon drift tubes detectors in 65 nm CMOS technology

S.A.A. Shah,[a,*] M. De Matteis,[a] M. Fras,[b] O. Kortner,[b] H. Kroha,[b] R. Richter[b] and A. Baschirotto[a]

[a] *Physics Department 'G. Occhialini', University of Milano-Bicocca, Milano, Italy*
[b] *Max-Planck-Institute for Physics, Munich, Germany*

E-mail: s.shah4@campus.unimib.it

Abstract: A 4-channel front-end electronics chip in 65 nm CMOS technology (ASD65 nm) for muon drift tube chambers at high background counting rates in the ATLAS detector at High-Luminosity LHC and in future high-energy collider experiments is presented. Each channel of the ASD65 nm chip is a mixed-signal processing circuit consisting of a Charge Sensitive Preamplifier (CSP), a two-stage shaper, and a timing discriminator. The CSP exhibits a peaking time of 11 ns and a sensitivity of 1.1 mV/fC. The peaking time of the full analog chain is 14.6 ns. The minimum signal-to-noise ratio of the channel is 15 dB for the minimum input charge of 5 fC, and it rises to 40.5 dB for the maximum input charge of 100 fC. At the output, the time representation of input signal is provided in both, CMOS level as well as low-voltage-differential-signal. Each channel consumes a current of 10.6 mA from a single 1.2 V supply, and occupies an area of 0.235 mm^2. The specified performance parameters of the ASD65 nm have been achieved for 60 pF parasitic capacitance of the detector connected the input terminal.

Keywords: Front-end electronics for detector readout; Analogue electronic circuits

*Corresponding author.

https://doi.org/10.1088/1748-0221/17/07/C07012

Contents

1 Introduction

Muon Drift Tube (MDT) detectors are the main precision tracking detectors of the muon spectrometer of the ATLAS experiment at the Large Hadron Collider (LHC) [1]. The sense wires of the drift tubes are connected to the channels of an ASD chip [2] to process the signals of the ionization electrons created by muons traversing the tubes filled with argon:CO_2 (93:7) gas mixture. After more than a decade of successful operation, the ATLAS experiment has to be upgraded to cope with the increased data and radiation rates at the High Luminosity LHC (HL-LHC) [3]. To cope with the new challenges, a new state-of-the-art version of the ASD chip [4] has been developed in 130 nm CMOS technology, operated from a single 3.3 V supply voltage, and it will be used for the ATLAS MDT chambers at HL-LHC [3]. It is operated in dual mode, either with a signal charge measurement using a Wilkinson ADC (W-ADC) or in Time-over-Threshold (ToT) mode. The further objective in the process of improving the MDT readout electronics is reducing the power consumption in a long-term sustainable technology while preserving all functionalities and performance parameters of the 130 nm CMOS ASD [4]. In this new design (ASD65 nm), the technology is scaled down to TSMC 65 nm CMOS, and the circuit is operated from a single 1.2 V supply voltage. With the key target of power and area efficiency optimization, the complete analog channel architecture has been changed, and each block of the analog channel has been designed according to the new architecture. Each channel is composed by the cascade of a single-ended CSP, a differential two-stage shaper with bipolar shaping scheme, and a discriminator. It has a single ToT mode of operation, eliminating W-ADC mode. Sizes of the passive components have been thoroughly optimized, resulting in a four-fold shrinkage in shaper area with respect to the previous design. SLVS drivers interface the ASD65 nm to the front-end board. The power consumption of each channel is 12.8 mW, which is lower by 61.2% than in the previous design. Each channel occupies an area of 0.235 mm^2, which is only 58.75% of the area in the previous design. These significant savings are achieved while maintaining the performance in terms of peaking time of the analog channel of 14.6 ns and SNR of 15 dB. Linear sensitivity of 1.1 mV/fC and 8 mV/fC is

2022 JINST 17 C07012

achieved at the output of CSP and of the shaper, respectively, for input charges in the range of 5 to 100 fC. The paper is organized as follows. Section 2 presents the ASD65 nm CMOS circuit design. In section 3 the simulation results of the design are presented. Section 4 draws conclusions.

2 Implementation of the front-end electronics circuit

The block diagram of a single ASD65 nm channel is shown in figure 1. Each channel consists of an analog and a digital section. The analog section is composed of an input stage (CSP) and a differential two-stage shaper. The CSP converts and amplifies the input current pulse into a voltage pulse, which is further amplified and shaped by the shaper stage in bipolar scheme to reduce baseline shift at high counting rates. The output of the analog stage is fed into the discriminator, which compares the incoming signal to a programmable threshold value (with nominal value 3 to 5 standard deviations above the noise level) to produce the digital output. The digital output signal carries arrival time information of the incoming signal. At the output, SLVS drivers connect the ASD65 nm channels to the front-end board.

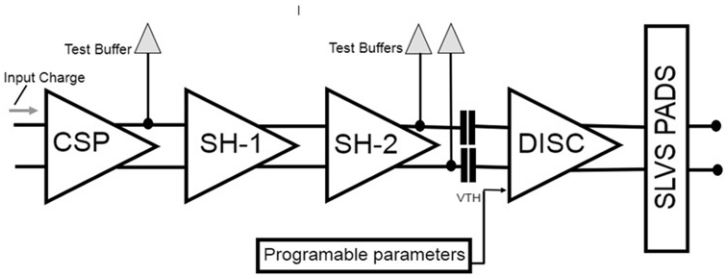


Figure 1. Generic block diagram of one channel of the ASD65 chip.

2.1 Charge sensitive preamplifier

In designing of ASD65 nm, special attention is dedicated to CSP design in order to achieve the required functional parameters without increasing the low noise level and the power load. Signal-to-noise ratio and speed of response to input pulse are the two most important parameters for muon detector application and are largely defined by the CSP block. They are optimized by suitable input device transconductance (gm1) and by designing the amplifier with large unity-gain bandwidth.

CSP is designed using two-stage, single-ended amplifier. The transistors of the input differential pair are decisive for an optimum trade-off between noise and power consumption. To improve noise performance, they are designed with large size (W/L = 580 µm/330 nm) and large nominal current (1.475 mA) to operate in sub-threshold region for performing high transconductance value of 25 mA/V. This technique has as trade-off increased power consumption. To minimize the power consumption a single-ended topology is used in the CSP design, as it consumes lower power compared to fully differential amplifier. Moreover, the number of stages in overall design is minimized and the operating voltage is reduced from 3.3 V to 1.2 V, resulting in a significantly

2022 JINST 17 C07012

power efficient overall design. To make the CSP response faster, the operational amplifier of this block is designed with large UGB of 2.4 GHz with a phase-margin of 60 degree, ensuring CSP stability. These design parameters achieve a peaking time of 11 ns at CSP output.

2.2 Shaper

The CSP output signal is filtered by a two-stage shaper block, which converts it into a bipolar pulse. Each stage of the shaper is based on a two-stage differential amplifier. The conversion of analog chain from single-ended at the CSP output to differential is for the purpose of achieving high power-supply rejection. The transistors of the input differential pair are operated in sub-threshold region, and they have a transconductance value of 2.5 mA/V. The choice of using a two-stage topology, along with being more robust to load, is its ability to provide maximum output swing. The transistors in the second stage of each amplifier are designed with an overdrive voltage of <100 mV, hence providing linear response up to 1 V. Each block of the shaper has an input impedance network and a resistive feedback network to implement the poles and zeroes for bipolar shaping.

The DC-gain and UGBW of the amplifiers are 45 dB and 500 MHz, respectively. With these parameters, the shaper pass-band gain shows a variation of less then 4% compared to the one with ideal amplifiers. Transient noise simulations have been performed to assess the thermal noise contribution. The three-stage shaper of the previous design utilized large capacitors, which occupy large area on the chip. For area efficiency, along with minimizing the number of stages, sizing of the shaper passive elements are revised in this design and are reduced by a 4× ratio.

The frequency response of each stage of the analog channel is plotted in figure 2. The shaper exhibits a pass-band width of 1.06–172.6 MHz and a pass-band gain of 17.6 dB.

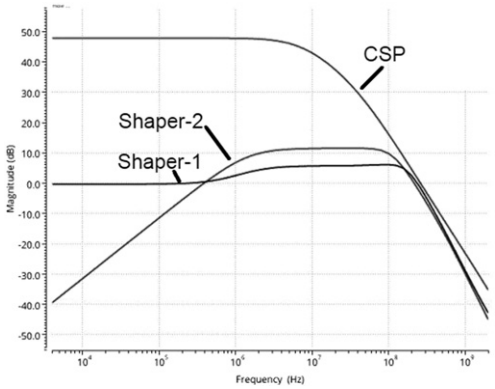


Figure 2. CSP and shaper stage 1 and 2 frequency responses.

2.3 Digital circuit design

The digital part of the device includes discriminator, shift registers, programmable dead time block, channel mode selection unit etc. The discriminator compares the output of the analog section to a threshold value, yielding the digital ToT output pulse. The discriminator threshold value is

programmable up to 256 mV with LSB of 2 mV across the common mode voltage. The embedded comparator is based on a high-gain, two-stage uncompensated amplifier. A hysteresis block is added that unbalances the currents in the differential pair of discriminator by a programmable value to provide hysteresis up to 50 mV. The dead time block is used to introduce a delay in discriminator response of up to 500 ns, programmable in steps of 30 ns. A digital word carried by a 50 bit shift register sets all programmable channel parameters. A novel technique of parallel arrays of SIPO-PISO blocks is applied in the design of the shift register to monitor that correct data is loaded into channel. When the digital word is loaded from SIPO block into channel, it is loaded into PISO block as well, which is based on parallel-in serial-out interface. The PISO block contents can be read through an output PAD, and, hence, it can be verified. The digital word is passed from an external board through a JTAG interface.

3 Simulation results

The design is validated by simulating input charges (QIN) in the full required input range of 5 to 100 fC. The large detector capacitance (60 pF) is taken into account in the design and simulations. The design performance is also tested with respect to process, voltage and temperature (PVT) variations to check for robustness of the design.

Figure 3 shows the output signal of the analog section and the SLVS drivers. The sensitivity of the CSP and of the shaper is 1.1 mV/fC and 8 mV/fC, respectively. Figure 3 shows that the ASD65 nm device exhibits linear sensitivity with increasing input charge from 20 fC to 100 fC. Test point buffers, based on a common drain topology, have been added at the output of CSP and shaper. Design exhibits peaking time of 11 ns at the CSP output and 14.8 ns at the analog chain output. The total layout area of the design as shown in figure 4 is 4 mm^2.

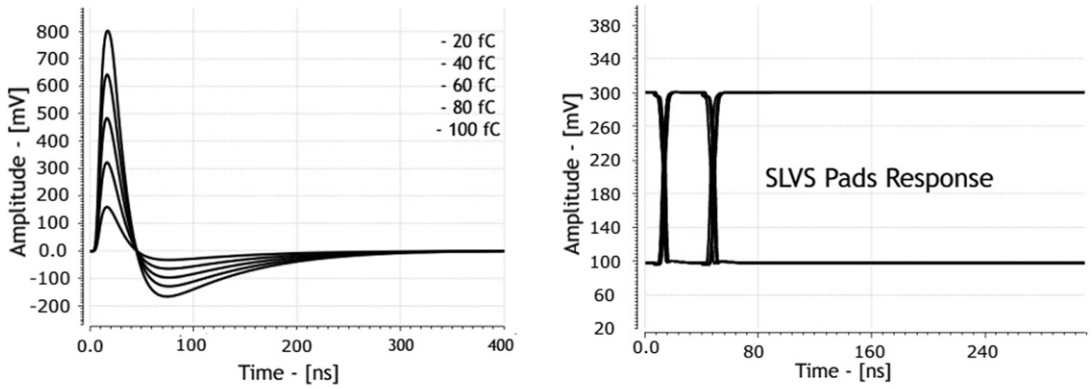


Figure 3. (a) Shaper output vs. input charge (b) SLVS pads response.

2022 JINST 17 C07012

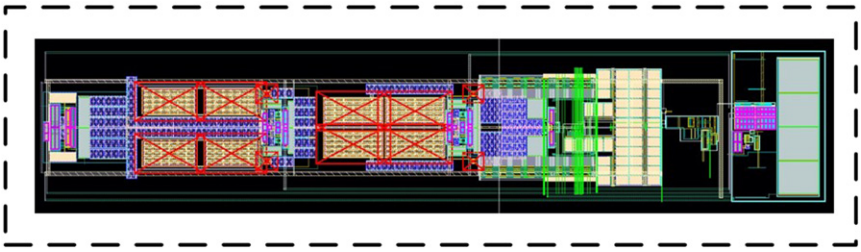


Figure 4. ASD65 single channel layout.

Table 1 summarizes the simulated performance and functional parameters of the present ASD65 nm chip as compared to the previous design.

Table 1. Comparison of main parameters.

Parameter	ASD65nm	ASD 130 nm
Technology	65 nm	130 nm
Channel Area	0.235 mm^2	0.4 mm^2
Supply Voltage	1.2 V	3.3 V
Channel Power	12.8 mW	33 mW
Detector Capacitance	60 pF	60 pF
Shaping Function	Bipolar	Bipolar
Input Charge	5-100 fC	5-100 fC
Signal Peaking Time	14.6 ns	15 ns
Sensitivity	8 mV/fC	14 mV/fC
SNR	15 dB	15 dB

4 Conclusions

The design of a new 4-channel amplifier-shaper-discriminator (ASD65 nm) chip in 65 nm-CMOS technology for the MDT detectors in the ATLAS experiment is presented. The chip is an advanced version of the MDT ASD chip designed and produced for the next (phase-2) upgrade of the ATLAS detector [3], revised to reduce power consumption and chip area while achieving the same performance parameters. The comparison of the most important performance parameters of the new ASD65 nm chip design to the ones of the previous implementation in 130 nm CMOS technology (see table 1) shows that each channel in new design is 61.2% power efficient and utilizes 58.75% of the area of the previous version. The key performance parameters, signal quality (SNR), peaking time and input signal dynamic range, are the same as for the previous design.

References

[1] ATLAS collaboration, G. Aad et al., *The ATLAS experiment at the CERN Large Hadron Collider,* 2008 *JINST* **3** S08003.

[2] Y. Arai et al., *On-chamber readout system for the ATLAS MDT muon spectrometer, IEEE Trans. Nucl. Sci.* **51** (2004) 2196.

2022 JINST 17 C07012

6.2 Poster

6.2.1 TWEPP 2021

6.2.2 TWEPP 2022

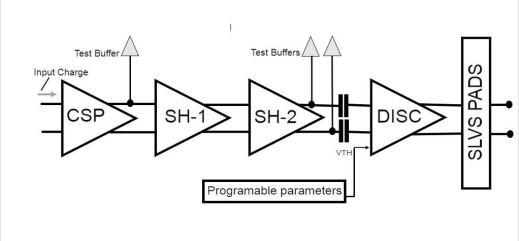
A Four-Channels Front End Electronics for ATLAS Muon-Drift-Tubes Detectors in 65nm CMOS Technology

S.A.A.Shah, M.De Matteis, A.Baschirotto
University of Milan-Bicocca, Milan, Italy
R.Richter , H.Kroha, M.Fras,
Max-Planck-Institut for Physics, Munich, Germany

Introduction

- ATLAS experiment designed to explore the proton-proton collisions at the CERN
- Ionizing track crossing a MDT tube generates a string of electrons which drift towards the anode wire
- The MDT chamber design is optimized for precision tracking
- AFE Electronics detect arrival of charge and give information regarding Charge arrival time and amount of charge
- Higher speed (for higher instantaneous luminosity), lower area, robust Front-End Electronics are needed

Functional diagram of the ASD using bipolar shaping



- Charge Sensing Preamplifier (CSP)->DA1->DA2->DA3(three shaping stages) -> discriminator -> SLVS PADS
- The Design area is 2×2=4 mm2

Design Specification

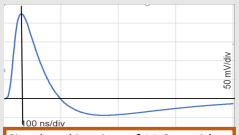
Parameters	Values (This Work)	Values ASD 130nm
CMOS Technology	65nm	130nm
Total Area	4mm²	7.638mm²
Supply Voltage	1.2V	3.3V
Channel Power	16mW	33mW
Detector Parasitic Cap	60pF	60pF
Shaping Function	Bipolar	Bipolar
Shaper Stages	Two	Three
Input Charge	5—100fC	5—100fC
Signal Peaking Time	14.6ns	15ns
Front End Sensitivity	8mV/fC	14mV/fC
Input noise density	1.1 nV/√Hz	1.3 nV/√Hz
SNR at Min Input Charge	15 dB	15 dB

Novelty In Design

- This AFE Design is a new, advance version of a CHIP, designed in 130nm CMOS process, being used in ATLAS experiment
- Scaling down the technology to 65nm CMOS process
- Operating at Low Supply Voltage of 1.2V
- Minimum and Simplified Architecture
  - Two Stage Shaper
  - No Pre-Discriminator Stage
  - Single Mode of operation (ToT Mode)
- Improving Passive elements sizing
  - Targeting Area Efficient Design
- Replacing LVDS by SLVS pads
  - Power Efficient, High Speed
- New Block of PISO-SIPO to confirm the correctness of Digital contents for Chip operation
- Variable Dead Time up to 500ns with a step of 30ns

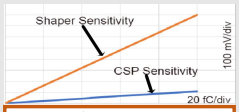
Methodology

- CSP, first stage of Design, performs charge to Voltage conversion
- A 2-Stage Single Ended amplifier topology is used for this stage
- Amplifier of Bandwidth of 2.4Hz is designed for Fast Peaking time
- Peaking Time of CSP is 11ns
- High Transconductance of 25mA/V is set, targeting minimum noise
- Input noise density of CSP is 1.1 nV/√Hz
- Linear sensitivity of 1.1mV/fC for 5-100fC range
- SNR at CSP output is 14.5 dB



Signal peaking time of 14.6 ns with 60 pF detector capacitance

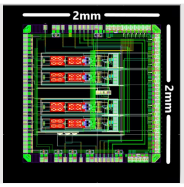
- 2 Stage Shaper is designed to Implement Bipolar Scheme
- Implementing Two Poles
  - FP1=1.55MHz & FP2=1.41MHz
- Implementing Two Zeroes
  - FZ1=0.77MHz & FZ2=0.365MHz
- Pass Band gain of Shaper 17.6 dB
- Linear sensitivity of 8mV/fC for 5-100fC range



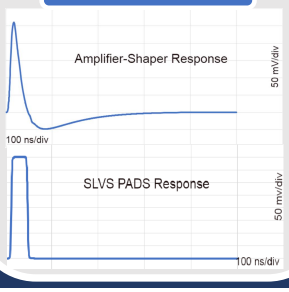
Sensitivity of CSP and Shaper is 1.1mV/fC and 8mV/fC respectively

- Uncompensated 2 Stage OP Amp used for Discriminator
- To set threshold Voltage, two 8-Bit String DACs are used
- A variable threshold of up to 256mV can be set with LSB of 2mV
- SLVS PADS are used to convert signal to external low-level signal
- Voltage swing of 200 mV on a 100 Ω load
- Common Mode voltage of 200 mV

Chip Layout



Signal Response



Fast Tracking Read-Out Electronics for ATLAS sMDT Detectors in 65 nm CMOS

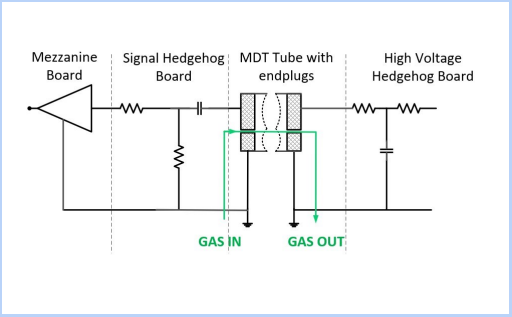
S.A.A.Shah[1], L.Sharifi[1] ,M.De Matteis[1], R.Richter[2], H.Kroha[2], A.Baschirotto[1]

University of Milano-Bicocca, Italy[1]; Max-Planck-Institute for Physics, Munich, Germany[2]

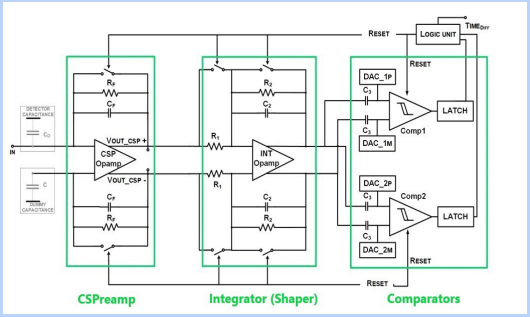
Abstract

The upgradation of Large Hadron Collider (LHC) to discover novel physics particles demands improvement in read-out electronics for charge detection at higher rate. This work presents a 4-channel readout electronics for small-diameter Muon-Drift-Tube (sMDT) detectors. The system is composed by the cascade of Analog signal processing front-end and a Digital section to set the critical design parameters such as threshold voltages and reset time. The design is optimized largely for higher detection rate of events at High Luminosity of LHC and thus significantly reducing the impact of pile-up events and eliminating use of long deadtime zone. Analog chain of the design consists of Charge-Sensitive-Preamplifier, to convert input charge into voltage pulse, followed by a single stage shaper. Significance of this work is in fast resetting of all channels to baseline, after extracting the useful information, and not waiting for the complete processing of input signal. Design operates with a 5 –100 fC input charge range. The design is realized in 65 nm technology and is operated from 1.2 V supply.

ATLAS Experiment and MDT Scheme



4x FEE Channel Block Scheme

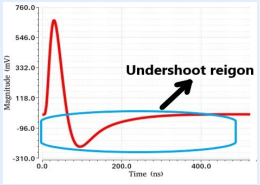


Introduction

- ATLAS experiment is designed to explore the proton-proton collisions at the CERN
- To determine energy and direction of secondary particles, emerging from the p-p collisions, a sequence of specialized detectors are used
- The MDT chamber design is optimized for precision tracking of the particles generated
- Readout Electronics detect incoming input charge and give information regarding charge arrival time and amount of charge arrived
- For higher hit rate (higher instantaneous luminosity) and tougher environment, because of upgradation of ATLAS, robust and fast Front-End Electronics are needed

Novelty in Design

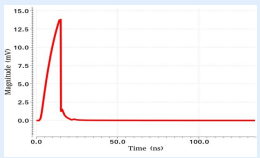
- The readout electronics currently used in ATLAS experiment are known as ASD, Amplifier Shaper Discriminator, and are designed in 130 nm CMOS process
- It is based on Bipolar-shaping of all incoming charges
- Every Bipolar pulse has an unwanted long tail in it's undershoot, ranging up to 500 ns
- As a result, the ASD must go into a dead-time stage of up to 800 ns, depending on drift time
- The dead-time logic slow down the process
- A novel approach of fast resetting the channel to baseline, targeting higher data rate
- Rather then processing the complete analog signal, entire channel is reset as soon as the required information is obtained
- Baseline restoration time is reduced drastically, design is ready to detect any consecutive charge



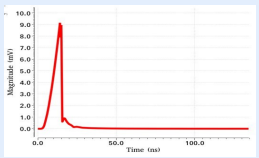
Bipolar pulse of ASD Channel

Design Structure

- CSPreamp, first stage of Design, performs charge to voltage conversion
- 2-Stage fully differential amplifier with high gain bandwidth
- To reduce noise, the input differential Mosfets pair has a gm of 25mA/V
- CSP have a switch *S1* in parallel of its feedback path, for reset purpose
- To guarantee stability in the whole reset cycle, the feedback switch is closed only after activation of additional compensation
- Single Stage Shaper designed using differential two-stage amplifier topology
- Shaper Transfer function can be approximated to a single pole system with a time constant given by $1/(2\,(R_2{*}C_2))$

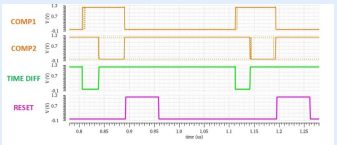


CSP Output



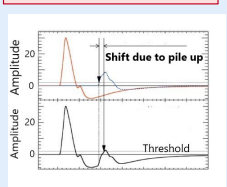
INT Output

- Each channel has two comparators
- TIME_DIFF encodes information regarding incoming charge pulse
- Logic Unit triggers reset-mode when an event has been completed
- After the fast reset phase, the design is ready for detection of new charges



Logic Unit Signals

In our design since we eliminate the undershoot pulse, no pile-up of event happens



Signal Pile up in ASD

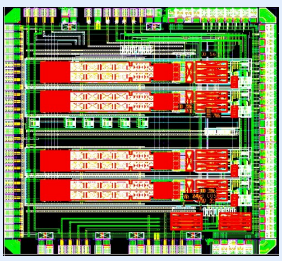
Performance Resume

Parameters	Value
CMOS Technology	65 nm
Total Area	4 mm^2
Supply Voltage	1.2 V
Channel Number	4
Detector Parasitic Cap	60 pF
Input Impedance	120 Ω
Channel Current Consumption	25 mA
Input Charge	5—100 fC
Maximum Time Difference	10 – 50 ns

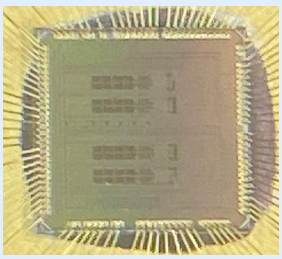
Design Picture

- The entire read-out electronics design is of size 2mm*2mm

Layout View



Chip Picture



7 Conclusions

This thesis is dedicated on the read-out front-ends for High Energy Physics (HEP) experiments by analysing the major challenges in the development of CMOS integrated circuits for high rate gaseous particle detectors. The current front end electronics being used in the experiment are in old technologies, the ASD1 was designed in the, now unavailable, Agilent 500 nm technology. For the design of ASD2, the 130 nm process by IBM (later Global Foundries) was selected. However with rapid change and scaling down in technology a new readout electronics circuit is required in a long sustainable technology that matches the performance parameters of the ASD1 and ASD2.

Starting from this consideration, the core of this thesis concerned with the development a new readout electronics designed in 65nm CMOS technology, which is significantly-power and area-efficient design. The measurements in this thesis showed the results from the first version of the design. The second version of the design, which is an improved version, is expected to arrive in February 2023 with a better performance. The following version of the current design aims to replace the chip currently used, designed in 500m, and 130nm technology.

With the main target of designing a significantly power efficient design, the FEE was deeply optmized by selecting the right topologies, better RC sizing and utilizing minimum architecture. With these considerations FEE channel is 61.3 percent more power efficient and utilizes only 58.75 percent of the area as compared to the previous version.

Powerful and robust electronics are required to correctly work in presence of High Luminosity levels. For this purpose a real experiment type environment is realized in the lad for measurement by taking into account all the parasitic and secondary effects. FEE chip has been interfaced with the 'Mezzanine Board' in order to have a complete characterization in time and frequency domains. The most important performance have been reported in Chapter 4 and 5. In particular, the channel features a linear sensitivity at the Comparator input of 8 mV/fC and a fast peaking time of 11 ns. The measured results demonstrate that the new design has a major sensing capability and is capable to detect any charge that arrives in range of 5fC-100fC.

FEE V2 aims to pass the version 1 by an improvement in SLVS pads rise time and addition of monitor buffers which will allow us to look inside the channel in measurement phase. The Version 2 is expected to arrive in February 2023 and will be tested in the same testing environment.

References

[1] L. Evans and P. Bryant, LHC Machine, JINST 3 (2008) S08001.

[2] ATLAS Collaboration, G. Aad et al., The ATLAS Experiment at the CERN Large Hadron Collider, JINST 3 (2008) S08003.

[3] CMS Collaboration, S. Chatrchyan et al., The CMS experiment at the CERN LHC, JINST 3 (2008) S08004.

[4] ATLAS Collaboration, G. Aad et al., Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC, Phys.Lett. B716 (2012) 1.

[5] CMS Collaboration Collaboration, S. Chatrchyan et al., Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC, Phys.Lett. B716 (2012) 30.

[6] LHCb Collaboration, A. Augusto Alves, Jr. et al., The LHCb Detector at the LHC, JINST 3 (2008) S08005.

[7] ALICE Collaboration, K. Aamodt et al., The ALICE experiment at the CERN LHC, JINST 3 (2008) S08002.

[8] LHCf Collaboration, O. Adriani et al., The LHCf detector at the CERN Large Hadron Collider, JINST 3 (2008) S08006.

[9] TOTEM Collaboration, G. Anelli et al., The TOTEM experiment at the CERN Large Hadron Collider, JINST 3 (2008) S08007.

[10] MoEDAL Collaboration, J. Pinfold et al., Technical Design Report of the MoEDAL Experiment, CERN-LHCC-2009-006. MoEDAL-TDR-001, CERN, Geneva, June 2009, https://cds.cern.ch/record/1181486.

[11] ATLAS Public Luminosity Results. https://twiki.cern.ch/twiki/bin/view/AtlasPublic/LuminosityPublicResults.

[12] ATLAS Collaboration, G. Aad et al., Measurement of the Higgs boson mass from the H $\rightarrow \gamma\ \gamma$ and H $\rightarrow$ Z Z ! 4ζ channels with the ATLAS detector using 25 fb^{-1} of pp collision data, arXiv:1406.3827 [hep-ex].

[13] CMS Collaboration, S. Chatrchyan et al., Observation of a new boson with mass near 125 GeV in pp collisions at $\sqrt{s} = 7$ and 8 TeV, JHEP 1306 (2013) 081.

[14] L. Arnaudon et al., Linac4 Technical Design Report, CERN report, CERN-AB-2006-084, CERN, Geneva, Dec. 2006, http://cds.cern.ch/record/1004186.

[15] F. Bordry, "LHC schedule approved by CERN management and LHC experiments." http://lhc-commissioning.web.cern.ch/lhc-commissioning/schedule/LHC 20schedule 202015-2034 20FkBordry 202-december-2013.pdf, Dec. 2013.

[16] ATLAS Collaboration, ATLAS Insertable B-Layer Technical Design Report, CERN report, CERN-LHCC-2010-013. ATLAS-TDR-19, CERN, Geneva, Sept. 2010, http://cds.cern.ch/record/1291633.

[17] G. Aielli et al., Proposal for the Upgrade of the Elevator Regions in the ATLAS Barrel Muon Spectrometer, ATL-MUON-INT-2014-001, CERN, Geneva, Jan 2014.

[18] ATLAS Collaboration, Letter of Intent for the Phase-I Upgrade of the ATLAS Experiment, CERN report, CERN-LHCC-2011-012, CERN, Geneva, Nov. 2011, http://cds.cern.ch/record/1402470.

[19] ATLAS Collaboration, M. L. Gonzalez Silva et al., New Small Wheel Technical Design Report, CERN report, CERN-LHCC-2013-006, CERN, Geneva, June 2013, http://cds.cern.ch/record/1552862.

[20] ATLAS Collaboration, Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment, CERN report, CERN-LHCC-2012-022, CERN, Geneva, Dec. 2012, http://cds.cern.ch/record/1502664.

[21] E. Simioni et al., The Topological Processor for the future ATLAS Level-1 Trigger: from design to commissioning, arXiv:1406.4316 [physics.ins-det].

[22] P. Schwegler, O. Kortner, H. Kroha, and R. Richter, Improvement of the L1 trigger for the ATLAS muon spectrometer at high luminosity, Nucl. Instr. Meth. A 718 (2013) 245 . Bibliography

[23] S. Nowak et al., A Muon Trigger with high pT-resolution for Phase-II of the LHC Upgrade,based on the ATLAS Muon Drift Tube Chambers, ATL-MUON-PROC-2014-002, CERN, Geneva, June 2014, https://cds.cern.ch/record/1711641.

[24] M. De Matteis et al., "An 8-channels O.13m-CMOS front-end for ATLAS MDT-detectors," 2015 IEEE SENSORS, 2015.

[25] De Matteis et al., An Eight-Channel 0.13- μm -CMOS Front End for ATLAS Muon Drift-Tube Detectors, IEEE Sensors Journal, vol. 17, no. 11 (2017).

[26] M. De Matteis et al., "The new octal amplifier–shaper–discriminator chip for the ATLAS MDT chambers at HL-LHC", Nuclear Instruments and Methods in Physics Research

[27] L. G. ¯ E. SHELDON, "Partial-symmetries of weak interactions," Selected Papers on Gauge Theory of Weak and Electromagnetic Interactions, p. 171, 1981.

[28] S. Weinberg, "A model of leptons," Physical review letters, vol. 19, no. 21, p. 1264, 1967.

[29] A. Salam and J. C. Ward, "Weak and electromagnetic interactions," Il Nuovo Cimento (1955-1965), vol. 11, no. 4, pp. 568–577, 1959.

[30] A. Collaboration et al., "Observation of a new particle in the search for the standard model higgs boson with the atlas detector at the lhc," arXiv preprint arXiv:1207.7214, 2012.

[31] J. Snuverink, The atlas muon spectrometer: commissioning and tracking. oai: cds. cern. ch: 1232051. PhD thesis, Ph. D. Thesis, Twente, 2009. Presented on 16 Oct, 2009.

[32] Y. Arai et al., "Atlas muon drift tube electronics, 2008."

[33] C. Atlas andW. Armstrong, "Atlas technical proposal for a general-purpose pp experiment at the large hadron collider," 1994.

[34] W. Armstrong,W. Burris, D. Gingrich, P. Green, L. Greeniaus, J. Hewlett, L. Holm, J. Mcdonald, S. Mullin,W. Olsen, et al., "Atlas: technical proposal for a generalpurpose pp experiment at the large hadron collider at cern," 1994.

[35] A. M. Group and M. Livan, "Monitored drift tubes in atlas," Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 384, no. 1, pp. 214–218, 1996.

[36] G. Aad, E. Abat, J. Abdallah, A. Abdelalim, A. Abdesselam, O. Abdinov, B. Abi, M. Abolins, H. Abramowicz, E. Acerbi, et al., "The atlas experiment at the cern large hadron collider," Journal of Instrumentation, vol. 3, no. S08003, 2008.

[37] C. Posch and E. Hazen. Total ionizing dose radiation hardness of the ATLAS MDT-ASD and the HP-Agilent 0.5 um CMOS process. ATL-ELEC-2002-001, ATL-COM-ELEC-2002-001, 2002

[38] W. Riegler, MDT Efficiency, Double Track Separation, CERN-ATL-MUON-97-173, 1997.

[39] W. Riegler and M. Aleksa. Bipolar versus unipolar shaping of MDT signals. ATL-MUON-99-003. ATL-COM-MUON-99-007, 1999.

[40] JEDEC Standard JESD8-13 2001 Scalable Low-Voltage Signaling for 400 mV (SLVS-400) (Solid State Technology Association, Printed in U.S.A.)

[41] Hugo Daniel Hernandez 2014 Design review: SLVS Tx and Rx blocks (SAMPA review) (indico.cern.ch/event/308952)

[42] Bonacini S, Kloukinas K and Moreira P 2009 E-link: A radiation-hard low-power electrical link for chip-to-chip communication Proc. of the TWEPP-09, CERN-2009-06 pp 422–5 (http://cdsweb.cern.ch/record/1235849)

[43] Piotr Kmon et al., Design of 4 Gbps SLVS-type Transmitter in 55 nm CMOS, 24th International Conference "Mixed Design of Integrated Circuits and Systems"

Acknowledgements

I would like to thank my colleagues that I met during my three years of PhD school. In particular, I would like to mention Leila Sharifi and Federico Farry for their help and guidance which helped me in learning many new concepts in circuit designing.

I am deeply grateful to Prof. Andrea Bachirotto and Marcello De Matties for giving me the opportunity to work in an extremely exciting project and for their continuous support throughout my PhD degree.

I would also like to thanks our colleagues from Max Plank Institute Munich, especially, Robert Richter, Hubert Kroha, Markus Fras and Sergey Abovyan for their contribution to the Project.

I would also like to thank my family for supporting my studies and for many opportunities that I had during my years as a Bachelor, Master and PhD student.